525.442 FPGA Design Using VHDL

Syllabus

Instructor Contact

Ramsey Hourani
Work: 443.778.9154
E-mail: hourani525442@gmail.com

Blackboard Messaging should be used for all Email correspondence. You may use personal Email if no other options are available.

I will typically respond to emails within 72 hours or earlier. If an issue is urgent, you are to indicate its urgency in the subject line and I will respond as soon as I am available to respond.

Office Hours via Adobe Connect

For more information regarding Adobe Connect, please see the Adobe Connect Information page located in Help & Support on the left menu.

This course will use Adobe Connect to facilitate weekly, synchronous office hours. You are not required to participate in office hours; however, you may find them very beneficial for receiving more timely answers to questions related to the course content and assignments.

Office Hours are set for Wednesday from 5:30 pm to 7:00 pm and are held via Adobe Connect. This is the only synchronous activity for the class where you can interact with the instructor in real time. If the time is not convenient, e-mail me to let him know and I will do my best to accommodate you. Recordings of the office hours are available to you and it may be possible to make other arrangements.

Course Description

This course covers the design of digital systems using VHSIC Hardware Description Language (VHDL) and its implementation in Field Programmable Gate Arrays (FPGAs). This technology allows cost-effective unique system realizations by enabling design reuse and simplifying custom circuit design. The design tools are first introduced and used to implement basic circuits. More advanced designs follow, focusing on integrating the FPGA with external peripherals, simple data processing applications, utilizing soft-core processors, and using intellectual property (IP) cores.

Prerequisites

No specific course is required as a pre-requisite. However, a solid understanding of digital logic fundamentals is required.

Course Goals

This course covers the design of digital systems using VHDL and its implementation in FPGAs. By the end of this course, you will be able to describe a system using synthesizable VHDL code, synthesize the design and map it onto an FPGA for verification. You will also acquire the skillset to utilize the Xilinx ISE synthesis tools as well as the Xilinx ISIM simulator to verify the behavioral performance of the designs under test.

Course Objectives

In this course, we will be learning fundamentals of VHDL with an emphasis on coding for synthesis, good digital design practices, and writing VHDL testbenches for exercising the designs. Each student will complete a number of assignments using a development board based on the Xilinx Spartan 3E FPGA.

By the end of the course, you will be able to:

- Describe the behavior and performance of designs targeting FPGAs
- Translate a functional system description into appropriate digital blocks coded in VHDL
- Perform synthesis, place-and-route and map a digital design onto an FPGA using Xilinx ISE tools
- Utilize the Digilent Nexys2 development boards throughout the semester
- Simulate, via Xilinx ISIM, the behavior of VHDL designs using testbenches written in VHDL
- Convert between different VHDL data types using arithmetic libraries
- Embed a programmable microprocessor in an FPGA design and write functional assembly code

Course Structure

The course content is divided into modules which can be accessed by clicking Course Modules on the left menu. A module will have several sections including the overview, content, readings, discussions, and assignments. You are encouraged to preview all sections of the module before starting. Most modules run for a period of seven (7) days, exceptions are noted on the Course Outline page. You should regularly check the Calendar and Announcements for assignment due dates.

Optional Textbook

Rushton, A. (1998). *VHDL for logic synthesis* (2nd ed.). Hoboken, NJ: John Wiley & Sons, Inc.
ISBN: 047198325X
ISBN-13: 978-0471983255

Required Software

Xilinx ISE

You will need access to a recent version of **Xilinx ISE** 13.1 or newer (**DO NOT install Vivado**). You can download the Xilinx ISE webpack from:
http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html

Note: Xilinx ISE can only be installed on Windows 7 (or older), if you have a Windows machine. It cannot be easily installed on Windows 8, Linux or a Mac. There may be solutions to using Xilinx ISE if you have a machine other than Windows 7, but you me be responsible for arriving at a solution that works for you. More information can be found about ISE Design Suite Operating System Support on the following link:
ISE Design Suite Operating System Support

Adept from Digilent

You will also need access to Digilent Adept for programming the FPGAs on the development boards. You can download the Digilent Adept tool from:
http://digilentinc.com/Products/Detail.cfm?NavPath=2,66,828&Prod=ADEPT2

Required Hardware

Each registered student will be assigned an FPGA development board and several passive components at the beginning of the semester. Each student is responsible for getting access to a VGA monitor with VGA cable, an oscilloscope and basic tools for building a simple passive circuit such as low-pass filter.

Note: If you are registered for the course and receive a development board, but withdraw from the course before its completion, you are expected to **mail the development board back to the EP program**, along with the various components.

Technical Requirements

You should refer to Help & Support on the left menu for a general listing of all the course technical requirements.

Student Coursework Requirements

It is expected that each module will take approximately 12–16 hours per week to complete. Here is an approximate breakdown: reading the assigned sections of the texts (approximately 1–2 hours per week) as well as some outside reading, listening to the audio annotated slide presentations (approximately 1–2 hours per week), and working on lab assignments (approximately 10–12 hours per week).

This course will consist of four basic student requirements:

1. **Preparation and Participation (Module Discussions)** (10% of Final Grade Calculation)

   You are responsible for reading all assigned material and being prepared for discussion. The majority of readings are from datasheets and manuals.

   Part one of your grade for module discussion is to **post your initial response to the discussion questions by the weekend** for that module week. Posting a response to the discussion question is part one of your grade for module discussions (i.e., Timeliness).

   Part two of your grade for module discussion is your interaction (i.e., **responding to classmate postings with thoughtful responses**) with at least two classmates (i.e., Critical Thinking). Just posting your response to a discussion question is not sufficient; I would like you to interact with your classmates. Be detailed in your postings and responses to your classmates' postings. Feel free to agree or disagree with your classmates. Please ensure that your postings are civil and constructive. This grade will be determined by the instructor at the end of the semester.

   I will monitor module discussions and will respond to some of the discussions as discussions are posted. In some instances, I will summarize the overall discussions and post the summary for the module.

   Evaluation of preparation and participation is based on contribution to discussions.

   Preparation and participation is evaluated by the following grading elements:

   Preparation (5% of final grade) is graded as follows:

   5 = Responds in detail to discussion question by the weekend the module officially starts

   4 = Responds briefly to discussion question by the weekend the module officially starts or responds in detail after the weekend the module officially starts

   3 = Responds briefly to discussion question after the weekend the module officially starts

   2 = Responds in detail to discussion question after due date

   1 = Responds briefly to discussion question after due date

   0 = Does not respond to discussion topic by due date

Participation (5% of final grade) is determined at the end of the semester and is graded as follows

5 = Responds to 15 or more other posts throughout the semester

4 = Responds to 10 to 14 other posts throughout the semester

3 = Responds to 7 to 9 other posts throughout the semester

2 = Responds to 4 to 6 other posts throughout the semester

1 = Responds to 3 or less other posts throughout the semester

0 = Does not respond to other posts at all throughout the semester

2. **Lab Assignments** (45% of Final Grade Calculation)

Assignments are referred to as lab assignments even though you don't need an actual lab to work through them; you can work on your assignments in your office (if permitted) or at home. Lab assignments are given to you every week or every other week and are graded out of 100 points per assignment. I will give you the design requirements and you will construct a design in VHDL. You will then implement the design on the assigned development board for verification. Unless otherwise specified, each assignment will count equally towards the cumulative 45% of the class grade. Assignment submissions will include VHDL source files, UCF files, *bit* files as well as document files that include a documented report for each assignment. Remember that all Figures and Tables in your documents should be captioned and labeled appropriately. **All files for each submission should be zipped into a single project file and submitted via Blackboard**.

All assignments are due according to the dates in the Calendar.

Late submissions will be reduced by 5 points of the possible 100 points per assignment for each week late. This includes assignments submitted late due to work-related travel. It is the students' responsibility to make sure they can manage their course work with their professional work. If there are extenuating circumstances (such as medical emergencies) which make it impossible for you to get the assignment submitted on time, then there will be no late penalty.

Lab assignments are to be completed independently. Helping each other with tool-related problems, class material, or general VHDL knowledge is allowed and encouraged using the discussion forum. Copying assignments from other students or from the Web is not allowed. Exceptions to this are using snippets of code I present in the modules as partial solutions to the assignments.

Assignments are to be well documented and appropriately designed. Simply getting the design to meet requirements for demonstration is not grounds for 100 points. The design should be done in a well-organized, understandable way, with appropriate comments. After the first assignment, I will often ask that the design should always be accompanied by a block diagram of your design – this should be developed BEFORE you start to implement your design. Analyzing the FPGA resource utilization for each assignment is necessary and required.

Each lab assignment lists several items I will look for when evaluating your submissions. Meeting all items may not guarantee a complete grade. It is my discretion how points are awarded, or deducted, for each lab assignment. For example, bugs not specifically detailed in the lab description are still considered as bugs. Copying and pasting the resource utilization summary without analyses is not acceptable.

The combination of all these factors plays a role in determining the lab grade.

Lab Assignments are graded as follows:

100–90 = A—Design submitted on time that completely meets ALL specifications outlined in the assignment and is free of bugs. The student also carried out the following for each lab assignment:

- Implemented a well-organized design
- Included well-commented VHDL code
- Included a block diagram of the design
- Analyzed the design by estimating and studying the resource utilization
- Constructed a well-organized report

89–80 = B—A majority of the design requirements met that may include a few bugs the instructor happens to notice. Points can be deducted for poorly coded or poorly commented VHDL; even if the design works fine on the FPGA. Points can also be deducted for incomplete analyses, reports or missing block diagrams.

79–70=C—Design partially works with at least half of the specifications met. Submission does not include design analyses, block diagrams or report. VHDL coding style does not follow good design practices and lacks comments.

<70=F—Design does not work at all and submission fails to demonstrate any understanding of the design process.

3. **Quizzes** (10% of Final Grade Calculation)

Brief quizzes will be assigned for each module and will be due by the posted due date. The quizzes cover, in a very straight-forward manner, concepts presented in the module lectures. The lowest quiz score will be dropped. There will be a quiz for every module unless told otherwise.

Quizzes are graded as follows:

10 - 8 = A

7 - 6 = B

6 - 5 = C

< 5 = F

Late quiz submissions will not be accepted. As a result, I will drop the lowest quiz grade.

4. **Exam** (35% of Final Grade Calculation)

The only exam for the course will be available in the week of Module 10 and is referred to as a Midterm Exam. You will have a two day block within which you will have six hours to complete the exam and submit the solution via Blackboard. The exam will consist of eight problems where some problems are further divided into several parts. The midterm will cover concepts and material covered up to and including Module 9. This includes material covered in lecture videos, class discussions (forums), quizzes, lab assignments, assigned and optional readings, hosted videos and recorded office hours. You may use your course notes and module materials for the exam. Since this is a course that discusses VHDL code and syntax in detail***, you will be expected to write VHDL code using correct syntax to solve some of the exam problems***.

100–90 = A

89–80 = B

69–60 = C

<60 = F

Grading

Assignments are due according to the dates posted in your Blackboard course site. You may check these due dates in the Course Calendar or the Assignments in the corresponding modules. I will post grades one week after assignment due dates. If you do not receive a grade on an assignment that you have turned in, please ask of its whereabouts; it may need to be resubmitted.

Assignments are expected to be submitted using Blackboard as indicated in the assignment instructions; it will be considered late if it is received after that time. Special circumstances (e.g., temporary lack of internet access) can be accommodated if you inform me in advance. Assignments that are unjustifiably late will have the grade reduced by 5 points per assignment for each week it is late.

Instructors generally do not directly grade spelling and grammar. However, egregious violations of the rules of the English language will be noted without comment. Consistently poor performance in either spelling or grammar is taken as an indication of poor written communication ability that may detract from your grade.

A grade of A indicates achievement of consistent excellence and distinction throughout the course—that is, conspicuous excellence in all aspects of assignments and discussion in every week.

A grade of B indicates work that meets all course requirements on a level appropriate for graduate academic work. These criteria apply to both undergraduates and graduate students taking the course.

EP uses a +/- grading system (see “Grading System”, *Graduate Programs* catalog, p. 9).

Final grades for this course are based on the following scale

Letter Grade	Final Average
A+	100-98
A	97-94
A−	93-90
B+	89-87
B	86-83
B−	82-80
C	79-70
F	<70

Final grades for this course will be determined by the following weighting:

Item	% of Grade
Preparation and Participation (Module Discussions)	10%
Lab Assignments	45%
Quizzes	10%
Exam	35%

Late Assignment Submissions Due to Travel

It happens that students will have work-related travel plans and will be in a situation where they cannot work on a particular assignment due to lack of internet access or the lack of personal time due to extended work days or both. If you know you will have travel plans, please inform the instructor ahead of time. While difficult, it is possible to catch up with the course work and material due to missing one week of class. However, missing more than one week of class will make it very difficult to catch up and submit subsequent assignments on time. It is the students' responsibility to manage their travel plans during the semester and to catch up on all course material.

Help & Support

You should refer to Help & Support on the left menu for a listing of all the student services and support available.

Academic Misconduct Policy

You should read policies pertaining to academic misconduct and netiquette at http://ep.jhu.edu/genpolguid. Please read below how the Academic Misconduct Policy applies to your course.

Collaborations and discussions between students are key ingredients to success in a graduate course. You are encouraged to discuss the course material with each other as you sort through concepts that may be difficult to comprehend or controversial. However, the line between collaboration and cheating needs to be carefully delineated. Whenever you turn in work with your name on it to be evaluated, graded and included in your record it must represent an individual effort by you alone. If you include direct quotes from any source in your discussions, written assignments, the final exam, or any other submission for which you will receive a grade you must provide attribution. Students using published material without reference, or copying the work of another individual will receive a warning at the first incident. Any further incidents will result in the student receiving a zero on the assignment and the matter will be referred to the Associate Dean. Contact us if you have any questions, no matter how slight, about this policy, or if you have questions about a particular assignment.

Plagiarism

Plagiarism is defined as taking the words, ideas or thoughts of another and representing them as one's own. If you use the ideas of another, provide a complete citation in the source work; if you use the words of another, present the words in the correct quotation notation (indentation or enclosed in quotation marks, as appropriate) and include a complete citation to the source. See the course text for examples.

Policy on Disability Services

Johns Hopkins University (JHU) is committed to creating a welcoming and inclusive environment for students, faculty, staff and visitors with disabilities. The University does not discriminate on the basis of race, color, sex, religion, sexual orientation, national or ethnic origin, age, disability or veteran status in any student program or activity, or with regard to admission or employment. JHU works to ensure that students, employees and visitors with disabilities have equal access to university programs, facilities, technology and websites.

Under Section 504 of the Rehabilitation Act of 1973, the Americans with Disabilities Act (ADA) of 1990 and the ADA Amendments Act of 2008, a person is considered to have a disability if c (1) he or she has a physical or mental impairment that substantially limits one or more major life activities (such as hearing, seeing, speaking, breathing, performing manual tasks, walking, caring for oneself, learning, or concentrating); (2) has a record of having such an impairment; or (3) is regarded as having such an impairment class. The University provides reasonable and appropriate accommodations to students and employees with disabilities. In most cases, JHU will require documentation of the disability and the need for the specific requested accommodation.
The Disability Services program within the Office of Institutional Equity oversees the coordination of reasonable accommodations for students and employees with disabilities, and serves as the central point of contact for information on physical and programmatic access at the University. More information on this policy may be found at http://web.jhu.edu/administration/jhuoie/disability/index.html or by contacting (410) 516-8075.

Disability Services

Johns Hopkins Engineering for Professionals is committed to providing reasonable and appropriate accommodations to students with disabilities.

Students requiring accommodations are encouraged to contact Disability Services at least four weeks before the start of the academic term or as soon as possible. Although requests can be made at any time, students should understand that there may be a delay of up to two weeks for implementation depending on the nature of the accommodations requested.

Requesting Accommodation

New students must submit a Student Request for Accommodation form along with supporting documentation from a qualified diagnostician that:

- Identifies the type of disability
- Describes the current level of functioning in an academic setting
- Lists recommended accommodations

Questions about disability resources and requests for accommodation at Johns Hopkins Engineering for Professionals should be directed to:
Mark Tuminello
Disability Services Coordinator
Phone 410-516-2306
Fax 410-579-8049
E-mail mtumine2@jhu.edu or ep-disability-svcs@jhu.edu