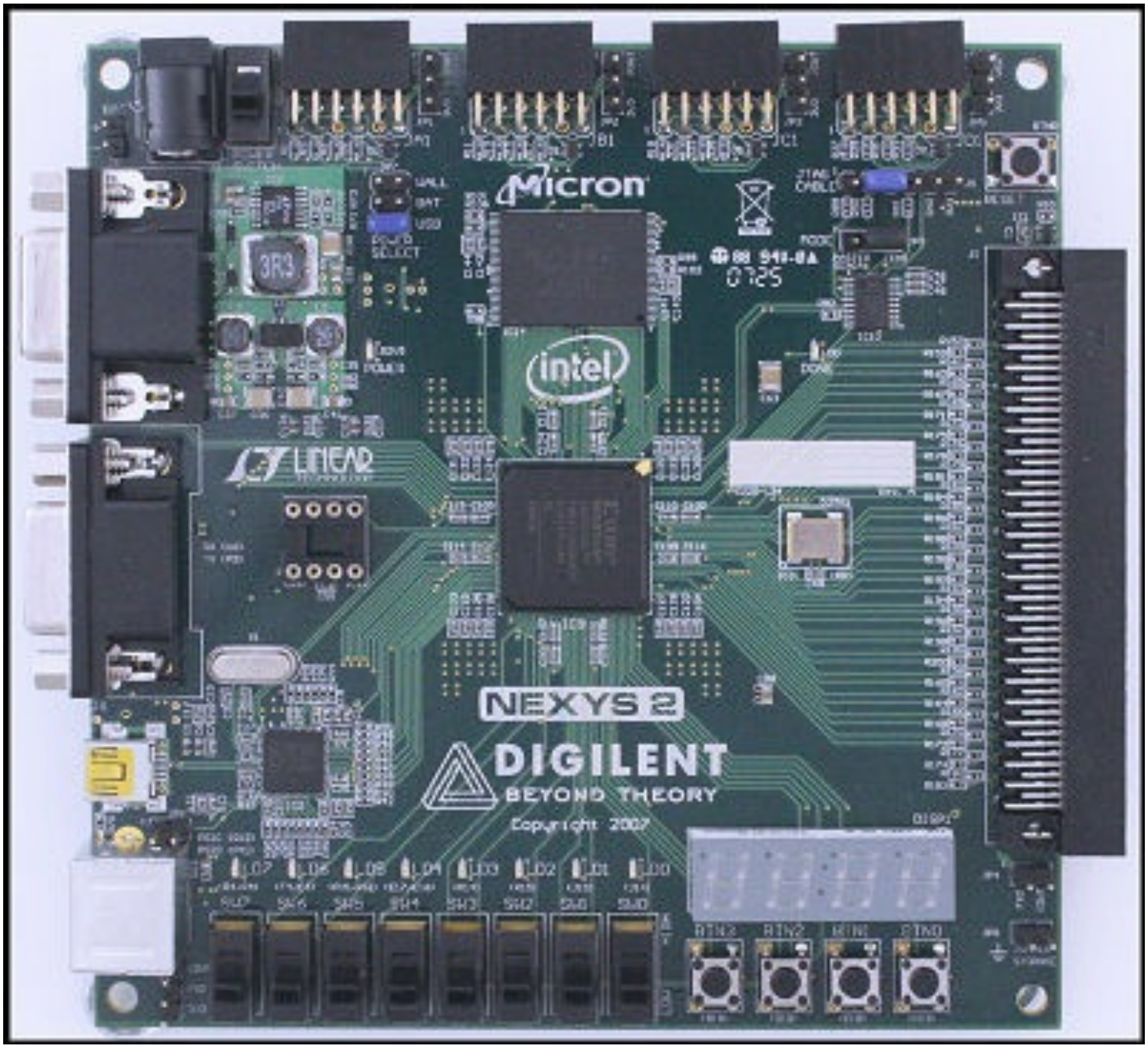
Getting Started With the NEXYS2 Spartan 3E Kit and Development Tools A Beginner’s Tutorial



Goal

In this tutorial, we will go through the creation of a simple FPGA design using the Xilinx Spartan 3E on the Digilent Nexys2 board. By no means will all features of the board or tools be covered, as this is intended to provide a starting point to those unfamiliar with the Xilinx tools and/or FPGA design in general.

Tools

1. Xilinx ISE

Install Xilinx ISE Version 13.1 or newer from the following website:

http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html

NOTE: Do not install the Xilinx Vivado Design Tools. We will not be using Xilinx Vivado for this course.

The process to download and install the Xilinx ISE tool **can take a long time**. The installation files are in the order of several GB and the installation process can take up to a day. You are responsible for installing the tools on any of your personal computer(s) and making sure that they work properly. Any issues you may encounter with the installation process would need to be resolved with the help of the Xilinx support center.

2. Digilent Adept

In addition to the Xilinx ISE tool, you will need to download the Digilent Adept utility which allows you to program the Nexys2 development board via USB. The Adept utility can be located at:

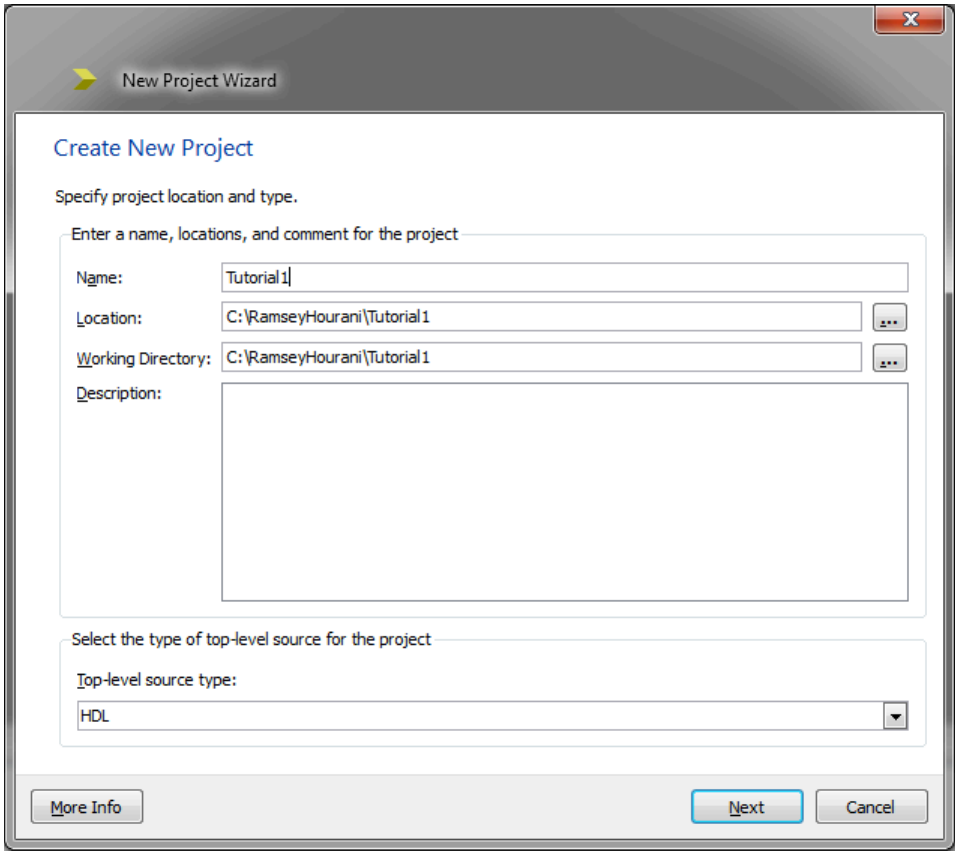
http://digilentinc.com/Products/Detail.cfm?NavPath=2,66,828&Prod=ADEPT2

Make sure you download the correct installation files for your operating system and confirm that the Adept tool can communicate with the Nexys2 development board, as explained later in this tutorial.

The Project

For this lesson, we will tackle the most basic of devices on the Nexys2 board; the slider switches and seven-segment display. Our goal is simple enough: use the 4 slider switches SW3 to SW0 to represent a 4-bit binary number whose value can be hex 0-F. We would like to display that value on the rightmost seven-segment display, and leave the rest of the digits blank.

To start the design, first start Xilinx ISE, and create a new Project with *File* → *New Project*. When specifying the project name and directory, pick a location without any spaces in the path (i.e. not the desktop). You will often find the Xilinx tools behave strangely with difficult to diagnose errors if you have spaces in the project path. Click Next to advance to the next page.



New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: Tutorial1

Location: C:\RamseyHourani\Tutorial1

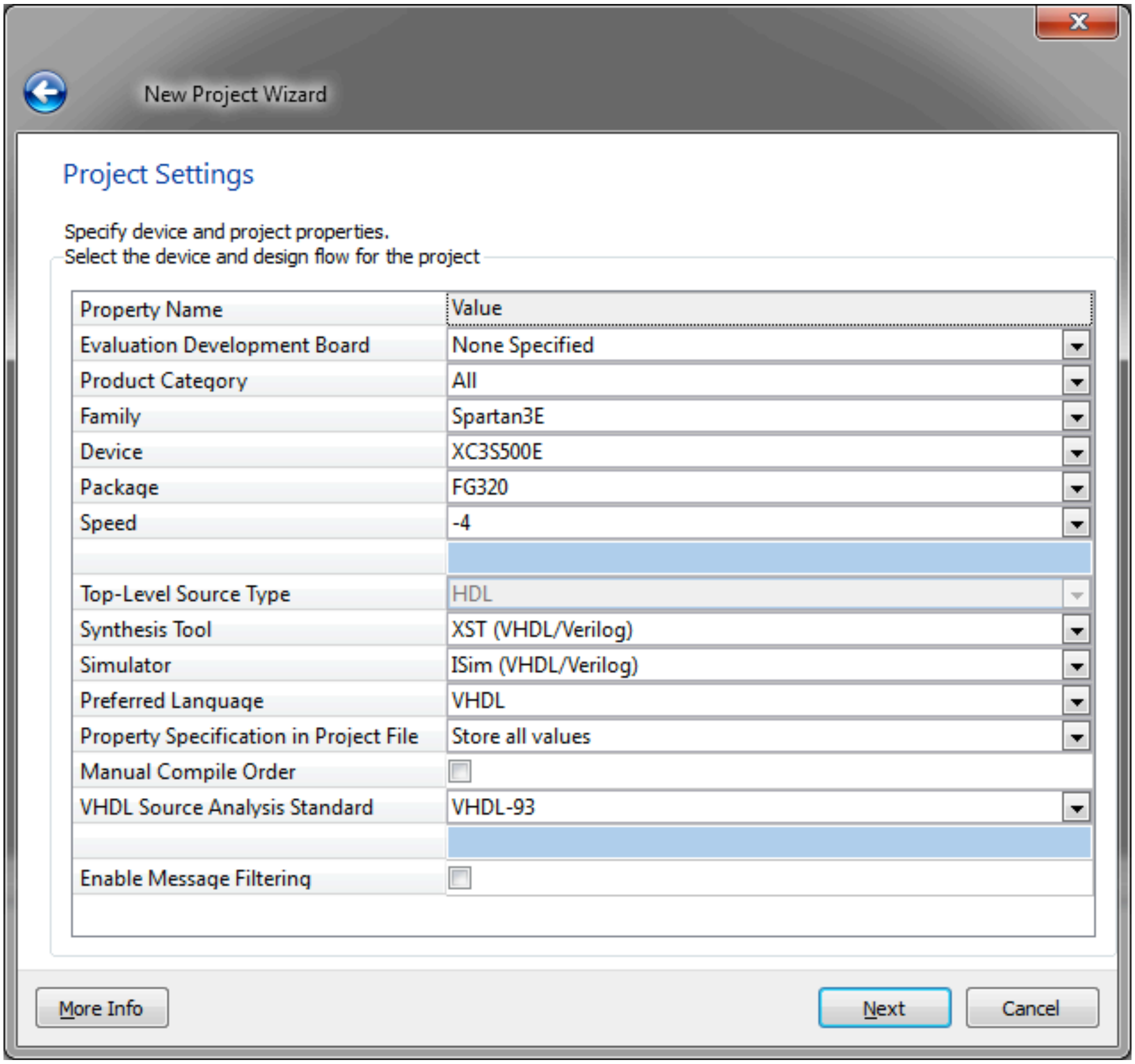
Working Directory: C:\RamseyHourani\Tutorial1

Description:

Select the type of top-level source for the project

Top-level source type: HDL

The next step will be to specify the FPGA you are targeting. This is the one that is on the Nexys2 board. The FGPA installed on the Nexys2 development board is the Spartan 3E XC3S500E-FG320-4. This FPGA has 500,000 gates, 320 pins and a speed grade of 4, which meets commercial standards, as opposed to military or flight standards. We will use the Xilinx Synthesis Tools (XST) and the Xilinx ISim simulator. The preferred language for the hardware description of our designs will be VHDL and VHDL-93 syntax is appropriate for this course.



Project Settings

Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	☐
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	☐

Once you've entered the necessary parameters as shown in the window above, click Next to advance to the next page, briefly look over the project summary and then click Finish to complete the project creation and begin the design process.

Entering VHDL

To describe the design, we will add one simple VHDL file to our project. This is best done using the ISE text editor. Start a new VHDL file by selecting *File* → *New* from the menu and then selecting "Text File". This will create a blank text file in the ISE editor.

Copy and paste the following snippet of VHDL code into the ISE text editor. Save this VHDL file as `toplevel.vhd`

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use work.all;

entity toplevel is Port (
   switches : in STD_LOGIC_VECTOR (3 downto 0);
   sevenseg : out STD_LOGIC_VECTOR (6 downto 0);
   anodes : out STD_LOGIC_VECTOR (3 downto 0));
end toplevel;

architecture Behavioral of toplevel is
begin

with switches select
sevenseg <=
   "1000000" when x"0" ,
   "1111001" when x"1" ,
   "0100100" when x"2" ,
   "0110000" when x"3" ,
   "0011001" when x"4" ,
   "0010010" when x"5" ,
   "0000010" when x"6" ,
   "1111000" when x"7" ,
   "0000000" when x"8" ,
   "0010000" when x"9" ,
   "0001000" when x"A" ,
   "0000011" when x"B" ,
   "1000110" when x"C" ,
   "0100001" when x"D" ,
   "0000110" when x"E" ,
   "0001110" when others;

anodes <= "1110";

end Behavioral;
```

After entering the VHDL code and saving the file, add the `top_level.vhd` source to the project by selecting *Project* → *Add Source* from the menu and then selecting the `top_level.vhd` file.

Assigning Pins

The next task is to assign our top level input and output ports to the correct FPGA locations. If we neglect this step, the pins would be assigned by the Xilinx software to random locations, which would not be good. To do this, we must first create a new file, the "User Constraints File" (`.ucf`). This will be done with *Project → New Source* as before and select "Text File".

Once the blank file opens in the text editor, add the following pin constraints to the file:

```
NET "anodes<0>" LOC = "F17";
NET "anodes<1>" LOC = "H17";
NET "anodes<2>" LOC = "C18";
NET "anodes<3>" LOC = "F15";

NET "sevenseg<0>" LOC = "L18";
NET "sevenseg<1>" LOC = "F18";
NET "sevenseg<2>" LOC = "D17";
NET "sevenseg<3>" LOC = "D16";
NET "sevenseg<4>" LOC = "G14";
NET "sevenseg<5>" LOC = "J17";
NET "sevenseg<6>" LOC = "H14";

NET "switches<0>" LOC = "G18";
NET "switches<1>" LOC = "H18";
NET "switches<2>" LOC = "K18";
NET "switches<3>" LOC = "K17";
```

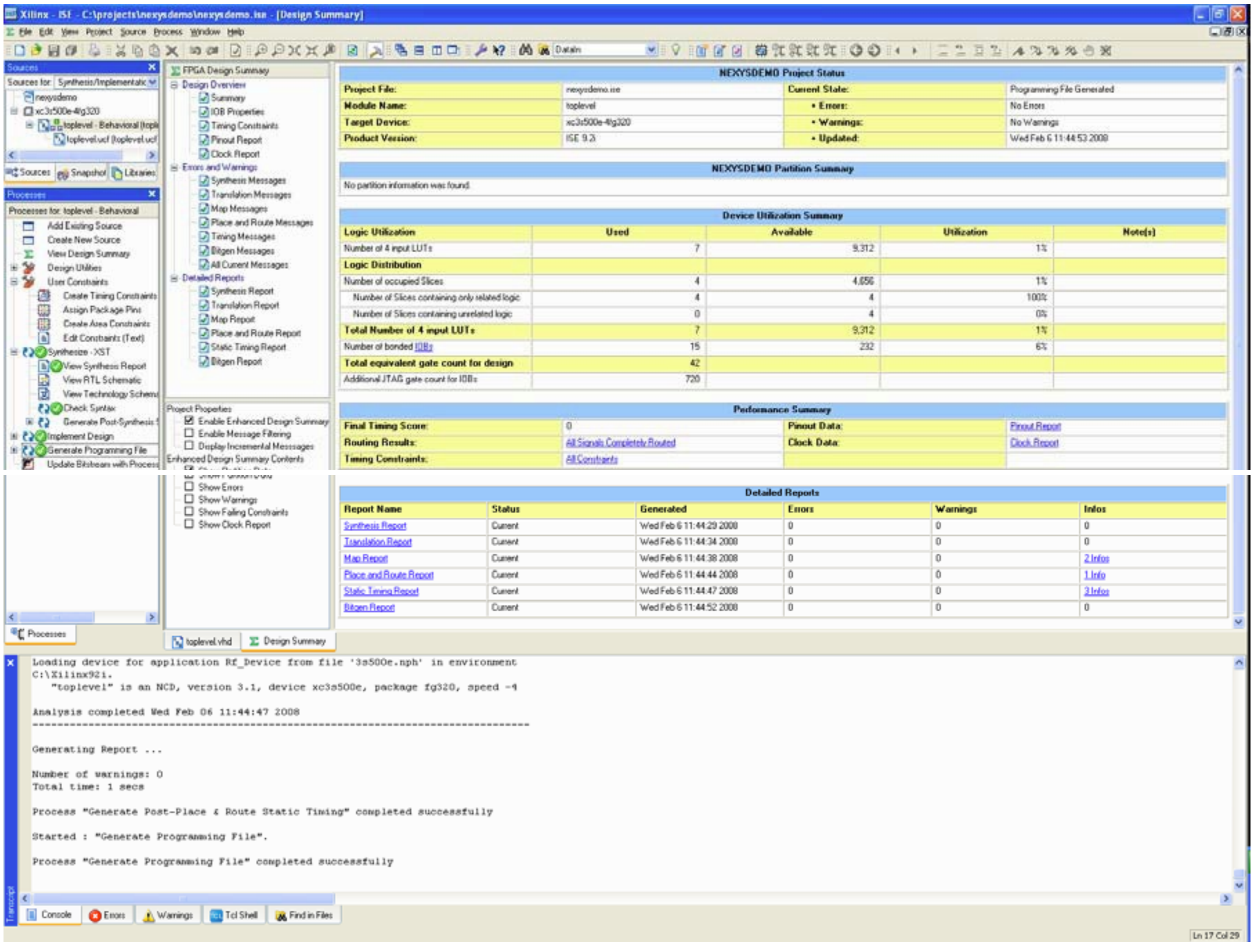
You can also download the complete UCF file for the Neyx2 board for the Digilent website. However, you will need to modify that UCF file to account for the top-level ports you have created.

Save the file as `top_level.ucf` and add the file to the project by selecting *Project → Add Source* from the menu.

Now we are ready to synthesize the design.

Synthesis, Place-&-Route, Generating Programming File

The next step in the process is to have the Xilinx ISE tool create a programming file for you which you can download to the FPGA. The whole process can be completed by clicking once on your top-level design in the Sources Pane, followed by a double-click on "Generate Programming File". This will run the whole process, and should complete as in the screenshot below.



NEXYSDEMO Project Status			
Project File:	nexysdemo.ise	**Current State:**	Programming File Generated
Module Name:	toplevel	**• Errors:**	No Errors
Target Device:	xc3s500e-4fg320	**• Warnings:**	No Warnings
Product Version:	ISE 9.2i	**• Updated:**	Wed Feb 6 11:44:53 2008

NEXYSDEMO Partition Summary

No partition information was found.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	7	9,312	1%	
Logic Distribution				
Number of occupied Slices	4	4,656	1%	
Number of Slices containing only related logic	4	4	100%	
Number of Slices containing unrelated logic	0	4	0%	
Total Number of 4 input LUTs	7	9,312	1%	
Number of bonded IOBs	15	232	6%	
Total equivalent gate count for design	42			
Additional JTAG gate count for IOBs	720			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints		

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed Feb 6 11:44:29 2008	0	0	0
Translation Report	Current	Wed Feb 6 11:44:34 2008	0	0	0
Map Report	Current	Wed Feb 6 11:44:38 2008	0	0	2 Infos
Place and Route Report	Current	Wed Feb 6 11:44:44 2008	0	0	1 Info
Static Timing Report	Current	Wed Feb 6 11:44:47 2008	0	0	3 Infos
Bitgen Report	Current	Wed Feb 6 11:44:52 2008	0	0	0

```
Loading device for application Rf_Device from file '3s500e.nph' in environment
C:\Xilinx92i.
   "toplevel" is an NCD, version 3.1, device xc3s500e, package fg320, speed -4

Analysis completed Wed Feb 06 11:44:47 2008
--------------------------------------------------------------------------------

Generating Report ...

Number of warnings: 0
Total time: 1 secs

Process "Generate Post-Place & Route Static Timing" completed successfully

Started : "Generate Programming File".

Process "Generate Programming File" completed successfully
```

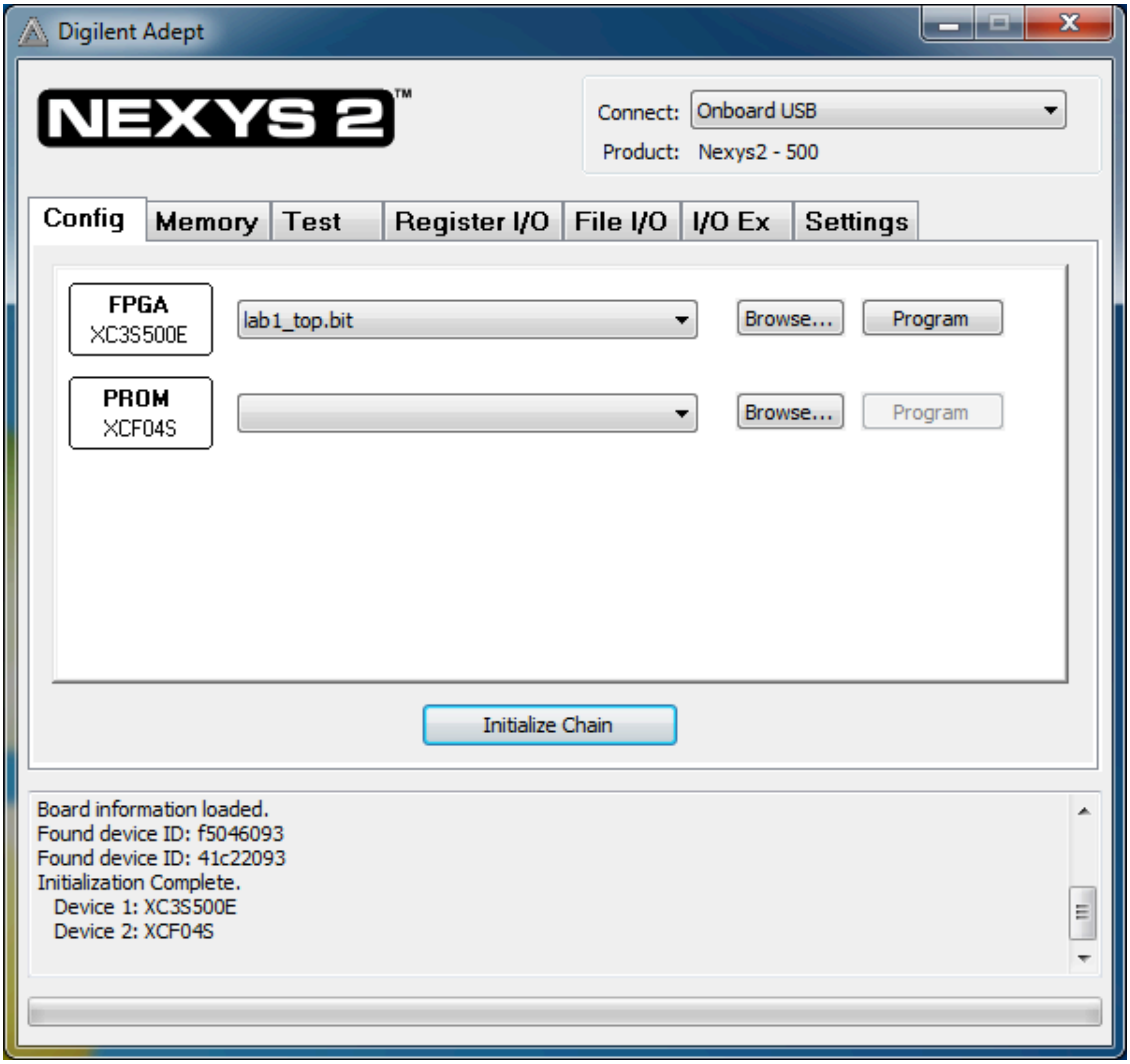
Configuration

Now that the programming (bit) file has been generated, it is time to load your design into the FPGA, and test it out. This can be done by using the Digilent Adept tool and the USB cable that accompanied the Nexys2 development board.

Configuration Using the USB Port and Digilent ADEPT Software Suite

Connect the USB cable from your computer to the development board. Power on the board and make sure that the board is powered (red power LED should turn on). Start up the Adept software and make sure that the Adept tool is able to recognize the Digilent Nexys-2 Board.

To program the **FPGA**, clock on the "Config" tab, then click on Browse button and browse to the configuration file and select your `top_level.bit` file. You can ignore the warning referencing the JTAG CLK. Similarly, if you would like to program the board to start on power-up, program the PROM (XCF04S) with the same bit file. Remember if loading your design from the PROM, the blue jumper needs to be connected to PROM. Note that newer versions of the Adept tool will have a slightly different view than the one shown below.



Connect: Onboard USB
Product: Nexys2 - 500

FPGA XC3S500E: lab1_top.bit

PROM XCF04S:

```
Board information loaded.
Found device ID: f5046093
Found device ID: 41c22093
Initialization Complete.
  Device 1: XC3S500E
  Device 2: XCF04S
```

Click “Program” and wait a couple of seconds. When configuration is complete, your FPGA should be operating as your VHDL design specified. If you would like the board to run with this configuration on power-up, just make sure that the Mode Jumper (JP9) is set in the “ROM” position. **Be careful not to switch jumpers while the board is powered on**. To switch a jumper, power off the board, move the jumper, then power on the board again.