# Media Computer System for the Altera DE2 Board

*For Quartus II 13.0*

## 1 Introduction

This document describes a computer system that can be implemented on the Altera DE2 development and education board. This system, called the *DE2 Media Computer*, is intended to be used for experiments in computer organization and embedded systems. To support these experiments, the system contains a processor, memory, video devices, and some simple I/O peripherals. The FPGA programming file that implements this system, as well as its design source files, can be obtained from the University Program section of Altera's web site.

## 2 DE2 Media Computer Contents

A block diagram of the DE2 Media Computer is shown in Figure 1. Its main components include the Altera Nios II processor, memory for program and data storage, an audio-in/out port, a video-out port with both pixel and character buffers, a video-in port, a PS/2 serial port, an Ethernet port, a USB port, a $16 \times 2$ character display, parallel ports connected to switches and lights, a timer module, an SD Card controller, an IrDA sender and reciever, and an RS 232 serial port. As shown in the figure, the processor and its interfaces to I/O devices are implemented inside the Cyclone®II FPGA chip on the DE2 board. A number of the components shown in Figure 1 are described in the remainder of this section, and the others are presented in section 4.

### 2.1 Nios II Processor

The Altera Nios®II processor is a 32-bit CPU that can be instantiated in an Altera FPGA chip. Three versions of the Nios II processor are available, designated economy (/e), standard (/s), and fast (/f). The DE2 Media Computer includes the Nios II/f version, which has an appropriate feature set for use in introductory experiments while also supporting more advanced applications. The Nios II processor is configured to include floating-point hardware support, which is described in section 4.9.

An overview of the Nios II processor can be found in the document *Introduction to the Altera Nios II Processor*, which is provided in the University Program's web site. An easy way to begin working with the DE2 Media Computer and the Nios II processor is to make use of a utility called the *Altera Monitor Program*. This utility provides an easy way to assemble and compile Nios II programs that are written in either assembly language or the C programming language. The Monitor Program, which can be downloaded from Altera's web site, is an application program that runs on the host computer connected to the DE2 board. The Monitor Program can be used to control the execution of code on Nios II, list (and edit) the contents of processor registers, display/edit the contents of memory on the DE2 board, and similar operations. The Monitor Program includes the DE2 Media Computer as a predesigned system that can be downloaded onto the DE2 board, as well as several sample programs in assembly language and C that show how to use the DE2 Media Computer's peripherals. Some images that show how the DE2 Media Computer

is integrated with the Monitor Program are described in section 8. An overview of the Monitor Program is available in the document *Altera Monitor Program Tutorial*, which is provided in the University Program web site.

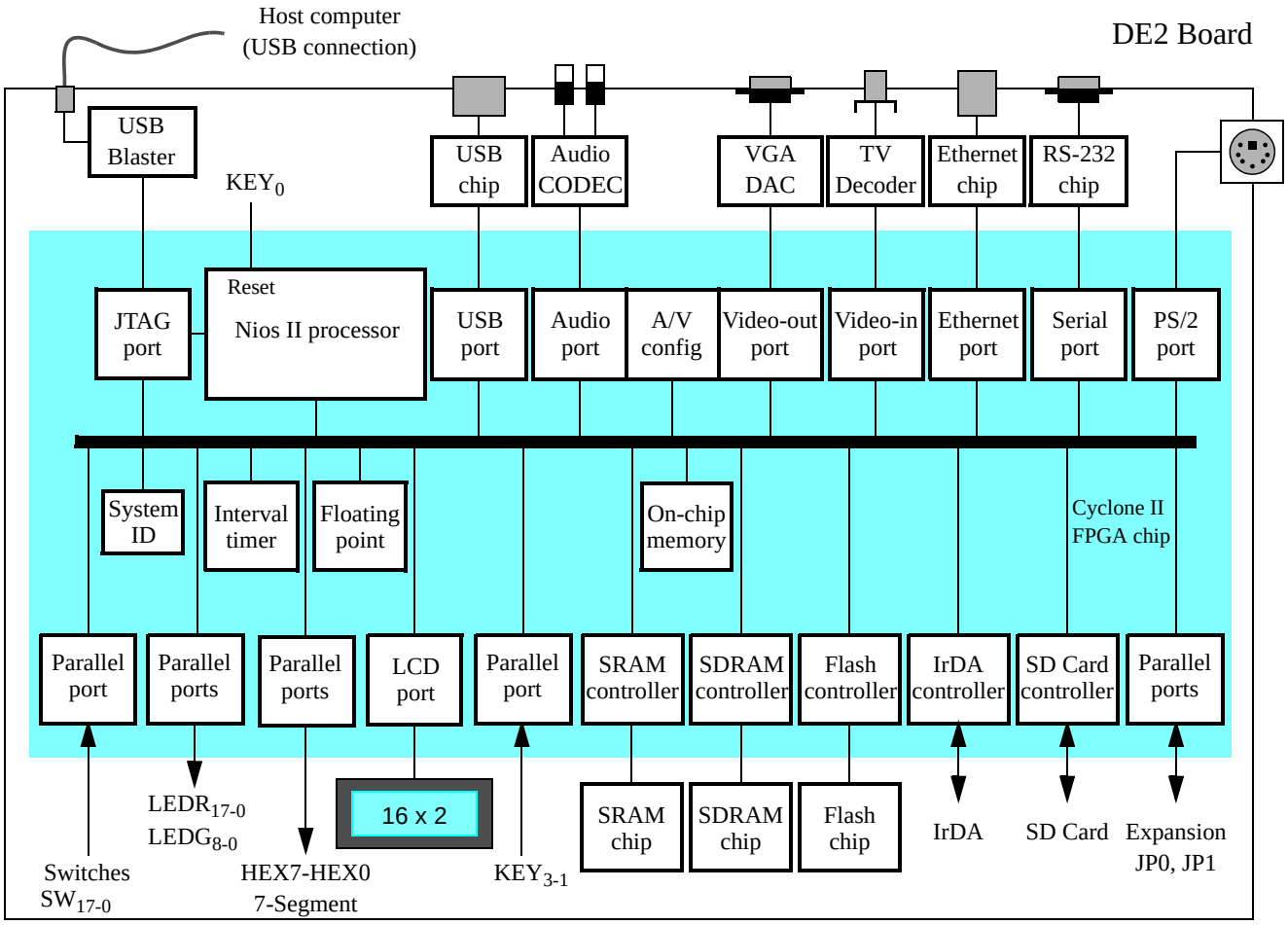



Figure 1. Block diagram of the DE2 Media Computer.

As indicated in Figure 1, the Nios II processor can be reset by pressing $KEY_0$ on the DE2 board. The reset mechanism is discussed further in section 3. All of the I/O peripherals in the DE2 Media Computer are accessible by the processor as memory mapped devices, using the address ranges that are given in the following subsections.

## 2.2 Memory Components

The DE2 Media Computer has three types of memory components: SDRAM, SRAM, and on-chip memory inside the FPGA chip. Each type of memory is described below.

### 2.2.1 SDRAM

An SDRAM Controller provides a 32-bit interface to the synchronous dynamic RAM (SDRAM) chip on the DE2 board, which is organized as 1M x 16 bits x 4 banks. It is accessible by the Nios II processor using word (32-bit), halfword (16-bit), or byte operations, and is mapped to the address space 0x00000000 to 0x007FFFFF.

### 2.2.2 SRAM

An SRAM Controller provides a 32-bit interface to the static RAM (SRAM) chip on the DE2 board. This SRAM chip is organized as 256K x 16 bits, but is accessible by the Nios II processor using word (32-bit), halfword (16-bit), or byte operations. The SRAM memory is mapped to the address space 0x08000000 to 0x0807FFFF.

### 2.2.3 On-Chip Memory

The DE2 Media Computer includes a 8-Kbyte memory that is implemented in the Cyclone II FPGA chip. This memory is organized as 8K x 8 bits, and spans addresses in the range 0x09000000 to 0x09001FFF. This memory is used as a character buffer for the video-out port, which is described in section 4.2.

### 2.2.4 SD Card

### 2.2.5 Flash

## 2.3 Parallel Ports

The DE2 Media Computer includes several parallel ports that support input, output, and bidirectional transfers of data between the Nios II processor and I/O peripherals. As illustrated in Figure 2, each parallel port is assigned a *Base* address and contains up to four 32-bit registers. Ports that have output capability include a writable *Data* register, and ports with input capability have a readable *Data* register. Bidirectional parallel ports also include a *Direction* register that has the same bit-width as the *Data* register. Each bit in the *Data* register can be configured

as an input by setting the corresponding bit in the *Direction* register to 0, or as an output by setting this bit position to 1. The *Direction* register is assigned the address *Base* + 4.

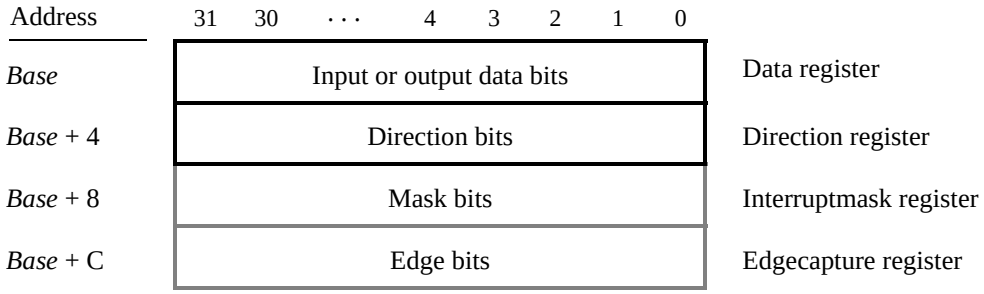



Figure 2. Parallel port registers in the DE2 Media Computer.

Some of the parallel ports in the DE2 Media Computer have registers at addresses *Base* + 8 and *Base* + C, as indicated in Figure 2. These registers are discussed in section 3.

### 2.3.1 Red and Green LED Parallel Ports

The red lights $LEDR_{17-0}$ and green lights $LEDG_{8-0}$ on the DE2 board are each driven by an output parallel port, as illustrated in Figure 3. The port connected to *LEDR* contains an 18-bit write-only *Data* register, which has the address 0x10000000. The port for *LEDG* has a nine-bit *Data* register that is mapped to address 0x10000010. These two registers can be written using word accesses, and the upper bits not used in the registers are ignored.

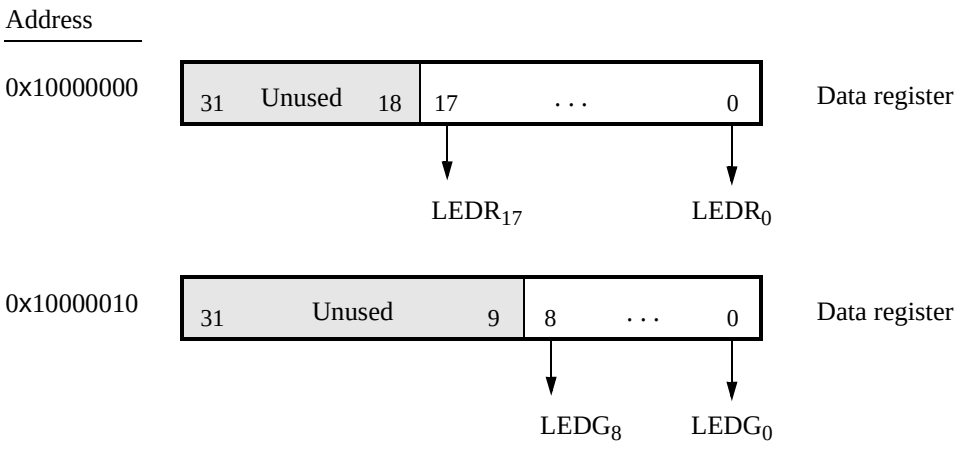



Figure 3. Output parallel ports for *LEDR* and *LEDG*.

### 2.3.2 7-Segment Displays Parallel Port

There are two parallel ports connected to the 7-segment displays on the DE2 board, each of which comprises a 32-bit write-only *Data* register. As indicated in Figure 4, the register at address 0x10000020 drives digits *HEX3* to *HEX0*,

and the register at address 0x10000030 drives digits *HEX7* to *HEX4*. Data can be written into these two registers by using word operations. This data directly controls the segments of each display, according to the bit locations given in Figure 4. The locations of segments 6 to 0 in each seven-segment display on the DE2 board is illustrated on the right side of the figure.

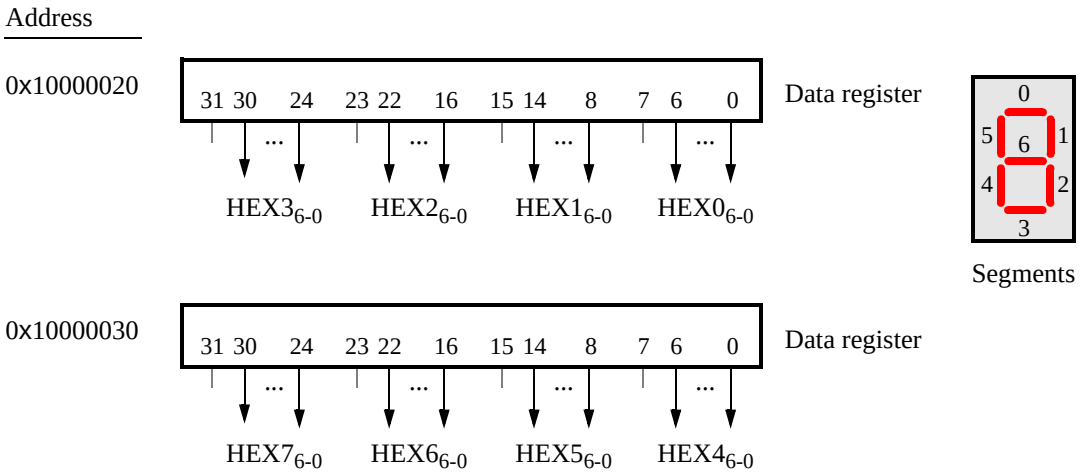



Figure 4. Bit locations for the 7-segment displays parallel ports.

### 2.3.3 Slider Switch Parallel Port

The $SW_{17-0}$ slider switches on the DE2 board are connected to an input parallel port. As illustrated in Figure 5, this port comprises an 18-bit read-only *Data* register, which is mapped to address 0x10000040.

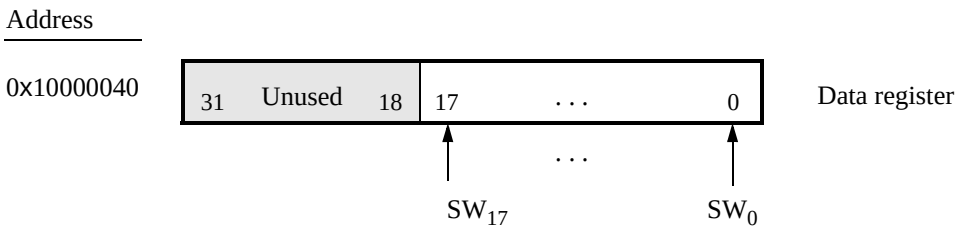



Figure 5. *Data* register in the slider switch parallel port.

### 2.3.4 Pushbutton Parallel Port

The parallel port connected to the $KEY_{3-1}$ pushbutton switches on the DE2 board comprises three 3-bit registers, as shown in Figure 6. These registers have the base addresses 0x10000050 to 0x1000005C and can be accessed using word operations. The read-only *Data* register provides the values of the switches $KEY_3$, $KEY_2$ and $KEY_1$. Bit 0 of the *Data* register is not used, because, as discussed in section 2.1, the corresponding switch $KEY_0$ is reserved for use as a reset mechanism for the DE2 Media Computer. The other two registers shown in Figure 6, at addresses

0x10000058 and 0x1000005C, are discussed in section 3.

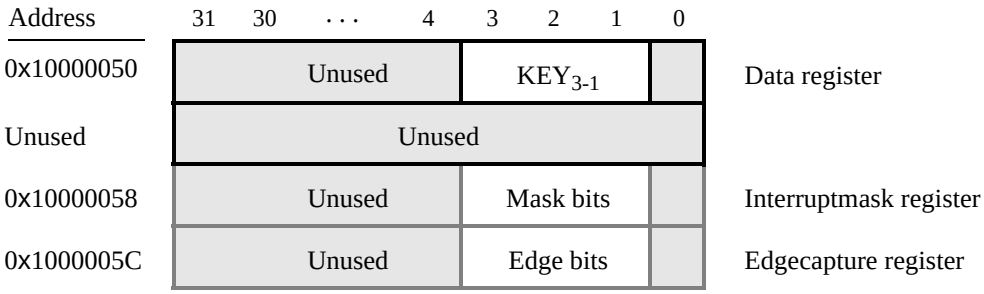



Figure 6. Registers used in the pushbutton parallel port.

### 2.3.5 Expansion Parallel Ports

### 2.3.6 Using the Parallel Ports with Assembly Language Code and C Code

The DE2 Media Computer provides a convenient platform for experimenting with Nios II assembly language code, or C code. A simple example of such code is provided in Figures 8 and 9. Both programs perform the same operations, and illustrate the use of parallel ports by using either assembly language or C code.

The code in the figures displays the values of the SW switches on the red LEDs, and the pushbutton keys on the green LEDs. It also displays a rotating pattern on 7-segment displays *HEX3* … *HEX0* and *HEX7* … *HEX4*. This pattern is shifted to the right by using a Nios II *rotate* instruction, and a delay loop is used to make the shifting slow enough to observe. The pattern on the HEX displays can be changed to the values of the SW switches by pressing any of pushbuttons $KEY_3$, $KEY_2$, or $KEY_1$ (recall from section 2.1 that $KEY_0$ causes a reset of the Nios II processor). When a pushbutton key is pressed, the program waits in a loop until the key is released.

The source code files shown in Figures 8 and 9 are distributed as part of the Altera Monitor Program. The files can be found under the heading *sample programs*, and are identified by the name *Getting Started*.

```
/*****************************************************************************
 * This program demonstrates the use of parallel ports in the DE2 Media Computer:
 *       1. displays the SW switch values on the red LEDR
 *       2. displays the KEY[3..1] pushbutton values on the green LEDG
 *       3. displays a rotating pattern on the HEX displays
 *       4. if KEY[3..1] is pressed, uses the SW switches as the pattern
*****************************************************************************/
.text                                   /* executable code follows */
.global _start
_start:
    /* initialize base addresses of parallel ports */
    movia     r15, 0x10000040           /* SW slider switch base address */
    movia     r16, 0x10000000           /* red LED base address */
    movia     r17, 0x10000050           /* pushbutton KEY base address */
    movia     r18, 0x10000010           /* green LED base address */
    movia     r20, 0x10000020           /* HEX3_HEX0 base address */
    movia     r21, 0x10000030           /* HEX7_HEX4 base address */
    movia     r19, HEX_bits
    ldwio     r6, 0(r19)                /* load pattern for HEX displays */

DO_DISPLAY:
    ldwio     r4, 0(r15)                /* load input from slider switches */
    stwio     r4, 0(r16)                /* write to red LEDs */
    ldwio     r5, 0(r17)                /* load input from pushbuttons */
    stwio     r5, 0(r18)                /* write to green LEDs */
    beq       r5, r0, NO_BUTTON
    mov       r6, r4                    /* copy SW switch values onto HEX displays */
WAIT:
    ldwio     r5, 0(r17)                /* load input from pushbuttons */
    bne       r5, r0, WAIT              /* wait for button release */
NO_BUTTON:
    stwio     r6, 0(r20)                /* store to HEX3 ... HEX0 */
    stwio     r6, 0(r21)                /* store to HEX7 ... HEX4 */
    roli      r6, r6, 1                 /* rotate the displayed pattern */
    movia     r7, 500000                /* delay counter */
DELAY:
    subi      r7, r7, 1
    bne       r7, r0, DELAY
    br        DO_DISPLAY

.data                                   /* data follows */
HEX_bits:
    .word 0x0000000F
.end
```

Figure 8. An example of Nios II assembly language code that uses parallel ports.

```
/*****************************************************************************
 * This program demonstrates the use of parallel ports in the DE2 Media Computer:
 *      1. displays the SW switch values on the red LEDR
 *      2. displays the KEY[3..1] pushbutton values on the green LEDG
 *      3. displays a rotating pattern on the HEX displays
 *      4. if KEY[3..1] is pressed, uses the SW switches as the pattern
*****************************************************************************/
int main(void)
{
   /* Declare volatile pointers to I/O registers (volatile means that IO load and store
      instructions (e.g., ldwio, stwio) will be used to access these pointer locations) */
   volatile int * red_LED_ptr      = (int *) 0x10000000;    // red LED address
   volatile int * green_LED_ptr    = (int *) 0x10000010;    // green LED address
   volatile int * HEX3_HEX0_ptr    = (int *) 0x10000020;    // HEX3_HEX0 address
   volatile int * HEX7_HEX4_ptr    = (int *) 0x10000030;    // HEX7_HEX4 address
   volatile int * SW_switch_ptr    = (int *) 0x10000040;    // SW slider switch address
   volatile int * KEY_ptr          = (int *) 0x10000050;    // pushbutton KEY address

   int HEX_bits = 0x0000000F;                   // pattern for HEX displays
   int SW_value, KEY_value;
   volatile int delay_count;                    // volatile so C compile does not remove loop

   while(1)
   {
       SW_value = *(SW_switch_ptr);             // read the SW slider switch values
       *(red_LED_ptr) = SW_value;               // light up the red LEDs
       KEY_value = *(KEY_ptr);                  // read the pushbutton KEY values
       *(green_LED_ptr) = KEY_value;            // light up the green LEDs
       if (KEY_value != 0)                      // check if any KEY was pressed
       {
           HEX_bits = SW_value;                 // set pattern using SW values
           while (*KEY_ptr);                    // wait for pushbutton KEY release
       }
       *(HEX3_HEX0_ptr) = HEX_bits;             // display pattern on HEX3 ... HEX0
       *(HEX7_HEX4_ptr) = HEX_bits;             // display pattern on HEX7 ... HEX4

       if (HEX_bits & 0x80000000)               /* rotate the pattern shown on the HEX displays */
           HEX_bits = (HEX_bits << 1) | 1;
       else
           HEX_bits = HEX_bits << 1;

       for (delay_count = 500000; delay_count != 0; --delay_count); // delay loop
   } // end while
}
```

Figure 9. An example of C code that uses parallel ports.

## 2.4 JTAG Port

The JTAG port implements a communication link between the DE2 board and its host computer. This link is automatically used by the Quartus II software to transfer FPGA programming files into the DE2 board, and by the Altera Monitor Program. The JTAG port also includes a UART, which can be used to transfer character data between the host computer and programs that are executing on the Nios II processor.

### 2.4.1 Using the JTAG UART with Assembly Language Code and C Code

## 2.5 Serial Port

## 2.6 IrDA Port

## 2.7 Interval Timer

The DE2 Media Computer includes a timer that can be used to measure various time intervals. The interval timer is loaded with a preset value, and then counts down to zero using the 50-MHz clock signal provided on the DE2 board. The programming interface for the timer includes six 16-bit registers, as illustrated in Figure 15. The 16-bit register at address 0x10002000 provides status information about the timer, and the register at address 0x10002004 allows control settings to be made. The bit fields in these registers are described below:

- *TO* provides a timeout signal which is set to 1 by the timer when it has reached a count value of zero. The *TO* bit can be reset by writing a 0 into it.
- *RUN* is set to 1 by the timer whenever it is currently counting. Write operations to the status halfword do not affect the value of the *RUN* bit.
- *ITO* is used for generating Nios II interrupts, which are discussed in section 3.
- *CONT* affects the continuous operation of the timer. When the timer reaches a count value of zero it automatically reloads the specified starting count value. If *CONT* is set to 1, then the timer will continue counting down automatically. But if *CONT* = 0, then the timer will stop after it has reached a count value of 0.
- (*START*/*STOP*) can be used to commence/suspend the operation of the timer by writing a 1 into the respective bit.

The two 16-bit registers at addresses 0x10002008 and 0x1000200C allow the period of the timer to be changed by setting the starting count value. The default setting provided in the DE2 Media Computer gives a timer period of 125 msec. To achieve this period, the starting value of the count is 50 MHz × 125 msec = $6.25 \times 10^6$. It is possible to capture a snapshot of the counter value at any time by performing a write to address 0x10002010. This

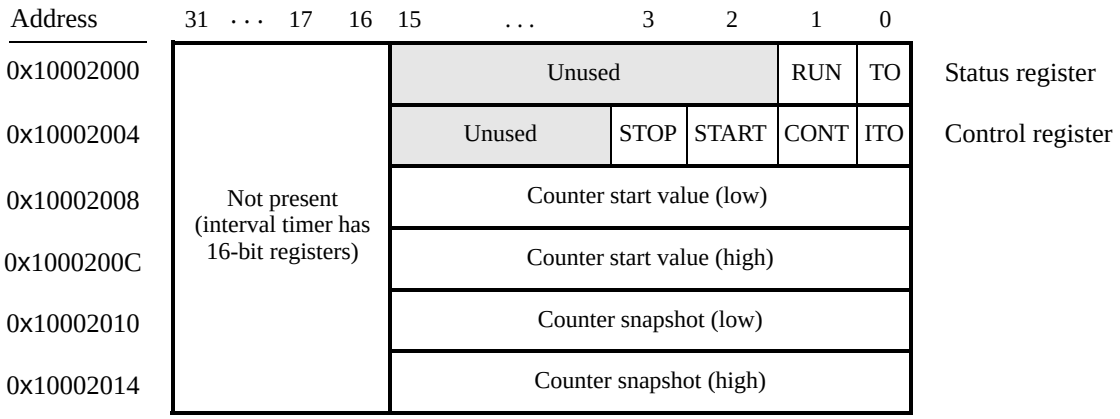



Figure 15. Interval timer registers.

write operation causes the current 32-bit counter value to be stored into the two 16-bit timer registers at addresses 0x10002010 and 0x10002014. These registers can then be read to obtain the count value.

### 2.8 System ID

The system ID module provides a unique value that identifies the DE2 Media Computer system. The host computer connected to the DE2 board can query the system ID module by performing a read operation through the JTAG port. The host computer can then check the value of the returned identifier to confirm that the DE2 Media Computer has been properly downloaded onto the DE2 board. This process allows debugging tools on the host computer, such as the Altera Monitor Program, to verify that the DE2 board contains the required computer system before attempting to execute code that has been compiled for this system.

## 3 Exceptions and Interrupts

The reset address of the Nios II processor in the DE2 Media Computer is set to 0x00000000. The address used for all other general exceptions, such as divide by zero, and hardware IRQ interrupts is 0x00000020. Since the Nios II processor uses the same address for general exceptions and hardware IRQ interrupts, the Exception Handler software must determine the source of the exception by examining the appropriate processor status register. Table 1 gives the assignment of IRQ numbers to each of the I/O peripherals in the DE2 Media Computer. The rest of this section describes the interrupt behavior associated with the interval timer, parallel ports, and serial ports in the DE2 Media Computer. Interrupts for other devices listed in Table 1 are discussed in section 4.

### 3.1 Interrupts from Parallel Ports

Parallel port registers in the DE2 Media Computer were illustrated in Figure 2, which is reproduced as Figure 16. As the figure shows, parallel ports that support interrupts include two related registers at the addresses *Base* + 8 and *Base* + C. The *Interruptmask* register, which has the address *Base* + 8, specifies whether or not an interrupt signal should

| I/O Peripheral | IRQ # |
|---|---|
| Interval timer | 0 |
| Pushbutton switch parallel port | 1 |
| USB Port | 2 |
| Ethernet Port | 3 |
| Audio port | 6 |
| PS/2 port | 7 |
| JTAG port | 8 |
| IrDA port | 9 |
| Serial port | 10 |
| JP1 Expansion parallel port | 11 |
| JP2 Expansion parallel port | 12 |

Table 1. Hardware IRQ interrupt assignment for the DE2 Media Computer.

be sent to the Nios II processor when the data present at an input port changes value. Setting a bit location in this register to 1 allows interrupts to be generated, while setting the bit to 0 prevents interrupts. Finally, the parallel port may contain an *Edgecapture* register at address *Base* + C. Each bit in this register has the value 1 if the corresponding bit location in the parallel port has changed its value from 0 to 1 since it was last read. Performing a write operation to the *Edgecapture* register sets all bits in the register to 0, and clears any associated Nios II interrupts.

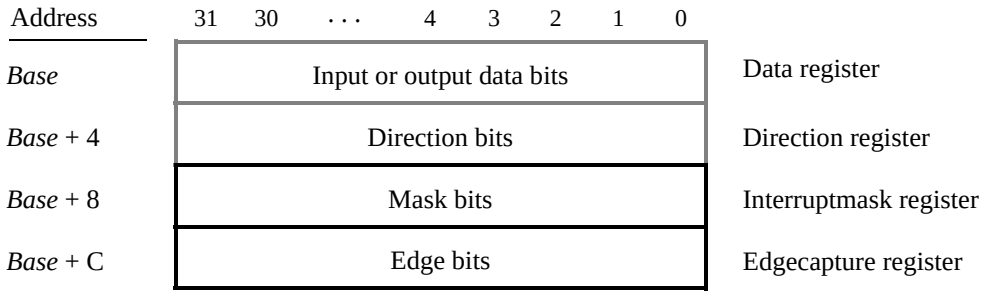



Figure 16. Registers used for interrupts from the parallel ports.

### 3.1.1 Interrupts from the Pushbutton Switches

Figure 6, reproduced as Figure 17, shows the registers associated with the pushbutton parallel port. The *Interrupt-mask* register allows processor interrupts to be generated when a key is pressed. Each bit in the *Edgecapture* register is set to 1 by the parallel port when the corresponding key is pressed. The Nios II processor can read this register to determine which key has been pressed, in addition to receiving an interrupt request if the corresponding bit in the interrupt mask register is set to 1. Writing any value to the *Edgecapture* register deasserts the Nios II interrupt request and sets all bits of the *Edgecapture* register to zero.

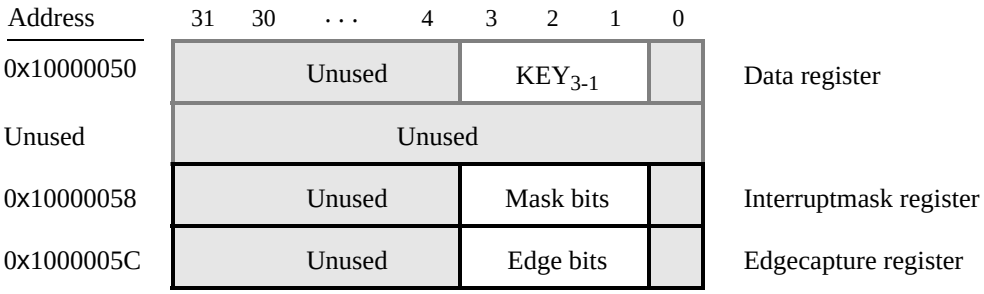



Figure 17. Registers used for interrupts from the pushbutton parallel port.

## 3.2 Interrupts from the JTAG UART

## 3.3 Interrupts from the serial port UART

## 3.4 Interrupts from the IrDA UART

## 3.5 Interrupts from the Interval Timer

Figure 15, in section 2.7, shows six registers that are associated with the interval timer. As we said in section 2.7, the bit $b_0$ (*TO*) is set to 1 when the timer reaches a count value of 0. It is possible to generate an interrupt when this occurs, by using the bit $b_{16}$ (*ITO*). Setting the bit *ITO* to 1 allows an interrupt request to be generated whenever *TO* becomes 1. After an interrupt occurs, it can be cleared by writing any value to the register that contains the bit *TO*.

## 3.6 Using Interrupts with Assembly Language Code

## 3.7 Using Interrupts with C Language Code

An example of C language code for the DE2 Media Computer that uses interrupts is shown in Figure 23. This code performs exactly the same operations as the code described in Figure 19.

To enable interrupts the code in Figure 23 uses *macros* that provide access to the Nios II status and control registers. A collection of such macros, which can be used in any C program, are provided in Figure 24.

The reset and exception handlers for the main program in Figure 23 are given in Figure 25. The function called *the_reset* provides a simple reset mechanism by performing a branch to the main program. The function named *the_exception* represents a general exception handler that can be used with any C program. It includes assembly language code to check if the exception is caused by an external interrupt, and, if so, calls a C language routine named *interrupt_handler*. This routine can then perform whatever action is needed for the specific application. In Figure 25, the *interrupt_handler* code first determines which exception has occurred, by using a macro from Figure 24 that reads the content of the Nios II interrupt pending register. The interrupt service routine that is invoked for the interval timer is shown in 26, and the interrupt service routine for the pushbutton switches appears in Figure 27.

The source code files shown in Figure 19 to Figure 27 are distributed as part of the Altera Monitor Program. The files can be found under the heading *sample programs*, and are identified by the name *Interrupt Example*.

```
#include "nios2_ctrl_reg_macros.h"
#include "key_codes.h"                  // defines values for KEY1, KEY2

/* key_pressed and pattern are written by interrupt service routines; we have to declare
 * these as volatile to avoid the compiler caching their values in registers */
volatile int key_pressed = KEY2;        // shows which key was last pressed
volatile int pattern = 0x0000000F;      // pattern for HEX displays
/*****************************************************************************
 * This program demonstrates use of interrupts in the DE2 Media Computer. It first starts the
 * interval timer with 33 msec timeouts, and then enables interrupts from the interval timer
 * and pushbutton KEYs
 *
 * The interrupt service routine for the interval timer displays a pattern on the HEX displays, and
 * shifts this pattern either left or right. The shifting direction is set in the pushbutton
 * interrupt service routine, as follows:
 *       KEY[1]: shifts the displayed pattern to the right
 *       KEY[2]: shifts the displayed pattern to the left
 *       KEY[3]: changes the pattern using the settings on the SW switches
*****************************************************************************/
int main(void)
{
    /* Declare volatile pointers to I/O registers (volatile means that IO load and store instructions
     * will be used to access these pointer locations instead of regular memory loads and stores) */
    volatile int * interval_timer_ptr = (int *) 0x10002000;     // interval timer base address
    volatile int * KEY_ptr = (int *) 0x10000050;                // pushbutton KEY address

    /* set the interval timer period for scrolling the HEX displays */
    int counter = 0x190000;                 // 1/(50 MHz) × (0x190000) = 33 msec
    *(interval_timer_ptr + 0x2) = (counter & 0xFFFF);
    *(interval_timer_ptr + 0x3) = (counter >> 16) & 0xFFFF;

    /* start interval timer, enable its interrupts */
    *(interval_timer_ptr + 1) = 0x7;        // STOP = 0, START = 1, CONT = 1, ITO = 1

    *(KEY_ptr + 2) = 0xE;                   /* write to the pushbutton interrupt mask register, and
                                             * set 3 mask bits to 1 (bit 0 is Nios II reset) */

    NIOS2_WRITE_IENABLE( 0x3 );     /* set interrupt mask bits for levels 0 (interval timer)
                                     * and level 1 (pushbuttons) */
    NIOS2_WRITE_STATUS( 1 );        // enable Nios II interrupts

    while(1);                       // main program simply idles
}
```

Figure 23. An example of C code that uses interrupts.

```
#ifndef __NIOS2_CTRL_REG_MACROS__
#define __NIOS2_CTRL_REG_MACROS__

/*****************************************************************************/
/* Macros for accessing the control registers.                               */
/*****************************************************************************/

#define NIOS2_READ_STATUS(dest) \
   do { dest = __builtin_rdctl(0); } while (0)

#define NIOS2_WRITE_STATUS(src) \
   do { __builtin_wrctl(0, src); } while (0)

#define NIOS2_READ_ESTATUS(dest) \
   do { dest = __builtin_rdctl(1); } while (0)

#define NIOS2_READ_BSTATUS(dest) \
   do { dest = __builtin_rdctl(2); } while (0)

#define NIOS2_READ_IENABLE(dest) \
   do { dest = __builtin_rdctl(3); } while (0)

#define NIOS2_WRITE_IENABLE(src) \
   do { __builtin_wrctl(3, src); } while (0)

#define NIOS2_READ_IPENDING(dest) \
   do { dest = __builtin_rdctl(4); } while (0)

#define NIOS2_READ_CPUID(dest) \
   do { dest = __builtin_rdctl(5); } while (0)

#endif
```

Figure 24. Macros for accessing Nios II status and control registers.

```
#include "nios2_ctrl_reg_macros.h"

/* function prototypes */
void main(void);
void interrupt_handler(void);
void interval_timer_isr(void);
void pushbutton_ISR(void);

/* global variables */
extern int key_pressed;

/* The assembly language code below handles Nios II reset processing */
void the_reset (void) __attribute__ ((section (".reset")));
void the_reset (void)
/*****************************************************************************
 * Reset code; by using the section attribute with the name ".reset" we allow the linker program
 * to locate this code at the proper reset vector address. This code just calls the main program
 *****************************************************************************/
{
   asm (".set     noat");                  // magic, for the C compiler
   asm (".set     nobreak");               // magic, for the C compiler
   asm ("movia  r2, main");                // call the C language main program
   asm ("jmp    r2");
}
/* The assembly language code below handles Nios II exception processing. This code should not be
 * modified; instead, the C language code in the function interrupt_handler() can be modified as
 * needed for a given application. */
void the_exception (void) __attribute__ ((section (".exceptions")));
void the_exception (void)
/*****************************************************************************
 * Exceptions code; by giving the code a section attribute with the name ".exceptions" we allow
 * the linker to locate this code at the proper exceptions vector address. This code calls the
 * interrupt handler and later returns from the exception.
 *****************************************************************************/
{
   asm (".set     noat");                  // magic, for the C compiler
   asm (".set     nobreak");               // magic, for the C compiler
   asm ( "subi    sp, sp, 128");
   asm ( "stw     et, 96(sp)");
   asm ( "rdctl   et, ctl4");
   asm ( "beq     et, r0, SKIP_EA_DEC");   // interrupt is not external
   asm ( "subi    ea, ea, 4");             /* must decrement ea by one instruction for external
                                            * interrupts, so that the instruction will be run */
```

Figure 25. Reset and exception handler C code (Part *a*).

```
asm ( "SKIP_EA_DEC:" );
asm ( "stw    r1, 4(sp)" );          // save all registers
asm ( "stw    r2, 8(sp)" );
asm ( "stw    r3, 12(sp)" );
asm ( "stw    r4, 16(sp)" );
asm ( "stw    r5, 20(sp)" );
asm ( "stw    r6, 24(sp)" );
asm ( "stw    r7, 28(sp)" );
asm ( "stw    r8, 32(sp)" );
asm ( "stw    r9, 36(sp)" );
asm ( "stw    r10, 40(sp)" );
asm ( "stw    r11, 44(sp)" );
asm ( "stw    r12, 48(sp)" );
asm ( "stw    r13, 52(sp)" );
asm ( "stw    r14, 56(sp)" );
asm ( "stw    r15, 60(sp)" );
asm ( "stw    r16, 64(sp)" );
asm ( "stw    r17, 68(sp)" );
asm ( "stw    r18, 72(sp)" );
asm ( "stw    r19, 76(sp)" );
asm ( "stw    r20, 80(sp)" );
asm ( "stw    r21, 84(sp)" );
asm ( "stw    r22, 88(sp)" );
asm ( "stw    r23, 92(sp)" );
asm ( "stw    r25, 100(sp)" );       // r25 = bt (skip r24 = et, because it was saved above)
asm ( "stw    r26, 104(sp)" );       // r26 = gp
// skip r27 because it is sp, and there is no point in saving this
asm ( "stw    r28, 112(sp)" );       // r28 = fp
asm ( "stw    r29, 116(sp)" );       // r29 = ea
asm ( "stw    r30, 120(sp)" );       // r30 = ba
asm ( "stw    r31, 124(sp)" );       // r31 = ra
asm ( "addi   fp, sp, 128" );

asm ( "call   interrupt_handler" );  // call the C language interrupt handler

asm ( "ldw    r1, 4(sp)" );          // restore all registers
asm ( "ldw    r2, 8(sp)" );
asm ( "ldw    r3, 12(sp)" );
asm ( "ldw    r4, 16(sp)" );
asm ( "ldw    r5, 20(sp)" );
asm ( "ldw    r6, 24(sp)" );
asm ( "ldw    r7, 28(sp)" );
```

Figure 25. Reset and exception handler C language code (Part *b*).

```
    asm ( "ldw    r8, 32(sp)" );
    asm ( "ldw    r9, 36(sp)" );
    asm ( "ldw    r10, 40(sp)" );
    asm ( "ldw    r11, 44(sp)" );
    asm ( "ldw    r12, 48(sp)" );
    asm ( "ldw    r13, 52(sp)" );
    asm ( "ldw    r14, 56(sp)" );
    asm ( "ldw    r15, 60(sp)" );
    asm ( "ldw    r16, 64(sp)" );
    asm ( "ldw    r17, 68(sp)" );
    asm ( "ldw    r18, 72(sp)" );
    asm ( "ldw    r19, 76(sp)" );
    asm ( "ldw    r20, 80(sp)" );
    asm ( "ldw    r21, 84(sp)" );
    asm ( "ldw    r22, 88(sp)" );
    asm ( "ldw    r23, 92(sp)" );
    asm ( "ldw    r24, 96(sp)" );
    asm ( "ldw    r25, 100(sp)" );          // r25 = bt
    asm ( "ldw    r26, 104(sp)" );          // r26 = gp
    // skip r27 because it is sp, and we did not save this on the stack
    asm ( "ldw    r28, 112(sp)" );          // r28 = fp
    asm ( "ldw    r29, 116(sp)" );          // r29 = ea
    asm ( "ldw    r30, 120(sp)" );          // r30 = ba
    asm ( "ldw    r31, 124(sp)" );          // r31 = ra

    asm ( "addi   sp, sp, 128" );
    asm ( "eret" );
}

/*****************************************************************************
 * Interrupt Service Routine: Determines the interrupt source and calls the appropriate subroutine
 *****************************************************************************/
void interrupt_handler(void)
{
    int ipending;
    NIOS2_READ_IPENDING(ipending);
    if ( ipending & 0x1 )                   // interval timer is interrupt level 0
        interval_timer_isr( );
    if ( ipending & 0x2 )                   // pushbuttons are interrupt level 1
        pushbutton_ISR( );
    // else, ignore the interrupt
    return;
}
```

Figure 25. Reset and exception handler C code (Part *c*).

```
#include "key_codes.h"                  // defines values for KEY1, KEY2

extern volatile int key_pressed;
extern volatile int pattern;
/*****************************************************************************
 * Interval timer interrupt service routine
 *
 * Shifts a pattern being displayed on the HEX displays. The shift direction is determined
 * by the external variable key_pressed.
 *
*****************************************************************************/
void interval_timer_isr( )
{
    volatile int * interval_timer_ptr = (int *) 0x10002000;
    volatile int * HEX3_HEX0_ptr = (int *) 0x10000020;      // HEX3_HEX0 address
    volatile int * HEX7_HEX4_ptr = (int *) 0x10000030;      // HEX7_HEX4 address

    *(interval_timer_ptr) = 0;                  // clear the interrupt

    *(HEX3_HEX0_ptr) = pattern;                 // display pattern on HEX3 ... HEX0
    *(HEX7_HEX4_ptr) = pattern;                 // display pattern on HEX7 ... HEX4

    /* rotate the pattern shown on the HEX displays */
    if (key_pressed == KEY2)                    // for KEY2 rotate left
        if (pattern & 0x80000000)
            pattern = (pattern << 1) | 1;
        else
            pattern = pattern << 1;
    else if (key_pressed == KEY1)               // for KEY1 rotate right
        if (pattern & 0x00000001)
            pattern = (pattern >> 1) | 0x80000000;
        else
            pattern = (pattern >> 1) & 0x7FFFFFFF;

    return;
}
```

Figure 26. Interrupt service routine for the interval timer.

```
#include "key_codes.h"                  // defines values for KEY1, KEY2

extern volatile int key_pressed;
extern volatile int pattern;

/*****************************************************************************
 * Pushbutton - Interrupt Service Routine
 *
 * This routine checks which KEY has been pressed. If it is KEY1 or KEY2, it writes this value
 * to the global variable key_pressed. If it is KEY3 then it loads the SW switch values and
 * stores in the variable pattern
*****************************************************************************/
void pushbutton_ISR( void )
{
    volatile int * KEY_ptr = (int *) 0x10000050;
    volatile int * slider_switch_ptr = (int *) 0x10000040;
    int press;

    press = *(KEY_ptr + 3);             // read the pushbutton interrupt register
    *(KEY_ptr + 3) = 0;                 // clear the interrupt

    if (press & 0x2)                    // KEY1
        key_pressed = KEY1;
    else if (press & 0x4)               // KEY2
        key_pressed = KEY2;
    else                                // press & 0x8, which is KEY3
        pattern = *(slider_switch_ptr); // read the SW slider switch values; store in pattern

    return;
}
```

Figure 27. Interrupt service routine for the pushbutton keys.

# 4 Media Components

This section describes the audio in/out port, video-out port, audio/video configuration module, video-in port, 16 × 2 character display, and PS/2 port.

## 4.1 Audio In/Out Port

The DE2 Media Computer includes an audio port that is connected to the audio CODEC (COder/DECoder) chip on the DE2 board. The default setting for the sample rate provided by the audio CODEC is 48K samples/sec. The audio port provides audio-input capability via the microphone jack on the DE2 board, as well as audio output functionality via the line-out jack. The audio port includes four FIFOs that are used to hold incoming and outgoing data. Incoming data is stored in the left- and right-channel *Read* FIFOs, and outgoing data is held in the left- and right-channel *Write* FIFOs. All FIFOs have a maximum depth of 128 32-bit words.

The audio port's programming interface consists of four 32-bit registers, as illustrated in Figure 28. The *Control* register, which has the address 0x10003040, is readable to provide status information and writable to make control settings. Bit *RE* of this register provides an interrupt enable capability for incoming data. Setting this bit to 1 allows the audio core to generate a Nios II interrupt when either of the *Read* FIFOs are filled 75% or more. The bit *RI* will then be set to 1 to indicate that the interrupt is pending. The interrupt can be cleared by removing data from the *Read* FIFOs until both are less than 75% full. Bit *WE* gives an interrupt enable capability for outgoing data. Setting this bit to 1 allows the audio core to generate an interrupt when either of the *Write* FIFOs are less that 25% full. The bit *WI* will be set to 1 to indicate that the interrupt is pending, and it can be cleared by filling the *Write* FIFOs until both are more than 25% full. The bits *CR* and *CW* in Figure 28 can be set to 1 to clear the *Read* and *Write* FIFOs, respectively. The clear function remains active until the corresponding bit is set back to 0.

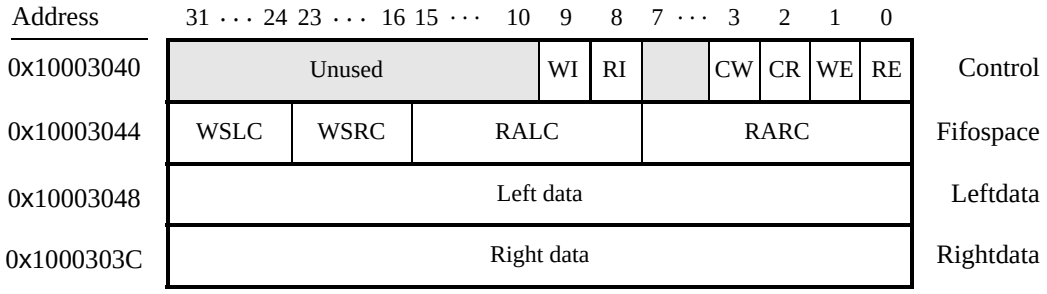



Figure 28. Audio port registers.

The read-only *Fifospace* register in Figure 28 contains four 8-bit fields. The fields *RARC* and *RALC* give the number of words currently stored in the right and left audio-input FIFOs, respectively. The fields *WSRC* and *WSLC* give the number of words currently available (that is, *unused*) for storing data in the right and left audio-out FIFOs. When all FIFOs in the audio port are cleared, the values provided in the *Fifospace* register are *RARC* = *RALC* = 0 and *WSRC* = *WSLC* = 128.

The *Leftdata* and *Rightdata* registers are readable for audio in, and writable for audio out. When data is read from these registers, it is provided from the head of the *Read* FIFOs, and when data is written into these registers it is

loaded into the *Write* FIFOs.

A fragment of C code that uses the audio port is shown in Figure 29. The code checks to see when the depth of either the left or right *Read* FIFO has exceeded 75% full, and then moves the data from these FIFOs into a memory buffer. This code is part of a larger program that is distributed as part of the Altera Monitor Program. The source code can be found under the heading *sample programs*, and is identified by the name *Media*.

```
volatile int * audio_ptr = (int *) 0x10003040;          // audio port address
int fifospace, int buffer_index = 0;
int left_buffer[BUF_SIZE];
int right_buffer[BUF_SIZE];
…
fifospace = *(audio_ptr + 1);                           // read the audio port fifospace register
if ( (fifospace & 0x000000FF) > 96)                     // check RARC, for > 75% full
{
    /* store data until the audio-in FIFO is empty or the memory buffer is full */
    while ( (fifospace & 0x000000FF) && (buffer_index < BUF_SIZE) )
    {
        left_buffer[buffer_index] = *(audio_ptr + 2);   //Leftdata
        right_buffer[buffer_index] = *(audio_ptr + 3);  //Rightdata
        ++buffer_index;
        fifospace = *(audio_ptr + 1);                   // read the audio port fifospace register
    }
}
…
```

Figure 29. An example of code that uses the audio port.

## 4.2 Video-out Port

The DE2 Media Computer includes a video-out port with a VGA controller that can be connected to a standard VGA monitor. The VGA controller supports a screen resolution of 640 × 480. The image that is displayed by the VGA controller is derived from two sources: a *pixel* buffer, and a *character* buffer.

### 4.2.1 Pixel Buffer

The pixel buffer for the video-out port reads stored pixel values from a memory buffer for display by the VGA controller. As illustrated in Figure 30, the memory buffer provides an image resolution of 320 × 240 pixels, with the coordinate 0,0 being at the top-left corner of the image. Since the VGA controller supports the screen resolution of 640 × 480, each of the pixel values in the pixel buffer is replicated in both the *x* and *y* dimensions when it is being displayed on the VGA screen.

Figure 31*a* shows that each pixel value is represented as a 16-bit halfword, with five bits for the blue and red components, and six bits for green. As depicted in part *b* of Figure 31, pixels are addressed in the memory buffer by using the combination of a *base* address and an *x,y* offset. In the DE2 Media Computer the pixel buffer uses the base address $(08000000)_{16}$, which corresponds to the starting address of the SRAM chip on the DE2 board. Using

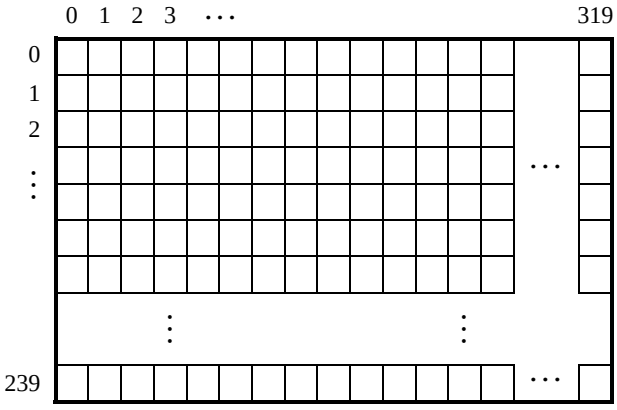
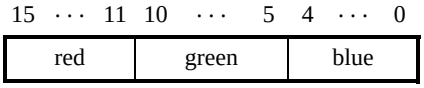


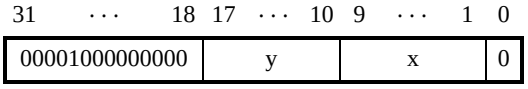

Figure 30. Pixel buffer coordinates.

this scheme, the pixel at location 0,0 has the address $(08000000)_{16}$, the pixel 1,0 has the address *base* + (00000000 000000001 0)$_2$ = $(08000002)_{16}$, the pixel 0,1 has the address *base* + (00000001 000000000 0)$_2$ = $(08000400)_{16}$, and the pixel at location 319,239 has the address *base* + (11101111 100111111 0)$_2$ = $(0803BE7E)_{16}$.

The pixel buffer includes a programming interface in the form of a set of registers. These registers allow the base address of the memory buffer used by the pixel buffer to be changed under software control, as well as providing status information. A detailed description of this programming interface is available in the online documentation for the Video-out port, which is available from Altera's University Program web site.




(a) Pixel values



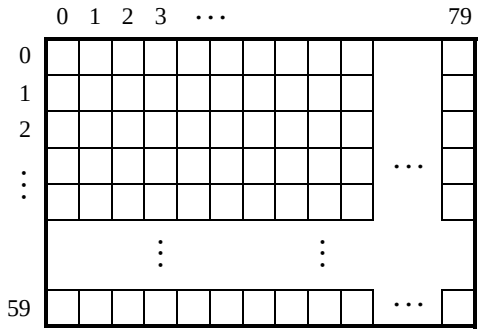

(b) Pixel buffer addresses

Figure 31. Pixel values and addresses.

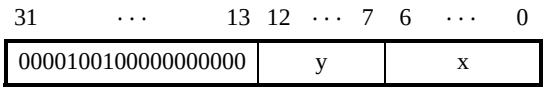
### 4.2.2 Character Buffer

The character buffer for the video-out port is stored in on-chip memory in the FPGA on the DE2 board. As illustrated in Figure 32*a*, the buffer provides a resolution of 80 × 60 characters, where each character occupies an 8 × 8 block of pixels on the VGA screen. Characters are stored in each of the locations shown in Figure 32*a* using their ASCII codes; when these character codes are displayed on the VGA monitor, the character buffer automatically generates

the corresponding pattern of pixels for each character using a built-in font. Part *b* of Figure 32 shows that characters are addressed in the memory by using the combination of a *base* address, which has the value $(09000000)_{16}$, and an *x,y* offset. Using this scheme, the character at location 0,0 has the address $(09000000)_{16}$, the character 1,0 has the address *base* + $(000000\ 0000001)_2 = (09000001)_{16}$, the character 0,1 has the address *base* + $(000001\ 0000000)_2 = (09000080)_{16}$, and the character at location 79,59 has the address *base* + $(111011\ 1001111)_2 = (09001DCF)_{16}$.




(a) Character buffer coordinates




(b) Character buffer addresses

Figure 32. Character buffer coordinates and addresses.

### 4.2.3 Using the Video-out Port with C code

A fragment of C code that uses the pixel and character buffers is shown in Figure 33. The first **while** loop in the figure draws a rectangle in the pixel buffer using the color *pixel_color*. The rectangle is drawn using the coordinates $x_1, y_1$ and $x_2, y_2$. The second **while** loop in the figure writes a null-terminated character string pointed to by the variable *text_ptr* into the character buffer at the coordinates *x*, *y*. The code in Figure 33 is included in the sample program called *Media* that is distributed with the Altera Monitor Program.

## 4.3 Audio/Video Configuration Module

The audio/video configuration module controls settings that affect the operation of both the audio port, the video-out port, and the video-in port. The audio/video configuration module automatically configures and initializes all of these ports whenever the DE2 Media Computer is reset. For typical use of the DE2 Media Computer it is not necessary to modify any of these default settings. In the case that changes to these settings are needed, the reader should refer to the audio/video configuration module's online documentation, which is available from Altera's University Program web site.

```
volatile short * pixel_buffer = (short *) 0x08000000;       // Pixel buffer
volatile char * character_buffer = (char *) 0x09000000;     // Character buffer
int x1, int y1, int x2, int y2, short pixel_color;
int offset, row, col;
int x, int y, char * text_ptr;
…
/* Draw a box; assume that the coordinates are valid */
for (row = y1; row <= y2; row++)
{
    col = x1;
    while (col <= x2)
    {
        offset = (row << 9) + col;
        *(pixel_buffer + offset) = pixel_color;             // compute halfword address, set pixel
        ++col;
    }
}
/* Display a text string; assume that it fits on one line */
offset = (y << 7) + x;
while ( *(text_ptr) )
{
    *(character_buffer + offset) = *(text_ptr);             // write to the character buffer
    ++text_ptr;
    ++offset;
}
```

Figure 33. An example of code that uses the video-out port.

## 4.4 Video-In Port

### 4.4.1 DMA Controller for Video

## 4.5 LCD Display Port

## 4.6 PS/2 Port

The DE2 Media Computer includes a PS/2 port that can be connected to a standard PS/2 keyboard or mouse. The port includes a 256-byte FIFO that stores data received from a PS/2 device. The programming interface for the PS/2 port consists of two registers, as illustrated in Figure 37. The *PS2_Data* register is both readable and writable. When bit 15, *RVALID*, is 1, reading from this register provides the data at the head of the FIFO in the *Data* field, and the number of entries in the FIFO (including this read) in the *RAVAIL* field. When *RVALID* is 1, reading from the *PS2_Data* register decrements this field by 1. Writing to the *PS2_Data* register can be used to send a command in the *Data* field to the PS/2 device.

The *PS2_Control* register can be used to enable interrupts from the PS/2 port by setting the *RE* field to the value 1. When this field is set, then the PS/2 port generates an interrupt when $RAVAIL > 0$. While the interrupt is pending the field *RI* will be set to 1, and it can be cleared by emptying the PS/2 port FIFO. The *CE* field in the *PS2_Control* register is used to indicate that an error occurred when sending a command to a PS/2 device.

A fragment of C code that uses the PS/2 port is given in Figure 38. This code reads the content of the *Data* register, and saves data when it is available. If the code is used continually in a loop, then it stores the last three bytes of data received from the PS/2 port in the variables $byte_1$, $byte_2$, and $byte_3$. This code is included as part of a larger sample program called *Media* that is distributed with the Altera Monitor Program.

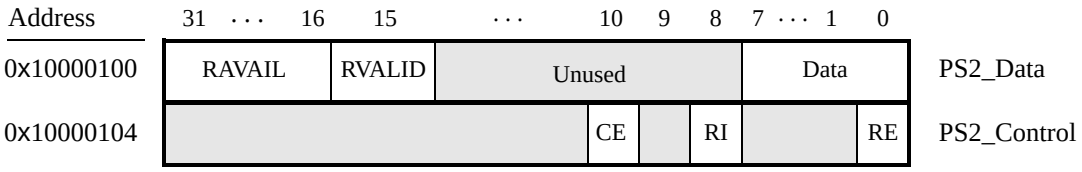



Figure 37. PS/2 port registers.

```
volatile int * PS2_ptr = (int *) 0x10000100;          // PS/2 port address
int PS2_data, RVALID;
char byte1 = 0, byte2 = 0, byte3 = 0;
…
PS2_data = *(PS2_ptr);                                // read the Data register in the PS/2 port
RVALID = PS2_data & 0x8000;                           // extract the RVALID field
if (RVALID)
{
    /* save the last three bytes of data */
    byte1 = byte2;
    byte2 = byte3;
    byte3 = PS2_data & 0xFF;
}
…
```

Figure 38. An example of code that uses the PS/2 port.

## 4.7 USB Port

## 4.8 10/100 Ethernet port

### 4.9 Floating-point Hardware

The Nios II processor in the DE2 Media Computer includes hardware support for floating-point addition, subtraction, multiplication, and division. To use this support in a C program, variables must be declared with the type *float*. A simple example of such code is given in Figure 42. When this code is compiled, it is necessary to pass the special argument -mcustom-fpu-cfg=60-2 to the C compiler, to instruct it to use the floating-point hardware support.

```
/*****************************************************************************
 * This program demonstrates use of floating-point numbers in the DE2 Media Computer
 *
 * It performs the following:
 *      1. reads two FP numbers from the Terminal window
 *      2. performs +, 1, *, and / on the numbers, then prints results on Terminal window
*****************************************************************************/
int main(void)
{
    float x, y, add, sub, mult, div;

    while(1)
    {
        printf ("Enter FP values X Y:\n");
        scanf ("%f", &x);
        printf ("%f ", x); // echo the typed data to the Terminal window
        scanf ("%f", &y);
        printf ("%f\n", y); // echo the typed data to the Terminal window
        add = x + y;
        sub = x - y;
        mult = x * y;
        div = x / y;
        printf ("X + Y = %f\n", add);
        printf ("X - Y = %f\n", sub);
        printf ("X * Y = %f\n", mult);
        printf ("X / Y = %f\n", div);
    }
}
```

Figure 42. An example of code that uses floating-point variables.

## 5 Modifying the DE2 Media Computer

It is possible to modify the DE2 Media Computer by using Altera's Quartus II software and Qsys System Integration tool. Tutorials that introduce this software are provided in the University Program section of Altera's web site. To modify the system it is first necessary to obtain all of the relevant design source code files. The DE2 Media Computer is available in two versions that specify the system using either Verilog HDL or VHDL.

Table 3 lists the names of the Qsys IP cores that are used in this system. When the DE2 Media Computer design files are opened in the Quartus II software, these cores can be examined using the Qsys System Integration tool. Each core has a number of settings that are selectable in the Qsys System Integration tool, and includes a datasheet that provides detailed documentation.

| **I/O Peripheral** | **Qsys Core** |
|---|---|
| SDRAM | SDRAM Controller |
| SRAM | SRAM Controller |
| On-chip memory character buffer | Character Buffer for VGA Display |
| SD Card | SD Card Interface |
| Flash | Altera UP Flash Memory IP Core |
| Red LED parallel port | Parallel Port |
| Green LED parallel port | Parallel Port |
| 7-segment displays parallel port | Parallel Port |
| Expansion parallel ports | Parallel Port |
| Slider switch parallel port | Parallel Port |
| Pushbutton parallel port | Parallel Port |
| PS/2 port | PS2 Controller |
| JTAG port | JTAG UART |
| Serial port | RS232 UART |
| IrDA port | IrDA UART |
| Interval timer | Interval timer |
| System ID | System ID Peripheral |
| Audio/video configuration port | Audio and Video Config |
| Audio port | Audio |
| Video port | Pixel Buffer DMA Controller |
| LCD display port | Character LCD 16x2 |
| Video In port | DMA Controller |

Table 3. Qsys cores used in the DE2 Media Computer.

The DE2 Media Computer includes a Nios II/f processor. When using the Quartus II Web Edition, compiling a design with a Nios II/s or Nios II/f processor will produce a time-limited SOF file. As a result, the board must remain connected to the host computer, and the design cannot be set as the default configuration, as discussed in Section 6. Designs using only Nios II/e processors and designs compiled using the Quartus II Subscription Edition do not have this restriction.

## 6 Making the System the Default Configuration

## 7 Memory Layout

Table 4 summarizes the memory map used in the DE2 Media Computer.

## 8 Altera Monitor Program Integration

| Base Address | End Address | I/O Peripheral |
|---|---|---|
| 0x00000000 | 0x007FFFFF | SDRAM |
| 0x08000000 | 0x0807FFFF | SRAM |
| 0x10003020 | 0x1000302F | VGA Pixel buffer control |
| 0x09000000 | 0x09001FFF | On-chip memory character buffer |
| 0x10003030 | 0x10003037 | Character buffer control |
| 0x0B000000 | 0x0B0003FF | SD Card |
| 0x0C000000 | 0x0C3FFFFF | Flash |
| 0x0BFF0000 | 0x0BFF0003 | Flash Erase control |
| 0x10000000 | 0x1000000F | Red LED parallel port |
| 0x10000010 | 0x1000001F | Green LED parallel port |
| 0x10000020 | 0x1000002F | 7-segment HEX3−HEX0 displays parallel port |
| 0x10000030 | 0x1000003F | 7-segment HEX7−HEX4 displays parallel port |
| 0x10000040 | 0x1000004F | Slider switch parallel port |
| 0x10000050 | 0x1000005F | Pushbutton parallel port |
| 0x10000060 | 0x1000006F | JP1 Expansion parallel port |
| 0x10000070 | 0x1000007F | JP2 Expansion parallel port |
| 0x10000100 | 0x10000107 | PS/2 port |
| 0x10001000 | 0x10001007 | JTAG UART port |
| 0x10001010 | 0x10001017 | Serial port |
| 0x10001020 | 0x10001027 | IrDA port |
| 0x10002000 | 0x1000201F | Interval timer |
| 0x10002020 | 0x10002027 | System ID |
| 0x10003000 | 0x1000301F | Audio/video configuration |
| 0x10003040 | 0x1000304F | Audio port |
| 0x10003050 | 0x10003051 | LCD display port |
| 0x10003060 | 0x1000306F | Video-In port |

Table 4. Memory layout used in the DE2 Media Computer.