Jeide, Matthew Date 10/21/24 Period 2

W11: DE 1.2.4 A Intro Flip-Flops / Sequential Logic

Read the introduction to Flip-Flops. Must show your work neatly on your Engineering Portfolio. Must show all work. Answer all the questions below after designing the Flip-Flop Sequential Gate in MultiSim.

Flip-Flops

In the **combinational logic** circuits above, a circuit immediately produces an output when an input is changed. As a switch is toggled to generate a new input, a new output is generated, and the previous output is discarded. To have more functionality, you can combine logic gates to create a circuit that remembers the previous output, in effect, creating memory. These types of circuits are called **sequential logic** devices, where the output states depend not only on the state of the inputs but also on the sequence in which they reach their present states. The D flip-flop is one such device.

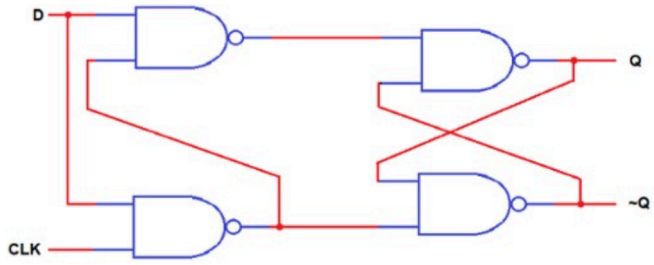


Figure 8. D Flip-flop made from NAND gates

A D flip-flop has an input D and a clock signal CLK. The clock signal is periodic and constantly changes between 0 (low) and 1 (high). When it changes, it triggers the flip-flop to process input D. The flip-flop generates two outputs, Q and ~Q (pronounced "not Q"). If Q is 1, ~Q is 0, and if Q is 0, ~Q is 1. With every pulse of the clock, the flip-flop reads its inputs and generates output. If the input changes before a new clock pulse, the flip-flop ignores the change, keeping its current output state until the next clock pulse. This configuration makes the device "sequential," allowing it to store data and act as memory.

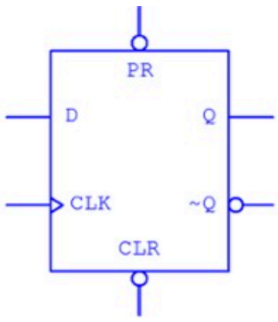


Figure 9. D Flip-flop symbol

A flip-flop is represented in a circuit by a simplified symbol shown at right. This NAND-gate diagram simplification hides the additional inputs called preset (PR) and clear (CLR). These inputs are *not* synchronized to the clock pulse and are used to force the flip-flop to a preset state (high or 1), or to a clear state (low or 0).

74LS74N

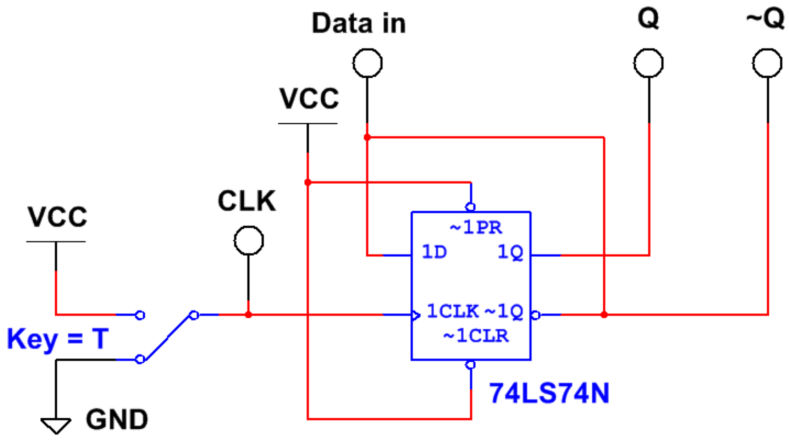
Jeide, Matthew Date 10/21/24 Period 2

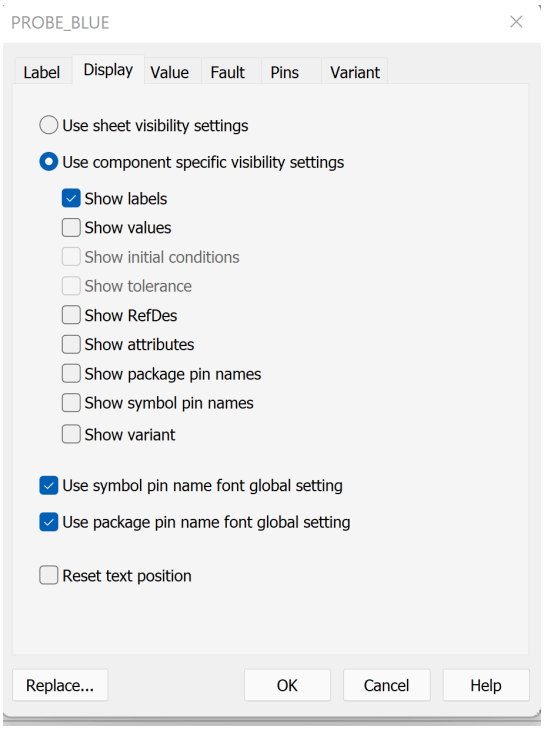
Flip-Flops

Using the MultiSim Circuit Design Software (CDS), enter the test circuit shown.

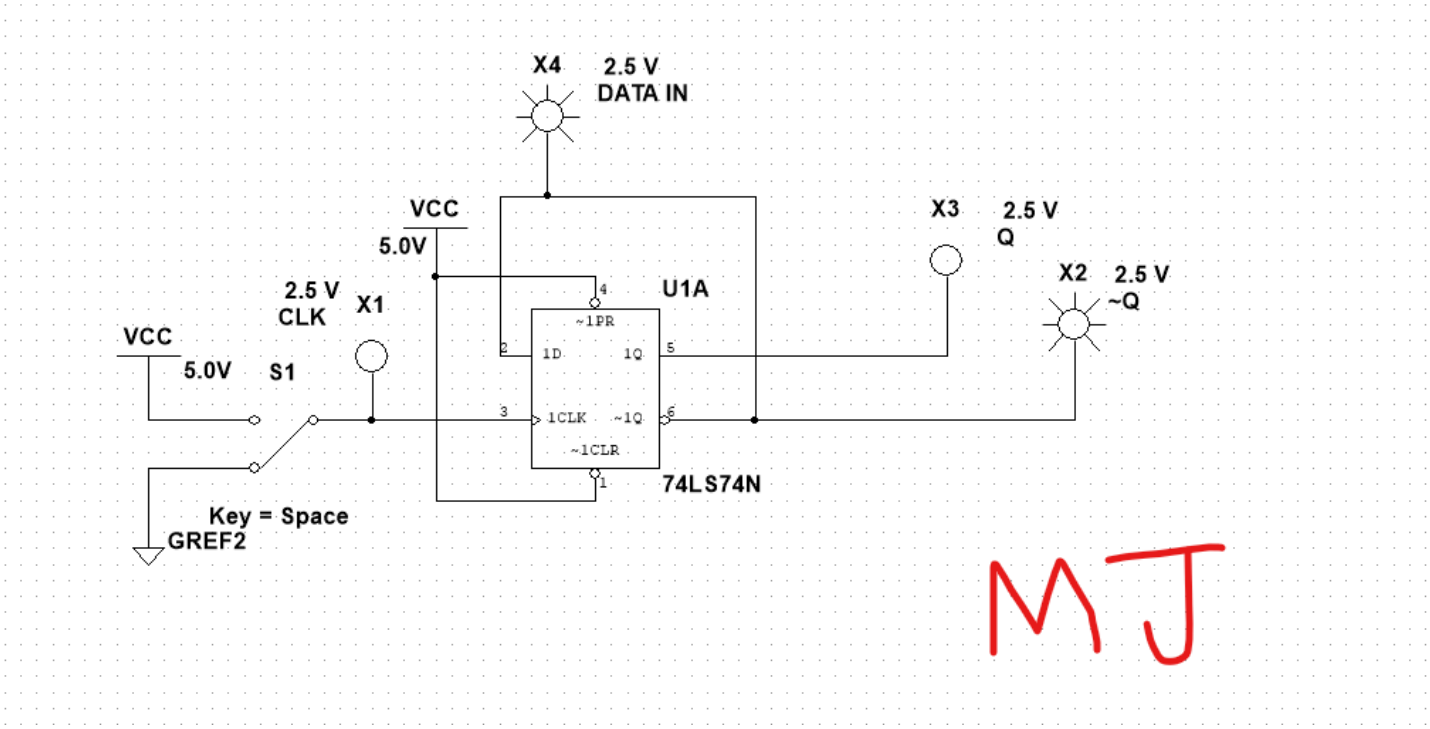
Use a switch for the input ***T*** and probes for the outputs ***Q*** and ***NOT_Q***.

- The 74LS74N has two inputs (***Data in*** and a clock signal ***CLK***). In this circuit, the clock signal input will be a switch ***T*** that you flip. The ***Data in*** is tied to the ***NOT_Q***.
- The 74LS74 also has preset and clear inputs. In this circuit, the **PR** (preset) and **CLR** (clear) are connected to 5V (high), which makes them both *inactive*. These PR and CLR inputs on the 74LS74 are said to be "*active low*" inputs. (It takes a low signal to activate them.)





Jeide, Matthew Date 10/21/24 Period 2



1. What pattern can you identify by toggling 13 consecutive times?

	Voltage (V)	Clock	Data in	Q	Not Q
1	0	0	1	0	1
2	5	1	0	1	0
3	0	0	0	1	0
4	5	1	1	0	1
5	0	0	1	0	1
6	5	1	0	1	0
7	0	0	0	1	0
8	5	1	1	0	1
9	0	0	1	0	1
10	5	1	0	1	0
11	0	0	0	1	0
12	5	1	1	0	1
13	0	0	1	0	1

Predict #14-20

14	5	1	0	1	0

Jeide, Matthew Date 10/21/24 Period 2

15	0	0	0	1	0
16	5	1	1	0	1
17	0	0	1	0	1
18	5	1	0	1	0
19	0	0	0	1	0
20	5	1	1	0	1

a. Toggle the input ***T*** several times until ***T*** is ***low*** and ***NOT_Q*** is ***low***. What do you observe?

When T is low and NOT_Q is also low, the flip flop does not toggle.

b. Starting with the switch on GROUND, what happens to output ***Q*** when the switch is moved from GROUND to VCC (5V)? This is one toggle of the switch. Explain below.

If the switch is moved from GROUND to VCC, output Q remains high if Data In is high, indicating that the flip flop changes with the clock signal being high and data in.

c. What happens to output ***Q*** when the switch is moved from 5V to GROUND? This is one toggle of the switch. Use your table to answer the questions.

When the switch is toggled, Output Q remains in its previous state until the next rising clock signal.

d. Toggle the switch one more time. What happened to output ***Q***? What does this tell you about *when* ***Q*** changes (toggles) in relation to *when* the input at the CLK Changes. (Helpful hint: It might help to cycle through a number of changes to spot this relationship of when Q changes.)

Output Q only changes on the rising edge of the clock, indicating the flip flop is edge-triggered.

e. What is the relationship of D Data in to Q *always*?

Jeide, Matthew Date 10/21/24 Period 2

f. What is the relationship of Q to NOT_Q *always*?

NOT_Q is always the opposite of Q.

g. The 74LS74N is called a "flip-flop". Based on your observations, can you explain the relationship between the D Data in, Q, NOT_Q, and the CLK signal? What does a flip-flop do?

A flip flop stores a bit of information, with Q reflecting the D input during the rising edge of the clock signal. The flip flop stores the value until the next rising clock signal.

Explore:

Later in this course, we will learn how to combine flip-flops to make transitions to desired outputs. The flip-flop is holding a bit of information, waiting for a signal to change (**memory**). But in this example, *you* are making the transition by flipping a switch. How can we make the flip-flop change without us providing the input directly?

Use an oscillator or clock generator.