Jeide, Matthew Date 2/14/2025 Period 2

W6/7B: DE [PROJECT] 2.4.1 Date of Birth Combinational Logic Circuit Design

Introduction

Your date of birth may make you unique in your class, but possibly not as unique as you think. With a worldwide birthrate of roughly 130 million per year, this means that on a daily basis, over 360,000 individuals may share the same date of birth (assuming births are distributed evenly across 365 days).

In a Digital Electronics classroom of 20 students, there is less than a 50% probability that two of you share the same date of birth. However, in a class larger than 23 students, the odds are greater than 50% that two people might share the same birthday. For more information about probabilities and birthdays, research “the birthday paradox”.

In this activity, you are going to design a circuit that will display your (hopefully unique) date of birth on a single, seven-segment display. This design will bring together all of the design techniques that you have learned throughout this lesson.

Equipment

Calculator (preferably one with a number base conversion feature)
Computer with Circuit Design Software (CDS)

- Breadboarding Hardware *or* Digital MiniSystem
- Integrated Circuits:
    - 74LS04 (Hex Inverter gates)
    - 74LS08 (Quad AND gates)
    - 74LS32 (Quad OR gates)
    - 74LS00 (Quad NAND gates)
    - 74LS02 (Quad NOR gates)
- 22-gauge solid wire
- Multipurpose Wire Stripper
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Distance Learning Support

The date of birth should be displayed in the MMDDYY format. For example, if you were born on May 12, 2001, your design will display 051201.

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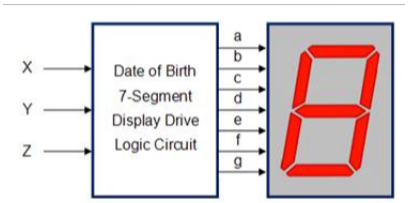
Procedure



1. Design a combinational logic circuit that has three inputs and seven outputs. When the inputs (X, Y, and Z) create a count from 000 to 111, the seven outputs (a through g) generate the logic required to display your date of birth on a seven-segment display (SSD).

   The date of birth will be displayed in the **MM-DD-YY** format. For example, if you were born on May 12, 2001, your design will display **05-12-01**.

X	Y	Z	Display	a	b	c	d	e	f	g
0	0	0	1	0	1	1	0	0	0	0
0	0	1	2	1	1	0	1	1	0	1
0	1	0	—	0	0	0	0	0	0	1
0	1	1	1	0	1	1	0	0	0	0
1	0	0	2	1	1	0	1	1	0	1
1	0	1	—	0	0	0	0	0	0	1
1	1	0	0	1	1	1	1	1	1	0
1	1	1	7	1	1	1	0	0	0	0

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a	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	0	1
$\overline{X}\,Y$	0	0
$X\,Y$	1	1
$X\,\overline{Y}$	1	0

b	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	1	1
$\overline{X}\,Y$	0	1
$X\,Y$	1	1
$X\,\overline{Y}$	1	0

c	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	1	0
$\overline{X}\,Y$	0	1
$X\,Y$	1	1
$X\,\overline{Y}$	0	0

d	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	0	1
$\overline{X}\,Y$	0	0
$X\,Y$	1	0
$X\,\overline{Y}$	1	0

e	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	0	1
$\overline{X}\,Y$	0	0
$X\,Y$	1	0
$X\,\overline{Y}$	1	0

f	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	0	0
$\overline{X}\,Y$	0	0
$X\,Y$	1	0
$X\,\overline{Y}$	0	0

g	$\overline{Z}$	Z
$\overline{X}\ \overline{Y}$	0	1
$\overline{X}\,Y$	1	0
$X\,Y$	0	0
$X\,\overline{Y}$	1	1

Equations

a. $X\overline{Z} + XY + \overline{X}\,\overline{Y}Z$

b. $\overline{X}\,\overline{Y} + \overline{X}Z + XY$

c. $XY + \overline{Z}\,\overline{Y}\,\overline{X} + Z\overline{X}Y$

d. $X\overline{Z} + \overline{X}\,\overline{Y}Z$

e. $X\overline{Z} + \overline{X}\,\overline{Y}Z$

f. $XY\overline{Z}$

g. $X\overline{Y} + \overline{X}Y\overline{Z} + \overline{X}\,\overline{Y}Z$

Insert a screenshot of your Brainstorm Design a-g.

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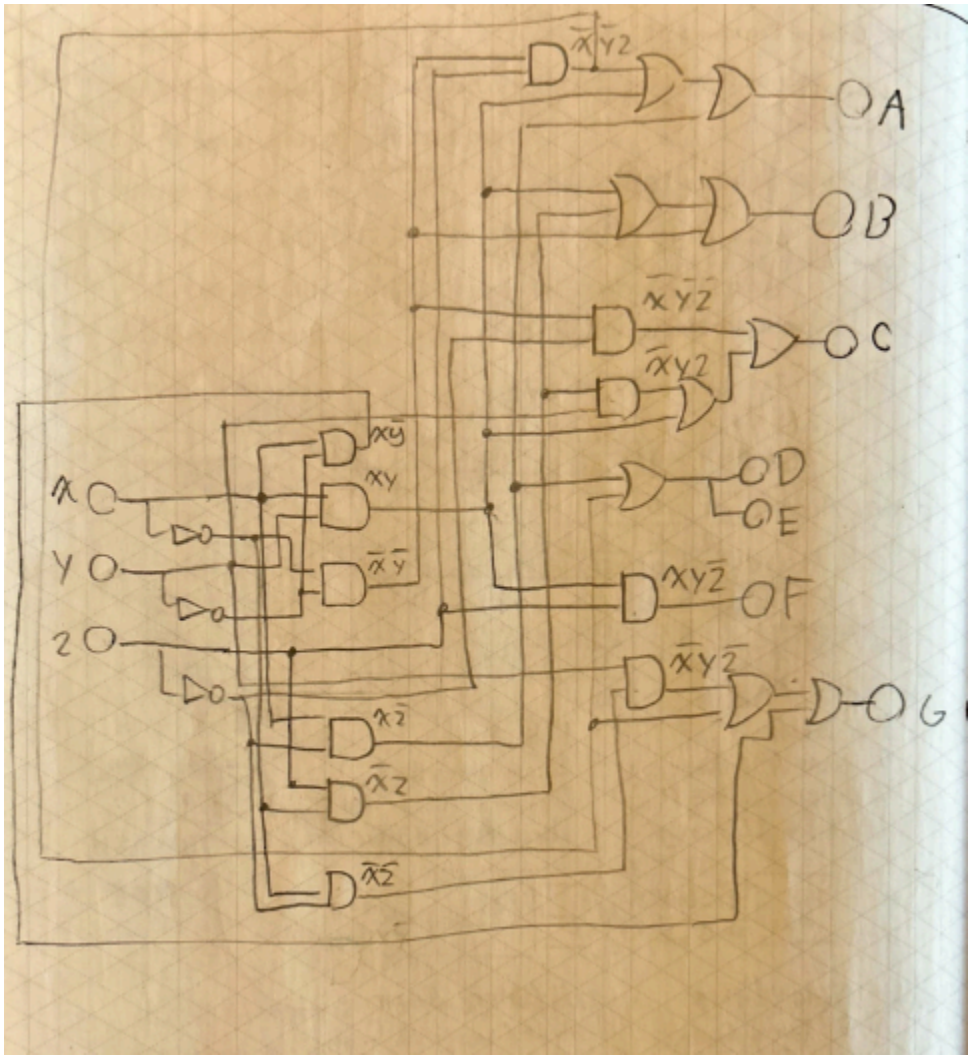

2. Detailed Design Specifications:
    a. The SSD must be a common cathode.
    b. Current limiting resistors (150 Ω — 270 Ω) must be used.
    c. The Karnaugh mapping technique must be used to obtain the simplified logic expression for each of the seven segments.

Insert your Karnaugh mapping technique and a logical expression for each of the seven segments. Make sure to include all truth tables and logic expressions.

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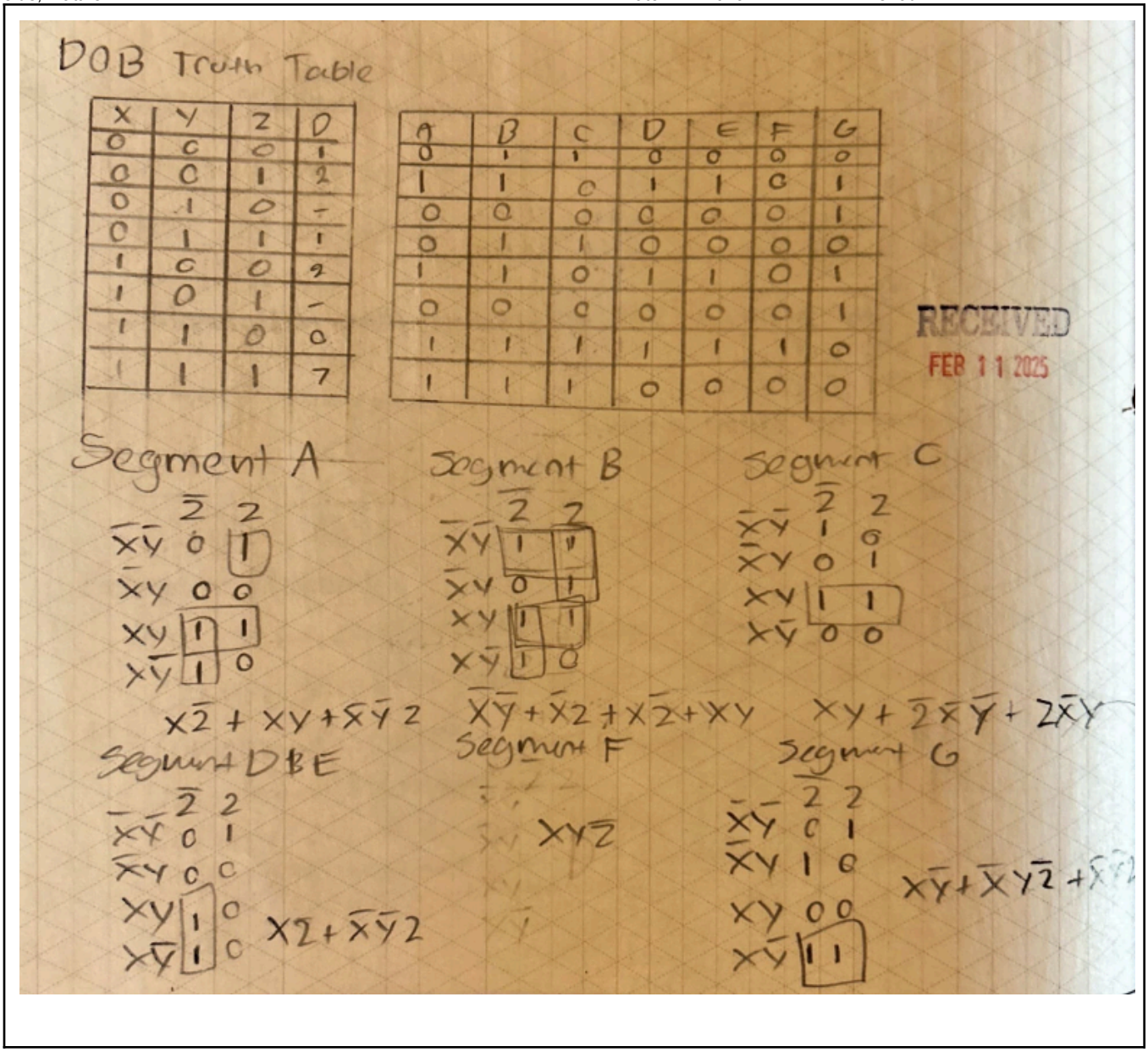

d. At least one segment must be implemented with NAND only logic.
e. At least one segment must be implemented with NOR only logic.
f. The implementation of the remaining segments is your choice.

Simulation

Using the Circuit Design Software (CDS), enter and test your Date of Birth design.

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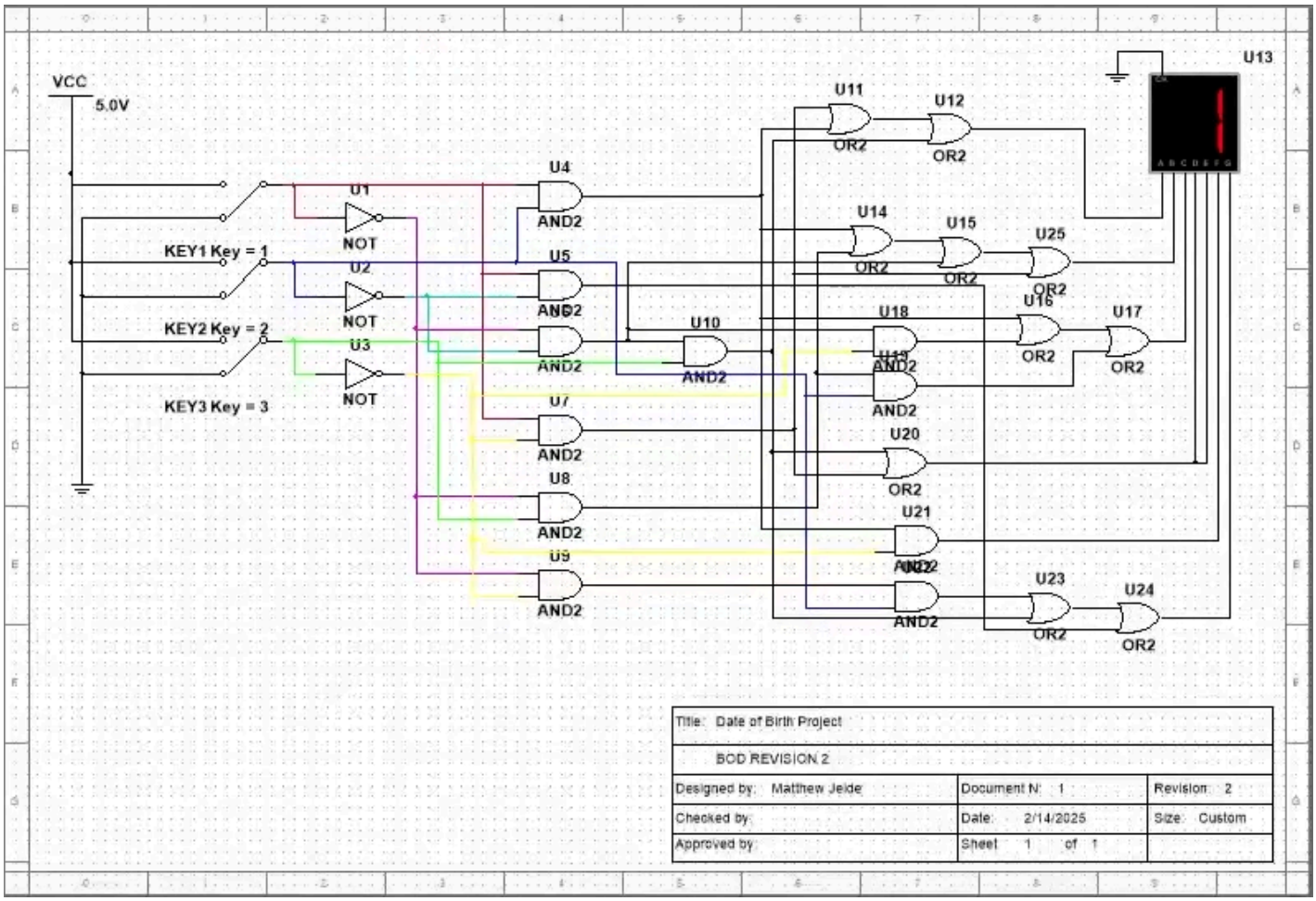
g. Use switches for the inputs X, Y, and Z.
h. If two SSD pins share the same input, you may need to reduce the resistance to get the segment to display.
i. Verify that the circuit is working as designed.
j. If the circuit is not working properly, review your design work and circuit implementation to identify your mistake. Make any necessary corrections and retest.
k. Be sure to document all changes in your engineering notebook.

Insert a screenshot and video of the Multisim design [EX: MM-DD-YY format]



Prototyping

3. Using the DMS, build and test your Date of Birth design.

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a. Verify that the circuit is working as designed. If it is not, do not change your design. You know that your design is good because you simulated it. If your circuit isn't working correctly, you must have built something incorrectly.
b. Review your circuit implementation to identify your mistakes, make the necessary corrections, and retest.
c. Be sure to document all changes in your engineering notebook.

Insert a video of your working breadboard design.

not avalible yet as this is a MULTISIM assignment

4. In the space provided below attach this completed worksheet to your E-Portfolio.

Insert your work on your E-Portfolio. Attach your E-Portfolio link here.
Make sure to include a video of the XOR and the XNOR adding the values.

https://sites.google.com/riversideunified.org/matthewjeide/projects/de-2024-2025/date-of-birth-project

Conclusion

Please answer in complete sentences. Minimum of three.

Write a conclusion (minimum 250 words) to describe the process that you used to design, simulate, and build your Date of Birth circuit. This conclusion must include all of your design work (truth table, K-Maps), preliminary and final schematics, parts list, and a digital photograph of your final circuit. The documentation should be complete enough that another student with the same knowledge of digital electronics could reproduce your design without any additional assistance.

Must write a 250-word conclusion explaining your design process, simulation, and how you built your Date of Birth Circuit.

The design and construction of the Date of Birth combinational logic circuit involved multiple key stages, including conceptualization, truth table development, Karnaugh map (K-Map) simplification, schematic design,

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simulation, and final prototyping.

The first step was to define the logic required to display a date of birth in MM-DD-YY format using a seven-segment display (SSD). This required determining the appropriate inputs and outputs. The three inputs (X, Y, Z) were designed to represent a binary count from 000 to 111, each corresponding to a segment display output. The truth table was developed to define the correct logic states for each of the seven segments (a through g) corresponding to the desired numerical outputs.

Once the truth table was established, Karnaugh maps were used to simplify the Boolean expressions for each segment. This step allowed us to minimize the number of required logic gates, improving efficiency and reducing hardware complexity. The resulting Boolean expressions dictated the selection and arrangement of logic gates in the circuit.

A preliminary schematic was developed using NI Multisim. The circuit incorporated various logic gate ICs, including the 74LS04 (Hex Inverter), 74LS08 (Quad AND), 74LS32 (Quad OR), 74LS00 (Quad NAND), and 74LS02 (Quad NOR) to implement the required logic functions.

Following schematic completion, the design was simulated within the CDS environment. This step ensured proper functionality before physical prototyping. Inputs were toggled to verify expected outputs, and minor logic refinements were made where necessary. Once simulation results confirmed correctness, the circuit was built on a breadboard using the specified ICs and wiring components.

During the prototyping stage, switches were used for the inputs X, Y, and Z to manually test the SSD display. The circuit will be meticulously wired according to the schematic, ensuring that each logic gate received the correct signals.

The final working circuit will be documented with a digital photograph, ensuring that future students could replicate the design. All design files, including the truth table, K-Maps, schematics, and component lists, were included in the project documentation. This comprehensive process ensured a fully functional Date of Birth combinational logic circuit and provided a clear

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methodology for others to follow.