Jeide, Matthew   Date 2/14/2025   Period 2
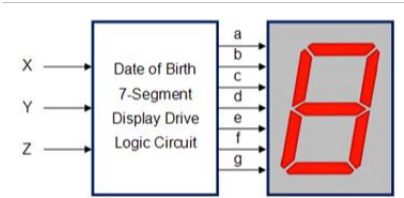
W6/7B: DE [SKETCH/MULTISIM BDAY] 2.4.1 Date of Birth Combinational Logic Circuit Design

Equipment

Calculator (preferably one with a number base conversion feature)
Computer with Circuit Design Software (CDS)
Breadboarding Hardware *or* Digital MiniSystem

- Integrated Circuits:
  - 74LS04 (Hex Inverter gates)
  - 74LS08 (Quad AND gates)
  - 74LS32 (Quad OR gates)
  - 74LS00 (Quad NAND gates)
  - 74LS02 (Quad NOR gates)
- 22-gauge solid wire
- Multipurpose Wire Stripper

1. Detailed Design Specifications:
   a. The SSD must be a common cathode.
   b. Current limiting resistors (150 Ω — 270 Ω) must be used.
   c. The Karnaugh mapping technique must be used to obtain the simplified logic expression for each of the seven segments.
   d. At least one segment must be implemented with NAND only logic.
   e. At least one segment must be implemented with NOR only logic.
   f. The implementation of the remaining segments is your choice (XOR and XNOR) can be used and will save you time.

Insert Circuit Sketch- Work must have a stamp to get credit.						
Last Name	First Name	Middle Name	Suffix	Grd	Age	Birthdate
Jeide	Matthew	Alexander	Jr	11	17	12/12/2007
Please be neat with your sketching. It makes it easier to make corrections if needed.						

DOB Truth Table

X	Y	Z	D
0	0	0	1
0	0	1	2
0	1	0	-
0	1	1	1
1	0	0	2
1	0	1	-
1	1	0	0
1	1	1	7

A	B	C	D	E	F	G
0	1	1	0	0	0	0
1	1	0	1	1	0	1
0	0	0	0	0	0	1
0	1	1	0	0	0	0
1	1	0	1	1	0	1
0	0	0	0	0	0	1
1	1	1	1	1	1	0
1	1	1	0	0	0	0

Segment A

$$\begin{array}{c|cc} & \bar{Z} & Z \\ \bar{X}\bar{Y} & 0 & 1 \\ \bar{X}Y & 0 & 0 \\ XY & 1 & 1 \\ X\bar{Y} & 1 & 0 \end{array}$$

$$X\bar{Z} + XY + \bar{X}\bar{Y}Z$$

Segment B

$$\begin{array}{c|cc} & \bar{Z} & Z \\ \bar{X}\bar{Y} & 1 & 1 \\ \bar{X}Y & 0 & 1 \\ XY & 1 & 1 \\ X\bar{Y} & 1 & 0 \end{array}$$

$$\bar{X}\bar{Y} + \bar{X}Z + X\bar{Z} + XY$$

Segment C

$$\begin{array}{c|cc} & \bar{Z} & Z \\ \bar{X}\bar{Y} & 1 & 2 \\ \bar{X}Y & 1 & 0 \\ XY & 1 & 1 \\ X\bar{Y} & 0 & 0 \end{array}$$

$$XY + \bar{Z}\bar{X}\bar{Y} + Z\bar{X}Y$$

Segment D & E

$$\begin{array}{c|cc} & \bar{Z} & Z \\ \bar{X}\bar{Y} & 0 & 1 \\ \bar{X}Y & 0 & 0 \\ XY & 1 & 0 \\ X\bar{Y} & 1 & 0 \end{array}$$

$$X\bar{Z} + \bar{X}\bar{Y}Z$$

Segment F

$$X\bar{Y}\bar{Z}$$

Segment G

$$\begin{array}{c|cc} & \bar{Z} & Z \\ \bar{X}\bar{Y} & 0 & 1 \\ \bar{X}Y & 1 & 0 \\ XY & 0 & 0 \\ X\bar{Y} & 1 & 1 \end{array}$$

$$X\bar{Y} + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z$$

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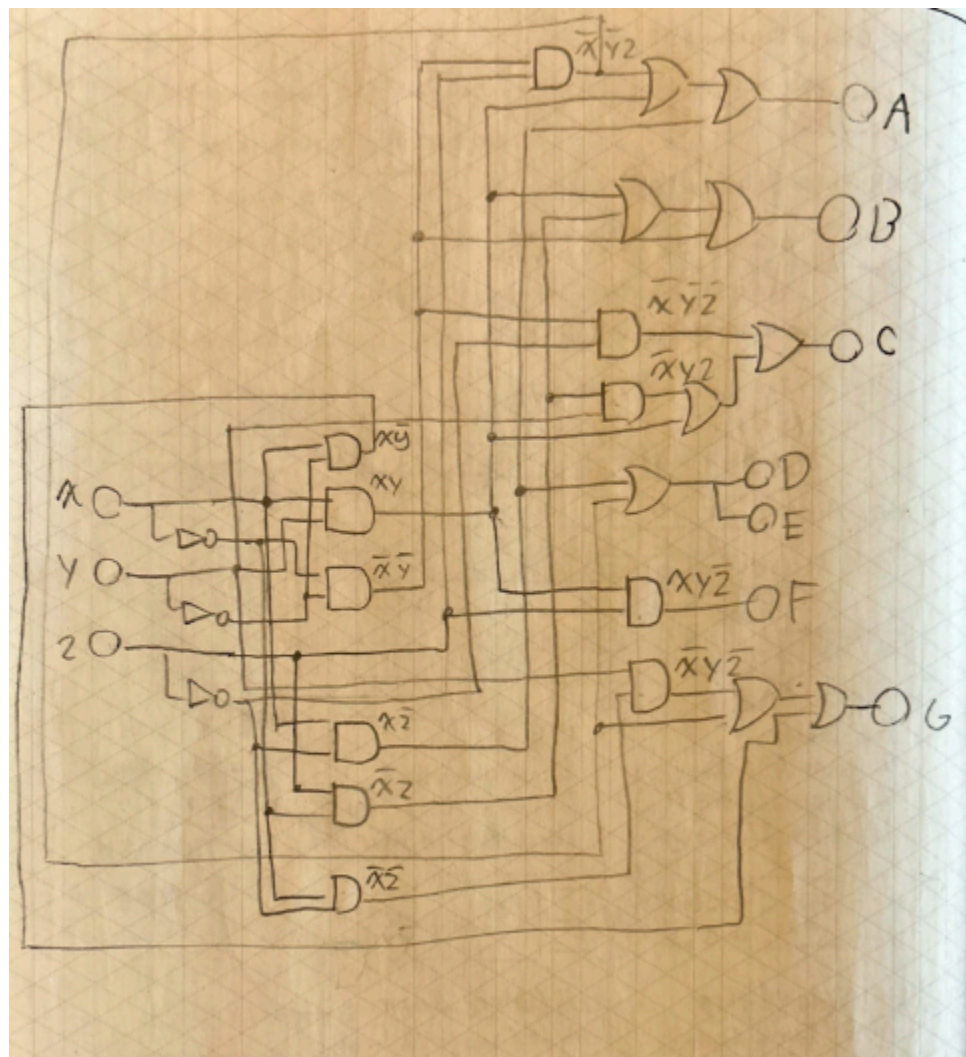
Simulation

Using the Circuit Design Software (CDS), enter and test your Date of Birth design.

> **WARNING:** At least one segment must be implemented with AND, OR, NOR, and NAND. We don't have enough chips to use only one type of AOI Chip.

g. The implementation of the remaining segments is your choice.

h. Use switches for the inputs X, Y, and Z.

i. If two SSD pins share the same input, you may need to reduce the resistance to get the segment to display.

j. Verify that the circuit is working as designed.

k. If the circuit is not working properly, review your design work and circuit implementation to identify your mistake. Make any necessary corrections and retest.

l. Be sure to document all changes in your engineering notebook.

Insert a screenshot and video of the Multisim design [EX: MM-DD-YY format]

Must include your name and date on the title block and the title of the assignment. Make sure to include a **PDF and a video.**
https://www.youtube.com/watch?v=_6YM0bM2M5s

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