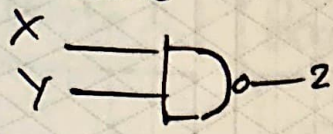
Title: NAND Universal Gate

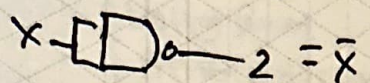
NAND Gate



$Z = \overline{XY} = \bar{X} + \bar{Y}$

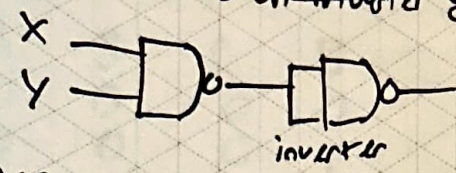
X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

NAND as an inverter gate



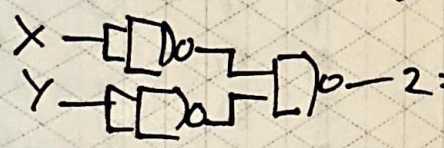
$Z = \bar{X}$ Equivalent to inverter

NAND GATE as an ~~inverter gate~~ AND



$Z = \overline{\overline{XY}} = XY$ Equivalent to AND Gate

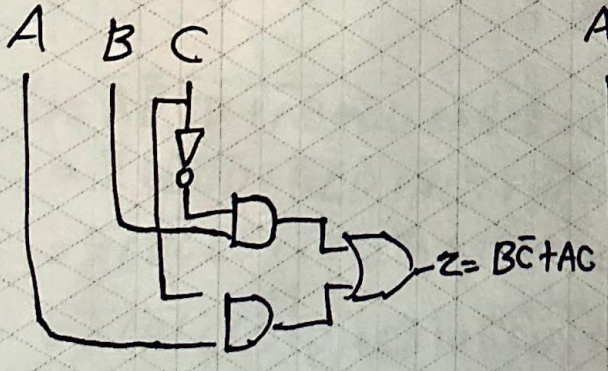
NAND GATE As an OR GATE

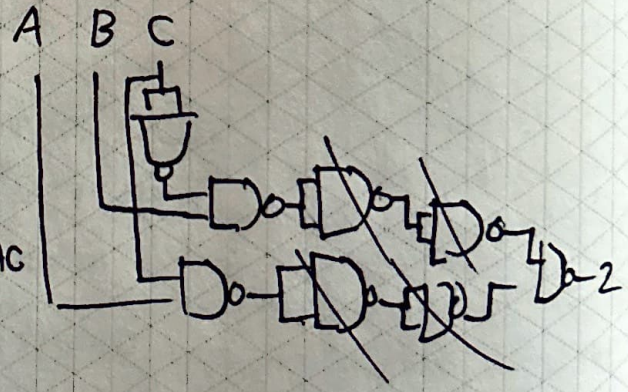


$Z = \overline{\bar{X}\,\bar{Y}} = \bar{\bar{X}} + \bar{\bar{Y}} = X + Y$ OR Gate

NAND Implementation Process

1. Design with AOI Logic
2. Replace every AND, OR, and INVERTER gate with its NAND equivalent
3. Redraw the circuit
4. Eliminate any double inversions
5. Redraw the final circuit.





Signature:	Date: 12/14/22	Team Members:
Witness:	Date:	
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