Design Specifications

Design a combinational logic circuit with the following specifications:

Three (3) inputs and (7) seven outputs.

As inputs count 000 to 111, the outputs (a-g) displays a date of birth (DOB) on a 7-segment display

The 7-segment display is a common cathode display

the DOB will be displayed in a MM-DD-YY format

DOB Truth Table

X	Y	Z	D
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	1
1	0	0	2
1	0	1	3
1	1	0	0
1	1	1	7

A	B	C	D	E	F	G
0	1	1	0	0	0	0
1	1	0	1	1	0	1
0	0	0	0	0	0	1
0	1	1	0	0	0	0
1	1	0	1	1	0	1
0	0	0	0	0	0	1
1	1	1	1	1	1	0
1	1	1	0	0	0	0

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Segment A

	$\bar{Z}$	Z
$\bar{X}\bar{Y}$	0	1
$\bar{X}Y$	0	0
XY	1	1
$X\bar{Y}$	1	0

$X\bar{Z} + XY + \bar{X}\bar{Y}Z$

Segment B

	$\bar{Z}$	Z
$\bar{X}\bar{Y}$	1	1
$\bar{X}Y$	0	1
XY	1	1
$X\bar{Y}$	1	0

$\bar{X}\bar{Y} + \bar{X}Z + X\bar{Z} + XY$

Segment C

	$\bar{Z}$	Z
$\bar{X}\bar{Y}$	1	0
$\bar{X}Y$	0	1
XY	1	1
$X\bar{Y}$	0	0

$XY + \bar{Z}\bar{X}\bar{Y} + Z\bar{X}Y$

Segment DBE

	$\bar{Z}$	Z
$\bar{X}\bar{Y}$	0	1
$\bar{X}Y$	0	0
XY	1	0
$X\bar{Y}$	1	0

$X\bar{Z} + \bar{X}\bar{Y}Z$

Segment F

$X\bar{Y}\bar{Z}$

Segment G

	2	2
$\bar{X}\bar{Y}$	0	1
$\bar{X}Y$	1	0
XY	0	0
$X\bar{Y}$	1	1

$X\bar{Y} + \bar{X}Y\bar{Z} + \bar{X}Z$

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Witness:	Date:	
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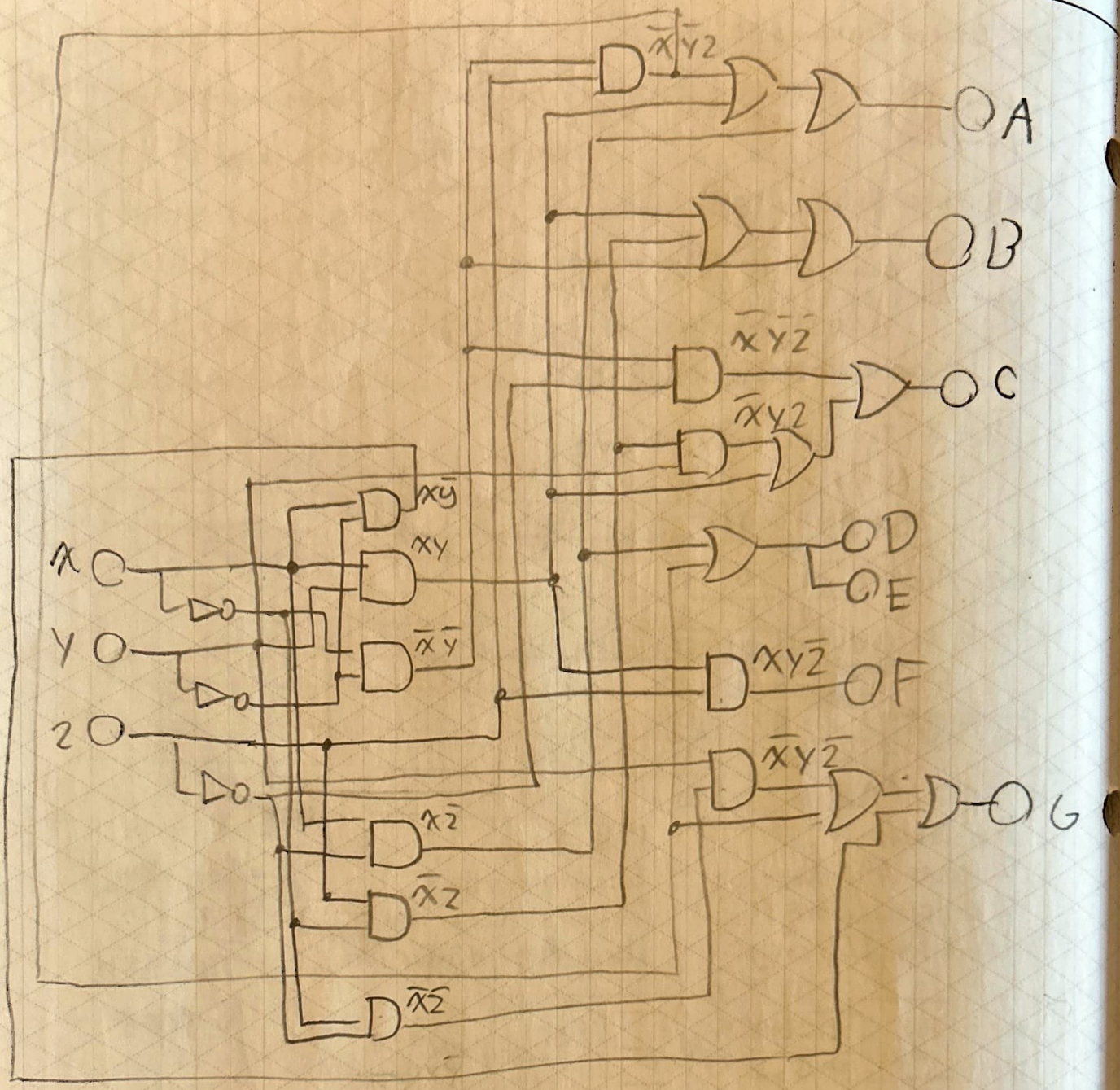

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