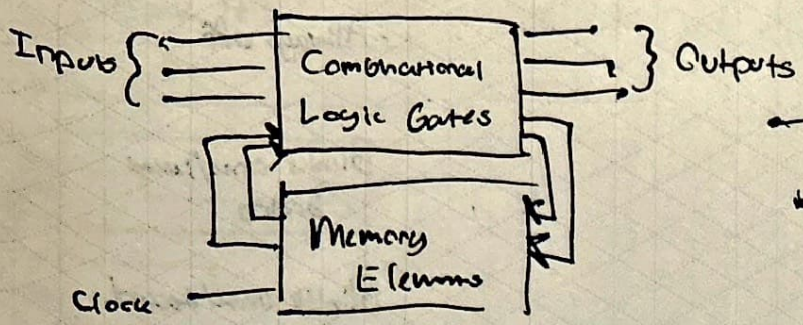
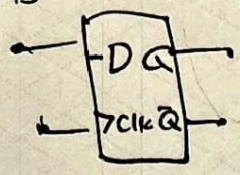
Title: Flip-Flops and Latches

Sequential Logic & the Flip-Flop



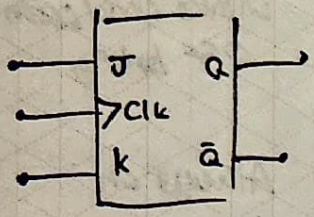
D Flip-Flop



D	clk	Q	Q̄
0	↑	0	1
1	↑	1	0

↑ rising edge of clock

J/K Flip-Flop: Excitation Table



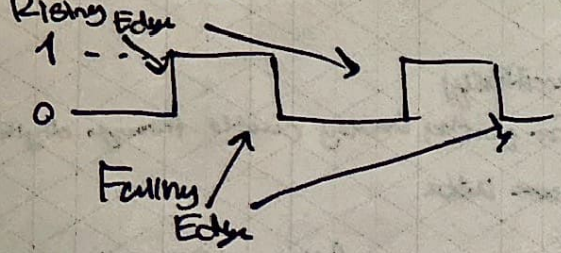
J	K	clk	Q
0	0	↑	Q_0
0	1	↑	0
1	0	↑	1
1	1	↑	$\bar{Q}_0$

No change
Clear
Set
Toggle

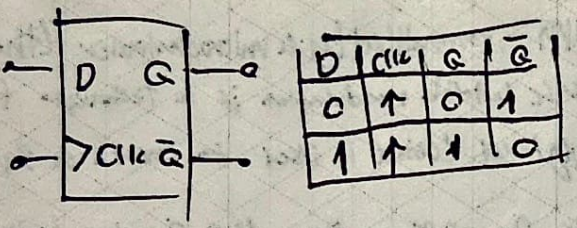
↑ rising edge of clock

Q̄ Complement of Q

Clock Edges



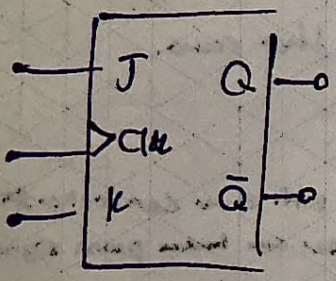
POS & NEG Edge triggered D



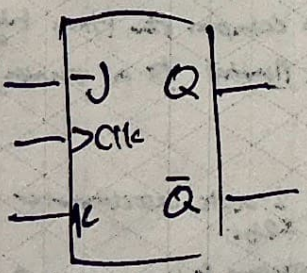
D	clk	Q	Q̄
0	↑	0	1
1	↑	1	0

Neg added a ○ to clk

POS & NEG Edge triggered D



J	K	clk	Q
0	0	↑	Q_0
0	1	↑	0
1	0	↑	1
1	1	↑	$\bar{Q}_0$



J	K	clk	Q
0	0	↓	Q_0
0	1	↓	0
1	0	↓	1
1	1	↓	$\bar{Q}_0$

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Witness:	Date:	
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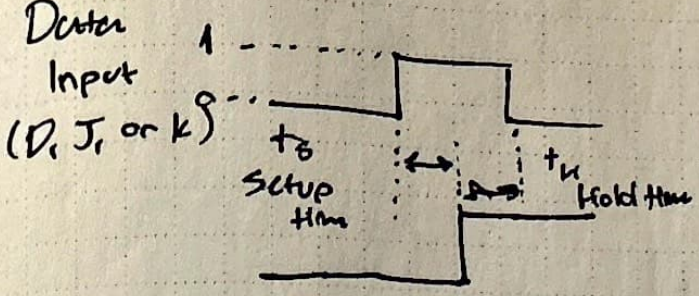
Flip-Flop timing



Setup time

The time interval before the occurrence of the clock signal during which the data input must be maintained

Hold time

The time interval after the active transition of the clock

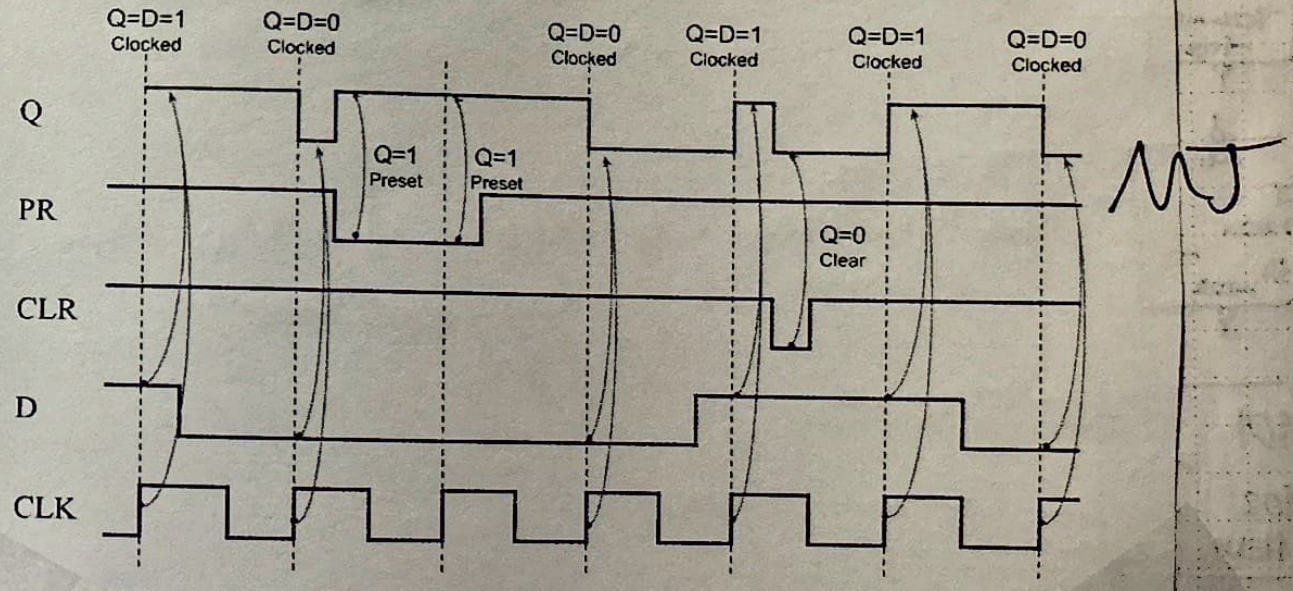
Asynchronous Inputs

Asynchronous inputs (Preset & Clear) are used to override the clock/data inputs and force the outputs to a predefined state.

The preset (PR) input forces the output to
$Q = 1$ & $\bar{Q} = 0$
The clear (CLR) input forces the output to
$Q = 0$ & $\bar{Q} = 1$

PR	CLR	CLK	D	Q	$\bar{Q}$	
1	1	↑	0	0	1	
1	1	↑	1	1	0	
0	1	X	X	1	0	Async Preset
1	0	X	X	0	1	Async Clear
0	0	X	X	1	1	Illegal

D Flip-Flop: PR & CLR Timing



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Witness:	Date:	
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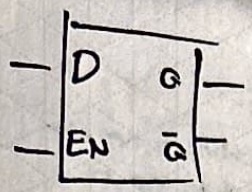
Title: Flip-Flops and Latches

Transparent D-Latch



EN	D	Q	Q̄
0	X	Q_0	$\bar{Q}_0$
1	0	0	1
1	1	1	0

EN: Enable

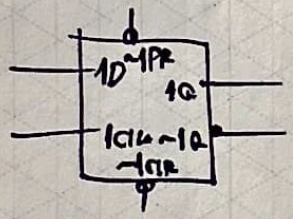
Flip-Flop Vs. Latch

The primary difference between a D-Flip-Flop and D-Latch is the EN/Clock input.

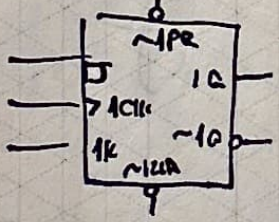
The flip-flop's CLOCK input is edge sensitive, meaning the flip-flop's output changes on the edge (rising or falling) of the CLOCK input.

The Latch's EN input is level sensitive, meaning the latch's output changes on the level (high or low) of the EN input

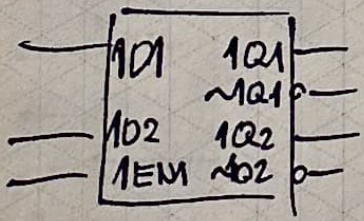
Flip-Flops and Latches



74LS74
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and complementary outputs



74LS76
Dual negative-edge-triggered J-K flip-flops with preset, clear, and complementary outputs



74LS75
Quad Latch

Signature:	Date: 1/12/23	Team Members:
Witness:	Date:	
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