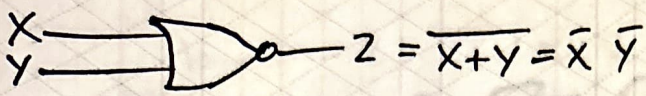
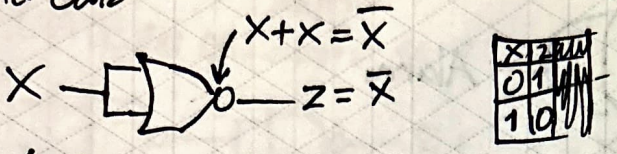
Title: Universal Gates NOR Logic Design

NOR Gate



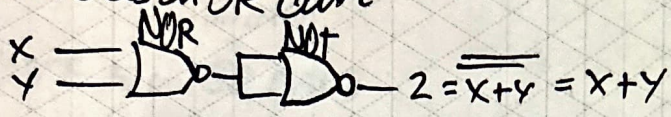
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

Inverter Gate



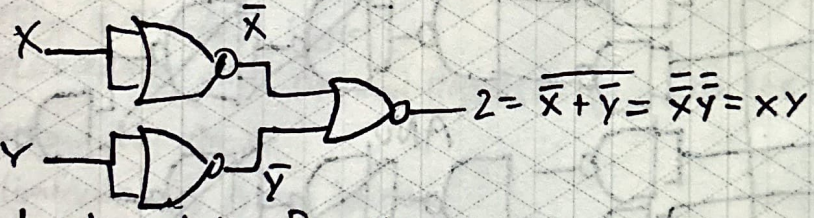
X	Z
0	1
1	0

NOR Gate as an OR Gate



X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

NOR Gate as an AND Gate



NOR Implementation Procedure

1. If starting from a logic circuit, implement the design with AOI logic
2. In the AOI implementation, identify and replace every AND, OR, and INVERTER gate with its NOR equivalent
3. Redraw the circuit
4. Identify and eliminate any obvious inversions e.g. back-to-back inverters
5. Redraw the final circuit

Signature:	Date: 1/7/25	Team Members:
Witness:	Date:	
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