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24-25 PLTW TEST REVIEW

Attach work below:

Instructions: Create a review sheet for the final exam with all the knowledge that you will need to remember. This sheet must have all the topics that we covered.

Sequential Logic

- Sequential Logic is different from combinational logic as sequential logic circuits can remember past events/inputs.
- Outputs depend on current inputs AND past states.
- Common examples of sequential logic is counters, registers, and state machines

Flip-Flops

- D Flip Flop (Delay/Data)
    - Stores a bit of data
    - Updates on rising edge of clock, Q = D.
    - Very predictable
    - Use case: holding data in registers, shift registers
- J/K Flip-Flop
    - More flexible: can set, reset, hold, or toggle
    - Inputs:
        - J = set, K = reset
        - J=K=1 -> Toggle (switch state)
        - J=K=0 -> Hold (no change)
        - J=1, K=0 -> Q = 1
        - J=0, K=1 -> Q = 0

Clock Signals

- A square wave used to synchronize logic.
- Tells flip flops when to update
- Rising edge (0 to 1) or falling edge (1 to 0) triggers changes.
- Period: time for one full wave.
- Frequency: How many cycles per second (Hz)
- Duty Cycle: % of time the signal is HIGH

Timing Diagrams

- Track how Q changes based on D, J/K, and the clock.
- D Flip Flop: Q follows D on rising clock edge.
- J/K Flip-Flop: Behavior depends on J/K inputs at the edge.

Counter Types

Asynchronous (Ripple) Counters

- Flip-Flops trigger one another
- Slower: delays “ripple” through
- Example: Now Serving Display

Synchronous Counters

- All flip-flops triggered by the same clock
- Faster, more reliable
- Example: 60-second Timer