Title: Setting Up PLTW S7 chip

1. In NI Multisim, go to "global options" Under options — ensure that the "Xilinx tools path" is setup correctly.

2. Create a new PLD Design in multisim
   - Use "Digilent PLTW S7" as the standard configuration
   - Give your design a name.
   - Select the connectors you wish to use in your design

3. Once the design has been compiled, create your circuit using only Logic gates — ICs are not available.

   - to test out your design before sending it off to the board, you can use "interactive digital constants" to test values on your design.

4. to export your design to the physical chip, click "transfer" and then "export to PLD", Use "program the connected PLD" and "refresh" the connected ~~design~~ device.
   Then, click "finish" and wait for a successful import.

LMT 2/25/25

Steps to implement DOE project with PLD

- Ensure NI multisim is setup properly
- Prepare the Breadboard and PLTW ~~circuit~~ device for programming
  — in this case, 3-inputs, and 7-outputs for the seven segment displays
- Design new logic for determining the current SSD outputs with the current inputs
- Export the design to the board
- Profit

LMT 2/25/25

Signature: Emma Quan	Date: 2/25/25	Team Members:
Witness:	Date:	
Continued From Page #		Continued On Page #