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**W8B: DE [PROJECT] 2.4.3 PLD Design: Date of Birth Using PLTW S7**

Warning Follow the instructions on the previous assignments and the ones below.

## Introduction

Most designers would probably not prototype a design on a breadboard the way you did on the Date of Birth Problem. As the size and complexity of combinational logic circuits increase (or any circuits), their implementation with discrete logic gates becomes impractical. It requires many components and can take a long time to create and troubleshoot if not wired correctly.

To address this problem, the electronics industry has turned to programmable logic devices for designs of any complexity. The current state-of-the-art device for programmable logic is the Field Programmable Gate Array (FPGA).

In this activity you will re-implement your Date of Birth design using the Field Programmable Gate Array (FPGA) on a PLD.

The original design specification from the Date of Birth Problem required that at least one of the segments be implemented in NAND logic and at least one of the segments be implemented in NOR. The reason for this requirement was to demonstrate the benefit in efficiency of NAND only and NOR only design implementations (fewer ICs as compared to AOI implementations).

With the FPGA implementation, this extra step of translating an AOI solution to a NAND (or NOR) solution is not necessary because the Xilinx Programming Software will automatically simplify the design into its most efficient implementation.

## Equipment

**These instructions are for use with the PLTW S7 module shown. If you do not have the PLTW S7 then ask your teacher to guide you to the correct activity. These instructions assume that all necessary software has been installed and configured for this course.**

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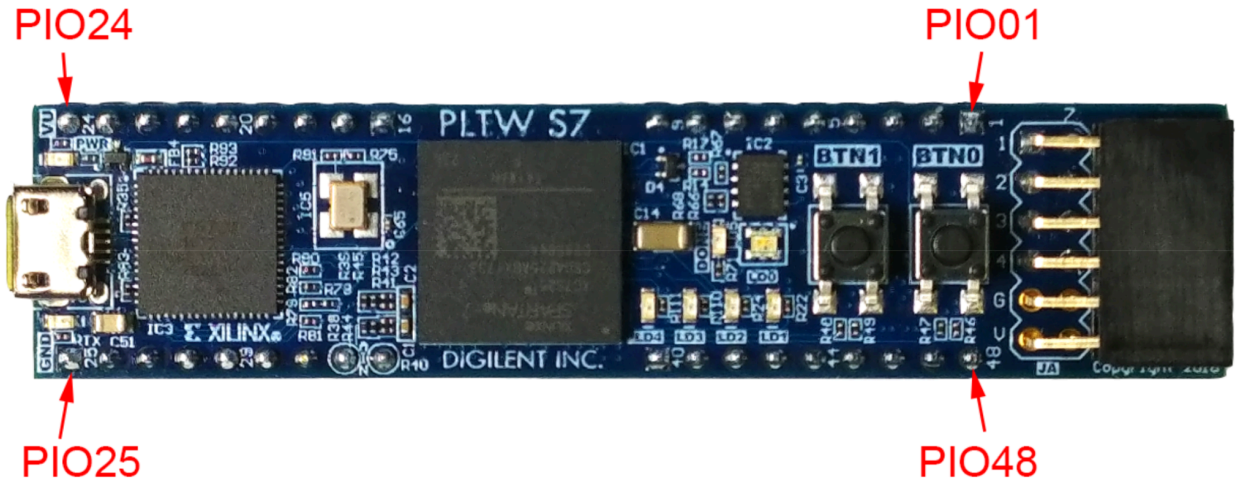


**Digital MiniSystem (myDAQ and myDigital Protoboard)**

- Digital MiniSystem (myDAQ and myDigital Protoboard)
- PLTW S7 FPGA Module
- #22-gauge solid wire
- Multipurpose Wire Stripper
- Computer with the following software
  - Circuit Design Software (CDS)
  - Xilinx Programming Software (XPS)

Procedure

## Circuit Design in PLD Design Mode

Although the birthday design has already been created in Design Mode of the CDS, it must be recreated in the PLD Design Mode of the CDS.

a. There are no design constraints on this PLD design. Using what you have learned, create your Date of Birth design in PLD Design Mode on the CDS.
b. Use your engineering notebook and previous tutorials as a guide to recreate the circuit as simply and quickly as possible.
c. There is not a seven-segment display option in PLD Design Mode that will let you simulate this circuit. You will need to test your design by programing the PLD and testing it on the breadboard.

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# Mapping PLD Pin Inputs/Outputs

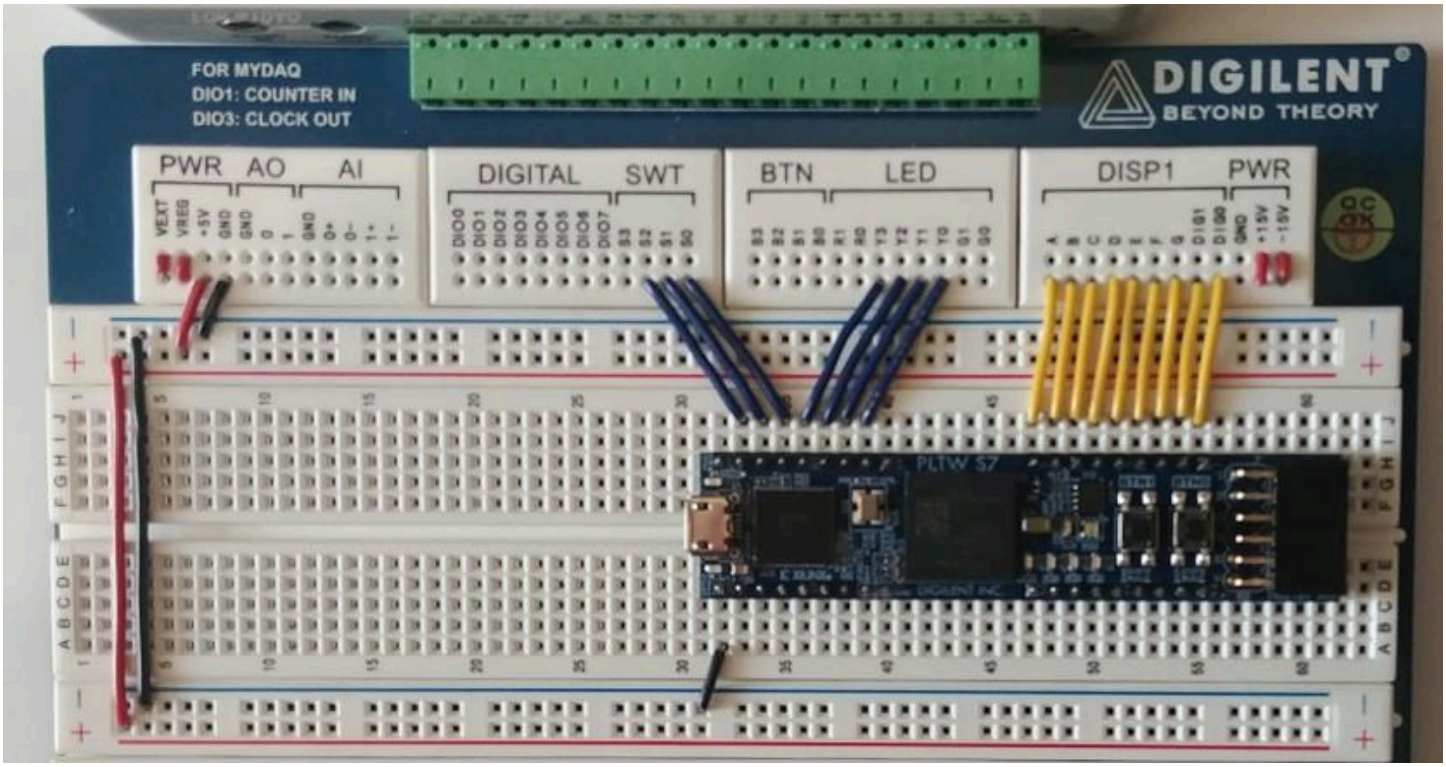


Figure 2. PLTW S7 on a myDigital Protoboard

2. Map the design's three inputs (X, Y, and Z) to the pin inputs/outputs (PIOs) shown in the image.

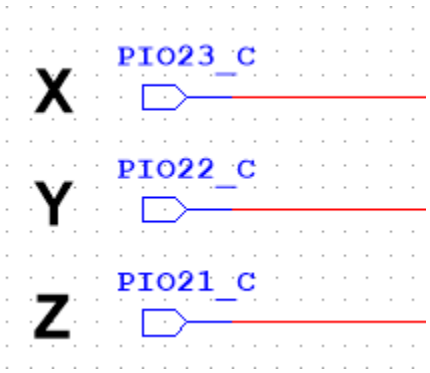


Figure 3. Input Pins

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3. Connect the DMS slide switches SW2(X), SW1(Y), and SW0(Z) to the PIOs shown in the physical wiring image SW2(X) to PIO23, SW1(Y) to PIO22, and SW0(Z) to PIO21. There are additional wires shown in the image that can be ignored for this activity. These will be used in future activities

4. The DMS has a Common Cathode SSD (0). To use DIG0, but not DIG1 then DIG0 must be connected to ground. Instead of physically placing a wire between DIG0 and GND it is more convenient to manage this in CDS.

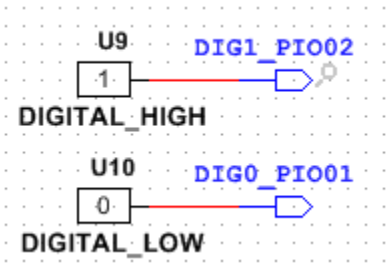


Figure 3. Input Pins

5. Connect PIO1 to DIG0 and PIO2 to DIG1. Refer to the physical wiring image.

6. Map the design's seven outputs (A, B, C, D, E, F, and G) to PIOs shown in the image.

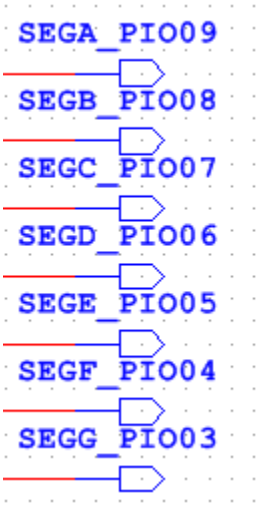


Figure 4. Output Pins

7. Connect the segments of the display labeled as DISP1A through DISPG to the PIOs shown in the physical wiring image (for example DISP1A to PIO9 and DISP1G to PIO3).

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8.The wires between PIO17 through PIO20 to the LED inputs are not used in this activity.

9. Connect the remaining power and ground wires as shown in the physical wiring image.

10. Design then test your project by transferring to the PLTW S7.

**CAREER CONNECTIONS**

Walt Maclay: Medical Wearables

Walt Maclay Source

The **Programmable Logic Device (PLD)** technology used in mobile devices, such as medical wearables and other medical monitoring devices, is a scaled-down version of the **Field Programmable Gate Array (FPGA)** you used in this lesson. A PLD is a good choice for mobile devices because of its electrical efficiency which does not generate much heat and its low power consumption to extend the time between battery charges. Source

Walt Maclay is the president and founder of Voler Systems, which specializes in many areas including medical devices, consumer products, wearable device design, and IoT design. Marclay has a well-established career as an electronics design engineer with Texas Instruments and Fairchild leading up to and continuing with the foundation of Voler Systems. Source

Task 1: In the space provided below attach a video of the "DOB" Programmed on the PLTW S7 PLD Chip.

| Insert your work on your E-Portfolio. Attach your E-Portfolio link here. Make sure to include a video of your PLD in operation. OR Gate PLD verbally explain the chip. |
| --- |
| https://sites.google.com/riversideunified.org/matthewjeide/projects/de-2024-2025/pltw-s7-date-of-birth-project |

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## Conclusion

Please answer in complete sentences. Minimum of three.

1. Describe the strategy you used to recreate the Date of Birth design in PLD design mode? Did you take any shortcuts to create the circuit quickly?

When recreating the Date of Birth design in the PLD design, it proved to be more of a challenge than originally thought. Originally, I believed I could just copy over the original design to the new PLD design and set up the connections again. However, it turns out that Multisim treats the logic gates from the two different designs as completely different parts and logic gates from normal design mode cannot be pasted into a PLD design. So the design had to be made from scratch, I made sure to reuse gates as best as possible, even though theoretically the PLTW S7 has the processing power for more gates, and I also used color coding for the wires as there was a lot of wire crossing.

2. List three advantages of implementing combinational logic design with programmable logic versus traditional discrete logic design.

There are numerous advantages to implementing combinational logic design with the programmable logic device, the biggest one being the time saved from wiring all of the logic for the combination logic and replacing it with just a single daughter board and a 3-minute upload. The PLTW S7 additionally has helpful features such as on-board LEDs, which are very helpful for debugging. On top of this, the PLTW S7 is much cleaner than the amount of chips and wires you would have to install for normal combinational logic, and considering the point of how feasible that could be depending on the complexity of the project.

On the other hand, the PLTW S7 does have some drawbacks, the uploads are quite lengthy, while shorter than manually wiring by hand, it involves several minutes of just waiting. Debugging the PLTW S7 is also much more frustrating because of this reason, waiting several minutes to upload the new code just for it to not work.