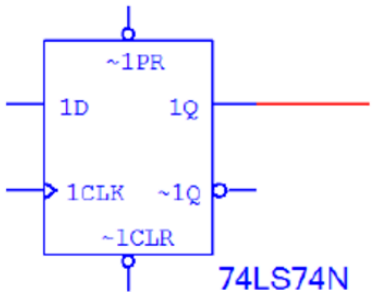
Jeide, Matthew 4/7/2025 Period 2

W14B: DE 3.1.1 Sequential Logic: D Flip-Flops and J/K Flip-Flops

Read the introduction to Flip-Flops. You must show your work neatly on your Google Draw. Check your answers using the oscilloscope on Multisim.

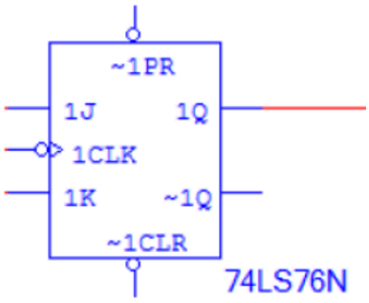
INTRODUCTION

Flip-flops are the fundamental building blocks of **sequential logic**. There are a variety of different flip-flop types and configurations. In this activity (and this course), we will only study two types of flip-flops: the D flip-flop that was introduced in Unit 1 and the J/K flip-flop. After reviewing the basic operation of the 74LS74 D and the 74LS76 J/K flip-flops, this activity will examine two applications of flip-flops.



D	CLK	Q	$\overline{Q}$
0	↑	0	1
1	↑	1	0

↑ : Rising Edge of Clock



J	K	CLK	Q	
0	0	↑	Q_0	No Change
0	1	↑	0	Clear
1	0	↑	1	Set
1	1	↑	$\overline{Q}_0$	Toggle

↑ : Rising Edge of Clock

$\overline{Q}$: Complement of Q

EQUIPMENT

- Computer with Circuit Design Software (CDS)

Before we jump into a discussion of practical applications of J/K or D flip-flops, let's revisit how flip-flops work.

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Flip-flops

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1. 1. For the 74LS74 D flip-flop shown in Figure 2, complete the timing diagram for the output signal **Q**. Note that the **CLK** input for this flip-flop is a positive edge **trigger**and both the **PR** and **CLR** asynchronous inputs are active low.

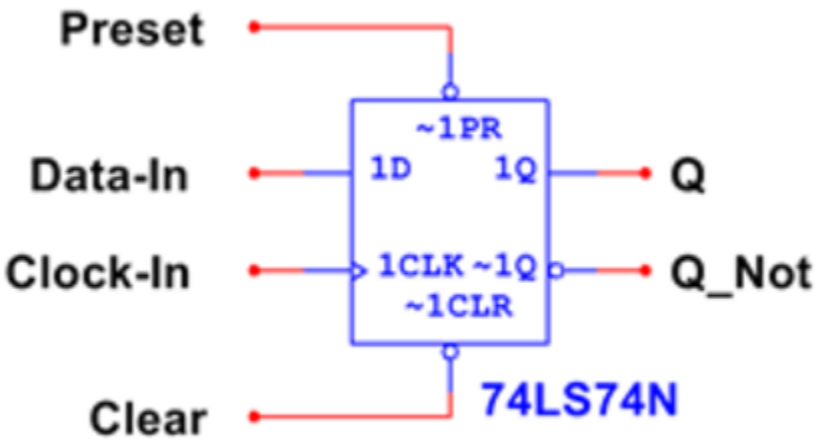

Figure 2. The logic symbol of a D flip-flop

Show the graph for Q and use the truth table to help you identify valuable information. Replace.

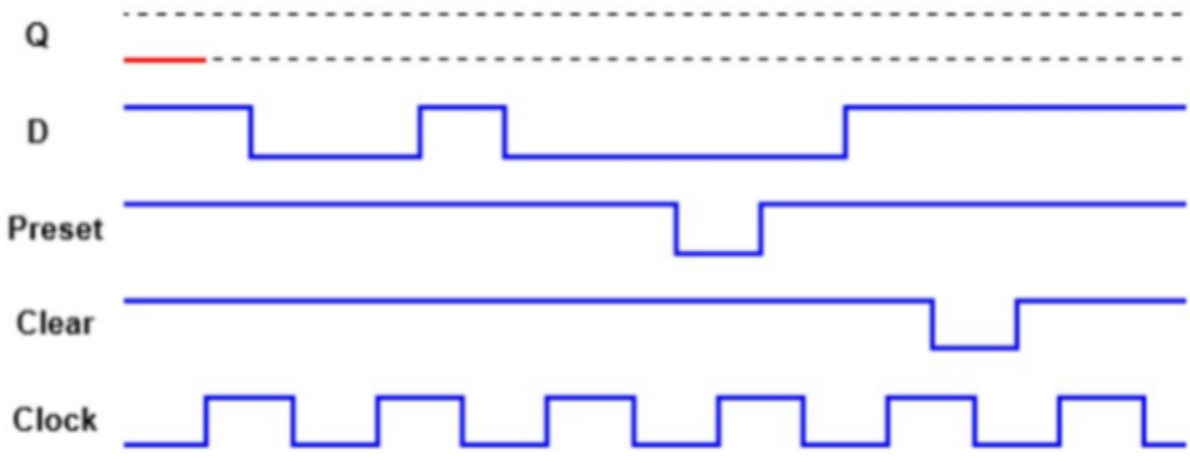

Figure 3. Flip-flop Signals

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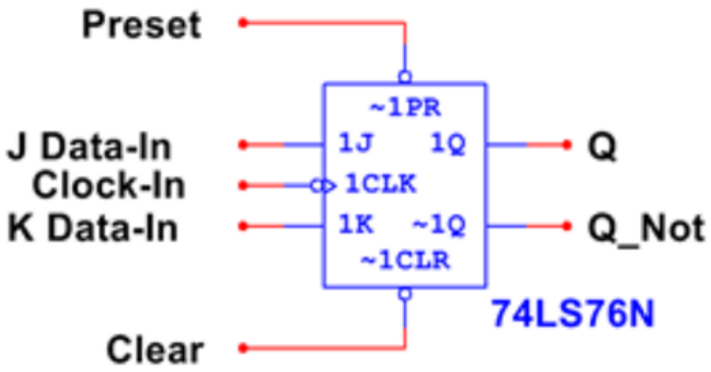
2. For the 74LS76 J/K flip-flop shown in Figure 4, complete the timing diagram for the output signal **Q**. Note that the **CLK** input for this flip-flop is a **negative edge trigger** and both the **PR** and **CLR** asynchronous inputs are active low.



Complete the table for “Que”

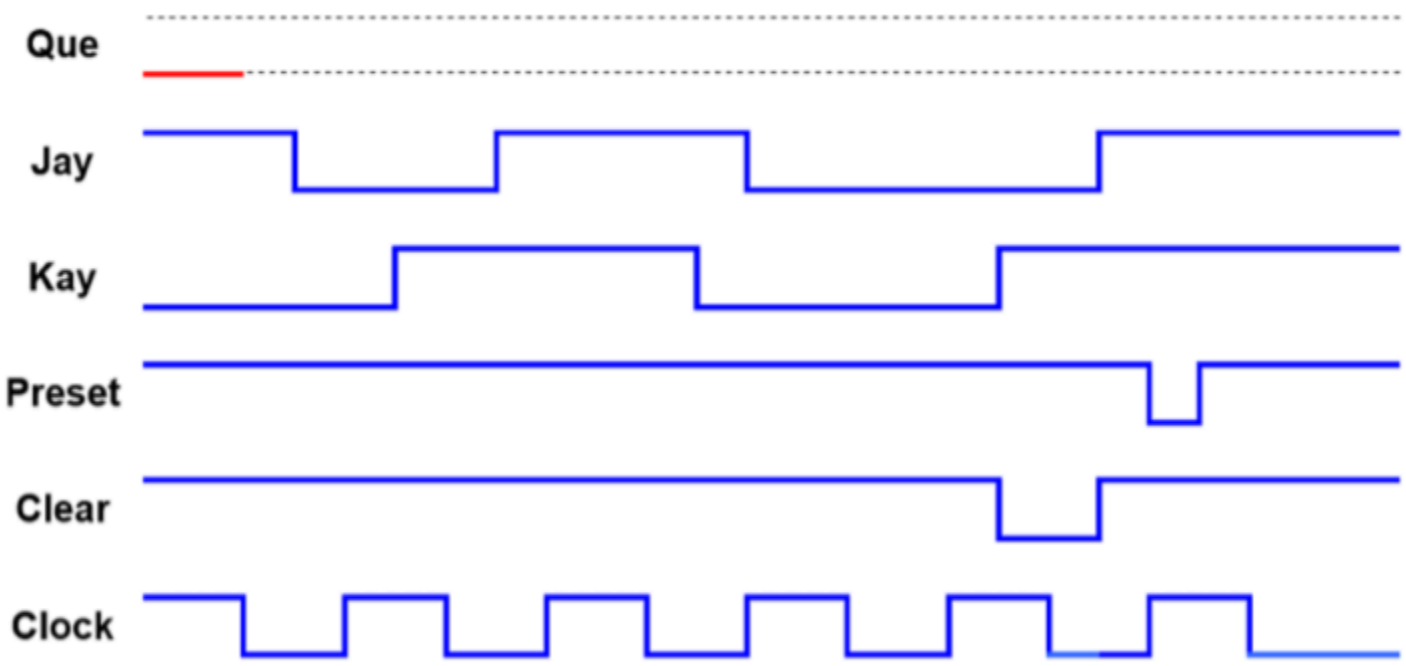


Figure 5. J/K flip-flop Signals

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D and J/K flip-flops

Let's examine some simple applications of the D and J/K flip-flops.

When flip-flops were discussed briefly in Unit 1, we saw that a D flip-flop could be used to create a *Divide-by-Two* circuit. Remember, a *Divide-by-Two* circuit is one that generates a **clock**output that is half the **frequency**of the clock input. Likewise, a *Divide-by-Two* circuit can be implemented with a J/K flip-flop.

3. Examine the J/K flip-flop shown in Figure 6.

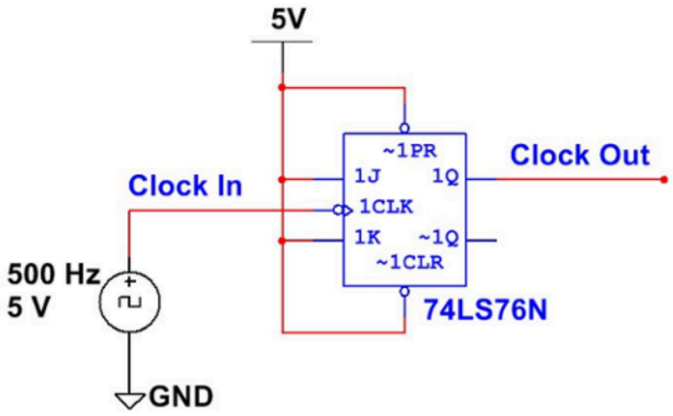

Figure 6. J/K Divide-by-Two Circuit

Complete Clock_Out

a. In your notebook, predict the timing diagram for a J/K *Divide-by-Two* circuit.

Figure 7. J/K Divide-by-Two Circuit Signals

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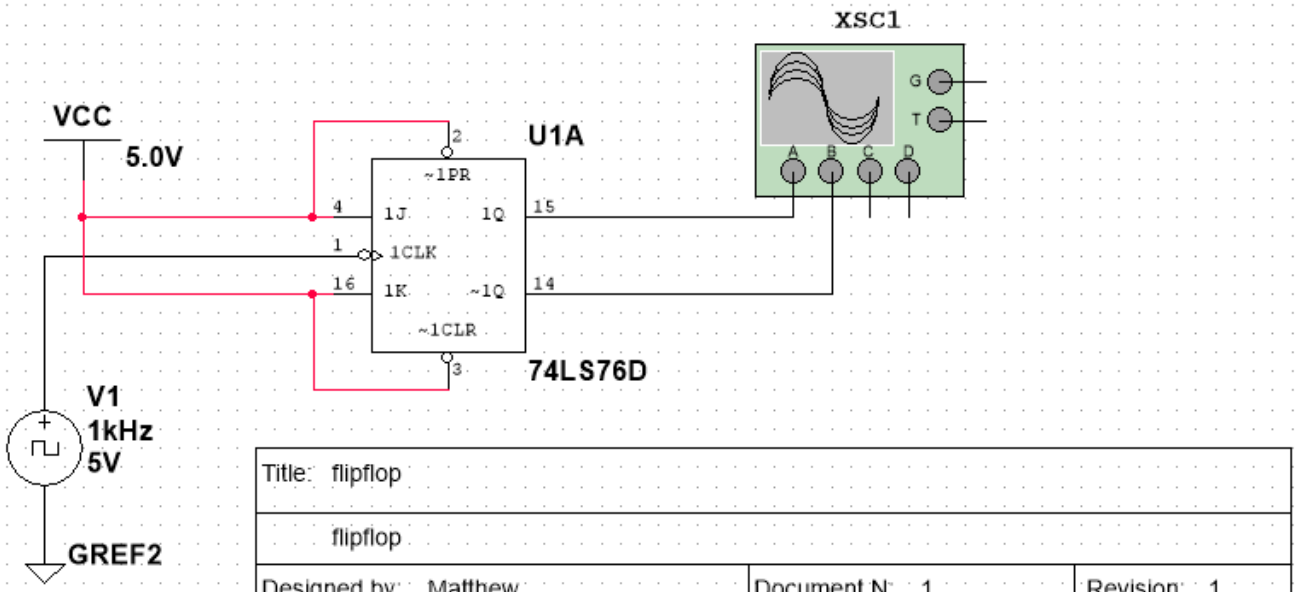
Multisim Graph with Oscillation



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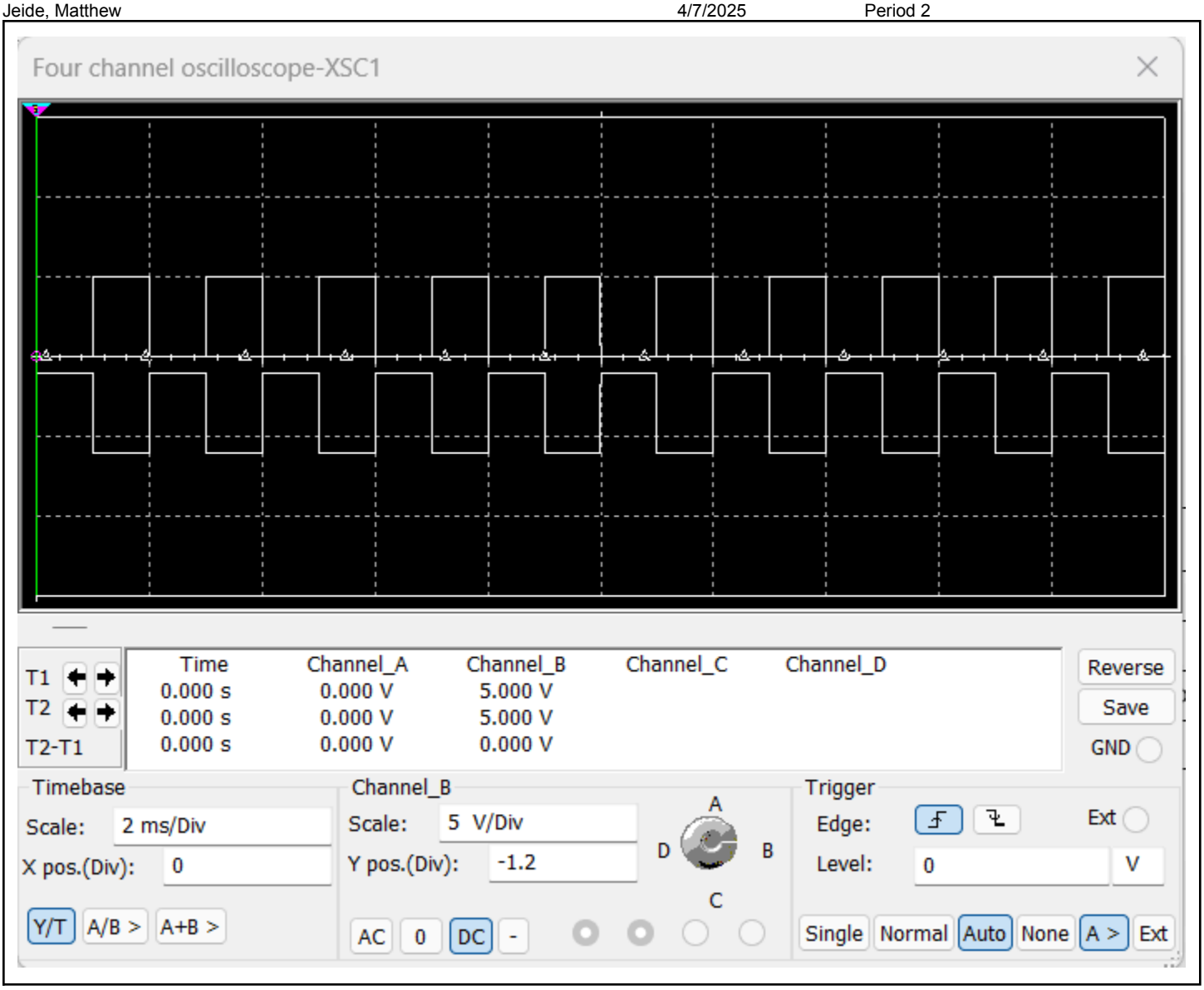

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b. Using the CDS, enter the *Divide-by-Two* circuit, adding an oscilloscope to monitor the two signals **Clock_In** and **Clock_Out**.

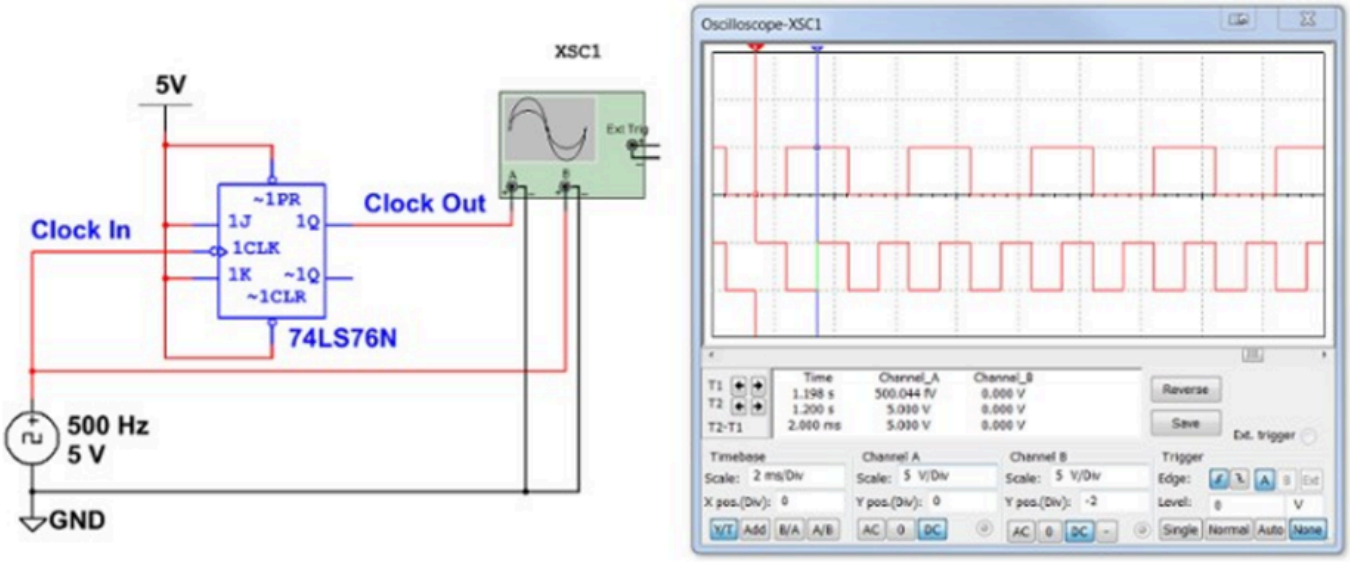


Figure 8. J/K Divide-by-Two Circuit Oscilloscope

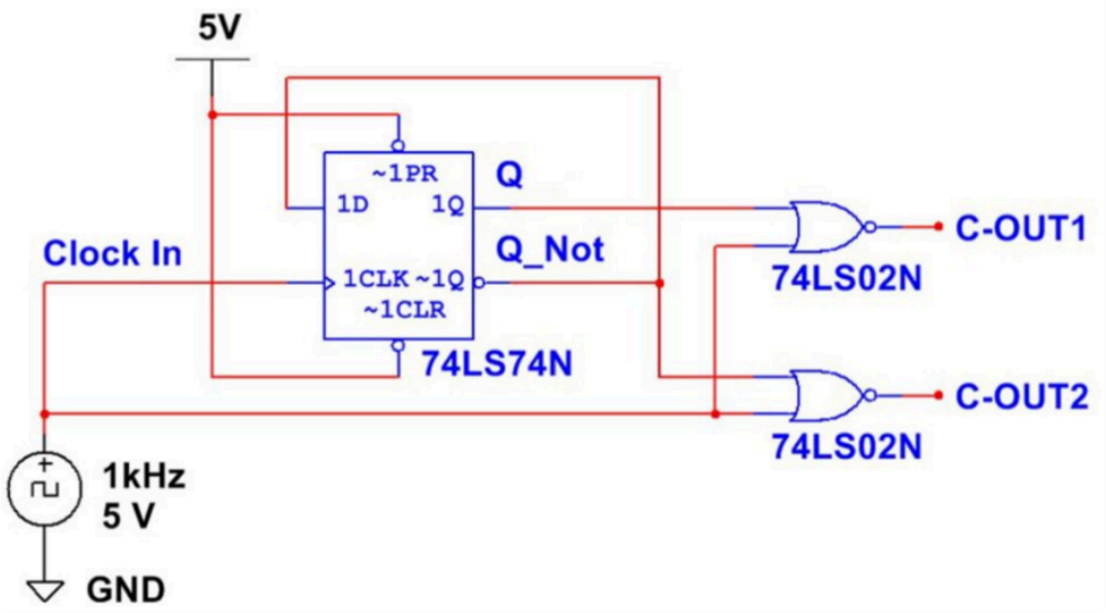
c.Run the simulation and capture several **periods** of the output signal. Verify that the circuit is working as expected and that the output signal matches your predictions from step 3a. If the results do not match, review your work and make necessary corrections.

4. Change the frequency of **Clock_In** to 20 kHz and re-simulate. What effect did this change have on the frequency of the output signal **Clock_Out**?

Frequency of Clock_Out
F=1/Period A J/K flip-flop is configured as a divide-by-two circuit toggles its output on every rising edge of the input clock, so it effectively halves the input clock frequency. Clock_out frequency becomes 10 kHz.

5. The circuit shown in Figure 10 generates two non-overlapping signals at the same frequency. These signals, **C-OUT1** and **C-OUT2**, were frequently used by

early microprocessor systems that required four clock transitions all synchronized by one clock.



Complete the graphics below.

a. In your notebook, complete the timing diagram below for the *Non-Overlapping Signal Generator* circuit.

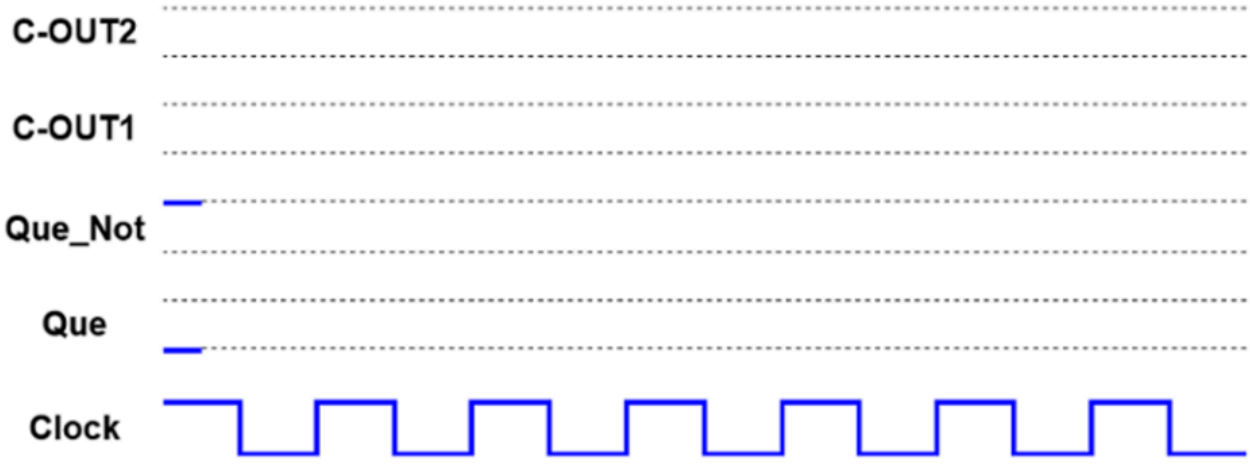


Figure 10. Non-Overlapping Signals

Create a graphic using an oscilloscope on Multisim and attach the graphic below.

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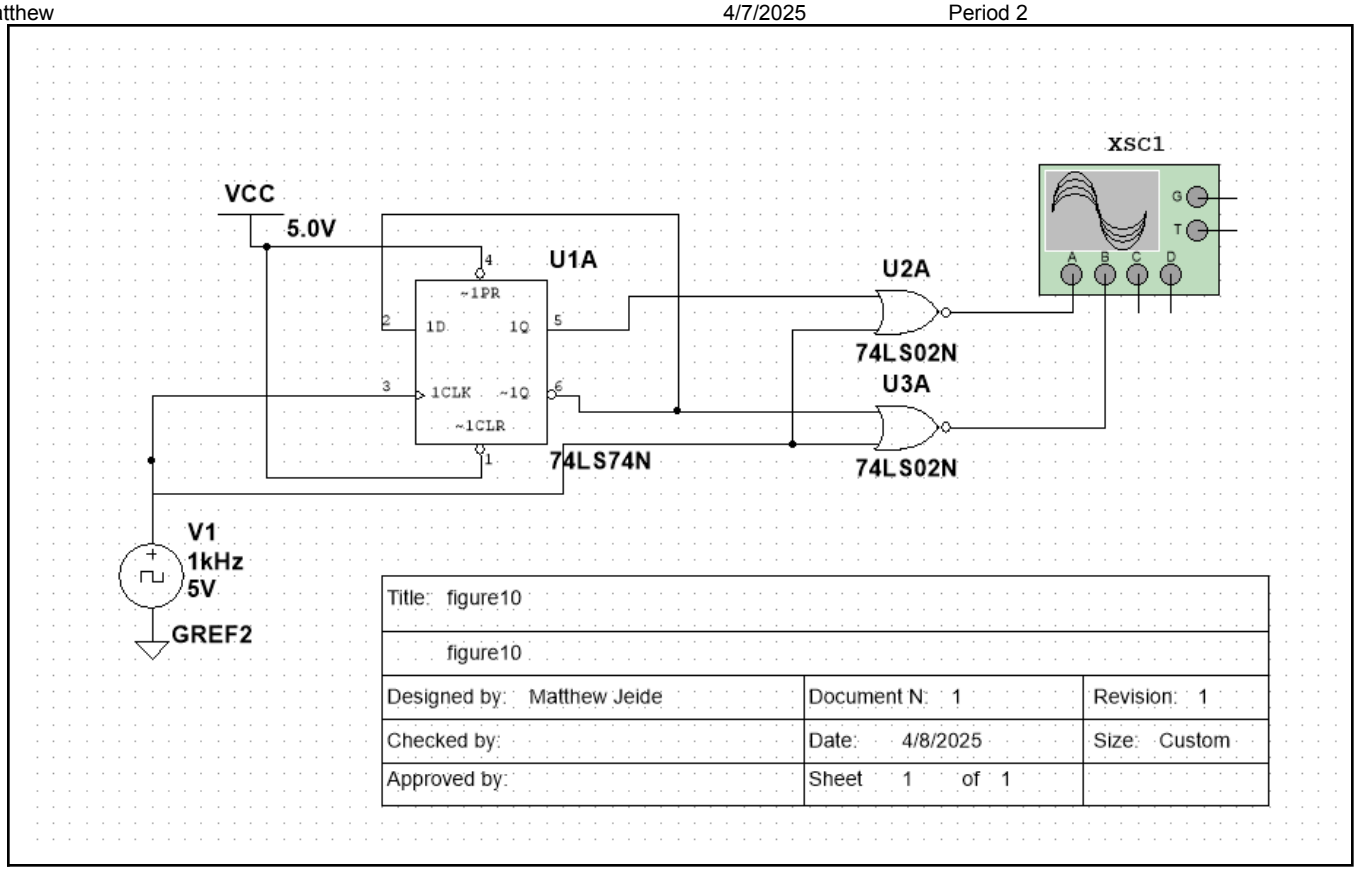

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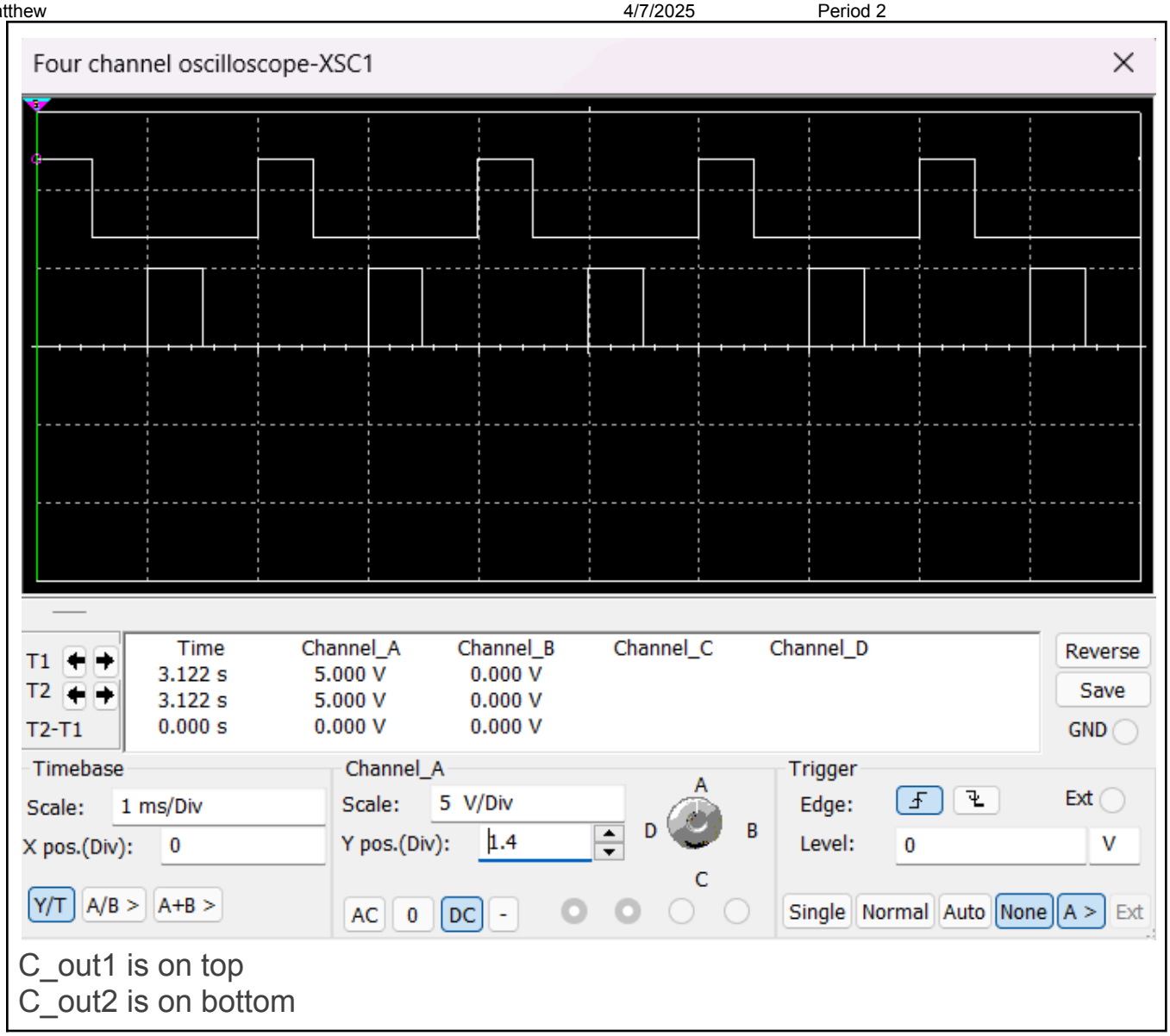

C_out1 is on top
C_out2 is on bottom

b. Using the CDS, enter the *Non-Overlapping Signal Generator* circuit. Add an oscilloscope to monitor the three signals **Clock**, **C-OUT1**, and **C-OUT2**. Run the simulation and capture several periods of the output signals. Verify that the circuit is working as expected and the output signals match the predictions from step 5a. If the results do not match, review your work and make any necessary corrections.

c. The input signal, **Clock**, was a 1 kHz square wave with a 50% **duty cycle**. What is the frequency and duty cycle of the output signals **C-OUT1** and **C-OUT2**?

25% duty cycle for both, 250Hz.

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d.Change the **Clock** frequency to 2 KHz and re-simulate. What effect did this change have on the frequency of the output signals **C-OUT1** and **C-OUT2**?

The frequency doubled to 500Hz.

e. What effect did this change have on the duty cycle of the output signals **C-OUT1** and **C-OUT2**?

No change, the ratio off the duty cycle is still the same.

CONCLUSION

Write using complete sentences.

1. Flip-flops have both synchronous and asynchronous inputs. Describe each input type and give an example of each.

Synchronous inputs are dependent on the clock signal, for example a D input on a D flip flop. Asynchronous inputs are not dependent on the clock signal, for example a clear or set signal can force a flip-flop's output regardless of the clock.

2. Match each of the four input symbols with their signal type.

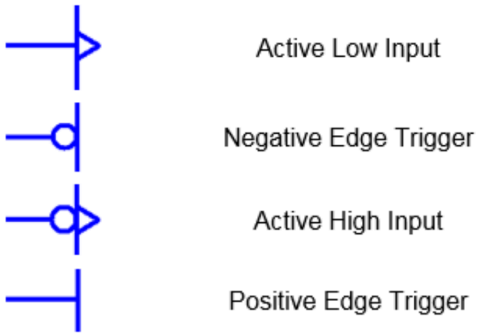

Figure 12. Input Symbols

1. Positive Edge Trigger
2. Active Low Input
3. Negative Edge Trigger
4. Positive Trigger

3. Describe the functional difference between a D flip-flop and a D latch.

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A flip flop is edge triggered (responds only on a clock edge), a latch is level sensitive (responds as long as the clock is high).