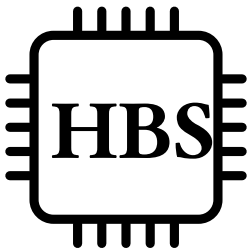

Hardware Build System
User Manual

Revision 0.0

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Abstract

This document serves as the official user manual for Hardware Build System (HBS). HBS is a Tcl-based, minimal common abstraction approach for build system for hardware designs. The main goals of the system include simplicity, readability, a minimal number of dependencies, and ease of integration with the existing Electronic Design Automation (EDA) tools.

keywords: automation, hardware build system, hardware design, hardware synthesis, project maintenance, testbench runner, simulation, FPGA, ASIC, productivity

Contents

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Glossary

Not all terms defined in the glossary list are used in the user manual. Some of them are formally defined because they are helpful when discussing, for example, core definition.

core

Tcl namespace in which `hbs::Register` proc is called.

core name

Name of the Tcl namespace in which `hbs::Register` is called. For example, if `hbs::Register` is called in namespace `lib::pkg::my-core`, then `my-core` is the core name.

core path

Tcl namespace for the core. For example, if `hbs::Register` is called in namespace `lib::pkg::my-core`, then `lib::pkg::my-core` is the core path.

dependency

A target on which at least one other target depends. The dependency is an argument for at least one `hbs::AddDep` proc call.

depender

A target depending on at least one another target. Within a depender body the `hbs::AddDep` proc is called at least once.

flow

An ordered set of actions taken by a tool to produce a result specified by a user.

hbs file

A file with `.hbs` extension containing valid Tcl code.

proc

A Tcl procedure.

stage

A piece of a tool flow with a clearly defined task and output. The number and types of stages depend on a tool. For example, the GHDL has analysis, elaboration and simulation stages.

target

A proc, which name does not start with the floor character (_), defined in core.

target name

The name of the target in the target path. For example, if the target path is `lib::pkg::my-core::my-target`, then the target name is `my-target`.

target path

The Tcl path for the target. For example, if proc `my-target` is defined in the core with the core path `lib::pkg::my-core`, then the target path is `lib::pkg::my-core::my-target`.

tool

A software capable of processing hardware description sources or output from another tool. Example tools are: GHDL, Verilator, yosys, Vivado, nvc, etc.

to run a target

To execute commands defined in the target.

1 Overview

Hardware Build System (HBS) is a build system for hardware design projects. A build system for hardware design collects and processes files required for FPGA programming, ASIC production, running functional simulation, or carrying out formal verification. The files required to obtain desired output usually include much more than just classic hardware description files such as VHDL or SystemVerilog sources. For example, any synthesis or place and route tool requires also design contraints, at least for pin location and timing closure analysis. Moreover, most of real projects are not implement from scratch and utilize third-party IP cores. Those IP cores might be provided in different formats. Sometimes, they might even be encrypted. HBS tries to support all files that might potentially be required to generate final result. HBS does not limit to managing only pure hardware description files.

HBS was created out of frustration with all existing build systems for hardware designs.

2 Installation

All installation methods require that `hbs` and `hbs.tcl` files are placed in the same directory. There are four preferred installation methods.

1. Copy `hbs` and `hbs.tcl` files to your project. This is preferred if you want to modify HBS source files change its default behavior. It is not advised to change the default behavior, but if you need, feel free to adjust the build system to your project needs.
2. Copy `hbs` and `hbs.tcl` files to one of the directories in the `$PATH` environment variable.
3. Clone the repository and add its path to the `$PATH` environment variable.
4. Clone the repository and add an alias to the `hbs` file in `.bashrc` file (or equivalent).

2.1 Dependencies

HBS has three dependencies, one mandatory and two optional.

1. `tclsh (version >= 8.5)`.
2. `python3` - required for testbench target detection, automatic testbench running and dependency graph generation. If mentioned functionalites are not required, you can directly used `hbs.tcl` script instead of the `hbs` Python wrapper.
3. `graphviz` - required only if user wants to generate a dependency graph.

3 Internal architecture

It was decided that HBS will be implemented using Tcl language because of the following reasons:

1. Implementing a hardware build system in Tcl allows the execution of build system code during the EDA tool flow. This, in turn, gives direct access to all EDA tool custom commands. Moreover, these custom commands can be evaluated in arbitrary places.
2. If the EDA tool provides the Tcl interface, then the Tcl shell is provided by the EDA tool vendor. The shell is nstalled during the installation of vendor tools. This implies that, in some cases, the build system user does not even have to install additional programs.
3. Executing arbitrary programs in arbitrary places in Tcl is very simple. There is a dedicated `exec` command for invoking subprocesses. If executing a subprocess requires prior dynamic arguments evaluation, the `exec` command call must be prepended with the `eval` command. Even in Python, invoking a subprocess is not so straighforward.

One of the most important things while designing the HBS was the separation of common build process operations that would constitute a common abstraction layer over EDA tools. At the end, it was decided that the following actions should constitute the common abstraction layer:

1. Target device setting - some EDA tools use the term “part” instead of “device,” for example, Vivado. Simulation EDA tools do not require a device setting. However, all synthesis EDA tools require

information on the target device. This is why setting the device became part of the common abstraction layer.
2. File addition - this includes support for adding files of all formats supported by a given EDA tool.
3. Library setting - setting HDL file library.
4. HDL standard setting - setting HDL file standard revision. The build system has to manage this because some tools can not handle analyzing different design units using different standard revisions, for example, nvc. In such a case, the build system must decide what the common standard revision shall be used for analyzing all HDL files.
5. Dependency specification - this is the core feature of any build system.
6. Generics/parameters setting - configuring parametric designs must be an inherent feature of any hardware build system.
7. Design top module setting - all EDA tools carrying out simulation or synthesis requires information on the top module.
8. Code generation - a hardware build system must provide a simple way for automatic arbitrary code generation. This is further explained in Section 3.12.

3.1 General structure

The HBS is implemented in two files `hbs.tcl` and `hbs`. The first is implemented in Tcl, and the second in Python. The `hbs.tcl` file implements all the core features related directly to the interaction with the EDA tools. The `hbs.tcl` provides the following functions:
1. Dumping information about detected cores in JSON format.
2. Listing cores found in hbs files.
3. Listing targets for a given core.
4. Running target provided as a command line argument.

The `hbs` is a wrapper for the `hbs.tcl` and serves the following additional functions:
1. Showing documentation for hbs Tcl symbols.
2. Generating dependency graph.
3. Listing testbench targets.
4. Running testbench targets.

By default, the user calls the `hbs` program. However, if none of the additional functions are required, the user can call the `hbs.tcl` directly. In such a case, the whole build system is limited to a single file.

3.2 Cores and cores detection

When the user calls `hbs` (or `hbs.tcl`), all directories, starting from the working directory, are recursively scanned to discover all files with the `.hbs` extension (symbolic links are also scanned). Files with the `.hbs` extension are regular Tcl files that are sourced by the `hbs.tcl` script. However, before sourcing hbs files, the file list is sorted so that scripts with shorter path depth are sourced as the first ones. For example, let us assume the following three hbs files were found:
- `a/b/c/foo.hbs`,
- `d/bar.hbs`,
- `e/f/zaz.hbs`.

Then, they would be sourced in the following order:
1. `d/bar.hbs`,
2. `e/f/zaz.hbs`,
3. `a/b/c/foo.hbs`.

Such an approach allows controlling when custom symbols (Tcl variables and procedures) are ready to use. For example, if the user has a custom procedure used in multiple hbs files, then the user can create

separate `utils.hbs` file contaning utility procedures, and place it in the the project root directory. This guarantees that `utils.hbs` will be sourced before any hbs file in subdirectories. Within hbs files, the user usually defines cores and targets, although the user is free to have any valid Tcl code in hbs files.

The below snippet presents a very basic flip-flop core definition. The flip-flop core has a single target named `src`. The core consists of a single VHDL file.

```
namespace eval flip-flop {
  proc src {} {
    hbs::AddFile flip-flop.vhd
  }
  hbs::Register
}
```

To register a core, the user must explicitly call `hbs::Register` procedure at the end of the core namespace. Such a mechanism helps to distinguish regular Tcl namespaces from Tcl namespaces representing core definitions. If the user forgets to register a core, the build system gives a potential hint. An example error message is presented below.

```
[user@host tmp] hbs run lib::core::tb
checkTargetExists: core 'lib::core' not found, maybe the core is not:
  1. registered 'hbs doc hbs::Register',
  2. sourced 'hbs doc hbs::IgnoreRegexes'.
```

Each core is identified by its unique path. The core path is equivalent to the namespace path in which `hbs::Register` is called. Using the namespace path as the core path gives the following possibilities:

1. The user can easily stick to the VLNV identifiers if required. This is presented in the below snippet. In this case, the flip-flop core path is `vendor::library::flip-flop::1.0`.

   ```
   namespace eval vendor::library::flip-flop::1.0 {
     proc src {} {
       hbs::AddFile flip-flop.vhd
     }
     hbs::Register
   }
   ```

2. The user can define arbitrary deep core paths (limited by the Tcl shell). This is presented in the below snippet. In this case, the core path consists of seven parts.

   ```
   namespace eval a::b::c::d::e::f::flip-flop {
     proc src {} {
       hbs::AddFile flip-flop.vhd
     }
     hbs::Register
   }
   ```

3. The user can nest namespaces to imitate the structure of libraries and packages. This is presented in following snippet.

   ```
   namespace eval lib {
     namespace eval pkg1 {
       namespace eval d-flip-flop {
         proc src {} {
   ```

```
        hbs::AddFile d-flip-flop.vhd
      }
      hbs::Register
    }
    namespace eval t-flip-flop {
      proc src {} {
        hbs::AddFile t-flip-flop.vhd
      }
      hbs::Register
    }
  }
  namespace eval pkg2 {
    namespace eval jk-flip-flop {
      proc src {} {
        hbs::AddFile jk-flip-flop.vhd
      }
      hbs::Register
    }
  }
}
```

Three flip-flop cores are defined in the snippet. The below snippet presents output for listing flip-flop cores.

```
[user@host tmp]$ hbs list-cores
lib::pkg1::d-flip-flop
lib::pkg1::t-flip-flop
lib::pkg2::jk-flip-flop
```

3.2.1 Excluding hbs files from being sourced

Sometimes a file with the `.hbs` extension is not a valid hbs file, or maybe you want to temporarily disable valid hbs files from being sourced. HBS provides a built-in mechanism for excluding files with the `.hbs` extension from being sourced. This is achieved using the `hbs::AddIgnoreRegex` function. You just have to call this function in one of valid hbs files. The function will be executed once the file containing the call is sourced.

Usually the hbs file containing calls to the `hbs::AddIgnoreRegex` proc is placed in the project root directory. This is becuase hbs files placed in the project root directory are sourced before hbs files placed in subdirectories. Order of hbs files sourcing is described in Section 3.2.

Arguments provided to the `hbs::AddIgnoreRegex` proc are treated as regular expressions. This allows for ignoring multiple paths using a single regex. However, you are free to provide multiple ignore regex, and all of them will be checked while sourcing hbs files.

3.3 Targets and targets detection

HBS automatically detects targets. Targets are all Tcl procedures defined in the scope of core namespaces (namespaces with a call to `hbs::Register`). However, to allow users to define custom utility procedures within cores, procedures with names starting with the floor character (_) are not treated as core targets. The below snippet presents an example edge detector core definition.

```
namespace eval vhdl::simple::edge-detector {
  proc src {} {
```

```
    hbs::SetLib "simple"
    hbs::AddFile src/edge_detector.vhd
  }
  proc _tb {top} {
    hbs::SetTool "ghdl"
    hbs::SetTop $top
    src
    hbs::SetLib ""
  }
  proc tb-sync {} {
    _tb "tb_edge_detector_sync"
    hbs::AddFile tb/tb_sync.vhd
    hbs::Run
  }
  proc tb-comb {} {
    _tb "tb_edge_detector_comb"
    hbs::AddFile tb/tb_comb.vhd
    hbs::Run
  }
  hbs::Register
}
```

The core path is `vhdl::simple::edge-detector`. The core has three targets: `src`, `tb-sync`, `tb-comb`, and one utility procedure `_tb`. The `_tb` procedure was defined to share calls common for testbench targets `tb-sync` and `tb-comb`. Moreover, all target procedures are also regular Tcl procedures. Such an approach allows for calling them in arbitrary places. The `_tb` procedure calls the `src` procedure because the `edge_detector.vhd` file is required for running testbench targets.

All targets are represented by a unique target path. Target path consists of the core path and target name. For example, the `src` target of the edge detector has the following path `vhdl::simple::edge-detector::src`.

3.4 Testbench targets

HBS is capable of automatically detecting testbench targets. Testbench targets are targets which names:

1. start with the `tb-` or `tb_` prefix,
2. end with the `-tb` or `_tb` suffix,
3. equal `tb`.

For example, for the following hbs file:

```
namespace eval my-core {
  proc tb {} {
    puts "Hello from tb"
  }
  proc my-tb {} {
    puts "Hello from my-tb"
  }
  proc tb_my {} {
    puts "Hello from tb_my"
  }
  hbs::Register
}
```

the `hbs` program detects the following testbench targets:

```
[user@host tmp] hbs list-tb
my-core::my-tb
my-core::tb
my-core::tb_my
```

3.5 Running targets

HBS allows running any target of registered cores. Even if the target itself has nothing to do with the hardware design. For example, running target `print` from the following snippet:

```
namespace eval core {
  proc print {} {
    puts "Hello!"
  }
  hbs::Register
}
```

Results with the following output:

```
[user@host tmp]$ hbs run core::print
Hello!
```

However, in most cases, you want to run a target related to the flow of the set EDA tool. In such a case, instead of manually calling all of the required tool commands, you can call the `hbs::Run` procedure in the core target procedure. The `hbs::Run` procedure has an optional argument accepting the stage after which the tool flow should stop. This is further described in Section 3.9. After `hbs::Run` returns, the user can continue processing. For example, the user can run scripts analyzing code coverage or preparing additional reports.

3.6 Target parameters

As core targets are just Tcl procedures, they can have parameters. Moreover, parameters can have optional default values. Additionally, HBS allows to provide command line arguments to the run target. This is a very convenient feature in build systems. The blow snippet presents a very simplified example.

```
namespace eval core {
  proc target {{stage "bitstream"}} {
    puts "Running until $stage"
    # hbs::Run commented out because this is just an example.
    #hbs::Run $stage
  }
  hbs::Register
}
```

The core does not build any hardware design. However, the example shows how the build stage can be passed from the command line to an EDA tool. The blow snippet presents output from running the target with different `stage` parameter values.

```
[user@host tmp]$ hbs run core::target
Running until bitstream
[user@host tmp]$ hbs run core::target synthesis
Running until synthesis
```

Another practical example of target parameters usage is setting the simulator for testbench target from the command line or changing the top-level module. What target parameters are used for is limited only by your imagination, and Tcl semantics.

3.7 Target context

An engineer implementing a given core, you control the dependencies of the core. However, you do not control who will use the core and how. As targets are regular Tcl procedures, there is a need for a mechanism allowing the core author to evaluate the target procedure in the invariant environment. Such a mechanism in HBS is called the target context.

The target context assures that the following variables are not affected by dependee or dependency target execution:

1. HDL library,
2. HDL standard,
3. top module name,
4. arguments prefix,
5. arguments suffix,
6. the core path,
7. the target name,
8. the target path.

Below snippet presents an example of the target context mechanism.

```
namespace eval pkg {
  namespace eval foo {
    proc src-foo {} {
      hbs::SetLib "lib-foo"
      hbs::AddDep pkg::bar::src-bar
      puts "foo lib: $hbs::Lib"
      puts "foo core: $hbs::ThisCorePath"
      puts "foo target: $hbs::ThisTarget"
    }
    hbs::Register
  }
  namespace eval bar {
    proc src-bar {} {
      hbs::SetLib "lib-bar"
      puts "bar lib: $hbs::Lib"
      puts "bar core: $hbs::ThisCorePath"
      puts "bar target: $hbs::ThisTarget"
    }
    hbs::Register
  }
}
```

The below snippet presents the output from running the `pkg::foo:src-foo` target. As can be seen, setting library in a target of one core, does not affect library in the target of another core.

```
[user@host tmp] hbs run pkg::foo::src-foo
bar lib: lib-bar
bar core: pkg::bar
bar target: src-bar
foo lib: lib-foo
```

```
foo core: pkg::foo
foo target: src-foo
```

3.8 Target dependencies

In HBS, targets might depend on other targets instead of cores depending on cores. Such an approach allows for fine-grained control of dependencies.

To declare target dependency, you must call the `hbs::AddDep` procedure within the target procedure. The first argument is the dependency path. The remaining arguments are optional and are passed to the dependency procedure as arguments.

To add multiple distinct dependencies, the user must call `hbs::AddDep` multiple times. The ability to pass custom arguments to dependency was evaluated as much more advantageous than the ability to add multiple dependencies with a single `hbs::AddDep` call.

The `hbs::AddDep` internally calls the dependency procedure with the provided arguments. It also tracks dependencies so that generating a dependency graph is possible. Within a single flow, each target procedure can be run at most once with a particular set of arguments. This implies that if multiple target procedures add the same dependency with the same arguments, the dependency procedure is run only once during the first `hbs::AddDep` call. To enforce some target procedure rerun, the user can always directly call the target. However, enforcing target procedure rerun usually is an alert that a regular Tcl procedure shall be used instead of the core target procedure.

The bloew snippet contains an example core definitions for presenting target dependency rules.

```
namespace eval core-a {
  proc target {} {
    hbs::AddDep core-b::target
    hbs::AddDep core-c::target
    hbs::AddDep generator-core::gen a
    hbs::AddDep generator-core::gen x
    puts "core-a::target"
  }
  hbs::Register
}
namespace eval core-b {
  proc target {} {
    hbs::AddDep core-c::target
    hbs::AddDep generator-core::gen b
    hbs::AddDep generator-core::gen x
    puts "core-b::target"
  }
  hbs::Register
}
namespace eval core-c {
  proc target {} {
    puts "core-c::target"
  }
  hbs::Register
}
namespace eval generator-core {
  proc gen {arg} {
    puts "generator-core::gen $arg"
  }
```

```
  hbs::Register
}
```

There are four cores: `core-a`, `core-b`, `core-c`, `generator-core`. `core-a` depends on `core-b` and `core-c`. `core-b` depends on `core-c`. Moreover, cores `core-a` and `core-b` depend on the `generator-core`. However, they use different argument values for generation.

The below snippet presents output from running target `core-a::target`.

```
[user@host tmp]$ hbs run core-a::target
core-c::target
generator-core::gen b
generator-core::gen x
core-b::target
generator-core::gen a
core-a::target
```

As can be seen, the `core-c::target` is run only once, even though both `core-a::target` and `core-b::target` depend on it. This is because `core-c::target` has no arguments and can be added as a dependency only once. On the other hand, `generator-core::gen` is run three times. This is because `generator-core::gen` is added as a dependency four times, and three times with a distinct argument value.

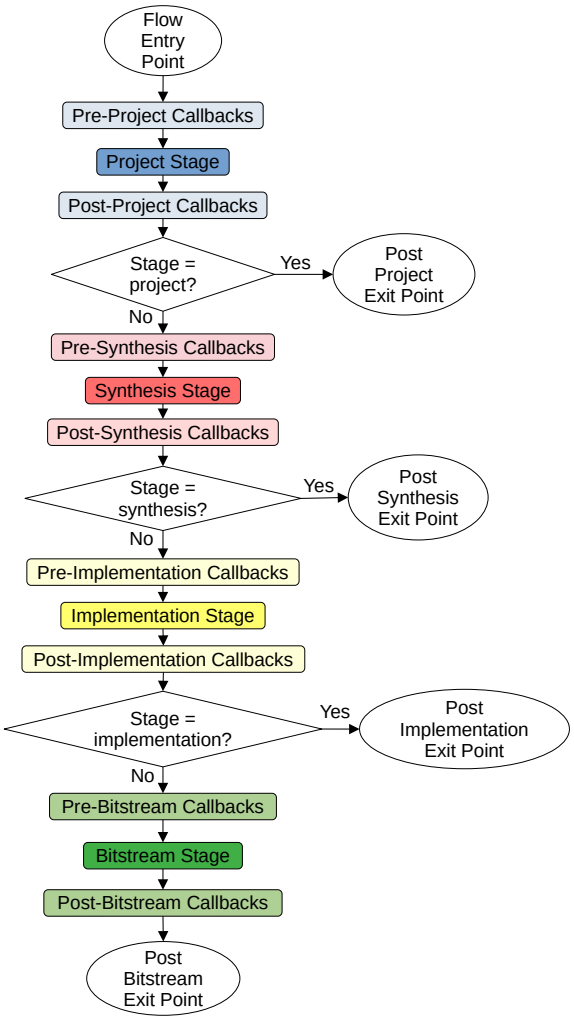
3.9 EDA tool flow and stages

The primary function of any hardware build system is to provide the ability to build a design. What the term "build" actually means usually depends on the EDA tool. For some, it is only synthesis; for others, it is synthesis and implementation, and yet for others it might be simulation or just code linting. Each EDA tool is characterized by a distinct flow consisting of different stages. To mimic this behavior, HBS supports the following stages (alphabetical order):

1. analysis - HDL files analysis,
2. bitstream - device bitstream generation,
3. elaboration - design elaboration,
4. implementation - design implementation,
5. project - project creation,
6. simulation - design simulation,
7. synthesis - design synthesis.

Not all stages make sense for all EDA tools. Which stages are present in the given tool flow depends on that tool implementation. Namely, on the implementation of the `hbs::<tool>::run` procedure. This is a tool private procedure. This procedure is called at the end of the `hbs::Run` procedure execution, which is a HBS public procedure.

The below figure shows the structure of the tool flow for the Vivado project mode (`vivado-prj`).



There are four stages: project, synthesis, implementation and bitstream. Each stage is wrapped by custom, user-defined callbacks. The number of callbacks is unlimited. Callbacks in any pre or post stage are executed in the order you add them. You can add a callback by calling a dedicated HBS API procedure. For example, to add a post synthesis callback you can call the `hbs::AddPostSynthCb` procedure. Callbacks can be added with custom argument values.

The post stage callbacks and pre stage callbacks for adjacent stages were added for two reasons.

1. To clearly communicate which stage the callback refers to. For example, configuring implementation settings based on the synthesis results can be done in a post-synthesis callback or pre-implementation callback. However, as the callback modifies the implementation settings, it is probably better to add it using the `hbs::AddPreImplCb`, than `hbs::AddPostSynthCb`.
2. To introduce, to some extent, a manageable order of callbacks execution. The pre and post callbacks of a given stage are executed in the order they are added. If some nested dependencies add callbacks for the same pre or post stage, then the order of callbacks execution depends on the order of `hbs::AddDep` calls. However, if the result of one of the callbacks depends on the result of the other one, then relying on a user to call the `hbs::AddDep` procedures in proper order is error prone. In such a case, the callback that must be executed as the first one can be added to the post-synthesis callbacks, and the second callback can be added to the pre-implementation callbacks. Such an approach is immune to the order of `hbs::AddDep` calls.

You can utilize stage callbacks in any desired way. However, the primary purpose of stage callbacks is to adjust the design build based on the results from a particular stage. For example, you might want to configure additional implementation settings based on the synthesis results. You might even terminate the tool flow in a given callback and report an error if certain conditions are not met.

3.10 EDA tool commands custom arguments

The HBS has a minimal common abstraction layer. You perform all the actions not covered by the abstraction layer by directly calling EDA tool commands. For example, generating extra timing or clock network reports. However, some of the actions are hidden under the HBS API. For example, adding or analyzing HDL files. EDA tool commands used to perform actions hidden under common API usually have some parameters that are not used by default. Nevertheless, sometimes there is a need to specify additional parameters. In such a case, there are two possible solutions.

1. The first option is to bypass the HBS API and directly call the underlying EDA tool command. The drawback of this approach is that the user must manually handle the current context. For example, when adding an HDL file, the user must manually specify the library or standard revision. Bypassing HBS API also bypasses the target context!
2. The second option is to set the underlying command arguments prefix or suffix. This can be achieved with the `hbs::SetArgsPrefix` and `hbs::SetArgsSuffix` procedures. The argument prefix is always appended after the command name, and the argument suffix is always appended after all command arguments.

The below snippet presents Ethernet Management Data Input/Output (MDIO) core definition.

```
namespace eval vhdl::ethernet {
  namespace eval mdio {
    proc src {} {
      hbs::SetLib "ethernet"
      hbs::AddFile mdio.vhd
    }
    proc tb {} {
      hbs::SetTool "nvc"
      hbs::AddPostElabCb hbs::SetArgsPrefix "--messages=compact"
      src

      hbs::SetLib ""
      hbs::AddFile tb/tb-mdio.vhd
      hbs::SetTop "tb_mdio"
      hbs::Run
    }
    hbs::Register
  }
}
```

The core has one testbench target utilizing the nvc simulator. Nvc report messages occupy multiple lines by default. However, this can be changed by specifying the `--messages=compact` argument when running the simulation. As running the simulation is the last stage of the nvc flow, the call to `hbs::SetArgsPrefix` must be wrapped by the call to the `hbs::AddPostElabCb` procedure.

The below snippet shows commands executed by the HBS to run the simulation. The `--messages=compact` argument was appended right after the `nvc` command.

```
[user@host vhdl-ethernet]$ hbs run vhdl::ethernet::mdio::tb
nvc --std=2019 -L. --work=ethernet -a vhdl/vhdl-ethernet/mdio.vhd
nvc --std=2019 -L. --work=work -a vhdl/vhdl-ethernet/tb/tb-mdio.vhd
nvc --std=2019 -L. -e tb_mdio
nvc --messages=compact --std=2019 -L. -r tb_mdio --wave
```

3.11 HBS API extra symbols

The HBS API consists not only of symbols related to the common EDA abstraction layer. For example, there are extra `hbs::Exec` and `hbs::CoreDir` procedures. The first one is a wrapper for the Tcl standard `exec` procedure. Before calling `exec`, the `hbs::Exec` changes the working directory to the directory where the currently evaluated core is defined. When `exec` returns, the `hbs::Exec` restores the working directory. The `hbs::CoreDir` procedure allows the user to get the path of the directory in which the currently evaluated core is defined.

HBS also provides users with the following extra variables:

1. `hbs::ThisCorePath` - the path of the core which target is currently being run,
2. `hbs::ThisTargetPath` - the path of the target which is currently being run,
3. `hbs::ThisTargetName` - the name of the target which is currently being run,
4. `hbs::TopCorePath` - the path of the top core beign run,
5. `hbs::TopTargetPath` - the path of the top target being run,
6. `hbs::TopTarget` - the name of the top target being run,
7. `hbs::TopTargetArgs` - the list with command line arguments passed to the top target.

To get the list of all HBS public symbols you can run `hbs doc` command in the shell.

3.12 Code generation

Code generation in the hardware design domain is omnipresent, as it significantly speeds up the implementation process. For example, hardware-software co-design system on chip projects usually have some tool automatically generating register files. Even in pure FPGA designs, it is common to generate descriptions at the register transfer level from some higher-level programming abstraction. That is why it is important for any hardware build system to provide as simple mechanism for code generation as possible.

Some existing hardware build systems do not allow the direct calling of an arbitrary external program in arbitrary places during the build process. Instead, you have to define so-called generators. Only then can you call the generator wihtin core definitions. However, such an approach has some drawbacks:

1. The generator call requires an extra layer of indirection. Generators are defined in different places than they are used, which decreases the readability of the description.
2. The generator call syntax does not resemble shell command call syntax. Generators are usually regular applications that can be executed in a shell. Calling a generator within the build system using syntax similar to shell seems natural.

In HBS, there is no formal concept of generator. Anything can be a generator, as generators are just regular Tcl procedures. This means that generators can be target procedures (tracked by dependency system) or core internal Tcl procedures (not tracked by the dependnecy system).

The below snippet presents an example of calling an external code generator tracked by the dependnecy system. In actual usage, the call to the shell `echo` command would be replaced with a call to the proper code generator program. Calls to the `hbs::AddFile}` are commented out because no EDA tool was set.

```
namespace eval core {
  proc top {} {
    hbs::AddDep generator::gen "foo"
    puts "Adding file top.vhd"
    # hbs::AddFile top.vhd
  }
  hbs::Register
}
namespace eval generator {
  proc gen {name} {
    exec echo "Generating $name.vhd" >@ stdout
    puts "Adding file $name.vhd"
    # hbs::AddFile "$name.vhd"
  }
  hbs::Register
}
```

The following snippet presents how to achieve the same result without tracking the generator as a dependency. This task is even more straightforward, as you can call an external generator program directly in the target procedure.

```
namespace eval core {
  proc top {} {
    exec echo "Generating foo.vhd" >@ stdout
    puts "Adding file foo.vhd"
    # hbs::AddFile "foo.vhd"

    puts "Adding file top.vhd"
    # hbs::AddFile top.vhd
  }
  hbs::Register
}
```

4 Command line interface commands

4.1 `doc` - viewing HBS API documentation

The `doc` command was added to ease viewing documentation for HBS Tcl symbols. The command is executed by the `hbs` file, so Python is required for the command to work. If no argument is provided for the `doc` command, then `hbs` prints a list of all HBS Tcl public symbols. To get more information on the particular symbol, simply provide is as an argument for the `doc` command. The below snippet presents an example of `doc` command output.

```
[user@host ~] hbs doc SetStd
# Sets standard revision for HDL files.
#
# To get the value of currently set standard revision simply
# read the value of hbs::Std variable.
#
# Standard revision for a given file must be set before adding a file.
# For example:
#   hbs::SetStd 2008
```

```
#   hbs::AddFile entity.vhd
proc SetStd {std}
```

4.2 `dump-cores` - dumping cores information

The `dump-cores` command allows dumping information about found cores into JSON format. The generated JSON data can be used for further processing. For example, the graph command utilizes data from JSON dump to generate the dependency graph. The command is executed by the `hbs.tcl` file, so Python is not required for the command to work. If you do not like the default behavior of the `hbs` Python wrapper, you can write your own. Simply utilize dumped JSON data as a stream from `hbs.tcl` to your wrapper.

4.3 `graph` - generating dependency graph

4.4 `help` - displaying help message for commands

The `help` command serves as a standard help message display command. If no argument is provided, then the help message regards the `hbs` general use. If argument is provided for the `help` command, then it must be a valid command name. In such a case, `hbs` prints help message for the provided command. The below snippets presents help message for the `dump-cores` command.

```
[user@host tmp] hbs help dump-cores
Dump info about cores found in .hbs files in JSON format.

  hbs dump-cores

The JSON is directed to stdout.
If you want to save it in a file simply redirect stdout.
```

4.5 `list-cores` - listing cores found in hbs files

The `list-cores` command allows listing all cores discovered by the HBS. The `list-cores` command is executed by the `hbs.tcl` file, so the command does not require Python to work. The below snippet presents an output for listing all cores in the VHDL APB library.

```
[user@ahost apb] hbs list-cores
vhdl::amba5::apb::bfm
vhdl::amba5::apb::cdc-bridge
vhdl::amba5::apb::checker
vhdl::amba5::apb::crossbar
vhdl::amba5::apb::mock-completer
vhdl::amba5::apb::pkg
vhdl::amba5::apb::serial-bridge
vhdl::amba5::apb::shared-bus
```

The below snippet presents an output for listing various bridge cores in the same APB library.

```
[user@ahost apb] hbs list-cores bridge
vhdl::amba5::apb::cdc-bridge
vhdl::amba5::apb::serial-bridge
```

Please note that you can provided arbitrary strings to the `list-cores` command. The core is listed if its core path contains at least one string provided in arguments. For example, the below snippet presents an output for listing all cores containg the `bri` or `bar` string in the same APB library.

```
[user@host apb] hbs list-cores bri bar
vhdl::amba5::apb::cdc-bridge
vhdl::amba5::apb::crossbar
vhdl::amba5::apb::serial-bridge
```

4.6 `list-targets` - listing targets for discovered cores

The `list-targets` command allows listing all targets discovered by the HBS. The command is analogous to the `list-cores` command but works on targets instead of cores. The `list-targets` command is executed by the `hbs.tcl` file, so the command does not require Python to work. The below snippet presents an output for listing `src` targets in the VHDL APB library.

```
[user@host apb] hbs list-targets src
vhdl::amba5::apb::bfm::src
vhdl::amba5::apb::cdc-bridge::src
vhdl::amba5::apb::checker::src
vhdl::amba5::apb::crossbar::src
vhdl::amba5::apb::mock-completer::src
vhdl::amba5::apb::pkg::src
vhdl::amba5::apb::serial-bridge::src
vhdl::amba5::apb::shared-bus::src
```

The name "src" is preferred name for a core target if the core has only one target containing all sources required for core utilization. However, this is not a formal requirement, so feel free to name your targets however you want.

4.7 `list-tb` - listing testbench targets

The `list-tb` command allows listing all testbench targets discovered by HBS. The `list-tb` command is analogous to the `list-targets` command, but it works solely on testbench targets instead of all targets. The command is executed by the `hbs` file and requires Python to work. The below snippet presents an output for listing testbench targets for bridges in the VHDL APB library.

```
[user@host apb] hbs list-tb bridge
vhdl::amba5::apb::cdc-bridge::tb-to-faster
vhdl::amba5::apb::cdc-bridge::tb-similar-slower
vhdl::amba5::apb::cdc-bridge::tb-similar-faster
vhdl::amba5::apb::cdc-bridge::tb-to-slower
vhdl::amba5::apb::serial-bridge::tb-write
vhdl::amba5::apb::serial-bridge::tb-read
```

If no arguments are provided for the `list-tb` command, then all testbench targets for all discovered cores are listed.

4.8 `run` - running targets

The `run` command allows running target procedures. Usually, targets are run to carry out the build process or simulation. However, the user is free to carry out any action in the target being run. You can, for example, use targets for software recompilation.

Running targets is described in Section 3.5, Section 3.6, and Section 3.7.

4.9 `test` - running testbench targets

The `test` command allows running all automatically discovered testbench targets. The `test` command is executed by the `hbs` file and requires Python to work. By default, testbench targets are run in

parallel. The default number of workers equals the number of threads on your CPU. If you provide extra arguments to the `test` command, only testbench targets which path contain at least one of the provided strings are run. The below snippet presents an output for running all testbenched of the bus functional model in the VHDL APB library.

```
[user@host ap] hbs test bfm
running 4 targets with 16 workers

vhdl::amba5::apb::bfm::tb-readb   passed  warnings: 1
vhdl::amba5::apb::bfm::tb-read    passed  warnings: 1
vhdl::amba5::apb::bfm::tb-write   passed  warnings: 1
vhdl::amba5::apb::bfm::tb-writeb  passed  warnings: 1

time:     0 h 0 min 0 s
targets:  4
passed:   4
failed:   0
errors:   0
warnings: 4
```

4.10 `version` - displaying HBS version

The `version` command displays version of installed HBS. This might be helpful if the same build procedure works on one machine, but does not work on another. Based on the versoin and changelog, you can quickly discover differences. The blow snippet shows an example output for the `version` command.

```
[user@host ~ 0] hbs version
1.0
```

4.11 `whereis` - locating cores definition

The `whereis` command allows easily locating .hbs files in which given cores are defined The `whereis` command is executed by the `hbs` file, so the command requires Python to work. The below snippet presents an example of locating core definition.

```
[user@host vsc8211-tester] hbs whereis serial-bridge
vhdl::amba5::apb::serial-bridge  /tmp/vsc8211-tester/gw/apb/apb.hbs
```

You can locate multiple cores in a single call by providing multiple arguments to the command. The below snippet presents an example:

```
[user@host vsc8211-tester] hbs whereis bridge mdio
vhdl::amba5::apb::serial-bridge  /tmp/vsc8211-tester/gw/apb/apb.hbs
vhdl::ethernet::mdio             /tmp/vsc8211-tester/gw/vhdl-ethernet/ethernet.hbs
```

5 Tcl tips

5.1 Support for arrow keys in `tclsh`

If you every tried to use `tclsh` to REPL (read-eval-print-loop), you probably realized that `tclsh` by default does not support arrow keys. You can't fix a typo in a line without deleting some line content. There is also no command history support. However, this can be improved. The first solution is install

the `rlwrap` programm and call `rlwrap tclsh` instead of `tclsh`. To make it shorter to type, you can define an alias for your shell of choice, for example, for bash alias `tclsh='rlwrap tclsh'`. The second option is to install the Tcl `tclreadline` package. This package often comes as OS distro package. For example, on Debian/Ubuntu, you can install it with `apt install tcl-tclreadline`. Once installed, create `.tclshrc` file in your home directory and add the following content:

```
package require tclreadline
tclreadline::Loop
```

Not only you will get support for arrow keys and command history, but also improved prompt.

5.2 Passing variadic arguments to proc

To pass variadic arguments to a proc, the last proc parameter must be called `args`. You can then easily iterate over the arguments using the `foreach` loop. The below example is taken directly from the hbs Tcl source code.

```
proc AddIgnoreRegex {args} {
  foreach reg $args {
    hbs::dbg "adding ignore regex $reg"
    lappend hbs::IgnoreRegexes $reg
  }
}
```