ANALOG DEVICES

ADV7181C

Integrated Multi-Format SDTV/HDTV Video Decoder and RGB Graphics Digitizer

DATASHEET MANUAL

September 2010

1 Introduction to ADV7181C Hardware Manual

1.1 Description of the Hardware Manual

This manual provides a detailed description of the functionality and features supported by the ADV7181C.

1.2 Disclaimer

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1.3 Number Notations

Notation Description

Notation	Description
Bit N	Bits are numbered in little endian format, that is, the least significant bit of a number is referred to as bit 0
V[X:Y]	Bit field representation covering bit X to Y of a value or a field V
0xNN	Hexadecimal (base-16) numbers are preceded by the prefix 0x
0bNN	Binary (base-2) numbers are preceded by the prefix 0b
NN	Decimal (base-10) are represented using no additional prefixes or suffixes

1.4 Register Access Conventions

Mode	Description
R/W	Memory location has read and write access.
R	Memory location is read access only. A read always returns 0 unless specified otherwise.
W	Memory location is write access only.

1.5 Acronyms and Abbreviations

Acronym/Abbreviation	Description
ADC	Analog to Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
CP	Component Processor
CSC	Color Space Converter/Conversion
Csync/CS	Composite Synchronization
DID	Data Identification Word
DCM	Decimation
DDR	Double Data Rate
DE	Data Enable
DLL	Delay Locked Loop
DPP	Data Preprocessor
DVI	Digital Visual Interface
DUT	Device Under Test (designate the ADV7181C unless stated otherwise)
ED	Enhanced Definition
EAV	End of Active Video
EQ	Equalizer
EMC	Electromagnetic Compatibility
HD	High Definition
HDCP	High Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HDTV	High Definition Television
Hsync	Horizontal Synchronization
IC	Integrated Circuit
I^2C	Inter Integrated Circuit
LLC	Line Locked Clock
LSB	Least Significant Bit
Mbps	Megabit per Second
MPEG	Moving Picture Expert Group
ms	Millisecond
MSB	Most Significant Bit
OTP	One Time Programmable
Rx	Receiver
SA	Slave Address
SAV	Start of Active Video
SD	Standard Definition
SMPTE	Society of Motion Picture and Television Engineers
SNR	Signal to Noise Ratio
SDR	Single Data Rate
SOG	Sync on Green
SOY	Sync on Y
SSPD	Synchronization Source Polarity Detector
STDI	Standard Identification

Acronym/Abbreviation	Description
TMDS	Transition Minimized Differential Signaling
Tx	Transmitter
VBI	Video Blanking Interval
VDP	VBI Data Processor
Vsync	Vertical Synchronization
XTAL	Crystal Oscillator

2 Introduction

The ADV7181C is a high-quality single chip multi-format video decoder and graphics digitizer. This multi-format decoder supports the conversion of PAL, NTSC and SECAM standards in the form of composite or S-Video into a digital ITU-R BT.656 format. The ADV7181C also supports the decoding of a component RGB/YPbPr video signal into a digital YCrCb or RGB pixel output stream. The support for component video includes standards such as 525i, 625i, 525P, 625P, 720P, 1080i, and many other HD and SMPTE standards.

Graphic digitization is also supported by the ADV7181C. It is capable of digitizing RGB graphics signals from VGA to XGA rates, and converting them into a digital RGB or YCrCb pixel output stream. SCART and overlay functionality are enabled by the ADV7181C's ability to process simultaneously CVBS and Standard Definition RGB signals. The mixing of these signals is controlled via the Fast Blank pin.

The ADV7181C contains two main processing sections. The first section is the Standard Definition Processor (SDP), which processes all PAL, NTSC and SECAM signal types. The second section is the Component Processor (CP), which processes YPbPr and RGB component formats including RGB graphics.

2.1 Analogue Front End

The ADV7181C analogue front end comprises four 10-bit 110 MHz Noise Shaped Video® ADCs that digitize the analogue video signal before applying it to the SDP or CP. The analogue front end employs differential channels to each ADC to ensure high performance in a mixed signal application. The front end includes a 6-channel input mux that enables multiple video signals to be applied to the ADV7181C, and optional internal anti aliasing filters with approximately 6 MHz bandwidth.

Current and voltage clamps are positioned in front of each ADC to ensure the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in either the CP or SDP. The ADCs are configured to run in 4X oversampling mode when decoding composite and S-Video inputs; 2X oversampling is performed for component 525i, 625i, 525P and 625P sources. All other video standards are 1X oversampled. In oversampling the video signals, a reduction in the cost and complexity of external anti aliasing filters can be obtained with the benefit of increased signal to noise ratio (SNR).

2.2 Standard Definition Processor

The SDP section is capable of decoding a large selection of baseband video signals in composite and S-Video formats. The video standards supported by the SDP include PAL B/D/I/G/H, PAL60, PAL M, PAL N, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7181C can automatically detect the video standard and process it accordingly.

The SDP has a 5-line super-adaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required.

Video user controls like brightness, contrast, saturation and hue are also available within the SDP section of the ADV7181C.

The ADV7181C implements a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7181C to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, camcorders, etc. The SDP also contains a Chroma Transient Improvement (CTI) processor. This processor increases the edge rate on chroma transitions, resulting in a sharper video image.

The SDP section also has a Macrovision® 7.1 detection circuit that allows it to detect Type I, II and III protection levels and report this to the user. The decoder is fully robust to all Macrovision signal inputs.

2.3 Component Processor

The CP section is capable of decoding/digitizing a wide selection of component video formats in any color space. Component video standards supported by the CP include 525i, 625i, 525P, 625P, 720p, 1080i, 1250i, VGA up to XGA @ 70Hz and so on.

A fully programmable color space conversion (CSC) matrix is placed between the analogue front end and the CP section. This enables YPbPr to DDR-RGB and RGB to YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

The CP section of the ADV7181C also contains an AGC block. In cases where no embedded sync is preset, the video gain can be set manually. The AGC section is preceded by a digital clamp circuit that ensures the video signal is clamped to the correct blanking level.

The output section of the CP is highly flexible. It can be configured in Single Data Rate mode (SDR) with one data packet per clock cycle. In SDR mode, a 16-/20-bit 4:2:2 is possible. In these modes, HS, VS and FIELD/DE (where applicable) timing reference signals are provided.

The CP section contains circuitry to enable the detection of Macrovision encoded YPbPr signals for 525i, 625i, 525P and 625P. It is also designed to be fully robust to these types of signals.

VBI extraction of CGMS data is also performed by the CP section of the ADV7181C for interlaced, progressive and high definition scanning rates. The data extracted can be read back over the I^2C® interface.

2.4 Detailed Functionality of ADV7181C

2.4.1 Analogue Front End

The analogue front-end functionality includes:

- Four 110 MHz noise shaped video 10-bit ADCs
- Six analogue input channel mux enables multi-source connection without the requirement of an external mux
- Four current and voltage clamp control loops ensure any DC offsets are removed from the video signal
- Four internal anti-alias filters to remove out-of-band noise on standard definition input video signals

2.4.2 User Programmable Video Output Formats

The user programmable video output formats include:

- Composite and S-Video pixel data output modes:
    - 8-/10-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS and FIELD
    - 16-/20-bit YCrCb with embedded time codes and/or HS, VS and FIELD
- Component pixel data output modes:
    - SDR 8-/10-bit 4:2:2 YCrCb for 525i, 625i
    - SDR 16-/20-bit 4:2:2 YCrCb for all standards
    - DDR 8-/10-bit 4:2:2 YCrCb
    - DDR 12-bit 4:4:4 RGB

2.4.3 Composite and S-Video Processing

Composite and S-Video processing functionality includes:

- Support for NTSC (J, M, 4.43), PAL (B, D, I, G, H, M, N, 60) and SECAM B/D/G/K/L standards in the form of CVBS and S-Video
- Super adaptive 2D 5-line comb filters for NTSC and PAL giving superior chrominance and luminance separation for composite video
- Full automatic detection and autoswitching of all worldwide standards (PAL/NTSC/SECAM)
- Automatic gain control with white peak mode ensuring the video is always processed without loss of the video processing range
- ADLLT
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs, tuners, etc.
- CTI
- Luminance Digital Noise Reduction (DNR)

- Color controls including hue, brightness, saturation, contrast, and Cr and Cb offset controls
- Certified Macrovision copy protection detection on composite and S-Video for all worldwide formats (PAL/NTSC/SECAM)
- 4X oversampling (54 MHz) for CVBS, S-video and YUV modes
- Line Locked Clock (LLC) output
- Letterbox detection supported
- Free run output mode providing stable timing when no video input is present
- Vertical Blanking Interval Data processor
    - Teletext
    - Video Programming System (VPS)
    - Vertical Interval Time Codes (VITC)
    - Closed Caption (CC) and Extended Data services (XDS)
    - Wide Screen Signaling (WSS)
    - Copy Generation management system (CGMS)
    - Gemstar 1x/2x electronic program guide compatible
- Single 28.63636 MHz crystal required
- Subcarrier Frequency Lock (SFL) output for downstream video encoder
- Differential gain typically = 0.5%
- Differential phase typically = 0.5°

2.4.4 Component Video Processing

Component video processing functionality includes:

- 525i, 625i, 525P, 625P, 720P, 1080i formats and many other HDTV formats supported
- Automatic adjustments including gain (contrast) and offset (brightness); manual adjustment controls are also supported
- Support for analogue component YPbPr/RGB video formats with embedded sync or with separate HS, VS or CS
- Standard Identification (STDI) enabling system level component format detection
- Synchronization source polarity detector (SSPD) determining the source and polarity of the synchronization signals that accompany the input video
- Color space conversion matrix supports YCrCb-to- DDR RGB and RGB-to-YCrCb
- Certified Macrovision copy protection detection on component formats (525i, 625i, 525P and 625P)
- Free Run output mode providing stable timing when no video input is present
- Arbitrary pixel sampling support for non-standard video sources

2.4.5 RGB Graphics Processing

RGB graphics processing functionality includes:

- 110 MSPS conversion rate supports RGB input resolutions up to 1024 x 768 @ 70Hz (XGA)
- Automatic or manual clamp and gain controls for graphics modes
- Contrast and brightness controls

- 32 phase DLL allowing optimum pixel clock sampling
- Automatic detection of sync source and polarity by SSPD block
- Standard identification enabled by STDI block
- RGB can be color space converted to YCrCb and decimated to a 4:2:2 format for video-centric backend IC interfacing
- Data enable (DE) output signal supplied for direct connection to HDMI/DVI Tx
- Arbitrary pixel sampling support for non-standard video sources

2.4.6 Additional Features

- HS, VS and FIELD outputs with programmable position, polarity and width
- Low power consumption: 1.8V digital core, 3.3V analogue and digital I/O, low power power-down mode and green PC mode
- 64-pin 10mm x 10mm lead (Pb)-free LQFP package.
- Temperature grade: -40°C to +85°C

2.5 Applications

- Automotive entertainment
- LCD/DLP projectors
- HDTVs
- HDTV STBs with PVR
- DVD recorders with progressive scan input support
- AVR – Audio Video Receiver

2.6 Functional Block Diagram

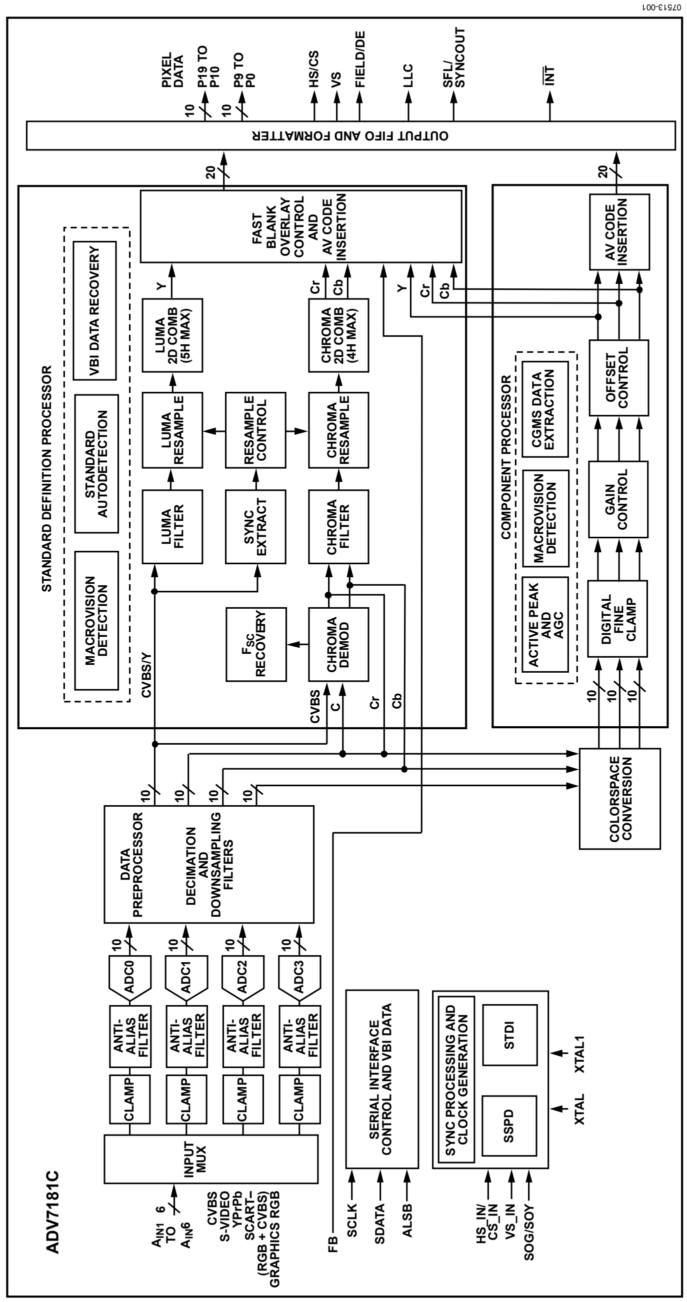


Figure 1: Functional Block Diagram

2.7 Pin Description

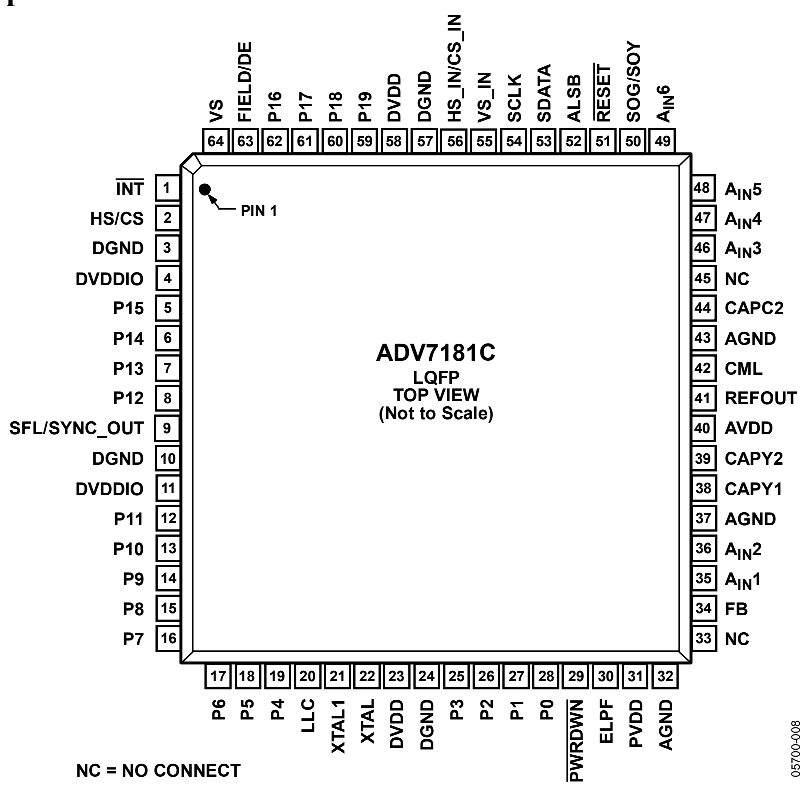


Figure 2: Pin Configuration

Table 1: Pin Function Description

Pin No.	Mnemonic	Type	Function
3, 10, 24, 57	DGND	G	Digital Ground.
32, 37, 43	AGND	G	Analog Ground.
4, 11	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
23, 58	DVDD	P	Digital Core Supply Voltage (1.8 V).
40	AVDD	P	Analog Supply Voltage (3.3 V).
31	PVDD	P	PLL Supply Voltage (1.8 V).
34	FB	I	Fast Switch Overlay Input. This pin switches between CVBS and RGB analog signals.
35, 36, 46, 47, 48, 49	AIN1 to AIN6	I	Analog Video Input Channels.
28, 27, 26, 25, 19, 18, 17, 16, 15, 14, 13, 12, 8, 7, 6, 5, 62, 61, 60, 59	P0-P19	O	Video Pixel Output Port.
1	INT	O	Interrupt. This pin can be active low or active high. When SDP/CP status bits change, this pin triggers. The set of events that triggers an interrupt is under user control.
2	HS/CS	O	HS is a Horizontal Synchronization Output Signal (SDP and CP modes). CS is a Digital Composite Synchronization Signal (and can be selected while in CP mode).
64	VS	O	Vertical Synchronization Output Signal (SDP and CP modes).
63	FIELD/DE	O	Field Synchronization Output Signal (all interlaced video modes). This pin also can be enabled as a Data Enable signal (DE) in CP mode to allow direct connection to a HDMI/DVI Tx IC.

Pin No.	Mnemonic	Type	Function
53	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
54	SCLK	I	I^2C Port Serial Clock Input (max clock rate of 400 kHz).
52	ALSB	I	This pin selects the I^2C address for the ADV7181C control and VBI readback ports. ALSB set to Logic 0 sets the address for a write to control port of 0x40 and the readback address for the VBI port of 0x21. ALSB set to a logic high sets the address for a write to control port of 0x42 and the readback address for the VBI port of 0x23.
51	RESET	I	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7181C circuitry.
20	LLC	O	LLC is a line-locked output clock for the pixel data.
22	XTAL	I	Input pin for 28.63636 MHz crystal, or can be overdriven by an external 3.3 V 28.63636 MHz clock oscillator source to clock the ADV7181C.
21	XTAL1	O	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V 28.63636 MHz clock oscillator source is used to clock the ADV7181C. In crystal mode, the crystal must be a fundamental crystal.
30	ELPF	O	The recommend external loop filter must be connected to this ELPF pin.
9	SFL/SYNC_OUT	O	Subcarrier Frequency Lock (SFL). This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. SYNC_OUT is the sliced sync output signal available only in CP mode.
41	REFOUT	O	Internal Voltage Reference Output.
42	CML	O	Common-Mode Level Pin (CML) for the internal ADCs.
38, 39	CAPY1, CAPY2	I	ADC Capacitor Network.
44	CAPC2	I	ADC Capacitor Network.
56	HS_IN/CS_IN	I	Can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
55	VS_IN	I	VS Input Signal. Used in CP mode for 5-wire timing mode.
50	SOG/SOY	I	Sync on Green/Luma Input. Used in embedded sync mode.
29	PWRDWN	I	A logic low on this pin places the ADV7181C in a power-down mode.
33, 45	NC		No Connect Pins. These pins are not connected internally.

2.8 Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Parameter	Rating
A_{VDD} to AGND	4 V
D_{VDD} to DGND	2.2 V
P_{VDD} to AGND	2.2 V
D_{VDDIO} to DGND	4 V
D_{VDDIO} to A_{VDD}	−0.3 V to +0.3V
P_{VDD} to D_{VDD}	−0.3 V to +0.3 V
D_{VDDIO} – P_{VDD}	−0.3 V to +2 V
D_{VDDIO} – D_{VDD}	−0.3 V to +2 V
A_{VDD} – P_{VDD}	−0.3 V to +2 V
A_{VDD} – D_{VDD}	−0.3 V to +2 V
Digital Inputs Voltage to DGND	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage to DGND	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to AGND	AGND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Table 3: Ordering Guide

Model	Temperature Range	Package Description
ADV7181CBSTZ[1]	-40 to +85degC	LQFP
ADV7181CBSTZ-REEL[1]	-40 to +85degC	LQFP
ADV7181CWBSTZ[1]	-40 to +85degC	LQFP (Automotive)
ADV7181CWBSTZ-REEL[1]	-40 to +85degC	LQFP (Automotive)

Notes:

- The ADV7181C is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and is able to withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with SnPb solder pastes at conventional reflow temperatures of 220°C to 235°C.

- Stresses above those listed in Table 2 can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

[1] Z=RoHS compliant part

2.9 ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

3 Analogue Front End

3.1 Analogue Input Muxing

The ADV7181C has an integrated analogue muxing section, which allows more than one source of video signal to be connected to the decoder. Figure 3 outlines the overall structure of the input muxing provided in the ADV7181C.

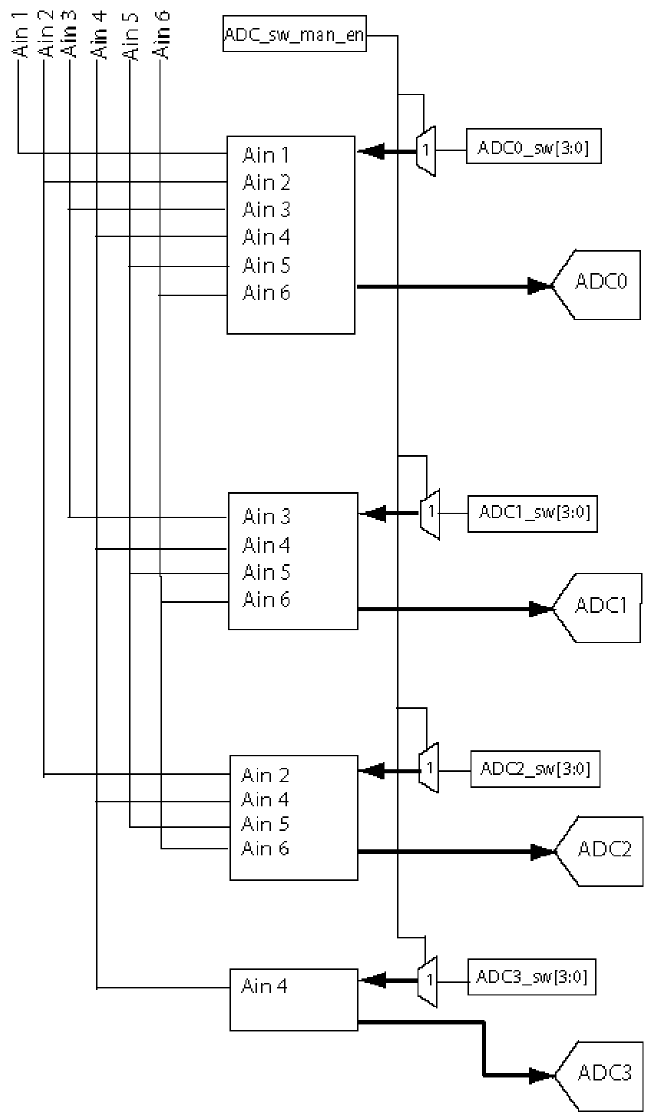


Figure 3: ADV7181C Internal Pin Connections

It is recommended for the ADV7181C to use the ADC mapping in Table 4.

Table 4: Recommended ADC Mapping

Mode	Required ADC Mapping	Ain Channel	Core	Configuration to Format Follow on Blocks in Correct Format
CVBS	ADC0	CVBS = Ain 1	SD	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
YC/YC auto	Y = ADC0 C = ADC1	Y= Ain 2 C = Ain3	SD	INSEL[3:0] = 0000 SDM_SEL[1:0] = 11 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Component YUV	Y = ADC0 U = ADC2 V = ADC1	Y = Ain 6 U = Ain 4 V = Ain 5	SD	INSEL[3:0] = 1001 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Component YUV	Y = ADC0 U = ADC2 V = ADC1	Y = Ain 6 U = Ain 4 V = Ain 5	CP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 1010
SCART RGB	CBVS = ADC0 G = ADC1 B = ADC3 R = ADC2	CVBS = Ain 2 G = Ain 6 B = Ain 4 R = Ain 5	SD	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Graphics RGB mode	G = ADC0 B = ADC2 R = ADC1	G = Ain 6 B = Ain 4 R = Ain 5	CP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0001 VID_STD[3:0] = 1100

The analog input muxes of the ADV7181C must be controlled directly. This is referred to as **manual input muxing**. The manual muxing is activated by setting the ADC_SWITCH_MAN bit. It only affects the analog switches in front of the ADCs. INSEL, SDM_SEL PRIM_MODE and VID_STD still have to be set so that the follow on blocks process the video data in the correct format.

Not every input pin can be routed to any ADC. There are restrictions in the channel routing imposed by the analog signal routing inside the IC. Refer to Table 5 for an overview of the routing capabilities inside the chip. The four mux sections can be controlled by the reserved control signal buses ADC0/1/2/3_SW[3:0].

Table 5 explains the ADC Mapping configuration.

ADC_SWITCH_MAN, Manual input muxing enable, IO Map, *Address C4, [7]*
ADC0_SW[3:0], ADC0 mux configuration, IO Map, *Address C3, [3:0]*
ADC1_SW[3:0], ADC1 mux configuration, IO Map, *Address C3, [7:4]*
ADC2_SW[3:0], ADC2 mux configuration, IO Map, *Address C4, [3:0]*

ADC3_SW[3:0], ADC3 mux configuration, IO Map, *Address F3 [7:4]*

Table 5: Manual MUX Settings for All ADCs

ADC_SWITCH_MAN to 1							
ADC0_sw_sel [3:0]	**ADC0 Connected to**	**ADC1_ sw_sel[3:0]**	**ADC1 Connected to**	**ADC2_ sw_sel [3:0]**	**ADC2 Connected to**	**ADC3_ sw_sel [3:0]**	**ADC3 Connected to**
0001	Ain1	0001	No connection	0001	No connection	0001	No connection
0010	Ain2	0010	No connection	0010	Ain2	0010	No connection
0100	Ain4	0100	Ain4	0100	Ain4	0100	Ain4
0101	Ain5	0101	Ain5	0101	Ain5	0101	No connection
0110	Ain6	0110	Ain6	0110	Ain6	0110	No connection
1100	Ain3	1100	Ain3	1100	No connection	1100	No connection

Note: It is strongly recommended to connect any unused analogue input pins to AGND.

3.1.1 Alternative Applications SD

A maximum of six CVBS inputs can be connected and decoded by the ADV7181C. As can be seen in Figure 3, this means that the sources will have to be connected to adjacent pins on the IC. This calls for a careful design of the PCB layout, for example, ground shielding between all signals that are routed through tracks that are physically close.

INSEL[3:0] Input Selection, *Address 0x00, [3:0]*

The INSEL bits allow the user to select an input format, i.e. configure the SDP core to process CVBS (Comp), S-Video (Y/C) or component (YPbPr) format.

INSEL[3:0] Low Bandwidth Input Selection

INSEL[3:0] is set to 1001 for the SD component.

SOG_SEL, SOG/SOY Connection Control, *Address C4, [6]*

Table 6: SOG/SOY Manual Mux Selection

SETADC_sw_man_en to 1	
SOG_SEL	Analogue Sync Stripper Connected to
0	SOG/SOY
1	Reserved

3.2 Bias Current Control

3.2.1 Bias Current Setting

IBIAS_SET[4:0] Bias Current Setting, *Address 0x3B, [7:3]*

This parameter sets the raw bias current value. The IBIAS_SET[4:0] value multiplies the fundamental bias value of 37.5uA to generate the overall bias current for the entire chip (refer to Equation 1).

$$I_{bias} = 37.5uA \bullet IBIAS\_SET[4:0]$$

Equation 1: Bias Current Calculation

Function

IBIAS_SET[4:0]	Description
10000	600 uA bias current

3.2.2 Xtal Clock Input Pin Functionality

XTAL_TTL_SEL, *Address 0x13 [2]*

The Xtal pad is normally part of the crystal oscillator circuit, powered from a 1.8V supply. For optimal clock generation, the slice level of the input buffer of this circuit is at approximately half the supply voltage. This makes it incompatible with TLL level signals.

If XTAL_TTL_SEL is set to 1, a different input buffer can be selected, which slices at TTL compatible levels. This inhibits operation of the crystal oscillator and, therefore, can only be used when a clock signal is applied.

Function

XTAL_TTL_SEL	Description
0	Crystal circuit operation
1	TTL level clock supplied

3.2.3 EN28XTAL Enable 28.63636 MHz Crystal Operation

The ADV7181C operates on only one base crystal frequency. This bit must be set for correct operation.

EN28XTAL Enable 28.63636 MHz Crystal Operation, *Address 0x1D, [6]*

Function

EN28XTAL	Description
0	Reserved
1	Xtal frequency is 28.63636 (8 x F_{SC} for NTSC)

3.3 Anti Alias Filters

The ADV7181C has optional anti aliasing filters on each of the four input channels. The filters are designed for SD video with approximately 6 MHz bandwidth and are most effective when 54 MHz ADC sampling is selected.

A plot of the filter response is shown in Figure 4. The filters can be individually enabled via I^2C under the control of AA_FILT_EN[3:0].

AA_FILT_EN[0], *Address 0xF3, [0]*
Function

AA_FILT_EN[0]	Description
0	Disables anti aliasing filter on channel 0
1	Enables anti aliasing filter on channel 0

AA_FILT_EN[1], *Address 0xF3, [1]*
Function

AA_FILT_EN[1]	Description
0	Disables anti aliasing filter on channel 1
1	Enables anti aliasing filter on channel 1

AA_FILT_EN[2], *Address 0xF3, [2]*
Function

AA_FILT_EN[2]	Description
0	Disables anti aliasing filter on channel 2
1	Enables anti aliasing filter on channel 2

AA_FILT_EN[3], *Address 0xF3, [3]*
Function

AA_FILT_EN[3]	Description
0	Disables anti aliasing filter on channel 3
1	Enables anti aliasing filter on channel 3

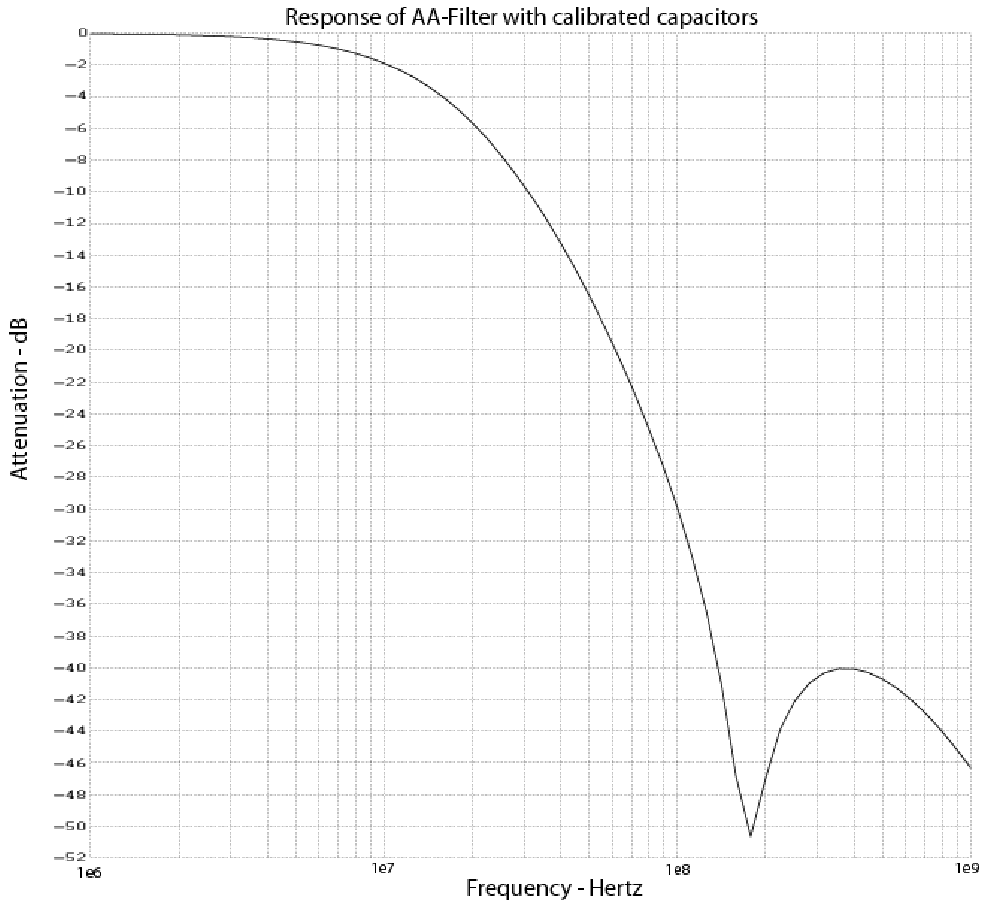


Figure 4: Response of Anti Aliasing Filter

3.4 SCART and Fast Blanking

The ADV7181C can support simultaneous processing of CVBS and RGB Standard Definition signals to enable SCART compatibility and overlay functionality.

This is available when PRIM_MODE[3:0] is set to 0000 to select Standard Definition Modulated. Once this is selected, timing extraction is always performed by the SDP on the CVBS signal.

Four basic modes are supported as follows:

1. **Static Switch Mode**.
   For static switch mode, the FB pin is not used. The timing is extracted from the CVBS signal, and either the CVBS content or RGB content can be output under the control of CVBS_RGB_SEL. This mode allows the selection of a full-screen picture from either source. Overlay is not possible in static switch mode.

2. **Fixed Alpha Blending**.
   For fixed alpha blending mode, the FB pin is not used. The timing is extracted from the CVBS signal, and an alpha blended combination of the video from the CVBS and RGB

sources is output. This alpha blending is applied to the full screen. The alpha blend factor is selected with the I^2C signal MAN_ALPHA[6:0]**.** Overlay is not possible in fixed alpha blending mode.

3. **Dynamic Switching (Fast Mux)**.
   In dynamic switching mode, the source selection is under the control of the Fast Blank (FB) pin. This enables dynamic multiplexing between the CVBS and RGB sources. With default settings, when logic HI is applied to the FB pin, the RGB source is selected; and when logic LO is applied to the FB pin, the CVBS source is selected. This mode is suitable for the overlay of subtitles, Teletext or other material. Typically, the CVBS source carries the main picture and the RGB source has the overlay data.

4. **Dynamic Switching with Edge-Enhancement**.
   This provides the same functionality as the dynamic switching mode but with ADI proprietary 'edge-enhancement' algorithms that improve the visual appearance of transitions for signals from a wide variety of sources.

3.4.1 System Diagram

A block diagram of the ADV7181C fast blanking configuration is shown in Figure 5.

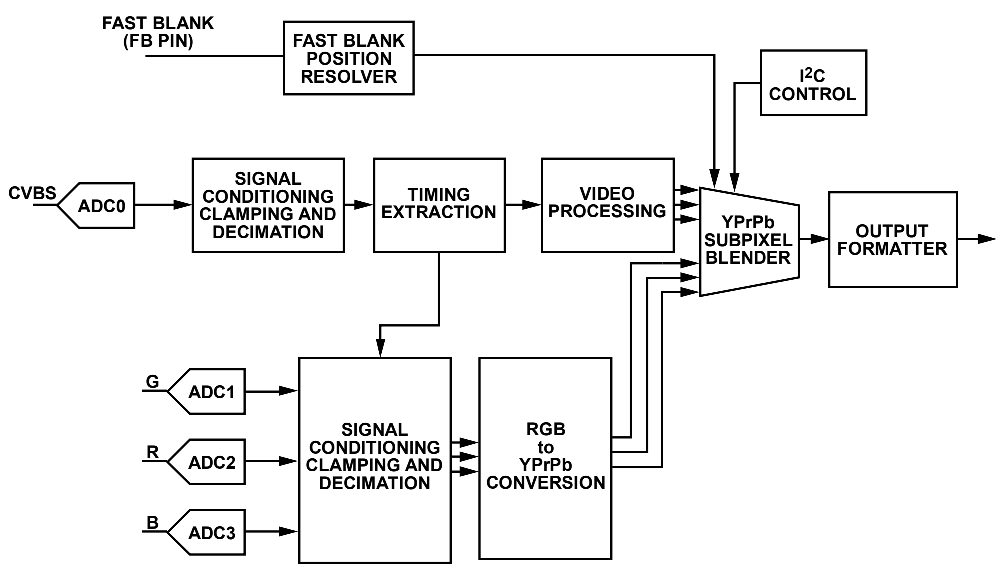


Figure 5: ADV7181C Fast Blanking Configuration

The CVBS signal is processed by the SDP and converted to YPbPr. The RGB signals are processed by sections of the CP and are also converted to YPbPr. Both sets of YPbPr signals are input to the Sub-Pixel Blender, which can be configured to operate in any of the four modes outlined in Section 3.4.

The Fast Blank Position Resolver determines the time position of the FB to a very high accuracy (< 1ns) and this position information is then used by the Sub-Pixel Blender in Dynamic Switching modes. This enables the ADV7181C to implement high performance multiplexing between the

CVBS and RGB sources, even when the RGB data source is completely asynchronous to the sampling crystal reference.

An anti aliasing filter is required on all four data channels (R, G, B, and CVBS). The order of this filter is reduced as all of the signals are sampled at 54 MHz.

The switched or blended data is output from the ADV7181C in the standard formats that exist for the SDP.

3.4.2 Top Level Control

FB_MODE[1:0] SCART/Fast Blanking Mode Selection, *Address 0xED, [1:0]*

FB_MODE controls which of the modes (described in the *SCART and Fast Blanking* section) is selected.

Function

FB_MODE[1:0]	Description
00 ⊂	Static Switch mode
01	Fixed Alpha Blending
10	Dynamic Switching (Fast Mux)
11	Dynamic Switching with Edge Enhancement

CVBS_RGB_SEL Static Mux Selection Control, *Address 0xED, [2]*

CVBS_RGB_SEL controls whether the video from the CVBS or the RGB source is selected for output from the ADV7181C.

Function

CVBS_RGB_SEL	Description
0 ⊂	CVBS source
1	RGB source

MAN_ALPHA_VAL[6:0] Alpha Blend Coefficient, *Address 0xEE, [6:0]*

When FB_MODE[1:0] = 01_b and Fixed Alpha Blending is selected, MAN_ALPHA_VAL[6:0] determines the proportion in which the video from the CVBS source and the RGB source are blended.

$$Video_{out} = Video_{CVBS} \times \left(1 - \frac{MAN\_ALPHA\_VAL[6:0]}{64}\right) + Video_{RGB} \times \frac{MAN\_ALPHA\_VAL[6:0]}{64}$$

Equation 2: Fixed Alpha Blending

The maximum valid value for MAN_ALPHA_VAL[6:0] is 1000000_b such that the alpha blender coefficients remain between 0 and 1.

Function

MAN_ALPHA_VAL[6:0]	Description
0000000 ⊂	Alpha Blend Coefficient (x 1/64)

FB_EDGE_SHAPE[2:0]

To improve the picture transition for high speed fast blank switching, an 'edge shape mode' has been designed. Depending on the format of the RGB inputs, it may be advantageous to apply this scheme to different degrees. These are selected via FB_EDGE_SHAPE[2:0]. Users are advised to try each of the settings and select the setting that is most visually pleasing in their system.

Function

FB_EDGE_SHAPE[2:0]	Description
000	No Edge Shaping
001	Level 1 Edge Shaping
010 ⊂	Level 2 Edge Shaping
011	Level 3 Edge Shaping
100	Level 4 Edge Shaping

3.4.3 Contrast Reduction

For overlay applications, text can be more readable if the contrast of the video directly behind the text is reduced. To enable the definition of a window of reduced contrast behind inserted text, the signal applied to the FB pin can be interpreted as a tri-level signal, as shown in Figure 6.

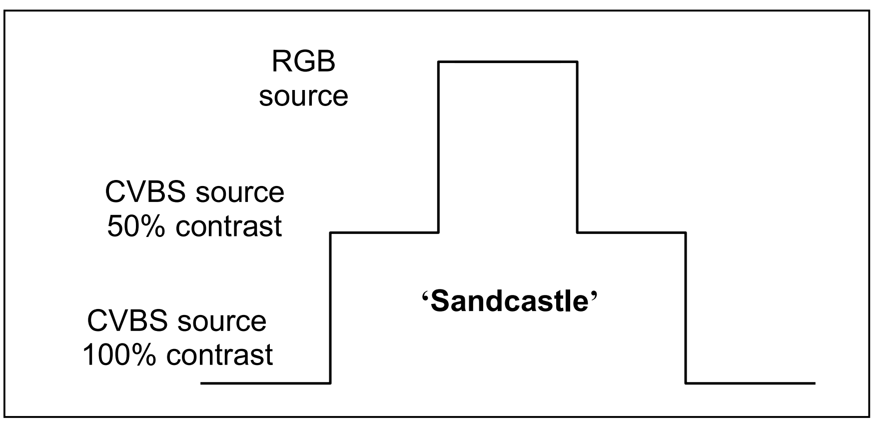


Figure 6: Fast Blank Signal with Contrast Reduction Enabled

CNTR_ENABLE Contrast Reduction Enable, *Address 0xEF, [3]*

This register enables the Contrast Reduction feature and changes the meaning of the signal applied to the FB pin.

Function

CNTR_ENABLE	Description
0 ⊂	Contrast reduction disabled: FB interpreted as bi-level signal
1	Contrast reduction enabled: FB interpreted as tri-level signal

CNTR_MODE[1:0], *Address 0xF1, [3,2]*

The contrast level in the selected contrast reduction box is selected using CNTR_MODE[1:0].

Function

CNTR_MODE[1:0]	Description
00 ⊂	25%
01	50%
10	75%
11	100%

FB_LEVEL[1:0], CNTR_LEVEL[1:0]

The internal fast-blank and contrast-reduction signals are resolved from the tri-level FB signal using two comparators, as shown in Figure 7. To facilitate compliance with different input level standards, the reference level to these comparators is programmable under the control of FB_LEVEL[1:0] and CNTR_LEVEL[1:0]. The resulting thresholds are given in Table 7.

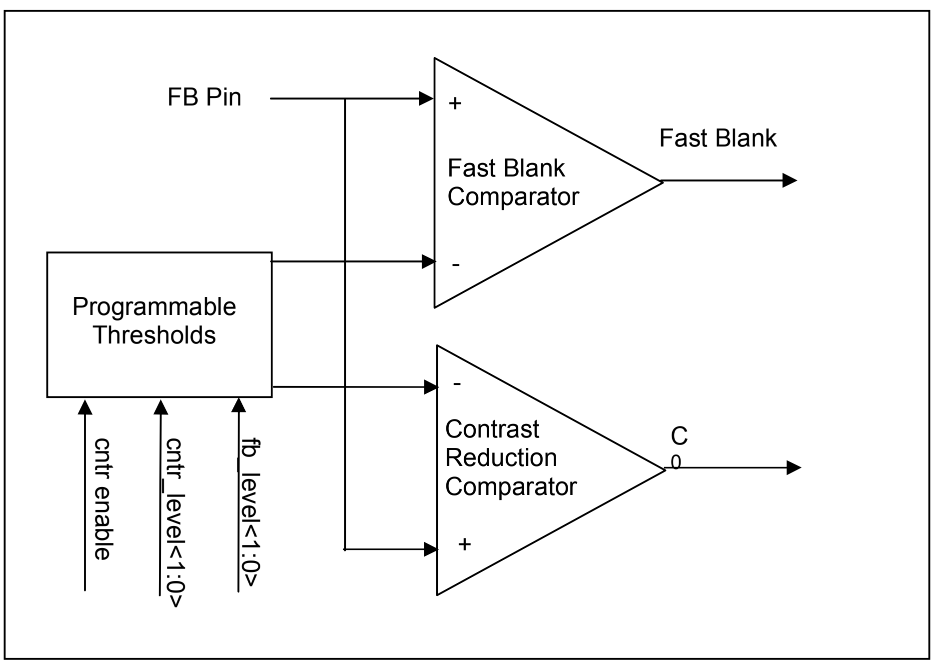


Figure 7: Fast Blank and Contrast Reduction Programmable Threshold

Table 7: Fast Blank and Contrast Reduction Programmable Threshold I^{2}C Controls

CNTR_ENABLE	FB_LEVEL[1:0]	Fast Blanking Threshold	CNTR_LEVEL[1:0]	Contrast Reduction Threshold
0	00	1.4 V	XX	n/a
0	01	1.6 V	XX	n/a
0	10	1.8 V	XX	n/a
0	11	2.0 V	XX	n/a
1	00	1.6 V	00	0.4 V
1	01	1.8 V	01	0.6 V
1	10	2.0 V	10	0.8 V
1	11	2.2 V	11	2.0 V

FB_LEVEL[1:0], *Address 0xF1, [5:4]*

Function

FB_LEVEL[1:0]	Description
00 ⊂	Controls reference level for Fast Blank comparator

CNTR_LEVEL[1:0], *Address 0xF1, [7:0]*

Function

CNTR_LEVEL[1:0]	Description
00 ⊂	Controls reference level for Contrast Reduction comparator

FB_INV, *Address 0xED, [3], Write only*

The interpretation of the polarity of the signal applied to the FB pin can be changed using FB_INV.

Function

FB_INV	Description
0 ⊂	Fast-blanking active HI
1	Fast-blanking active LO

3.4.4 Readback of FB Pin Status

FB_STATUS[3:0], *Address 0xED, [7:4]*

FB_STATUS[3:0] is a readback value that provides the system information on the status of the FB pins as follows:

Function

FB_STATUS[3:0]	Description
FB_STATUS[0]	FB_high. This bit goes high when the fast blank pin goes high
FB_STATUS[1]	FB_stat. Value of FB input pin at time of read.
FB_STATUS[2]	FB_fall. Indicates there has been a falling edge on FB since the last I^{2}C read. Value is cleared by current I^{2}C read – self-clearing bit.

Function

FB_STATUS[3:0]	Description
FB_STATUS[3]	FB_rise. Indicates there has been a rising edge on FB since the last I^{2}C read. Value is cleared by current I^{2}C read – self-clearing bit.

3.4.5 FB Timing

The critical information extracted from the FB signal is the time at which it switches relative to the input video. Due to small timing inequalities, either on the IC or on the PCB, it may be necessary to adjust the result by fractions of one clock cycle. This is controlled by FB_SP_ADJUST[3:0].

FB_SP_ADJUST[3:0], *Address 0xEF, [7:4]*

Function

FB_SP_ADJUST[3:0]	Description
0100	Adjustment to FB relative to sampling clock

Each LSB of FB_SP_ADJUST[3:0] corresponds to 1/8 of an ADC clock cycle. Increasing the value is equivalent to adding delay to the FB signal. The reset value is chosen to give equalized channels when the ADV7181C internal anti aliasing filters are enabled and there is no unintentional delay on the PCB.

3.4.5.1 Alignment of FB Signal

In the event of misalignment between the FB input signal and the other input signals (CVBS, RGB) or unequalized delays in their processing, it is possible to alter the delay of the FB signal. (For a finer granularity delay of the FB signal, refer to the description of FB_SP_ADJUST[3:0].)

FB_DELAY[3:0], *Address 0xF0, [3:0]*

Function

FB_DELAY[3:0]	Description
0100	Delay on FB signal in 28.63636 MHz clock cycles

FB_CSC_MAN, *Address 0xEE, [7]*

As shown in Figure 5, the data from the CVBS source and the RGB source are both converted to YPbPr before being combined. In the case of the RGB source, the Color Space Converter (CSC) must be used to perform this conversion. When SCART support is enabled, the parameters for the CSC are automatically configured correctly for this operation.

If the user wishes to use a different conversion matrix, this autoconfiguration can be disabled and then the CSC programmed manually.

Function

FB_CSC_MAN	Description
0	Automatic configuration of the CSC for SCART support
1	Manual programming of CSC required

4 Primary Mode and Video Standard

Setting the primary mode PRIM_MODE[3:0] and choosing a Video Standard VID_STD[3:0] are the most fundamental settings when configuring the ADV7181C. Refer to Table 8 for more details.

There are currently three main modes of operation on the ADV7181C. These three modes are controlled by PRIM_MODE[3:0] and are:

- **SD-M**
  This mode is referred to as Standard Definition mode. This covers all standard definition modes that have a modulated color subcarrier. Examples are PAL-BGHID, PAL-M/N, NTSC-M/N, SECAM and others.

  SD in YPbPr format (without a modulated color component) is the only exception; it too can be accepted in and processed by the SDP. ADI, however, recommends that SD-YPbPr should be processed like any other component video signal in COMP mode and routed through the Component Processor (CP) block.

- **COMP**
  Component video. This includes all video signals that arrive in a YPbPr (or YUV) analogue format. Typical examples are progressive and high definition video signals.

- **GR**
  Graphics. This mode is intended for RGB input signals with high bandwidth.

PRIM_MODE[3:0], Primary Mode, *Address 0x05, [3:0]*
VID_STD[3:0], Video Standard, *Address 0x06, [3:0]*

Table 8: Primary Mode and Video Standard Selection

PRIM_MODE[3:0]		**VID_STD[3:0]**				
Code	**Description**	**Processor**	**Code**	**Input Video**	**Output Resolution**	**Comment**
0000	**SD-M** (**S**tandard **D**efinition **M**odulated) e.g. CVBS/YC	SDP	0010	SD-4X1-M	720 x 480/576	4x oversampling
		CP	1010	SD 4x1 525i	720 x 480	YUV through CP
		CP	1011	SD 4x1 625i	720 x 576	YUV through CP
		CP	1100	SD 1x1 525i	720 x 480	YUV through CP
		CP	1101	SD 1x1 625i	720 x 576	YUV through CP
		CP	1110	SD 2x1 525i	720 x 480	YPbPr through CP
		CP	1111	SD 2x1 625i	720 x 576	YPbPr through CP
0001	**COMP** (Component Video) e.g. Y Pr Pb	CP	0000	SD 2x2 525i	1440 x 480	
		CP	0001	SD 2x2 625i	1440 x 576	
		CP	0010	SD 4x2 525i	1440 x 480	
		CP	0011	SD 4x2 625i	1440 x 576	
		CP	0100	PR 1x1 525p	720 x 480	
		CP	0101	PR 1x1 625p	720 x 576	
		CP	0110	PR 2x1 525p	720 x 480	
		CP	0111	PR 2x1 625p	720 x 576	
		CP	1000	PR 2x2 525p	1440 x 480	

PRIM_MODE[3:0]		VID_STD[3:0]				
Code	**Description**	**Processor**	**Code**	**Input Video**	**Output Resolution**	**Comment**
		CP	1001	PR 2x2 625p	1440 x 576	
		CP	1010	HD 1x1 720p	1280 x 720	
		CP	1011	Reserved	Reserved	
		CP	1100	HD 1x1 1125	1920 x 1080	
		CP	1101	HD 1x1 1125	1920 x 1035	
		CP	1110	HD 1x1 1250	1920 x 1080	
		CP	1111	HD 1x1 1250	1920 x 1152	
0010	**GR** (Graphics) e.g. R G B	CP	0000	SVGA	800 x 600 @ 56	
		CP	0001	SVGA	800 x 600 @ 60	
		CP	0010	SVGA	800 x 600 @ 72	
		CP	0011	SVGA	800 x 600 @ 75	
		CP	0100	SVGA	800 x 600 @ 85	
			0101	Reserved	Reserved	
			0110	Reserved	Reserved	
			0111	Reserved	Reserved	
		CP	1000	VGA	640 x 480 @ 60	
		CP	1001	VGA	640 x 480 @ 72	
		CP	1010	VGA	640 x 480 @ 75	
		CP	1011	VGA	640 x 480 @ 85	
		CP	1100	XGA	1024 x 768 @ 60	
		CP	1101	XGA	1024 x 768 @ 70	
			1110	Reserved	Reserved	
			1111	Reserved	Reserved	
0011	**RESERVED**		ALL	Reserved	Reserved	
0100	**RESERVED**		ALL	Reserved	Reserved	
0101	**RESERVED**		ALL	Reserved	Reserved	
0110	**RESERVED**		ALL	Reserved	Reserved	
0111	**RESERVED**		ALL	Reserved	Reserved	
1000	**RESERVED**		ALL	Reserved	Reserved	
1001	**RESERVED**		ALL	Reserved	Reserved	
1010	**RESERVED**		ALL	Reserved	Reserved	
1011	**RESERVED**		ALL	Reserved	Reserved	
1100	**RESERVED**		ALL	Reserved	Reserved	
1101	**RESERVED**		ALL	Reserved	Reserved	
1110	**RESERVED**		ALL	Reserved	Reserved	
1111	**RESERVED**		ALL	Reserved	Reserved	

Note: Some of the modes described have an inherent decimation built into them, e.g. 4X2, 2X1. For these modes, the main clock generator and the decimation filters in the DPP block are configured automatically. This ensures the correct data rate at the input to the SDP/CP block.

5 Global Control Registers

The listing of register control bits in this section affect the whole chip and are not dependent on the processor that is active, i.e. Standard Definition Processor (SDP) or Component Processor (CP).

5.1 Power-Save Modes

5.1.1 Power-Down

PWRDN[1:0], *Address 0x0F, [5] and [2]*

Setting the PWRDN bit switches the ADV7181C into a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip and thereby freezes its operation. No I^2C bits are lost during power down. The PWRDN bit also affects the analogue blocks and switches them into low current modes. The I^2C interface itself is unaffected and remains operational in power-down mode.

The ADV7181C leaves the power-down state if the PWRDN bit is set to 0 (via I^2C) or if the overall part is reset using the RESET pin.

Note: If PWRDN and PWRSAV are set simultaneously, PWRSAV takes priority.

Function

PWRDN[1:0]	Description
00	Chip operational
11	ADV7181C in chip wide power down

CP_PWRDN, *Address 0x0F, [3]*

To enable fast blanking, which requires simultaneous processing of CVBS and RGB, the CP is enabled for the SD mode of operation. In a power-sensitive application where fast-blanking support is not required, it is possible to stop the clock to the CP to reduce power.

Function

CP_PWRDN	Description
0	CP operational
1	CP in power-save mode

FB_PWRDN, *Address 0x0F, [1]*

To achieve very low power-down current, it is necessary to prevent activity on toggling input pins from reaching circuitry that could consume current. FB_PWRDN gates signals from the FB input pin.

Function

FB_PWRDN	Description
0 ⊂	FB input operational
1	FB input in power-save mode

5.1.2 Power-save Mode

PWRSAV, *Address 0x0F, [4]*

The PWRSAV bit allows the user to set the ADV7181C into a power-save mode that disables blocks of the ADV7181C, with the exception of the analogue sync stripper and some auxiliary digital blocks. Using the power-save mode, the ADV7181C still outputs sync information derived from the SOG or SOY pin.

The power-save mode can be used to implement an activity detection feature whereby an external device monitors the sync information as output from the ADV7181C while the rest of the IC is still in power-down mode, thus conserving energy. (Refer to Section 7.13.7 for more information.) The part will leave the power-save mode if the PWRSAV bit is set to 0 (via I^2C) or if the overall part is reset using the RESET pin.

Note: If the PWRDN and PWRSAV bits are set simultaneously, PWRSAV takes priority.

Function

PWRSAV	Description
0 ⊂	Chip operational
1	ADV7181C in power-save mode

5.1.3 ADC Power-down Control

The ADV7181C contains four 10-bit ADCs (ADC 0, ADC 1, ADC 2 and ADC3). It is possible to power down each ADC individually, if required.

When should you power down the ADCs?

- CVBS mode ADC 1, ADC 2 and ADC3 should be powered down to save on power consumption
- S-Video mode ADC 2 and ADC3 should be powered down to save on power consumption

PWRDN_ADC_0, *Address 0x3A, [3]*

Function

PWRDN_ADC_0	Description
0 ⊂	ADC normal operation
1	Powers down ADC 0

PWRDN_ADC_1, *Address 0x3A, [2]*

Function

PWRDN_ADC_1	Description
0 ⊂	ADC normal operation
1	Powers down ADC 1

PWRDN_ADC_2, *Address 0x3A, [1]*

Function

PWRDN_ADC_2	Description
0 ⊂	ADC normal operation
1	Powers down ADC 2

PWRDN_ADC_3, *Address 0x3A, [0]*

Function

PWRDN_ADC_3	Description
0 ⊂	ADC normal operation
1	Powers down ADC 3

5.2 Reset Control

Chip Reset (RES), *Address 0x0F, [7]*

Setting this bit is equivalent to controlling the Reset pin on the ADV7181C and will issue a full chip reset. All I^2C registers will be reset to their default values[1]. After the reset sequence, the part will immediately start to acquire the incoming video signal.

Important:

- After setting the RES bit (or initiating a reset via the pin), the part returns to the default mode of operation with respect to its primary mode of operation, etc. All I^2C bits will be loaded with their default values, which makes this bit self-clearing.
- Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5ms before any further I^2C writes are performed.
- The I^2C master controller will receive a no acknowledge condition on the ninth clock cycle when Chip Reset is implemented. Refer to Section 11 for a full description.

Function

RES	Description
0 ⊂	Normal operation
1	Starts reset sequence

1 Some register bits do not have a reset value specified. They will keep their last written value. Those bits are marked as having a reset value of ‘x’ in the register table.

5.3 Global Pin Control

5.3.1 Tristate Output Drivers

TOD, *Address 0x03, [6]*

This bit allows the user to tristate the output drivers of the ADV7181C. Upon setting the TOD bit, the following pins are tristated: P[19:0], HS, VS, FIELD, SFL.

Note that the timing pins (HS/VS/FIELD) can be forced active via the TIM_OE bit.

For additional details on tristate control, refer to the information on TRI_LLC and TIM_OE.

Individual drive strength controls are provided via DR_STR_XX bits. The ADV7181C does not support tri-stating via a dedicated pin.

Function

TOD	Description
0	Output drivers enabled
1	Output drivers tristated

5.3.2 Tristate LLC Driver

TRI_LLC, *Address 0x1D, [7]*

This bit allows the user to tristate the output driver for the LLC pin of the ADV7181C.

For additional details on tristate control, refer to the information on TOD and TIM_OE.

Individual drive strength controls are provided via DR_STR_XX bits. The ADV7181C does not support tri-stating via a dedicated pin.

Function

TRI_LLC	Description
0	LLC pin driver working according to DR_STR_C[1:0] setting (pin enabled)
1	LLC pin drivers tristated

5.3.3 Timing Signals Output Enable

TIM_OE, *Address 0x04, [3]*

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it to high forces the output drivers for HS, VS, and FIELD into the active, i.e. driving, state even if the TOD bit is set. If set to low, the HS, VS and FIELD pins are tristated, depending on the TOD bit. This functionality is useful if the decoder is to be used as a timing generator only. This may be the case if only the timing signals are to be extracted from an incoming signal or if the part is in free-run mode where a separate chip can output, for instance, a company logo picture.

For additional details on tristate control, refer to the information on TOD and TRI_LLC.

Individual drive strength controls are provided via DR_STR_XX bits. The ADV7181C does not support tri-stating via a dedicated pin.

Function

TIM_OE	Description
0	HS, VS, FIELD tristated according to TOD bit.
1	HS, VS, FIELD forced active all the time. DR_STR_S[1:0] setting determines drive strength.

5.3.4 Drive Strength Selection (Data)

DR_STR[1:0] *Address 0xF4, [5:4]*

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the P[19:0] output drivers.

For details on tristate control, refer to the information on DR_STR_C[1:0] and DR_STR_S[1:0].

Function

DR_STR[1:0]	Description
00	Reserved
01	Medium low drive strength (2X) for LLC1 up to 54 MHz
10	Medium high drive strength (3X) for LLC1 from 54 MHz to 110 MHz
11	High drive strength (4X)

5.3.5 Drive Strength Selection (Clock)

DR_STR_C[1:0] *Address 0xF4, [3:2]*

The DR_STR_C[1:0] bits allow the user to select the strength of the clock signal output driver (LLC pin). Refer to the information on DR_STR_S[1:0] and DR_STR[1:0].

Function

DR_STR[1:0]	Description
00	Reserved
01	Medium low drive strength (2X) for LLC1 up to 54 MHz
10	Medium high drive strength (3X) for LLC1 from 54 MHz to 110 MHz
11	High drive strength (4X)

5.3.6 Drive Strength Selection (Synchronization)

DR_STR_S[1:0] *Address 0xF4, [1:0]*

The DR_STR_S[1:0] bits allow the user to select the strength of the synchronization signals HS, VS and F. Refer to the information on DR_STR_C[1:0] and DR_STR[1:0].

Function

DR_STR[1:0]	Description
00	Reserved
01 ⊂	Medium low drive strength (2X) for LLC1 up to 54 MHz
10	Medium high drive strength (3X) for LLC1 from 54 MHz to 110 MHz
11	High drive strength (4X)

5.3.7 Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN *Address 0x04, [1]*

The Subcarrier Frequency Lock pin (SDP output only) has a double function. Firstly, the EN_SFL_PIN bit enables the output of Subcarrier Lock information (also known as 'GenLock') from the SDP core to an encoder in a decoder – encoder back-to-back arrangement. Secondly, it can output raw sync related information.

Function

EN_SFL_PIN	Description
0 ⊂	Subcarrier Frequency Lock output is disabled
1	Subcarrier Frequency Lock information is presented on the SFL pin

5.3.8 Polarity LLC Pin

PCLK *Address 0x37, [0]*
The polarity of the clock that leaves the ADV7181C via the LLC pin can be inverted using the PCLK bit. Note that this inversion affects the clock for SDP **and** CP.

Changing the polarity of the LLC clock output may be necessary in order to meet the setup and hold time expectations of follow-on chips. It is expected that these parameters must be met regardless of the type of video data (SD, PR, HD, and GR) that is transmitted. Therefore, the PCLK has been designed to be mode independent.

Function

PCLK	Description
0	Inverts LLC output polarity
1 ⊂	LLC output polarity normal (refer to Section 10.6)

6 Global Status Registers

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7181C; the other three registers contain status bits from the Standard Definition Processor (SDP) and the Component Processor (CP). The tables below indicate the block that is active in the case of each status bit.

6.1 STATUS 1

STATUS_1[7:0] *Address 0x10, [7:0]*

This read only register provides information about the internal status of the ADV7181C.

Notes:

- The lock related registers are described in more detail in Section 8.5.4. Refer to the information on timing in the descriptions of VS_COAST (SDP) and COL[2:0].
- It depends on the setting of the FSCLE bit whether the Status_1[0] and Status_1[1] are based solely on horizontal timing information or whether they are also based on the lock status of the color subcarrier.

Function

STATUS 1 [7:0]	Bit Name	Block	Description
0	IN_LOCK	SDP	In lock (right now)
1	LOST_LOCK	SDP	Lost lock (since last read of this register)
2	FSC_LOCK	SDP	Fsc locked (right now)
3	FOLLOW_PW	SDP	AGC follows peak white algorithm
4	AD_RESULT.0	SDP	Result of SDP autodetection,
5	AD_RESULT.1	SDP	
6	AD_RESULT.2	SDP	
7	COL_KILL	SDP	Color kill active

6.1.1 SDP Autodetection Result

AD_RESULT[2:0] *Address 0x10, [6:4]*

The AD_RESULT[2:0] bits report back on the findings from the SDP autodetection block. Refer to Section 8.5.2 for more information on the usage of the autodetection block.

Function

AD_RESULT[2:0]	Description
000	NTSM-MJ
001	NTSC-443
010	PAL-M
011	PAL-60

Function

AD_RESULT[2:0]	Description
100	PAL-BGHID
101	SECAM
110	PAL-Combination N
111	SECAM 525

6.2 STATUS 2

STATUS_2[7:0], *Address 0x12, [7:0]*

Notes:

- For the bits 2 and 3 to be meaningful, the Macrovision PS and AGC detection circuitry must be enabled (ON by default)
- Bits 4 and 5 are only applicable to the SD decoder
- Bit 6 and 7 are only meaningful if in TLLC mode (HD/PR/GR modes)

Function

STATUS 2 [7:0]	Bit Name	Block	Description
0	MVCS DET	SDP only	Detected Macrovision Color Striping
1	MVCS T3	SDP only	Macrovision Color Striping Protection conforms to type 3 (if high) to type 2 (if low)
2	MV_PS DET	SDP/CP	Detected Macrovision Pseudo Sync pulses
3	MV_AGC DET	SDP/CP	Detected Macrovision AGC pulses
4	LL_NSTD	SDP	Line length is non-standard
5	FSC_NSTD	SDP	Fsc frequency is non standard
6	CP_FREE_RUN	CP	CP is free-running (no valid video signal found)
7	TLLC_PLL_LOCK	CP	TLLC PLL is locked

6.3 STATUS 3

STATUS_3[7:0], *Address 0x13, [7:0]*

Function

STATUS 3 [7:0]	Bit Name	Block	Description
0	INST_HLOCK	SDP	Horizontal lock indicator (instantaneous)
1	GEMD	SDP	Gemstar detect
2	SD_OP_50Hz	SDP	Detects if 50 Hz or 60 Hz signal is present for SD
3	CVBS	SDP	Indicates if a CVBS signal is detected in 'YC/CVBS autodetection' configuration
4	FREE_RUN_ACT	SDP	SDP outputs a 'blue screen' (refer to information on DEF_VAL_AUTO_EN on page 101)
5	STD_FLD_LEN	SDP	Field length is correct for currently selected video standard
6	INTERLACED	SDP	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	SDP	Reliable sequence of swinging bursts detected

7 Component Processor

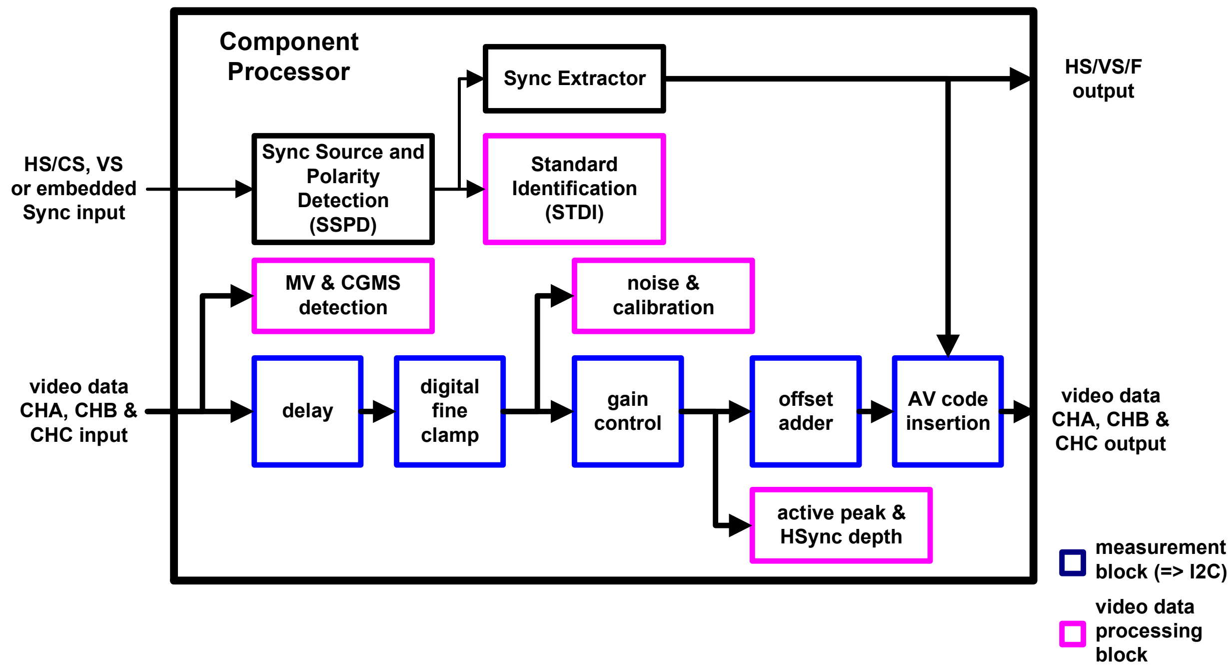


Figure 8: Component Processor Block Diagram

7.1 Introduction to Component Processor

A simplified block diagram of the Component Processor (CP) on the ADV7181C is shown in Figure 8. Data is supplied to the CP from the Data Preprocessor (DP). The CP circuitry is activated under the control of PRIM_MODE[3:0] and VID_STD[3:0]. Refer to Section 4 for more details on PRIM_MODE[3:0] and VID_STD[3:0].

The CP is activated for the following modes of operation:

- GR modes: PC graphic-based signal in RGB format
- HD modes: high definition video signals in YPbPr/RGB format
- PR mode: progressive scan video signal in YPbPr/RGB format, e.g. 525P and 625P
- SD modes: component standard definition in YPbPr/RGB format, e.g. 525i and 625i

Note: The CP is not used when decoding composite or S-Video signals.

The CP performs the following functions:

- Digital fine clamping of the video signal
- Manual and automatic gain control
- Manual offset correction
- Saturation

- Insertion of timing codes and blanking data

The CP also has the following capabilities:

- Generates HS, VS, FIELD and Data Enable (DE) timing reference outputs
- Detects the source from which the video is to be synchronized
- Measures noise and calibration levels
- Measures the depth of the horizontal sync pulse used for AGC
- Detects the presence of Macrovision encoded signals
- Extracts Copy Generation Management System (CGMS) data from the video input signal and makes it available over I^2C

7.2 Data Delay Block (CP)

The CP contains a programmable delay block. This block consists of three banks of flip-flops, which can be bypassed. Using those registers, the data on the three channels A, B and C can be individually delayed by one sampling clock-cycle or, alternatively, passed through undelayed.

DLY_A Data Delay Block in CP, *Address 0x67, [7]*
Function

DLY_A	Description
0 ⊂	Passes data through channel A
1	Delays data through channel A by one clock cycle

DLY_B Data Delay Block in CP, *Address 0x67, [6]*
Function

DLY_B	Description
0 ⊂	Passes data through channel B
1	Delays data through channel B by one clock cycle

DLY_C Data Delay Block in CP, *Address 0x67, [5]*
Function

DLY_C	Description
0 ⊂	Passes data through channel C
1	Delays data through channel C by one clock cycle

7.3 Analogue Video Signal Sampling

The ADV7181C has two main modes of operation for sampling the input video:

1. When the SDP is enabled, fixed 54 MHz sampling is applied at all three ADCs. The SDP processes the video signal and, using a line length tracking processor, resamples the incoming video so that 720 active pixel are always generated per line. Refer to Section 8 for more details. Note that no user I^2C settings are available for the PLL when in SDP mode as the PLL is controlled directly by the SDP.

2. When the CP is enabled, True Line Locked sampling is applied to the video signal being processed. This means that the incoming video signal's horizontal synchronization signal is applied to the PLL and multiplied up by the desired number of samples per line, which yields the pixel sampling clock used in CP mode.

7.3.1 CP PLL Control

For data that passes through the CP section of the ADV7181C, the ADCs are clocked by a multiplying PLL that locks to the incoming horizontal syncs. The multiplying factor of the PLL is implemented by means of a programmable divider in the feedback path. The divider value is normally decoded off the PRIM_MODE[3:0] and VID_STD[3:0] registers.

To allow the selection of non-standard sampling rates, access to the feedback divider is provided by means of the following values:

- The PLL divide ratio can be manually overwritten
- The VCO centre frequency can be set to one of four values

The feedback divider number is essentially equal to the total number of samples per line of video.

Notes:

- Small deviations from the nominal sampling frequency can be accommodated simply by slightly changing the feedback value.

- In some applications, it might be necessary to change the feedback divider value by a larger amount, e.g. to suit the target resolution of a digital screen. In this case, some internal windows, e.g. voltage clamp or active video, need to be adjusted too. Contact ADI with details of the desired mode of operation.

PLL_DIV_MAN_EN Enable Manual PLL Ratio Value (CP), *Address 0x87, [7]*

Function

PLL_DIV_MAN_EN	Description
0 ⊂	PLL feedback value derived automatically from PRIM_MODE[3:0] and VID_STD[3:0]
1	Uses PLL_DIV_RATIO[11:0] as the multiplying factor in the sampling PLL for CP

7.3.2 Manual PLL Divider Ratio Value

PLL_DIV_RATIO[11:0] *Address 0x87, [3:0]; Address 0x88, [7:0]*

The two registers, CP TLLC Control 1 and 2, have to be written to in sequence. The PLL divide ratio value used inside the ADV7181C will only be updated when both registers have been written to. (Refer to the information on I^{2}C Sequencer in Section 11.)

The order of the writes is important:

- Firstly, write to CP TLLC Control 1
- Secondly, write to CP TLLC Control 2

Only after the second write will all 12 bits of PLL_DIV_RATIO[11:0] be updated simultaneously.

The write sequence has the following effects:

- It is not possible to ‘tweak’ the TLLC frequency by selectively changing the LSBs of the divide ratio through several consecutive write operations to CP TLLC Control 2. All 12 bits have to be updated, even if the value changes only affect the LSBs or MSBs.

- For larger value changes, the write sequence prevents intermediate wrong PLL divide ratios from entering the TLLC PLL. Wrong values could happen if a newly updated PLL_DIV_RATIO[11:8] from a first I^{2}C write is combined with an old PLL_DIV_RATIO[7:0] from a previous write or vice versa. The write sequence inhibits this.

Function

PLL_DIV_RATIO[11:0]	Description
XXX	PLL feedback divider value. For this value to be active, the PLL_DIV_MAN_EN bit must be set. Also observe the VCO_RANGE[1:0] settings.

7.3.3 PLL Divide Ratio and DLL Phase Update Sequencing

PLL_DLL_UPD_VS_EN, *Address 0x87, [4]*

By default, the PLL Divide Ratio (described above) and the DLL Phase selection (refer to the description of DLL_PH[4:0] on page 45) are updated immediately. To prevent artifacts when these values switch during active video, it is possible to prevent the new values becoming active until the following VBI period. This is controlled via PLL_DLL_VS_UPD_EN.

Function

PLL_ DLL_VS_UPD_EN	Description
0	PLL Divide Ratio and DLL Phase update immediately
1	PLL Divide Ratio and DLL Phase update with following Vsync

7.3.4 CP VCO Range Setting

Setting the VCO range on the ADV7181C sets the nominal range of operation for the PLL. Figure 9 shows how these control bits set a predivider in the TLLC generator to keep the VCO operating in its natural frequency range.

VCO_RANGE_MAN Enable Manual PLL Operating Range (CP), *Address 0x8A, [7]*

Function

VCO_RANGE_MAN	Description
0 ⊂	PLL operating range is derived automatically from PRIM_MODE[3:0] and VID_STD[3:0]
1	PLL operating range is as given in VCO_RANGE[1:0] bits

VCO_RANGE[1:0] Manual PLL Operating Range (CP), *Address 0x8A, [6:5]*

The settings of VCO_RANGE[1:0] only become active if VCO_RANGE_MAN is set to 1. For all standards supported by PRIM_MODE and VID_STD, the appropriate VCO range is selected automatically.

Table 9: VCO Range Operating Range

Function	
VCO_RANGE[1:0]	**Description**
00 ⊂	TLLC range supported is [13.5 – 30 MHz] For this setting to be active, VCO_RANGE_MAN bit has to be set to 1
01	TLLC range supported is [30 – 45 MHz] For this setting to be active, VCO_RANGE_MAN bit has to be set to 1
10	TLLC range supported is [45 – 90 MHz] For this setting to be active, VCO_RANGE_MAN bit has to be set to 1
11	TLLC range supported is [90 – 110 MHz] For this setting to be active, VCO_RANGE_MAN bit has to be set to 1

The VCO of the ADV7181C incorporates the analogue VCO block followed by a predivider, as shown in Figure 9. The VCO_RANGE[1:0] controls this predivide, not the analogue VCO circuitry. It does not change the analogue behavior of the VCO as such.

The actual range of operation for the analogue VCO depends on supply and process. The operating point for the VCO is around 170 MHz for best performance, e.g. jitter. The range that the VCO can support under the worst conditions is 20 MHz to 220 MHz.

For non-standard video signals, the VCO_RANGE[1:0] should be set in such a way that the analogue VCO frequency is as close as possible to the ideal operating point of approximately 170 MHz.

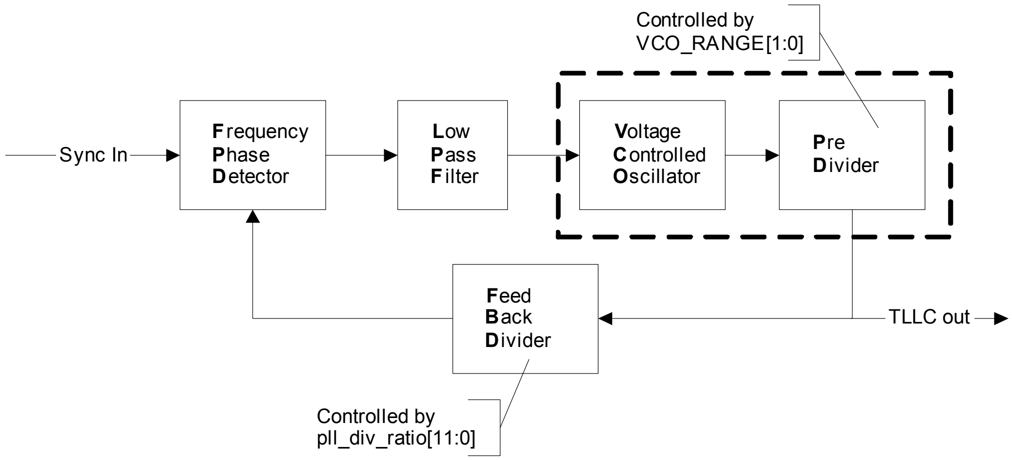


Figure 9: TLLC PLL Architecture

7.3.5 PLL Charge Pump Setting

The PLL charge pump current is set using the PLL_QPUMP[2:0] register. Customizing the PLL charge pump current affects the loop gain of the PLL and, hence, the dynamic behavior of the TLLC system. Note that this parameter is only meaningful in TLLC modes where the PLL is required to track the input video signal.

PLL_QPUMP[2:0] PLL Charge Pump Current Setting, *Address 0x3C, [2:0]*

This sets the PLL charge pump current. The following equation describes how the charge pump current is calculated for a particular mode. The closest setting for PLL_QPUMP[2:0] is then chosen.

$$PLL\ Natural\ Frequency = \frac{Hsync\ Frequency * 2\pi}{PLL\ Stability\ Ratio}$$

$$PLL\ Natural\ Frequency = \sqrt{\left(\frac{I_P * K_{VCO}}{C_t * N * P}\right)}$$

$$=> I_P = \left(\frac{Hsync\ Frequency * 2\pi}{PLL\ Stability\ Ratio}\right)^2 \left(\frac{C_t * N * P}{K_{VCO}}\right)$$

Equation 3: Charge Pump Current Calculation

Note: P = Post Divide Factor

N = PLL Divide Ratio
Kvco = VCO gain (in MHz/V) = 310
PLL Stability Ratio = SR
Ct = Loop Filter Capacitor Value (uF) = 0.082

Function

PLL_QPUMP[2:0]	Description
000	50 uA
001	100 uA
010	150 uA
011	250 uA
100	350 uA
101	500 uA
110	750 uA
111	1500 uA

7.3.6 Recommended Settings for CP PLL Modes of Operation

Refer to Table 10 and Table 11 for PLL recommended settings. Note that PLL_DIV_RATIO and VCO_RANGE parameters are automatically set up from the VID_STD settings; the only user required action is to program the PLL_QPUMP as per Table 10 and Table 11.

Table 10: PLL Recommended Settings for GR Modes

Graphics Standard	Active Pixels per Line/Frame	Vertical Frequency (Hz)	Horizontal Frequency (KHz)	Sampling Frequency (MHz)	Samples per Total Line	PLL Divisor	VCO Range	Charge Pump Current	P	Ip	Ipact	SR
VGA	640x480	59.93	31.460	25.17	800	800	00	100	6	409.6182	350	11.90
		72.81	37.860	31.50	832	832	01	100	4	411.2797	350	11.92
		75.00	37.500	31.50	840	840	01	100	4	407.3689	350	11.87
		85.01	43.270	36.00	832	832	01	101	4	537.1993	500	11.40
SVGA	800x600	56.25	35.160	36.00	1024	1024	01	101	4	436.5133	500	10.28
		60.32	37.880	40.00	1056	1056	01	101	4	522.5358	500	11.25
		72.19	48.080	50.00	1040	1040	10	100	2	414.5248	350	11.97
		75.00	46.880	49.50	1056	1056	10	100	2	400.1371	350	11.76
		85.06	53.670	56.25	1048	1048	10	101	2	520.5593	500	11.22
XGA	1024x768	60.00	48.360	65.00	1344	1344	10	101	2	542.0205	500	11.45
		70.07	56.480	75.00	1328	1328	10	110	2	730.4189	750	10.86

* Component out only

Table 11: PLL Recommended Settings for SD, PR and HD Modes

Video Standard	Lines per Frame	Active Pixels per Line/Frame	Vertical Frequency (Hz)	Horizontal Frequency (KHz)	Sampling Frequency (MHz)	Samples per total line	PLL Divisor	VCO Range	Charge Pump Current	P	Ip	Ipact	SR
1080i	1125	1920x1080	60	33.750	74.25	2200	2200	10	101	2	432.1020	500	10.23
1080i	1125	1920x1080	50	28.125	74.25	2640	2640	10	100	2	360.0850	350	11.16
720p	750	1280x720	60	45.000	74.25	1650	1650	10	101	2	576.1360	500	11.81
720p	750	1280x720	50	37.500	74.25	1980	1980	10	101	2	480.1134	500	10.78
480p 2X1	525	720x483	60	31.469	54.00	858	1716	10	011	2	293.0170	250	11.91
576p 2X1	526	720x576	50	31.250	54.00	864	1728	10	011	2	290.9778	250	11.87
480i 2X1	526	720x480	60	15.734	27.00	858	1716	00	011	6	219.7557	250	10.31
480i 4X1	525	720x480	60	15.734	54.00	858	3432	10	010	2	146.5038	150	10.87
576i 2X1	527	720x576	50	15.625	27.00	864	1728	00	011	6	218.2333	250	10.28
576i 4X1	525	720x576	50	15.625	54.00	864	3456	10	010	2	145.4889	150	10.83

7.3.7 Non-Standard CP PLL Modes of Operation

For all non-standard CP PLL modes, the PRIM_MODE and VID_STD must be to set to the nearest available standard to correctly configure the internal parameters of the CP core to decode the specific SD/HD/GR and Interlace/Progressive standard.

Depending on the required pixel clock frequency, the PLL Divisor Ratio, VCO Range and PLL_QPUMP settings must be set to configure the PLL to generate a stable LLC. Refer to Section 7.3.1 to set the correct PLL Divisor Ratio. The recommended VCO Range and PLL charge pump settings can be set by referring to Table 9 and Equation 3.

7.4 ADC Sampling Phase Control

The stability of this clock is a very important element in providing the clearest and most stable graphics image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (refer to Figure 10).

The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

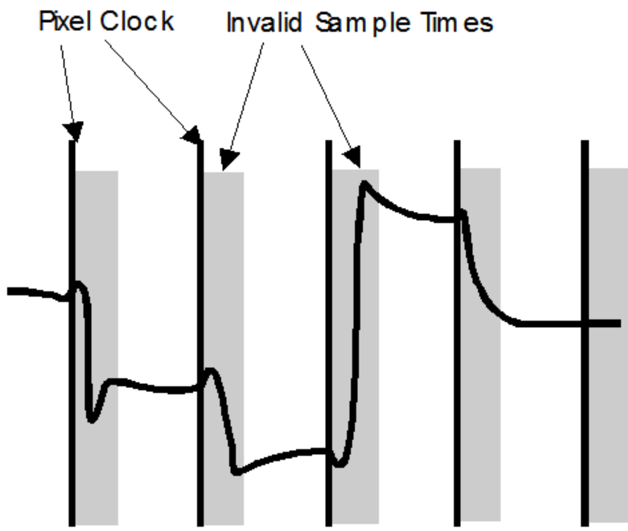


Figure 10: RGB Graphic Signal

7.4.1 Delay Locked Loop

When sampling an RGB graphics signal, as generated from PCs etc., the analogue input waveform is assumed to be a full bandwidth graphics signal that is sub-sampled. The signal will not have gone through a reconstruction filter but will show discrete levels and transitions in between. In this mode of operation, the ADCs must sample at the flat portions of the waveform and avoid the transition period.

To cater for this, a DLL has been implemented in the analogue front end (refer to Figure 11). This DLL divides the TLLC sampling clock into 32 evenly spaced phases. The DLL_PH[4:0] signal can be used to set the ADC sampling point to any of those phases.

The DLL can also be by-passed completely via the BYP_DLL bit. The control of the DLL is normally performed by a graphic backend chip connected to the ADV7181C; this is normally with a processor capable of selecting the optimum phase for sampling the RGB signal.

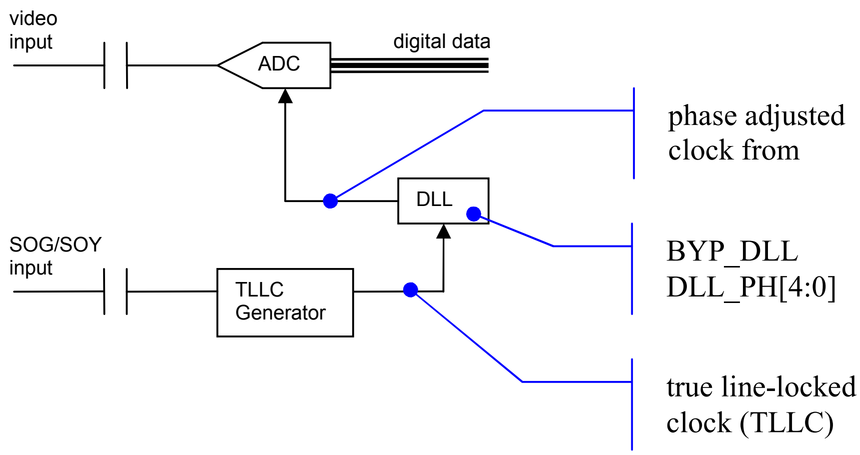


Figure 11: Delay Locked Loop

BYP_DLL Bypass DLL, *Address 0x6A, [5]*

Function

BYP_DLL	Description
0 ⊂	Includes the DLL in the clocking path of the ADCs
1	Bypasses the DLL completely

DLL_PH[4:0] Sample Phase Adjustment, *Address 0x6A, [4:0]*

Function

DLL_PH[4:0]	Description
00000 ⊂	Selects phase 0
XXXXX	Selects any of the other 31 phases

7.4.2 Latch Clock Setting

The latch clock setting is an internal ADC parameter that controls the data acquisition stage of the A/D conversion. For optimum ADC performance, it should be changed with increasing sampling frequency. The following table gives the recommended latch clock setting for specific sampling frequency ranges.

LATCH_CLK[3:0] Latch Clock, *Address 0x3A, [7:4]*

Function

LATCH_CLK[3:0]	Description
0001 ⊂	Recommended LLC range (13.5 MHz – 55 MHz)
0010	Recommended LLC range (55 MHz – 100 MHz)
0101	Reserved
0110	Reserved

7.4.3 Embedded Synchronization Slicer

An analogue circuit for detecting embedded sync information is provided on the ADV7181C. This sync slicer (sometimes referred to as the SOG/SOY block – Sync On Green/Y) is only used in CP modes and never used in SDP modes.

The sync slicer needs to see the video signal with the embedded sync. An analogue pin is provided, and is referred to as SOG/SOY (Sync On Green/Sync On Y).

The threshold at which a sync is being detected is programmable via the SOG_SYNC_LEV[4:0] bits. Note that SOG_SYNC_LEV[4:0] applies to both the SOG and the SOY function. The output of the sync detection block is muxed again with the digital HS input and the result is fed to a phase locked loop (PLL) to generate TLLC.

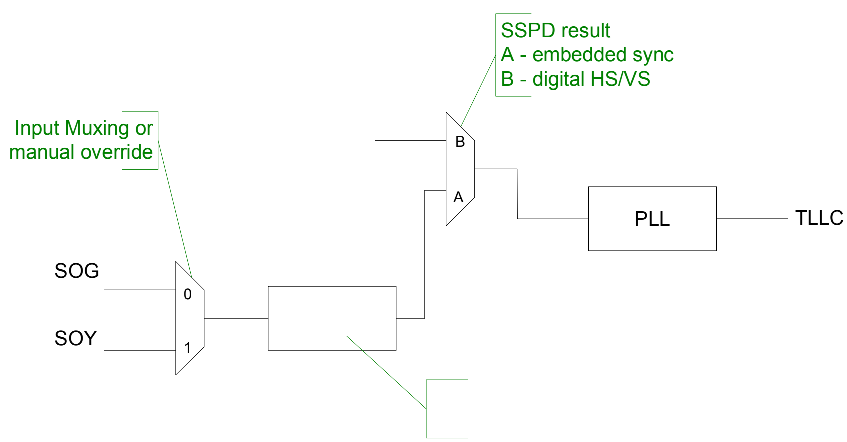


Figure 12: SOG, SOY, and HS Input Muxing

Notes:

- The input threshold on the digital HS signal can be selected via SYN_LOTRIG as described on page 66.
- Refer also to Section 7.11.

SOG_SYNC_LEV[4:0] Embedded Sync Trigger Level, *Address 0x3C, [7:4]*

The SOG_SYNC_LEV[4:0] bits allow the user to set the analogue trigger threshold for the sync detection.

$$V_{TH} = 300mV \bullet \frac{SOG\_SYNC\_LEV[4:0]}{32}$$

Equation 4: SOG_SYNC_LEV[4:0]

The trigger voltage is measured relative to the lowest analogue voltage level of the incoming video signal. For standard video signals, this is the bottom of the horizontal sync. However, if there is ringing around the horizontal sync edges, this might have to be taken into account (refer to Figure 13).

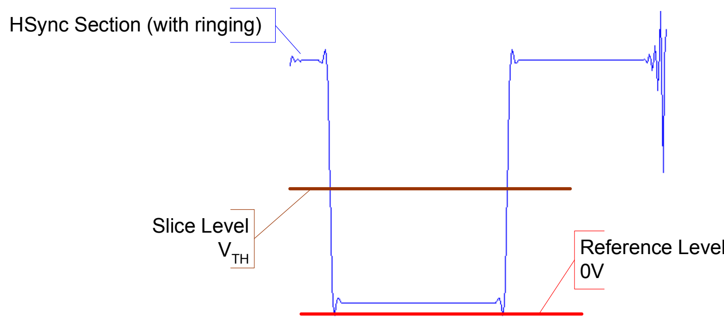


Figure 13: Synchronization Slice Level on Realistic Horizontal Sync

Function

SOG_SYNC_LEV[4:0]	Description
01011 ⇐	Threshold level is 103 mV above the lowest analogue voltage level within the input video line

TRI_LEVEL Tri-Level Sync Slicer Enable, *Address 0x69, [7]*

Setting the TRI_LEVEL bit enables a tri-level sync slicer to be operational. Tri-level syncs are usually found in HD-based video systems. By default, the ADV7181C uses the negative going sync edge for all video sources, including HD.

Notes:

- In future revisions, the selection of tri-level versus negative edge sync detection may be made automatic.
- Setting this bit while the input video is not of a HD type will most likely cause unstable operation of the part.

Function

TRI_LEVEL	Description
0 ⇐	Uses negative going edge for sync detection
1	Uses positive edge of tri-level sync for detection

7.5 Data Preprocessors

The Data Preprocessor (DPP) is positioned after ADC0, ADC 1, ADC2, and ADC3; it receives the data directly from these ADCs.

The DPP is made up of two main sections (refer to Figure 14):

1. Color space conversion (CSC) matrix supporting YCrCb-to- DDR RGB and RGB-to-YCrCb
2. Decimation filters with delay blocks.

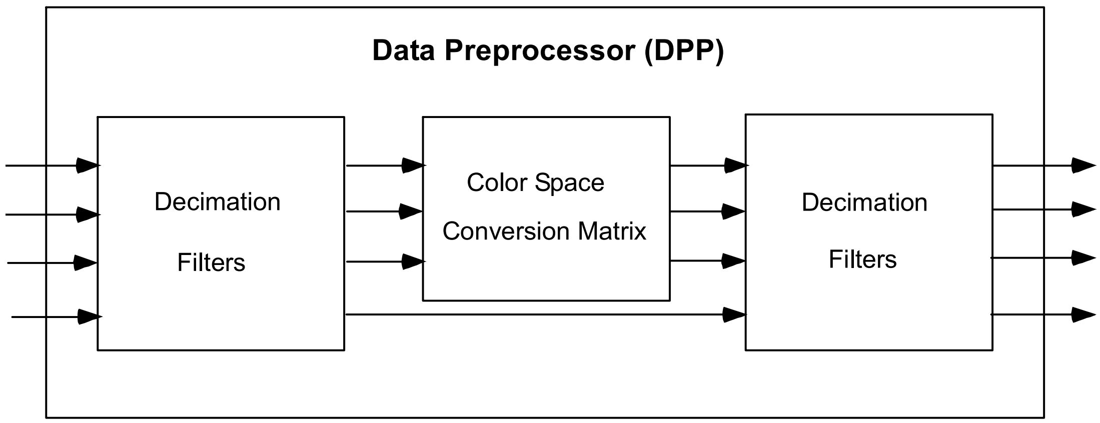


Figure 14: DPP Block Diagram

7.5.1 Color Space Conversion Matrix

The ADV7181C contains a fixed function color space conversion (CSC), which supports the following modes:

- SD RGB to YPrPb
- HD RGB to YPrPb
- Graphics RGB to YPrPb

7.6 Clamp Operation (CP)

For analogue signals that enter the CP block, there are two clamp methods applied to the video signal:

- An analogue voltage clamp block prior to the ADCs
- A digital fine clamp that operates after the DPP block

The analogue voltage clamp signal operates on the input video prior to digitization. Figure 15 shows the position within the active video lines where the voltage clamp switches on. The position of the window is changed automatically dependent on PRIM_MODE[3:0] and VID_STD[3:0] to suit the video standard in question.

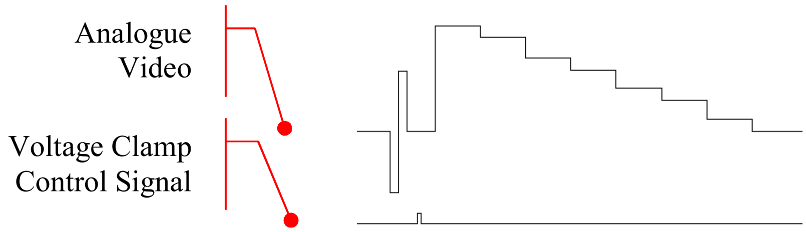


Figure 15: Position of Voltage Clamp Window

The CP contains a digital fine clamp block. Its main purpose is to compensate for variations of the voltage clamps in the analogue domain.

The digital fine clamp operates in three separate feedback loops, one for each channel. The incoming video signal level is measured at the back porch. The level error, i.e. clamp error, is compensated for by subtracting or adding a digital number to the data stream.

The digital clamp loop can be operated in an automatic or a manual mode with the following options:

- The clamp value is determined automatically on a line-by-line basis.
- The clamp loops can be frozen. This means that the currently active offsets will no longer be updated but will be applied permanently.
- The clamp value for channel A can be set manually (static value).
- The clamp values for channels B and C can be set manually.

Notes:

- The target clamp level for black input is a digital code of 0. This is to facilitate the highest possible signal to noise ratio (SNR). Some interfaces, e.g. ITU-R. BT656, require 'black' to correspond to a value other than 0. To facilitate this, there is an additional independent offset adder block after the gain multipliers for which separate fixed offset values can be supplied.
- Refer to the description in Section 7.8.

CLMP_FREEZE Freeze Digital Clamp (CP), *Address 0x6C, [5]*

The CLMP_FREEZE bit stops the three digital fine clamp loops for channels A, B and C updating. The currently active clamp values are applied continuously. All three loops are affected together; it is not possible to freeze the clamps for the channels individually.

Function

CLMP_FREEZE	**Description**
0 ⊂	Clamp loops operational, clamp value are updated on every active video line
1	Clamp loops are stopped, not updated anymore

CLMP_A_MAN Enable Manual Clamping for Channel A, *Address 0x6C, [7]*
Function

CLMP_A_MAN	**Description**
0 ⊂	Uses the digital fine clamp value determined by the on-chip clamp loop (CP)
1	Ignores internal digital fine clamp loop result, instead use CLMP_A[11:0]

CLMP_A[11:0] Manual Clamp Value for Channel A, *Address 0x6C, [3:0]; Address 0x6D, [7:0]*
Function

CLMP_A[11:0]	**Description**
xxxx xxxx xxxx	12-bit value to be subtracted from the incoming video signal. This value is only active if the CLMP_A_MAN bit is set.

To facilitate an external clamp loop for channels B and C, the internal clamp value determined by the digital fine clamp block can be overridden by manual values programmed in the I^2C. Both channels B and C are either in manual or automatic mode. There is no individual control for them. The corresponding control values are CLMP_BC_MAN, CLMP_B[11:0] and CLMP_C[11:0].

CLMP_BC_MAN Enable Manual Clamping for Channels B and C, *Address 0x6C, [6]*
Function

CLMP_BC_MAN	**Description**
0 ⊂	Uses the digital fine clamp value determined by the on-chip clamp loop (CP)
1	Ignores internal digital fine clamp loop result, instead use CLMP_B[11:0] for channel B and CLMP_C[11:0] for channel C

CLMP_B[11:0] Manual Clamp Value for Channel B, *Address 0x6E, [7:0]; Address 0x6F, [7:4]*
Function

CLMP_B[11:0]	**Description**
xxxx xxxx xxxx	12-bit value to be subtracted from the incoming video signal. This value is only active if the CLMP_BC_MAN bit is set.

CLMP_C[11:0] Manual Clamp Value for Channel C, *Address 0x6F, [3:0]; Address 0x70, [7:0]*
Function

CLMP_C[11:0]	**Description**
xxxx xxxx xxxx	12-bit value to be subtracted from the incoming video signal. This value is only active if the CLMP_BC_MAN bit is set.

CLAMP_AVG_FCTR[1:0] Manual Clamp Filtering Modes, *Address 0xC5, [7:6]*

The ADV7181C provides a special filter option for the auto clamp mode. The purpose of this filter is to provide a smoothening mechanism when manual clamping is being continuously changed in significant amounts by the auto clamping mechanism, based on either external or readback conditions in the ADV7181C.

The filter is an IIR filter with an effective function:

$$Y_N = (1-A)*Y_{N-1} + A*X_N$$

where A is the filter coefficient.

The value of A can vary from 1 to 1/32 lines. A value of '1' indicates no filtering of the clamp and is a pass through option for the auto clamp value.

CLAMP_AVG_FCTR[1:0]	Description
XXX	The 2 bit value indicates the filter coefficient affected
00	No filtering. Pass through coefficient A = 1.
01	Coefficient A = 1/8 lines
10	Coefficient A = 1/16 lines
11	Coefficient A = 1/32 lines

7.7 Component Processor Gain Operation

The digital gain block of the CP consists of three multipliers in the data paths of channel A, B and C, as well as one single automatic gain control loop. The gain control can be operated in the following modes:

- The gain value is determined automatically, based on a signal with an embedded horizontal sync pulse on channel A
- The automatic gain control loop can be frozen, e.g. after settling
- The gain values for the three channels can be programmed separately via I^2C registers

There is a detection block called Sync Source and Polarity Detector (SSPD), which is used to determine automatically the presence of external digital syncs, e.g. HS/VS, or embedded sync. The detection result of the SSPD block is used to enable/disable the **automatic** gain control mode.

In other words, if SSPD detects the presence of external (i.e. digital) sync signals, the gain block in the CP core is switched to manual gain mode because it is assumed that there is no embedded HSYNC present and it is, therefore, not possible to adjust the gain **automatically**.

If, however, SSPD does not find any external sync signal, it concludes that the sync must be embedded. This switches the gain block in the CP core into automatic mode. (Refer to Section 7.11.) This function can be disabled using AGC_MODE_MAN, as illustrated in Figure 16.

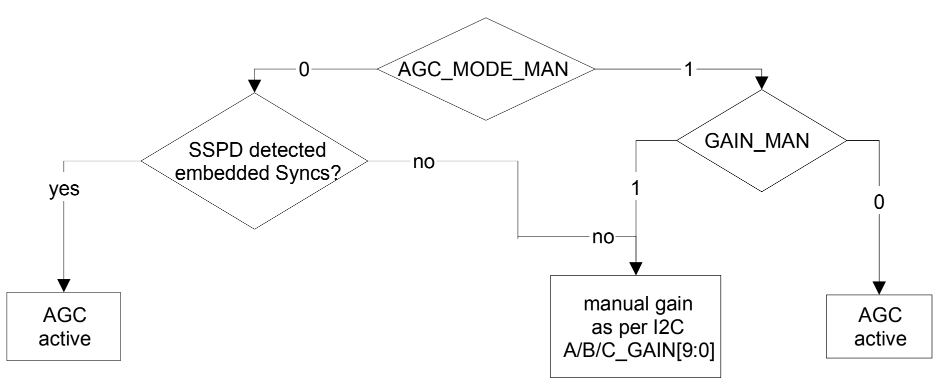


Figure 16: CP AGC Automatic Enable

AGC_MODE_MAN AGC Mode Manual Enable, *Address 0x73, [6]*

Function

AGC_MODE_MAN	**Description**
0 ⊂	Enables AGC based on SSPD decision
1	Gain operation controlled by GAIN_MAN

7.7.1 Automatic Gain Control

The automatic gain control (AGC) of the CP takes measurements of the signal on channel A and determines an appropriate gain value for all three channels. For the block to operate, it is necessary that a signal with an embedded synchronization pulse is fed through to channel A, e.g. Y or G. The AGC measures the depth of this synchronization pulse and compares it against a target value. The HSD_CHA[9:0] readback register is used to determine if there is a sync pulse on the data. If no sync pulse can be found, AGC cannot work and the manual gain control should be enabled.

The target value for the AGC can come from three sources. There are two predefined values of 300mV and 286mV (use the HS_NORM bit to decide between the two) and there is the option of setting an arbitrary target value by setting the AGC_TAR_MAN bit (enables the usage) and AGC_TAR[9:0] (sets the arbitrary target level).

In some applications, it is desirable to use the AGC to gain the signal to a smaller range, use the Offset block to preserve the syncs (by 'lifting' the whole video signal up), and thus output the full digitized waveform (including syncs) within the 10-bit output range. For this application, the AGC_TAR[9:0] value is very important. Refer to Section 7.8 for more information.

$$AGC\_TAR[9:0] = (Code_{White} - Code_{Black}) \bullet \frac{SyncHeight_{mV}}{VideoHeight_{mV}}$$

Equation 5: CP AGC Target Value

Note: The 10-bit target code for white is nominally 940, the target code for black is 64.

Examples:

$$AGC\_TAR_{HSync=286mV} = (940-64) \bullet \frac{286mV}{714mV} = 351_{dec}$$

$$AGC\_TAR_{HSync=300mV} = (940-64) \bullet \frac{300mV}{700mV} = 375_{dec}$$

An error signal is derived from the comparison of the measured sync depth and the target value. The error signal is weighted by a factor that allows different response times to be selected (use AGC_TIM[2:0] to select different time constants). The resulting gain value is applied to all three channels A, B and C.

The AGC_FREEZE bit allows the AGC loop to be stopped, i.e. frozen. If frozen, the currently active gain is no longer updated but is applied continuously to all three data streams.

HS_NORM Nominal Horizontal Sync Depth Selection, *Address 0x71, [3]*
Function

HS_NORM	**Description**
0 ⊂	AGC target is to scale the video as per 300 mV horizontal sync depth
1	AGC target is to scale the video as per 286 mV horizontal sync depth

AGC_TAR_MAN AGC Manual Target Level Enable, *Address 0x71, [5]*
Function

AGC_TAR_MAN	**Description**
0 ⊂	AGC operates on the basis of a 300 mV or 286 mV horizontal sync depth. Use HS_NORM to select between the two.
1	AGC operates on the basis of AGC_TAR[9:0].

AGC_TAR[9:0] AGC Manual Target Level, *Address 0x71, [7:6]; Address 0x72, [7:0]*
Function

AGC_TAR[9:0]	**Description**
xx xxxx xxxx	Sets the target value for the sync depth after gain has been applied (feedback system). (Refer to Equation 5.)

AGC_FREEZE AGC Freeze Enable, *Address 0x71, [4]*
Function

AGC_FREEZE	**Description**
0 ⊂	AGC loop operational
1	AGC loop frozen (no further updates, last gain value becomes static)

AGC_TIM[2:0] AGC Time Constant Selection, *Address 0x71, [2:0]*
Function

AGC_TIM[2:0]	**Description**
000 ⊂	100 lines
001	1 frame
010	0.5 seconds
011	1 second
100	2 seconds
101	3 seconds
110	5 seconds
111	7 seconds

7.7.1.1 Readback Signals from AGC Block

The following readback signals are provided:

- The presently used gain value can be read back through CP_AGC_GAIN[9:0]
- The depth of the sync pulse on channel A (before gaining) through HSD_CHA[9:0]
- The depth of the sync pulse on channel A (after gaining) through HSD_FB[9:0]
- The depth of the sync pulse on channel B (before gaining) through HSD_CHB[9:0]
- The depth of the sync pulse on channel C (before gaining) through HSD_CHC[9:0]

Notes:

- HSD_FB[9:0] is provided to allow an off-chip AGC loop to be implemented in a feedback architecture.
- HSD_CHA/B/C[9:0] is provided to allow the user in GR modes to find out if all three channels have sync pulses on them. If the input RGB has a sync pulse only on the Green channel and the CSC is used to convert RGB to YPbPr levels, the sync depth on Y will be too shallow (compare with conversion formula RGB to YPbPr). AGC_TAR[9:0] must be used to enable proper output levels after the AGC.
- The HSD_CHA[9:0] register information is also used to figure out if an automatic gain control (AGC) function is possible. Without a proper sync pulse on the data in channel A, no AGC loop can work and manual gain control should be used.

CP_AGC_GAIN[9:0] AGC Gain Read Back, *Address 0xA0, [1:0]; Address 0xA1, [7:0]*
Function

CP_AGC_GAIN[9:0]	**Description**
xx xxxx xxxx	Readback value of actually used gain on the data of channel A. Data format is 1.9 and hence composed of one integer and 9 fractional bits.

HSD_CHA[9:0] Horizontal Sync Depth Channel A Read Back, *Address 0xA7, [1:0]; Address 0xA8, [7:0]*
Function

HSD_CHA[9:0]	**Description**
xx xxxx xxxx	Readback value of measured horizontal sync depth on channel A (before gain multiplier). The value is presented in standard binary form.

HSD_CHB[9:0] Horizontal Sync Depth Channel B Read Back, *Address 0xA7, [3:2]; Address 0xA9, [7:0]*
Function

HSD_CHB[9:0]	**Description**
xx xxxx xxxx	Readback value of measured horizontal sync depth on channel B (before gain multiplier). The value is presented in standard binary form.

HSD_CHC[9:0] Horizontal Sync Depth Channel C Read Back, *Address 0xA7, [5:4]; Address 0xAA, [7:0]*
Function

HSD_CHC[9:0]	**Description**
xx xxxx xxxx	Readback value of measured horizontal sync depth on channel C (before gain multiplier). The value is presented in standard binary form.

HSD_FB[11:0] Horizontal Sync Depth Channel A Read Back, *Address 0xAB, [3:0]; Address 0xAC, [7:0]*

Function

HSD_FB[11:0]	**Description**
xx xxxx xxxx	Readback value of measured horizontal sync depth on channel A (after gain multiplier) for external feedback loop. The value is presented in twos complement form. This means that only a standard adder is needed to subtract the actual horizontal sync depth (as per HSD_FB) from a nominal value, as the HSD_FB value is already in negative format.

7.7.2 Manual Gain Control

The automatic gain control (AGC) can be completely disabled by setting the gain control block into a manual mode. By setting the GAIN_MAN bit, the gain factors for channels A, B and C are no longer taken from the AGC, but are replaced by three dedicated I^2C registers.

Using these factors with the HSD_FB[9:0] register, it is possible to implement an off-chip AGC if desired. The range for the gain is [0…1.998047].

$$X\_GAIN[9:0] = \text{int}(Gain * 512)$$

Equation 6: CP Manual Gain

Example:

Example Gain$_{dec}$	**Shifted**	**Integer**	**A_GAIN[9:0]**
0.98887	0.98887 * 512 = 506.30144	506	0x1FA
1.9980	1.9980 * 512 = 1022.976	1023	0x3FF

GAIN_MAN Manual Gain Control Enable (CP), *Address 0x73, [7]*

Function

GAIN_MAN	Description
0 ⊂	Gain factors for all three channels are generated by the AGC
1	The gains for the three channels are set by A_GAIN[9:0], B_GAIN[9:0] and C_GAIN[9:0]

A_GAIN[9:0] Manual Gain Value for Channel A (CP), *Address 0x73, [5:0]; Address 0x74, [7:4]*

Function

A_GAIN[9:0]	Description
xx xxxx xxxx	Sets the manual gain for the signal in channel A

B_GAIN[9:0] Manual Gain Value for Channel B (CP), *Address 0x74, [3:0]; Address 0x75, [7:0]*

Function

B_GAIN[9:0]	Description
xx xxxx xxxx	Sets the manual gain for the signal in channel B

C_GAIN[9:0] Manual Gain Value for Channel C (CP), *Address 0x75, [1:0]; Address 0x76, [7:0]*

Function

C_GAIN[9:0]	Description
xx xxxx xxxx	Sets the manual gain for the signal in channel C

7.7.3 Manual Gain FILTER Mode

The ADV7181C provides a special filter option for the manual gain mode. This is functional only when manual gain is enabled. The purpose of this filter is a smoothing mechanism when the manual gain value is continuously updated by an external system based on either external or readback conditions in the ADV7181C. The filter designed is an IIR filter with a transfer function of the form:

$$Y_N = (1-A)*Y_{N-1} + A*X_N$$

where A is the filter coefficient.

The values possible for A can vary from 1 (no filtering) to 1/128K. The value of coefficient A is chosen by programming CP_GAIN_FILT[3:0], as shown below.

CP_GAIN_FILT[3:0] Manual Clamp Filtering Modes, *Address 0x84, [7:4]*

Function

C_GAIN_FILT[3:0]	**Description**	**Time Constant**
0000	No filtering, i.e. Coefficient A = 1	Approx. 1/256 sec for SD
0001	Coefficient A = 1/128 Lines	Approx. 1/128 sec for SD
0010	Coefficient A = 1/256 Lines	Approx. 1/64 sec for SD
0011	Coefficient A = 1/512 Lines	Approx. 1/32 sec for SD
0100	Coefficient A = 1/1024 Lines	Approx. 1/16 sec for SD
0101	Coefficient A = 1/2048 Lines	Approx. 1/8 sec for SD
0110	Coefficient A = 1/4096 Lines	Approx. ¼ sec for SD
0111	Coefficient A = 1/8192 Lines	Approx. ½ sec for SD
1000	Coefficient A = 1/16K Lines	Approx. 1 sec for SD
1001	Coefficient A = 1/32K Lines	Approx. 2 sec for SD
1010	Coefficient A = 1/64K Lines	Approx. 4 sec for SD
1011	Coefficient A = 1/128K Lines	Approx. 8 sec for SD
1100-1111	Reserved for future use	----------

7.7.4 CP Peak Active Video Readback

The ADV7181C provides circuitry that monitors the active CP video on a field basis and records the largest value encountered during this time. It is intended to be used in a peak-white type AGC for signals that do not have an embedded horizontal sync pulse, and to provide feedback on the accurate function of the built-in AGC loop.

The ADV7181C itself does **not** provide a peak-white AGC. It merely monitors the input signal for the largest data value encountered in each of the three channels and presents those three values for readback via the I²C. The values are given in an unsigned format. There is no averaging or filtering before the peak detection.

$$(Peak\ video\ ampl - Clamp\ level) \times \left(\frac{4096}{1600}\right) \times CSC\_gain \times agc\_gain \times \left(\frac{1}{8}\right)$$

Equation 7: Peak Readback Value Equation

Example:

For: Peak voltage = 2.49V
Clamp level = 1.7V
CSC gain = 0.5
Manual gain = 5.469

it works out as:

$$(2490 - 1700) \times \left(\frac{4096}{1600}\right) \times 0.5 \times 0.569 \times \left(\frac{1}{8}\right) = 71.92\ dec = 47\ hex$$

Notes:

- The measurement is taken on a field basis (from one vertical sync to the next). The read out at any time refers to the previous field, not necessarily the current one.
- The tap-off point for the measurement is right after the gain multipliers. This means that clamping and AGC/manual gain have an affect on the results.

PKV_CHA[9:0] Peak Video Value on Channel A Read Back (CP), *Address 0xAD, [5:4], Address 0xAE, [7:0]*

Function

PKV_CHA[9:0]	Description
xx xxxx xxxx	Maximum encountered signal level during active video on channel A within the last field

PKV_CHB[9:0] Peak Video Value on Channel B Read Back (CP), *Address 0xAD, [3:2], Address 0xAF, [7:0]*

Function

PKV_CHB[9:0]	Description
xx xxxx xxxx	Maximum encountered signal level during active video on channel B within the last field

PKV_CHC[9:0] Peak Video Value on Channel C Read Back (CP), *Address 0xAD, [1:0], Address 0xB0, [7:0]*

Function

PKV_CHC[9:0]	Description
xx xxxx xxxx	Maximum encountered signal level during active video on channel C within the last field

7.8 Component Processor Offset Block

The offset block consists of three independent adders, one for each channel. Using the OFFSET_A, B and C registers, a fixed offset value can be added to the data. The actual offset used can come from two different sources:

1. The ADV7181C includes an automatic selection of the offset value, dependent on the PRIM_MODE[3:0] and VID_STD[3:0] settings.
2. A manual, user-defined value can be programmed.

When the OFFSET_A, B and C registers contain the value 0x3FF (reset default), the offset used is determined using the automatic selection process. For any other value in the OFFSET_A, B and C registers, the automatic selection is disabled and the user-programmed offset value is applied directly to the video. Refer to the flowcharts in Figure 17 and Figure 18.

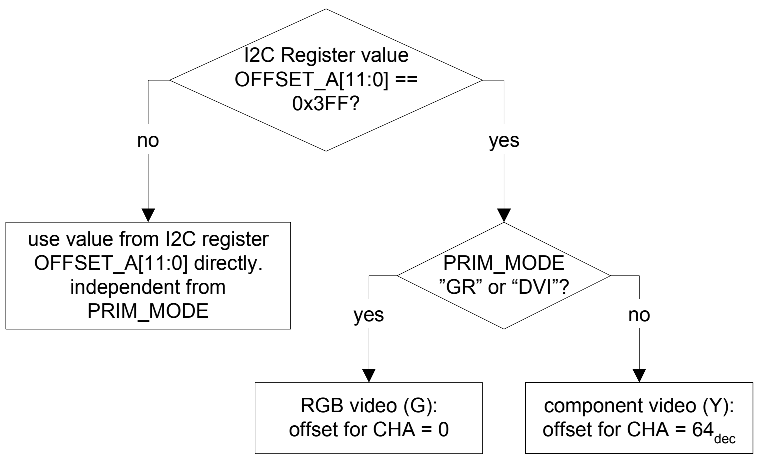


Figure 17: Channel A Automatic Value Selection

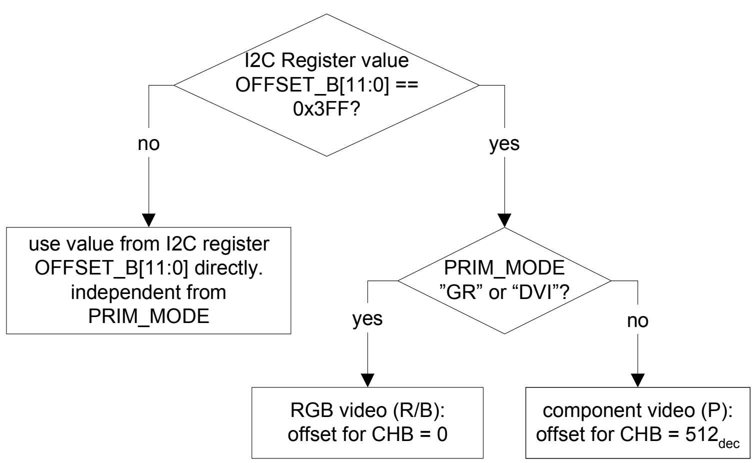


Figure 18: Channel B Automatic Value Selection

The selection process for channel C follows the same scheme and values as the channel shown in Figure 18.

In some applications, it is desirable to use the AGC to gain the signal to a smaller range, then use the Offset block to preserve the syncs (by 'lifting' the whole video signal up), and thus output the full digitized waveform (including syncs) within the 10-bit output range. For this application, the A/B/C_OFFSET[9:0] values are very important. Refer to AGC_TAR_MAN on page 53 for additional information.

For RGB type output data, the three offset values should be programmed to 0 or 64 (desired code output for black video). For YPbPr type output data, the A_OFFSET[9:0] should be set to 64 (desired code for black), the B_OFFSET[9:0] and C_OFFSET[9:0] (for Pr and Pb) are typically set to 512 (mid range).

Notes:

- Adding an excessive offset onto the data will result in clipping of the signal.
- The offset value can only be positive; it is an unsigned number.
- The offset values selected here only apply to active video. A separate control decides on the values to be written during the optional horizontal data blanking. (Refer to the information on BLANK_RGB_SEL on page 61.)
- ADV7181C employs sequencers for the offset values that prohibit intermediate wrong values to be applied. (Refer to the information on I^2C Sequencer in Section 11.)
- The I^2C sequencer treats the three offset values as separate entities. To update all three offset values, a single sweep of I^2C writes to CP Offset 1,2,3,4 is sufficient.

A_OFFSET[9:0] Channel A Offset (CP), *Address 0x77, [5:0]; Address 0x78, [7:4]*

Function

A_OFFSET[9:0]	Description
0x3FF	Adds value to digital data. Double buffering and I^2C sequencing applies by default.

Note: To change the A_OFFSET[9:0] value, register 0x77 and 0x78 must be written to in this order with **no** other I^2C access in between. (Refer to the information on I^2C Sequencer in Section 11.)

B_OFFSET[9:0] Channel B Offset (CP), *Address 0x78, [3:0]; Address 0x79, [7:2]*

Function

B_OFFSET[9:0]	Description
0x3FF	Adds value to digital data. Double Buffering and I^2C sequencing applies by default.

Note: To change the A_OFFSET[9:0] value, register 0x78 and 0x79 must be written to in this order with **no** other I^2C access in between. (Refer to the information on I^2C Sequencer in Section 11.)

C_OFFSET[9:0] Channel C Offset (CP), *Address 0x79, [1:0]; Address 0x7A, [7:0]*

Function

C_OFFSET[9:0]	Description
0x3FF	Adds value to digital data. Double Buffering and I^2C sequencing applies by default.

Note: To change the A_OFFSET[9:0] value, register 0x79 and 0x7A must be written to in this order with **no** other I^2C access in between. (Refer to the information on I^2C Sequencer in Section 11.)

7.9 CP Precision Bits

The two-bit control CP_PREC[1:0] selects rounding and truncation in the data path to 8, 9 or 10 bits. This must not be confused with the 'saturation=video function'. CP_PREC[1:0] controls rounding and truncation of the data within each channel to the specified bit width; it does not change the data level, only the precision (number of bits).

Note: Refer to the description of CPOP_SEL[3:0] for information on the output pins.

CP_PREC[1:0] Data Precision Control (CP), *Address 0x77, [7], [6]*

Function

CP_PREC[1:0]	Description
00	Rounds and truncates data in channels A, B and C to 10-bit precision
01	Rounds and truncates data in channels A, B and C to 9-bit precision
10	Rounds and truncates data in channels A, B and C to 8-bit precision
11	Rounds and truncates data in channels A, B and C to 8-bit precision

7.10 AV Code Block (CP)

The AV Code Block is used to insert AV codes into the video data stream. The codes follow the standards as outlined in **ITU-R BT.656-**4 and similar.

The following functions are supported by this block:

- The AV Code insertion can be enabled or disabled.
- Data between the EAV (end of active video) and SAV (start of active video) can be blanked, e.g. overwritten with default values. This function can be enabled or disabled. Also, the default blanking value can be set for RGB or YPbPr.
- The AV codes can be output on all channels or spread across the Y and PrPb buses for 20-bit output modes (refer to Figure 19).
- The F and V bits within the codes can be inserted directly or can be inverted before insertion.
- The position of the codes within the data stream (timing of the insertion) can be set to a default or can be slaved off the HS pin.

The insertion point for the AV codes is predetermined by default and is adjusted automatically to suit the current video standard as per the PRIM_MODE[3:0] and VID_STD[3:0] settings. To cater for non-standard signals, however, the AV code insertion point can also be taken off the HS signal before it goes to the pin. This gives the user great flexibility since the HS signal position can be programmed to quite a wide range with LLC accuracy.

AV_CODE_EN AV Code Insertion Enable (CP), *Address 0x7B, [1]*
Function

AV_CODE_EN	Description
0	Do not insert AV codes into the data stream
1 ⊂	Enables the insertion of AV codes

AV_POS_SEL Select AV Code Position(CP), *Address 0x7B, [2]*
Function

AV_POS_SEL	Description
0	Inserts SAV code at the falling edge of the HS signal and the EAV code at the rising edge of the HS signal. Note that the polarity control for the HS signal (PIN_inv_HS) has an effect on the positioning of the AV codes.
1 ⊂	Uses predetermined (default) position for AV codes.

AV_inv_V Invert V Bit in AV Code (CP), *Address 0x7B, [6]*
Function

AV_inv_V	Description
0 ⊂	Inserts V bit with default polarity
1	Inverts V bit before inserting it into the AV code

AV_inv_F Invert F Bit in AV Code (CP), *Address 0x7B, [7]*
Function

AV_inv_F	Description
0 ⊂	Inserts F bit with default polarity
1	Inverts F bit before inserting it into the AV code

AV_BLANK_EN Data Blanking Enable (CP), *Address 0x7B, [3]*
Function

AV_BLANK_EN	Description
0	Output clamped and gained data during the horizontal and vertical blanking time
1 ⊂	Replaces data in horizontal and vertical blanking period with default values

BLANK_RGB_SEL Select Blank Value RGB (CP), *Address 0x7B, [0]*
Function

BLANK_RGB_SEL	Description
0 ⊂	Blank values are: channel A (Y) = 64dec, channel B and C (Pr and Pb) = 512dec.
1	Blank values are: channel A, B and C = 64dec.

CP_DUP_AV Duplicate AV Code (CP), *Address 0x7B, [4]*
Function

CP_DUP_AV	Description
0	Spreads AV code over channel A and channel B (refer to Figure 19)
1 ⊂	Outputs AV code on channel A and duplicate on channel B (refer to Figure 19)

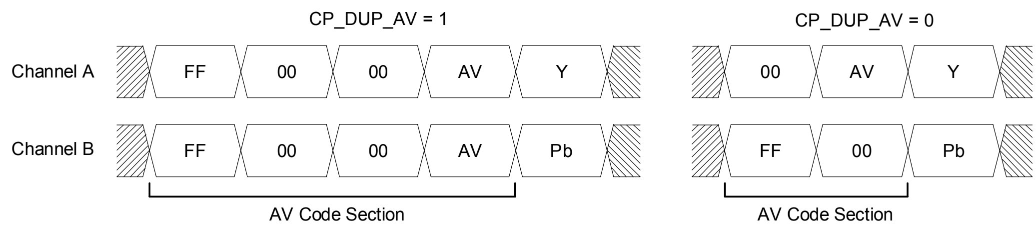


Figure 19: AV Code Output Options (CP)

7.11 Synchronization Source Polarity Detector

When processing component video signals, there are three possible sources for synchronization information from which the ADV7181C can extract timing:

- Embedded Sync as part of the input video signal, e.g. SOG/SOY
- External HS and VS as logic signals via HS_IN and VS_IN pins
- External CS (composite sync) as logic signal, via the HS_IN pin

The ADV7181C employs an SSPD block to enable it to determine where the sync source comes from and what polarity they are, in the case of external logic signals syncs such as HS and VS.

The functions of the SSPD block are:

- Automatic detection of the active sync source
- Automatic detection of the sync polarity, if applicable
- Readback on sync source and polarity detection
- Manual override for sync source via SYN_SRC[1:0]
- Manual override for polarity detection via POL_MAN_EN

The SSPD block can either operate in continuous or in single-shot mode. Continuous mode means that the block permanently monitors the inputs and updates its outputs. In single-shot mode, the SSPD block waits for a 0 to 1 transition on the TRIG_SSPD bit before it scans the sync inputs once. Single-shot operation is useful to avoid system scheduling conflicts.

The SSPD state machine searches for active sync signals in the following order of priority:

1. External HS/VS
2. External CS
3. Embedded Sync

If external HS/VS are found, the block decides on the sync polarity based on a measurement of the mark-space ratio of the HS/VS signals detected. The results from the SSPD detection are read back, but only after they are flagged as valid by the SSPD_DVALID flag. Refer to Figure 20 for information on the data exchange.

The following readback information is available from SSPD over I^{2}C:

- Active sync source (either result back from manual setting or result from autodetection)
- Activity report on the HS and VS pins
- Detected polarity on HS and VS

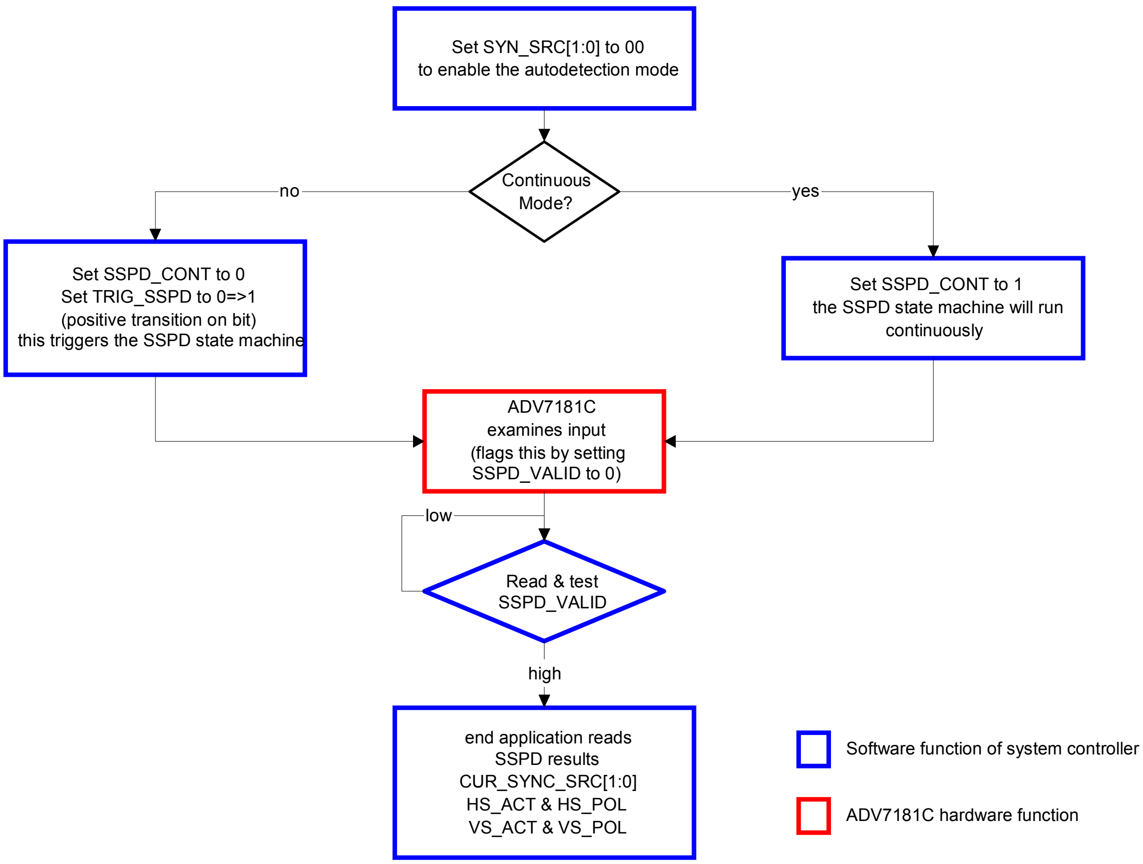


Figure 20: SSPD Autodetection Flowchart

Notes:

- Refer also to Section 7.4.3.
- The SSPD block actually decides on the sync signal routing in the chip. For example, if the automatic detection resulted in a detected external CS present, the ADV7181C configures itself automatically to actually use this CS signal. This is contrary to the function of the STDI block, which only measures and reports the results back.
- To select a sync source manually, use the SYN_SRC[1:0] settings.
- Ensure that the SOG_SEL bit (register 0xC4, bit 6) is set to zero.
- It must be noted that **all** readbacks (including the activity reports on HS and VS) depend on the SSPD state machine being triggered.

In other words, if activity was detected previously on an HS signal and a cable is unplugged, the state of the HS_ACT bit will not change until the SSPD state machine has been triggered again via the TRIG_SSPD bit when in non-continuous mode.

SSPD_CONT Sync Source and Polarity Detector Continuous Mode (CP), *Address 0x85, [1]*
Function

SSPD_CONT	Description
0	SSPD only works in one-shot mode (triggered by a 0 to 1 transition on the TRIG_SSPD bit)
1 ⊂	SSPD works continuously

TRIG_SSPD Trigger Sync Source and Polarity Detector (CP), *Address 0x85, [2]*
Function

TRIG_SSPD	Description
0 ⊂	A 0 to1 transition on the TRIG_SSPD bit causes the SSPD block to examine the currently presented sync signals. The TRIG_SSPD bit is **not** self-clearing – it must be reset by the user to prepare for the next trigger.
1	

SYN_SRC[1:0] SSPD Sync Source Selection (CP), *Address 0x85, [4:3]*
Function

SYN_SRC[1:0]	Description
00 ⊂	Autodetect mode for sync source – uses results of autodetection for sync signal routing. The result can be read back via the CUR_SYN_SRC[1:0] bits.
01	Manual setting: separate HS and VS on the respective pins.
10	Manual setting: external CS on the HS pin.
11	Manual setting: embedded sync on SOG/SOY (SOG or SOY dependent on input channel routing).

POL_MAN_EN Manual Overwrite for Polarity Detection SSPD (CP), *Address 0x85, [7]*
Function

POL_MAN_EN	Description
0 ⊂	Used result from SSPD polarity autodetection.
1	Manual overwrite: used POL_VS and POL_HS for polarity of HS/VS inputs. **Note:** POL_VS only operational when DS_OUT is set to a logic 1.

POL_VS Manual Overwrite for Polarity of VS SSPD (CP), *Address 0x85, [6]*
Function

POL_VS[1]	Description
0	VS pin carries negative polarity signal. For this bit to become active, the POL_MAN_EN bit must be set high.
1	VS pin carries positive polarity signal. For this bit to become active, the POL_MAN_EN bit must be set high.

[1] POL_VS is only operational when DS_OUT is set to logic 1.

POL_HS Manual Overwrite for Polarity of HS SSPD (CP), *Address 0x85, [5]*
Function

POL_HSCS	Description
0	HS pin carries negative polarity signal (HS or CS). For this bit to become active, the POL_MAN_EN bit must be set high.
1	HS pin carries positive polarity signal (HS or CS). For this bit to become active, the POL_MAN_EN bit must be set high.

7.11.1 SSPD Readback Signals

SSPD_DVALID SSPD Read Back Values Valid Read Back (CP), *Address 0xB5, [7]*
Function

SSPD_DVALID	Description
0	SSPD results not valid for readback
1	SSPD results valid (detection finished)

CUR_SYN_SRC[1:0] Current Sync Source Selection SSPD Read Back (CP), *Address 0xB5, [1:0]*
Function

CUR_SYN_SRC[1:0]	Description
00	Not used – not possible.
01	Separate HS and VS on the respective pins used.
10	External CS on the HS pin used.
11	Embedded sync on SOG/SOY used. (SOG or SOY dependent on input channel routing.)

CUR_POL_HS Currently Detected Polarity of HS SSPD (CP), *Address 0xB5, [3]*
Function

CUR_POL_HS	Description
0	HS pin carries negative polarity signal (HS or CS)
1	HS pin carries positive polarity signal (HS or CS)

HS_ACT Activity of HS SSPD (CP), *Address 0xB5, [4]*
Function

HS_ACT	Description
0	No activity detected
1	HS pin carries an active signal

CUR_POL_VS Currently Detected Polarity of VS SSPD (CP), *Address 0x B5, [5]*
Function

CUR_POL_VS	Description
0	VS pin carries negative polarity signal
1	VS pin carries positive polarity signal

VS_ACT Activity of VS SSPD (CP), *Address B5, [6]*
Function

VS_ACT	Description
0	No activity detected
1	VS pin carries an active signal

7.12 External Digital Synchronization Input Pins (CP)

The synchronization signals HS/VS can have low amplitude levels. The SYN_LOTRIG bit allows the user to reduce the threshold for those two inputs so that HS/VS signals with only 1.0 V amplitude can be accommodated. Refer to information on POL_VS on page 64, POL_HS on page 65, and POL_MAN_EN on page 64 for the manual control of the polarity of HS, CS and VS digital input signals.

SYN_LOTRIG External Sync Input Trigger Level, *Address 0x69, [6]*
Function

SYN_LOTRIG	Description
0 ⊂	Trigger level set for 3.3 V HS_IN/VS_IN pins (threshold approximately 1.5 V)
1	Trigger level set to cater for 1.0 V HS/VS pins (threshold approximately 0.6 V)

7.13 CP Output Synchronization Signal Positioning

The ADV7181C CP can output three primary and two secondary synchronization signals, as follows:

Primary:

- Horizontal synchronization timing reference output on the HS pin
- Vertical synchronization timing reference output on the VS pin
- Field timing reference output on the FIELD/DE pin, shared with the Data Enable (DE) timing reference output on the FIELD/DE

Secondary:

- Composite Synchronization (CS) timing reference output shared with the HS pin
- Data Enable, DE, (indicates active region) shared with the FIELD pin

Timing reference signals with shared pins are controlled via I^2C.

Table 12: CP Synchronization Signal Output Pins

Pin Name	Primary Signal (Default)	Secondary Signal	Controlled by I^2C Bit
HS	HS out	CS out	HS_OUT_SEL
FIELD	FIELD out	DE out	F_OUT_SEL

7.13.1 CP Primary Synchronization Signals

The three primary synchronization signals have certain default positions, depending on the video standard in use.

To allow for a glueless interface to downstream ICs, there is the facility to adjust the position of edges on the three primary sync signals. Refer to Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, Figure 26, and Figure 27, which show the nominal position of HS, VS and FIELD. The positions of those signals can be adjusted in both directions by using the following I^2C control bits:

- START_HS[9:0]
- END_HS[9:0]
- START_VS[3:0]
- END_VS[3:0]
- START_FE[3:0] (Start Field Even)
- START_FO[3:0] (Start Field Odd)

The START_xx and END_xx parameters are given as signed values. This means that rather than adjusting the absolute position of a signal, these adjustments allow the user to advance (negative value) or delay (positive value) the respective timing reference signals.

In addition, the polarity of the three primary and the two secondary sync signals can be inverted by using:

- PIN_IN_HS (also affects CS)
- PIN_INV_VS
- PIN_INV_F (also affects DE)

7.13.2 HS Timing Controls (CP)

Programming the registers listed in this section, the HS signal as shown in Figure 21 can be adjusted in the described manner.

Table 13: HS Default Timing (CP)

Symbol	Characteristic	Units	Note	525i	625i	525p	625p	720p	1080i
a	HSYNC to Start of Active Video		Default	118	128	116	126	256	188
				All values are for 1x outputs					
	START_HS Delay Range Max.			511	511	511	511	511	511
	START_HS Advance Range Max.	LLC1*		512	512	512	512	512	512
	END_HS Delay Range Max.			511	511	511	511	511	511
	END_HS Advance Range			512	512	512	512	512	512

Symbol	Characteristic	Units	Note	525i	625i	525p	625p	720p	1080i
	Max.								
d	HSYNC Width		Default	64	64	64	64	40	44
b	Active Video Samples			720	720	720	720	1280	1920
c	Total Samples/Line			858	864	858	864	1650	2200/ 2376

* $\frac{1}{LLC1}$ in Standard Definition 16-bit mode = $\frac{1}{13.5MHz}$ = 74ns.

$\frac{1}{LLC1}$ in Progressive Scan mode = $\frac{1}{27MHz}$ = 37ns.

$\frac{1}{LLC1}$ in High Definition mode = $\frac{1}{74.25MHz}$ = 13ns.

Symbols a, b, c, d refer to parameters in Figure 21.

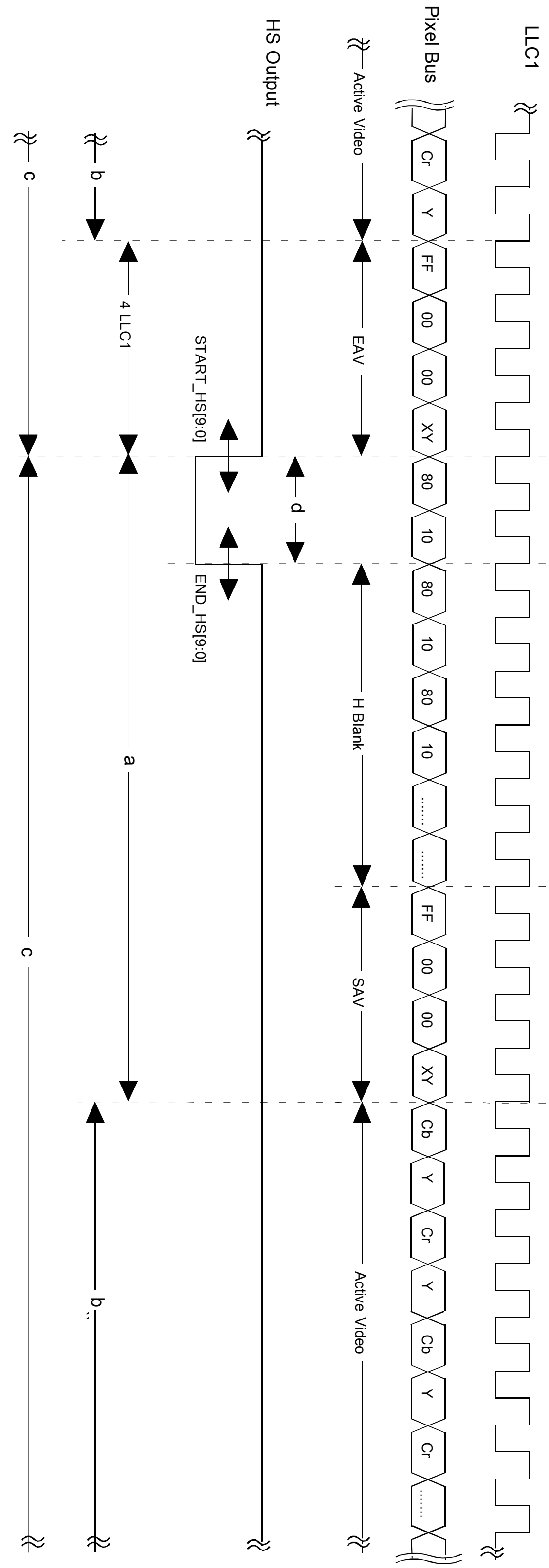


Figure 21: HS Timing (CP)

START_HS[9:0] Start HS Signal (CP), *Address 0x7C and 0x7E, [3:2] and [7:0]*

This word operates in a two's complement mode. Shifting the HS towards active video is achieved by selecting from the range 0x000 to 0x1FF. Shifting HS away from active video is achieved by selecting from the range 0x200 to 0x3FF. One lsb increment is equivalent to $\frac{1}{LLC1}$ sec.

Examples of how to control the begin of the HS timing signal:

START_HS[9:0]	Hex	Result	Note
0000000000b ⊂	0x000	No move	Default
0000000001b	0x001	1 x $\frac{1}{LLC1}$ sec shift later than default[1]	Minimum →
0100000000b	0x100	256 x $\frac{1}{LLC1}$ sec shift later than default	
0111111111b	0x1FF	511 x $\frac{1}{LLC1}$ sec shift later than default	Maximum →
1111111111b	0x3FF	1 x $\frac{1}{LLC1}$ sec shift earlier than default[2]	Minimum ←
1011111111b	0x3FE	256 x $\frac{1}{LLC1}$ sec shift earlier than default	
1000000000b	0x200	512 x $\frac{1}{LLC1}$ sec shift earlier than default	Maximum ←

P1P HS START closer to active video
P2P HS START away from active video

END_HS[9:0] END HS Signal (CP), *Address 0x7C and Address 0x7D, [1:0] and [7:0]*

This 10-bit word operates in a two's complement mode. Shifting the HS towards active video is achieved by selecting from the range 0x000 to 0x1FF. Shifting the HS away from active video is achieved by selecting from the range 0x200 to 0x3FF. One lsb increment is equivalent to $\frac{1}{LLC1}$ Sec.

Examples of how to control the end of the HS timing signal:

END_HS[9:0]	Hex	Result	Note
0000000000b ⊂	0x000	No move (default)	
0000000001b	0x001	1 x $\frac{1}{LLC1}$ sec shift later than default[1]	Minimum →
0100000000b	0x100	256 x $\frac{1}{LLC1}$ sec shift later than default	
0111111111b	0x1FF	511 x $\frac{1}{LLC1}$ sec shift later than default	Maximum →
1111111111b	0x3FF	1 x $\frac{1}{LLC1}$ sec shift earlier than default[2]	Minimum ←
1011111111b	0x3FE	256 x $\frac{1}{LLC1}$ sec shift earlier than default	
1000000000b	0x200	512 x $\frac{1}{LLC1}$ sec shift earlier than default	Maximum ←

P1P closer to active video P2P away from active video

PIN_INV _HS Polarity of HS Signal (CP), *Address 0x7C, [7]*

PIN_INV _HS controls the polarity of the HS signal.

Polarity	Description
0	Positive polarity of HS
1	Negative polarity of HS

7.13.3 VS Timing Controls (CP)

Programming of the VS timing signals is listed in this section. The VS signal is shown in Figure 21 Figure 22, Figure 23, Figure 24, Figure 25, Figure 26, and Figure 27 and can be adjusted in the described manner.

Table 14: VS Default Timing (CP)

Characteristic	Units	Direction	525i	625i	525p	625p	720p	1080i
Start_VS Range Max	Lines	→	7	7	7	7	7	7
Start_VS Range Min	Lines	←	8	8	8	8	8	8
End_VS Range Max	Lines	→	7	7	7	7	7	7
End_VS Range Min	Lines	←	8	8	8	8	8	8

START_VS[3:0] Start VS Signal (CP), *Address 0x7F, [3:0]*

This 4-bit word operates in a two's complement mode. Shifting the VS start edge towards active video is achieved by selecting from the range 0x00 to 0x07. Shifting the VS start edge away from active video is achieved by selecting from the range 0x08 to 0x0F. One lsb increment is equivalent to a 1 line shift.

Examples of how to control the start of the VS timing signal:

START_VS	Hex	Result	Note
0000b	0x00	No move (default)	
0001b	0x01	1 HS shift later than default[1]	Minimum →
0011b	0x03	3 HS shift later than default	
0111b	0x07	7 HS shift later than default	Maximum →
1111b	0x0F	1 HS shift earlier than default[2]	Minimum ←
1101b	0x0D	3 HS shift earlier than default	
1000b	0x08	8 HS shift earlier than default	Maximum ←

[1]VS closer to start of active video
[2]VS away from start of active video

END_VS[3:0] End VS Signal (CP), *Address 0x7F, [7:4]*

This 4-bit word operates in a two's complement mode. Shifting the VS end edge towards active video is achieved by selecting from the range 0x00 to 0x07. Shifting the VS end edge away from active video is achieved by selecting from the range 0x08 to 0x0F. One lsb increment is equivalent to 1 line shift.

Examples of how to control the end of the VS timing signal:

End_VS	Hex	Result	Note
0000b ⟲	0x00	No move (default)	
0001b	0x01	1 HS shift later than default[1]	Minimum ⟶
0011b	0x03	3 HS shift later than default	
0111b	0x07	7 HS shift later than default	Maximum ⟶
1111b	0x0F	1 HS shift earlier than default[2]	Minimum ⟵
1101b	0x0D	3 HS shift earlier than default	
1000b	0x08	8 HS shift earlier than default	Maximum ⟵

[1]VS closer to start of active video
[2]VS away from start of active video

PIN_INV _VS Polarity of VS Signal (CP), *Address 0x7C, [6]*

PIN_INV _VS controls the polarity of the VS signal.

Polarity	Description
0	Positive polarity of VS
1⟲	Negative polarity of VS

7.13.4 FIELD Timing Controls (CP)

Programming of the FIELD timing signals is listed in this section. The FIELD[1] signal is shown in Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, Figure 26, and Figure 27 and can be adjusted in the described manner.

Table 15: FIELD Default Timing (CP)

Characteristic	Units	Direction	525i	625i	525p	625p	720p	1080i
START_FE START_FO Range Max	Line	→	7	7	N/A	N/A	N/A	7
START_FE START_FO Range Min	Line	←	8	8	N/A	N/A	N/A	8

[1] Progressive systems do not have a Field signal.

START_FE[3:0] Start FIELD Even Signal (CP), *Address 0x80, [7:4]*

This 4-bit word operates in a two's complement mode. Shifting the Start FIELD Even edge towards active video is achieved by selecting from the range 0x00 to 0x07. Shifting the Start FIELD Even edge away from active video is achieved by selecting from the range 0x08 to 0x0F. One lsb increment is equivalent to 1 line shift.

Examples of how to control the Even field section of the FIELD timing signal:

START_FE	**Hex**	**Result**	**Note**
0000b ⊂	0x00	No move (default)	
0001b	0x01	1 HS shift later than default[1]	Minimum →
0011b	0x03	3 HS shift later than default	
0111b	0x07	7 HS shift later than default	Maximum →
1111b	0x0F	1 HS shift earlier than default[2]	Minimum ←
1101b	0x0D	3 HS shift earlier than default	
1000b	0x08	8 HS shift earlier than default	Maximum ←

[1]Closer to active video
[2]Away from active video

START_FO[3:0] Start FIELD Odd Signal (CP), *Address 0x80, [3:0]*

This 4-bit word operates in a two's complement mode. Shifting the Start FIELD Odd edge towards active video is achieved by selecting from the range 0x00 to 0x07. Shifting the Start FIELD Odd edge away from active video is achieved by selecting from the range 0x08 to 0x0F. One lsb increment is equivalent to 1 line shift.

Examples of how to control the Odd field section of FIELD timing signal:

START_F0	**Hex**	**Result**	**Note**
0000b ⊂	0x00	No move (default)	
0001b	0x01	1 HS shift later than default[1]	Minimum →
0011b	0x03	3 HS shift later than default	
0111b	0x07	7 HS shift later than default	Maximum →
1111b	0x0F	1 HS shift earlier than default[2]	Minimum ←
1101b	0x0D	3 HS shift earlier than default	
1000b	0x08	8 HS shift earlier than default	Maximum ←

[1]Closer to active video
[2]Away from active video

PIN_INV_F Polarity of Field Signal (CP), *Address 0x7C, [5]*

PIN_INV_F controls the polarity of the FIELD signal.

Polarity	Description
0 ⊂	Interlaced video : FIELD signal low for Odd field, high for Even field Progressive video: FIELD signal permanently low
1	Interlaced video: FIELD signal high for Odd field, low for Even field. Progressive video: FIELD signal permanently high

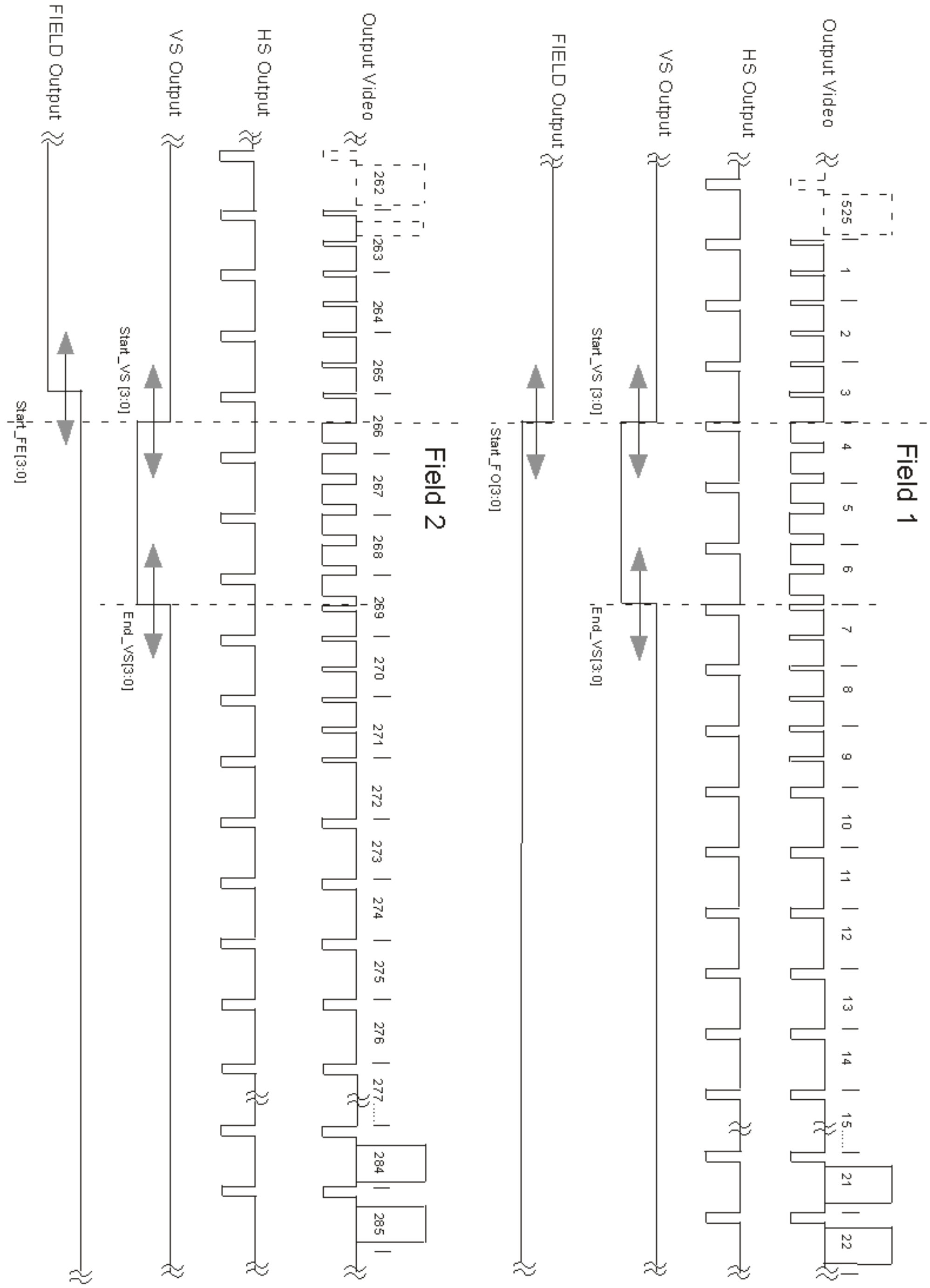


Figure 22: 525i VS Timing (CP)

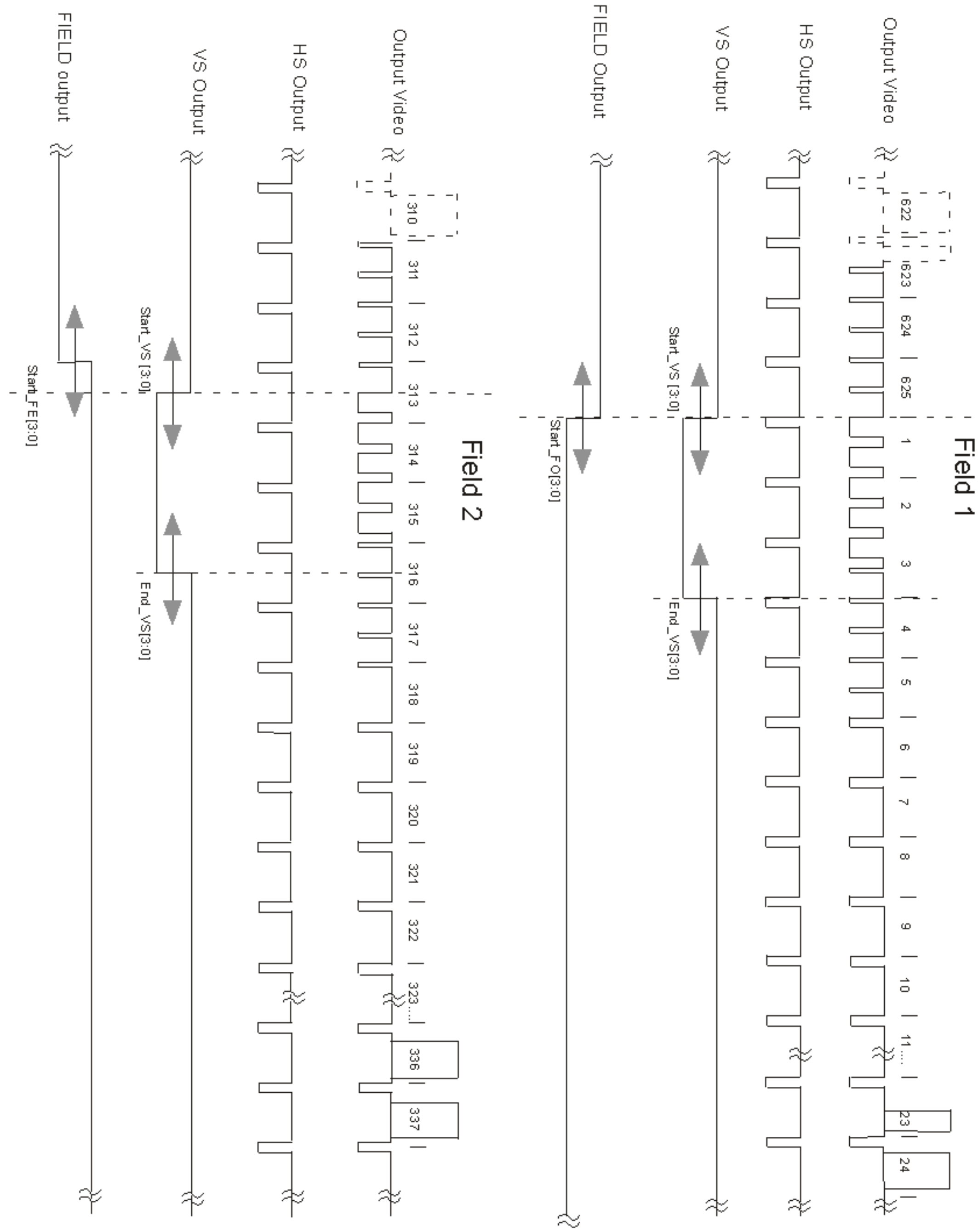


Figure 23: 625i VS Timing (CP)

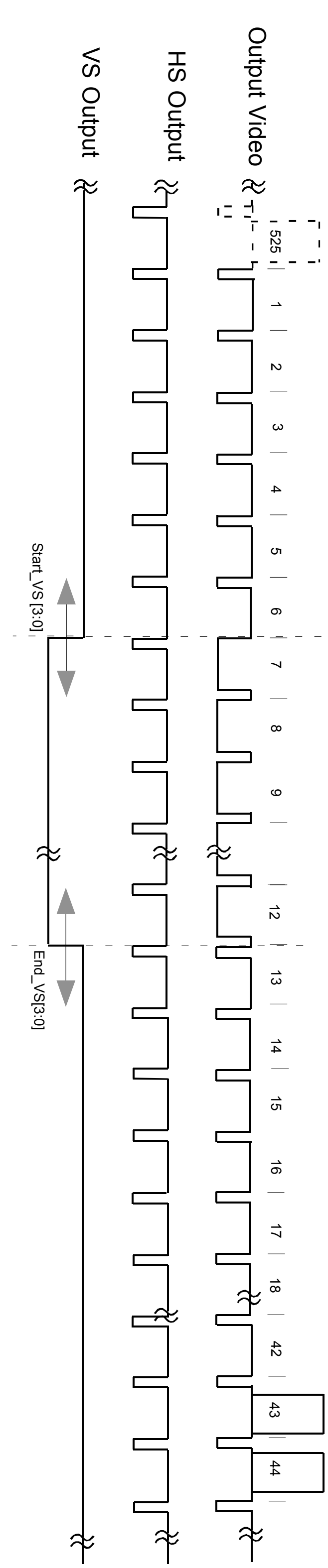


Figure 24: 525P VS Timing (CP)

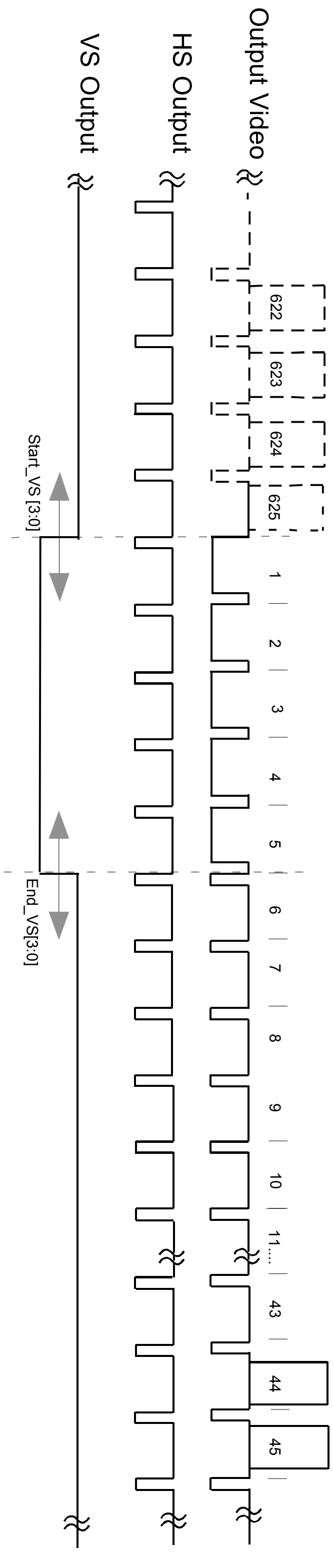


Figure 25: 625P VS Timing (CP)

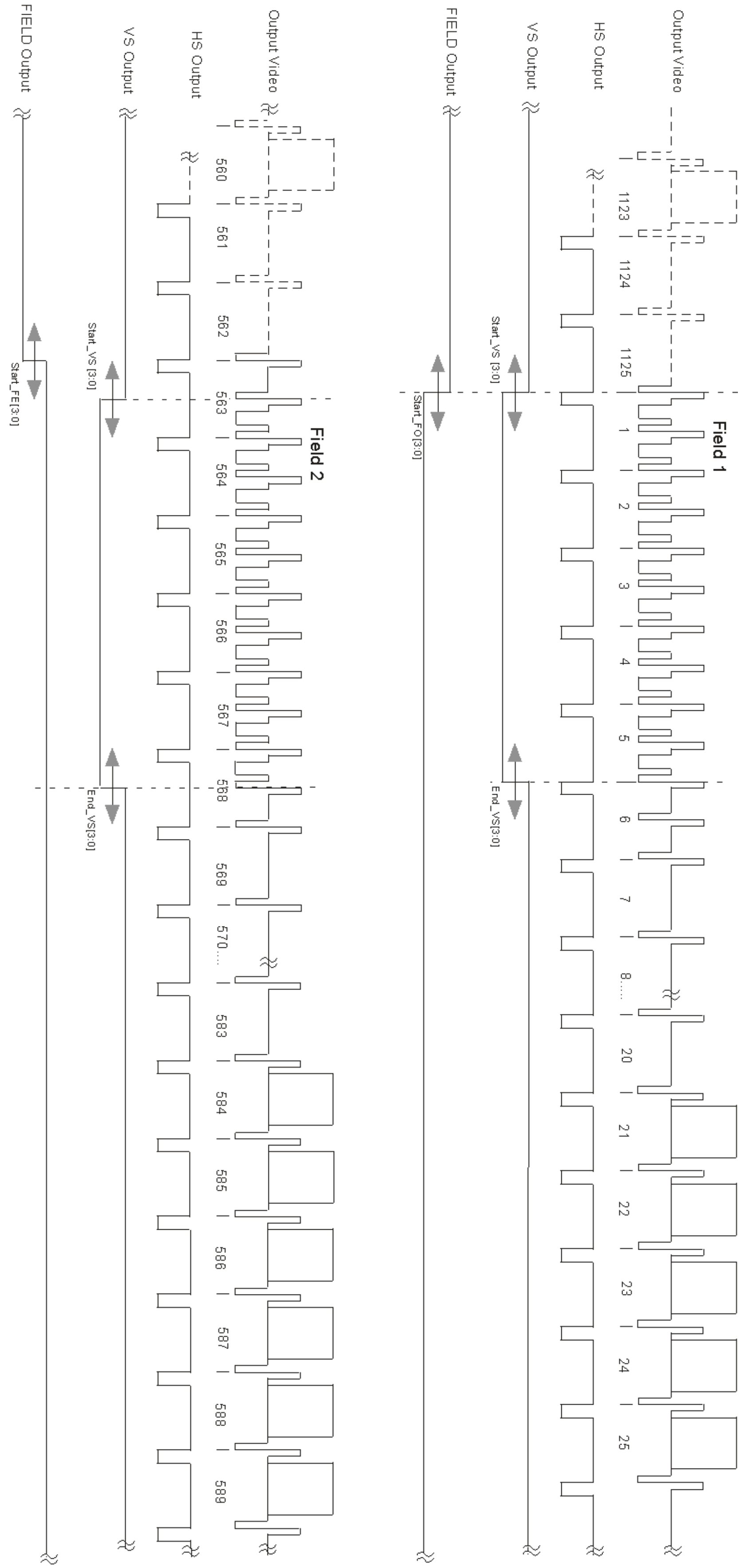


Figure 26: 1080i VS Timing (CP)

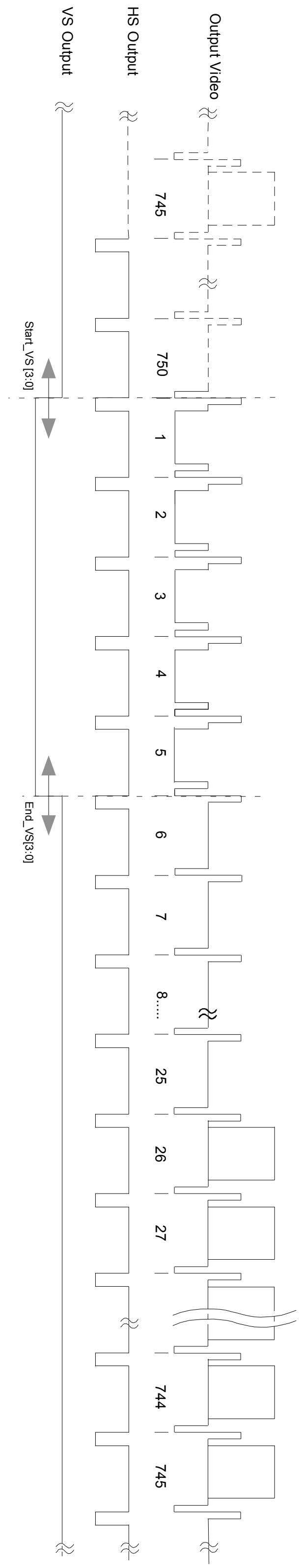


Figure 27: 720P VS Timing (CP)

7.13.5 240p, 540p, 1080p, and 1250p Support

INTLCD_240P_540P (CP), *Address 0x7B, [5]*

This bit decides if interlaced or progressive timing is output for a 240p/540p source.

Function

INTCLD_240P_540P	Description
0	Outputs interlaced timing – even field VSYNC transition is offset by a half line. Odd field VSYNC transition occurs at start of line.
1	Outputs progressive timing – even field VSYNC transition occurs at start of line. Odd field VSYNC transition occurs at start of line.

INTERLACED (CP), *Address 0x91, [6], Write only*

The user sets this bit to indicate whether the video signal input is to be 1080i or 1080p (at 25/30 Hz) or whether the input is to be 1250i or 1250p (at 25/30 Hz) for their respective PRIM_MODE[3:0] and VID_STD settings.

Function

INTERLACED	Description
0	Process 1080p/1250p (at 25/30Hz)
1	Process 1080i/1250i

7.13.6 Secondary Synchronization Signals (CP)

The secondary sync signals share their output pins with the primary ones, as shown in Table 12. The CS signal is a logic combination of HS and VS. Its polarity can be inverted using the PIN_INV_HS bit.

The DE signal allows the ADV7181C to interface gluelessly to a DVI transmitter. The DE signal marks active video on all active lines and could, therefore, also be described as an inverted blanking signal. The polarity of the DE signal can be changed by the PIN_INV_F bit.

Notes:

- The delay units are:
  - LLC1 clock cycles for HS. With nominal sampling, this is equivalent to pixels.
  - Video lines for VS and FIELD. These are obviously independent of the sampling rate, i.e. LLC1 clock speed.

- Synchronization information can also be passed on to downstream equipment by means of AV codes. There is an option in the AV code generation block that uses the position of the HS pin to trigger the insertion of SAV/EAV codes into the data stream.

7.13.7 Ancillary Synchronization Signal Output (CP)

The ADV7181C can provide ancillary synchronization information on the VS and the SFL pin. The following section describes the signals available. It should be noted that these signals are only available if the PRIM_MODE selection activates the CP core.

7.13.7.1 VS Pin

Figure 28 outlines the structure implemented in the ADV7181C. The signal sd_core_active is decoded off PRIM_MODE. A primary mode that activates the CP core must be selected for ancillary sync information to be output.

The DS_OUT bit then enables selection between a synchronous VS (synchronous to True Line Locked Clock) and an asynchronous version of the vertical sync. Depending on the application and the ultimate purpose of the timing signal, both of them can have distinct advantages:

- The **synchronous signals** can be captured with the TLLC clock. They accompany the data and determine the position of the vertical sync with pixel-accuracy. As a prerequisite, the TLLC clock must be locked and this requires PRIM_MODE, VID_STD and other I^2C registers to be configured correctly.
- The **asynchronous signals** are not aligned with the video pixel data. However, they are valid even if the TLLC is not locked to input video. For a digital VS input signal, the data path to the VS output pin is combinatorial. For embedded syncs, the vertical sync is extracted based on the 28.63636 MHz crystal clock. This makes both paths independent of the status of the TLLC clock. These synchronization signals can be used in a system that chooses to implement autodetection of the input video standard downstream with the use of a microprocessor.

The SSPD decides between embedded sync and digital input. Refer to Section 7.11 for further details.

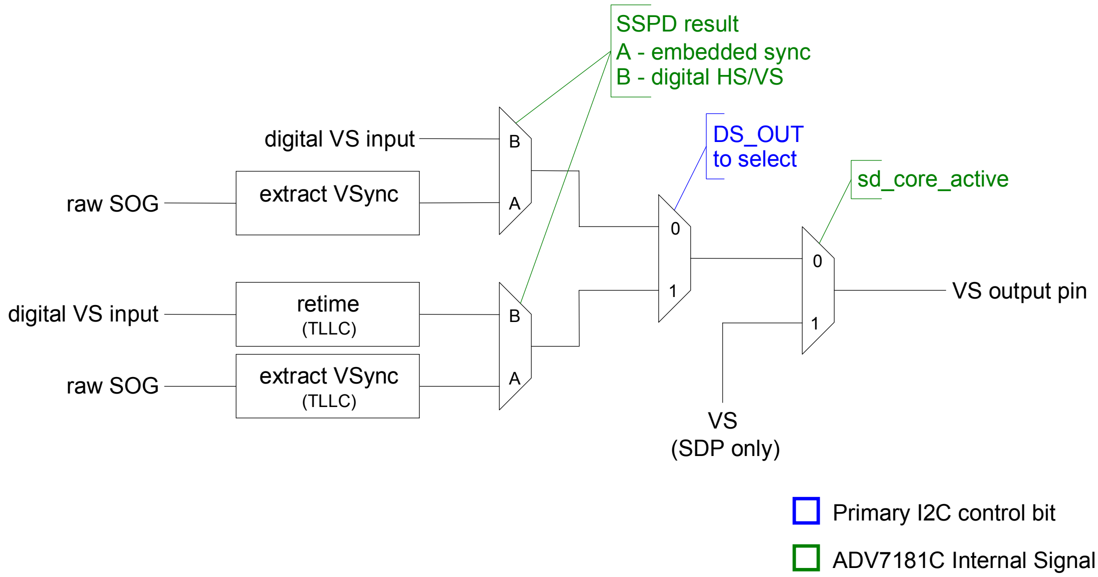


Figure 28: Ancillary Synchronization Information on VS Pin

7.13.7.2 SFL Pin (SDP and CP)

The ancillary synchronization information on the SFL pin is shown in Figure 29. Ancillary information can only be output if PRIM_MODE is programmed to activate CP (as shown by the sd_core_active signal, which is decoded from PRIM_MODE).

In PWRSAV mode, a logic combination of all possible synchronization signals is presented on the SFL pin. This enables a dynamic power-down system to be put in place. The activity signal, as shown, is intended to be used as a wake-up signal. While it will not be possible to determine easily the type of input signal (horizontal and vertical frequency) that is connected, the mere presence of synchronization information should be enough to trigger system operation.

The DS_OUT signal selects between the following signals:

- Asynchronous composite-style sync signal derived from either the digital HS and VS or the embedded sync (SOG). Macrovision impairments may be present.
- Sequence of generated horizontal sync pulses where Macrovision impairments, such as pseudo-sync pulses, have been removed.

Both signals are asynchronous in nature and do not follow fixed setup and hold time specifications with respect to the TLLC signal. They are based on either combinatorial signal paths through the ADV7181C or use digital logic that is driven off the 28.63636 MHz crystal clock. This makes them independent of the lock state of the TLLC.

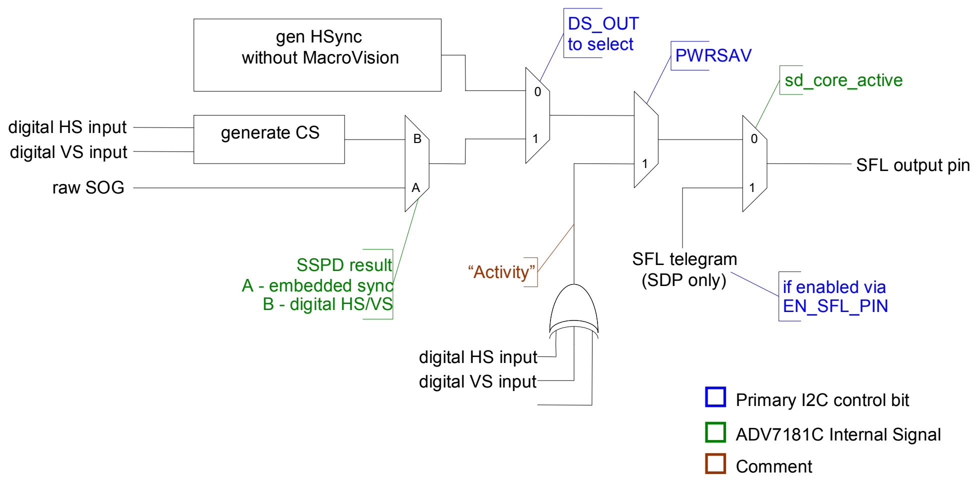


Figure 29: Ancillary Synchronization Information on SFL Pin

DS_OUT Digital Sync Output Selection (CP), *Address 0x85, [0]*

Refer to Section 7.13.7 for a detailed discussion on the function of the DS_OUT bit.

Function

DS_OUT	Description
0 ⊂	Outputs asynchronous VS
1	Outputs synchronous VS/asynchronous CS

7.14 Standard Detection and Identification

The standard detection and identification (STDI) block of the ADV7181C monitors the synchronization signals received on the SOY pin. STDI_LINE_COUNT_MODE must be set to 1 to enable the STDI block and achieve valid synchronization signal analysis. Four key measurements are performed:

- **Block Length BL[13:0]**
  This is the number of clock cycles in a block of eight lines. From this, the time duration of one line can be concluded. Note that the crystal frequency determines the clock cycle and that a crystal frequency of 28.63636 MHz should be used for the ADV7181C.
- **Line Count in Field LCF[10:0]**
  The LCF[10:0] readback value is the number of lines between two Vsyncs, that is, over one field.
- **Line Count in Vsync LCVS[4:0]**
  The LCVS[4:0] readback value is the number of lines within one Vsync period.
- **Field Length FCL[12:0]**
  This is the number of clock cycles in 1/256th of a field. Multiplying this value by 256 calculates the field length in clock cycles.

By interpreting these four parameters, it is possible to distinguish among the types of input signals.

A data valid flag, STDI_VALID, is provided that is held low during the measurements. The four parameters should only be read after the STDI_VALID flag has gone high. Refer to Table 16 for information on the readback values.

Notes:

- Types of synchronization pulses include horizontal synchronization pulses, equalization and serration pulses, and Macrovision pulses.
- Macrovision pseudo synchronization and AGC pulses are counted by the STDI block in normal readback mode. This does not prohibit the identification of the video signal.
- The ADV7181C only measures the parameters; it does not take any action based on these measurements. Therefore, the part helps to identify the input to avoid problems in the scheduling of a system controller, but it does not reconfigure itself.

STDI_DVALID, Standard Identification Data Valid Read Back, *Address 0xB1[7]*

Function

STDI_DVALID	Description
x	This bit is set by the ADV7181C as soon as the measurements of the STDI block are finished. A high level signals the validity of the BL, LCVS, LCF, and STDI_INTLCD parameters. To prevent false readouts, especially during the signal acquisition, the DVALID bit only goes high after recording four fields with the same length. As a result, the measurements can require up to five fields to finish.

STDI_LINE_COUNT_MODE, *Address 0x86[3]*

Function

STDI_ LINE_COUNT_ MODE	Description
0 ⊂	Disables the STDI functionality.
1	Enables STDI functionality. This enables valid readback of the STDI block registers.

BL [13:0], Block Length Readback, *Address 0xB1[5:0], Address 0xB2[7:0]*

Function

BL[13:0]	Description
xx xxxx xxxx	Number of clock cycles in a block of eight lines of incoming video. Data is only valid if STDI_DVALID is high.

LCVS [4:0], Line Count in Vsync Readback, *Address 0xB3[7:3]*

Function

LCVS[4:0]	Description
x xxxx	Number of lines within a vertical synchronization period. Data is only valid if STDI_DVALID is high.

LCF [10:0], Line Count in Field Readback, *Address 0xB3[2:0], Address 0xB4[7:0]*
Function

LCF[10:0]	Description
xx xxxx xxxx	Number of lines between two Vsyncs per one field/frame. Data is only valid if STDI_DVALID is high.

FCL [12:0], 1/256th of Field Length in Number of Crystal Clocks Read back, *Address 0xCA[4:0], Address 0xCB[7:0]*
Function

FCL[12:0]	Description
xxx	Number of crystal clocks (with the recommended 28.63636 MHz frequency) in 1/256th of a field. Data is only valid if STDI_DVALID is high.

7.14.1 STDI Readback Values for SD, PR, and HD

The readback values provided are only valid when using a crystal with the recommended 28.63636 MHz frequency.

Table 16: STDI Results for Video Standards (SD, PR, and HD)

Video Standard	BL [13:0]	LCF [10:0]	LCVS [4:0]
525i 60	14552 ± 80	261 ± 50	3 ± 3
240p 60	14552 ± 80	261 ± 50	2 ± 2
625i 50	14653 ± 80	311 ± 50	2 ± 2
288p 50	14654 ± 80	313 ± 50	2 ± 2
480p 60	7271 ± 40	524 ± 50	5 ± 2
720p 50	6101 ± 40	749 ± 50	4 ± 2
720p 60	5083 ± 40	749 ± 50	4 ± 2
1035i 30	6780 ± 40	562 ± 50	5 ± 2
1080i 25	7322 ± 40	1249 ± 50	0 ± 2
1080i 30	6780 ± 40	561 ± 50	4 ± 2
1080p 25	8137 ± 40	1124 ± 50	4 ± 2
1080p 50	4064 ± 40	1124 ± 50	4 ± 2
1080p 60	3385 ± 40	1124 ± 50	4 ± 2
1152i 50 Wide	7321 ± 40	623 ± 50	0 ± 2
1152i 50 Full	7321 ± 40	623 ± 50	4 ± 2

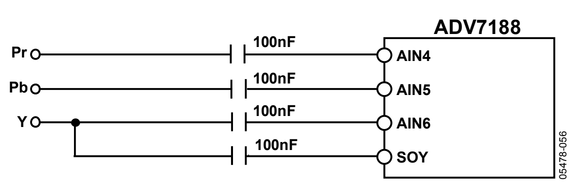


Figure 30: Example Connection of SOG/SOY Pin

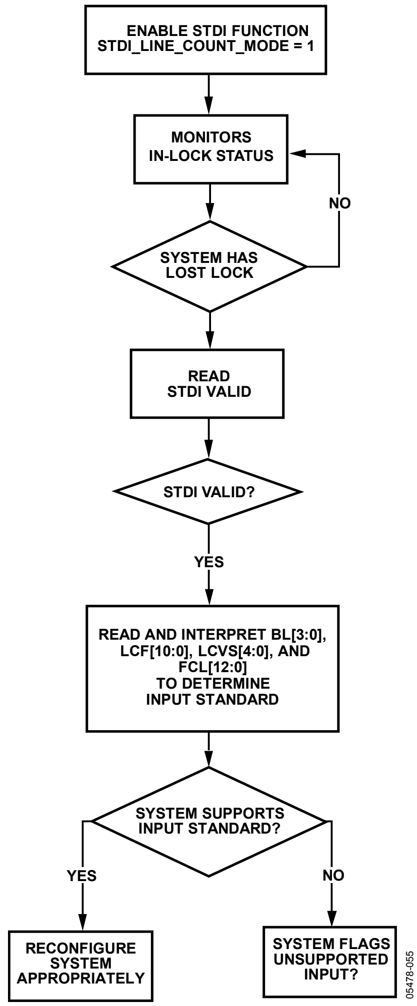


Figure 31: Example Use of STDI Block

7.15 Component Processor Horizontal Lock Status

The ADV7181C provides an I^2C readback value for the lock robustness. The measurement is based on an integration of the area of the horizontal sync that falls below the slicing threshold, as illustrated by Figure 32. The threshold level can be determined automatically or it can also be set by the customer via I^2C.

The quality of horizontal locking depends on the strength, i.e. depth, of the horizontal sync pulse. For shallow horizontal sync pulses, the area measured is going to be low and the locking is not as reliable as for a strong, i.e. deep, horizontal sync.

The number presented as ISD[8:0] is not intended to be an absolute measurement, but a relative one. A large value indicates robust locking; a small value shows an unreliable lock state. A system controller reading the ISD value via the I^2C interface must set appropriate thresholds for fully locked and partially locked.

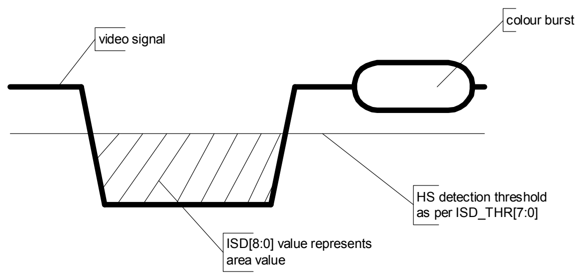


Figure 32: Synchronization Lock Robustness Measurement

The measurements are performed on a line-by-line basis on all video lines but not during the VBI. For video lines during the VBI, the result of the last active video line is kept.

The ISD[8:0] value changes dynamically on a line by line basis; the IFSD[8:0] is an averaged version of the ISD[8:0]. The averaging length can be set to 128 or 256 lines of video.

ISD_THR[7:0] ISD Threshold Value (CP), *Address 0x83, [7:0]*

Function

ISD_TH[7:0]	Description
00	The setting of 00 is special. A value of 00 causes the threshold to be calculated automatically. The threshold is set to (level of horizontal sync tip) + 0.5 * (horizontal sync depth).
All values other than 00	Slice level value is set to (ISD_THR[7:0] * 8) in a 12-bit data range.

IFSD_AVG ISD Averaging Selection (CP), *Address 0x84, [0]*

Function

ISFD_AVG	Description
0	ISD[8:0] is averaged over 128 lines of video to generate IFSD[8:0]
1	ISD[8:0] is averaged over 256 lines of video to generate IFSD[8:0]

ISD[8:0] ISD HLock Measurement Read Back (CP), *Address 0xA3, [0]; Address 0xA4, [7:0]*

Function

ISD[8:0]	Description
x xxxx xxxx	HLock measurement as defined above

IFSD[8:0] IFSD HLock Measurement Read Back (CP), *Address 0xA3, [1]; Address 0xA5, [7:0]*

Function

IFSD[8:0]	Description
x xxxx xxxx	Averaged version of ISD[8:0]. Refer to the description of IFSD_AVG on page 87 for information on the averaging function.

7.16 Component Processor VBI Data Support

The ADV7181C supports the decoding of CGMS-A for the following modes of operation:

Video Standard	CGMS-A Specification	Line Number for CGMS-A Data
480i	EIAJ CPR-1204	20 and 283 (Figure 33)
480P	EIAJ CPR-1204-1	41 (Figure 34)
720P	EIAJ CPR-1204-2	24 (Figure 35)
1080i	EIAJ CPR-1204-2	19 and 582 (Figure 36)

All VBI data registers are double buffered with the field signals. This means that data is extracted from the video lines and will appear in the appropriate I^2C registers with the next field transition. They will be static until the next field.

It is envisaged that the user starts an I^2C read sequence with VS, firstly examining the VBI Info register, address 0x90. It should be noted that the data registers are filled with decoded VBI data even if their corresponding detection bit is low. However, it is likely that bits within the decoded data stream are wrong.

CGMSD CGMS-A Sequence Detected (CP), *Address 0x90, [3]*

Logic 1 for this bit indicates that the data in the CGMS1, 2 and 3 registers is valid. The CGMSD bit goes high if a valid CRC checksum is calculated off a received CGMS packet.

Function

CGMSD	Description
0	No CGMS transmission detected, confidence low
1	CGMS sequence decoded, confidence high

CRC_ENABLE CRC CGMS-A Sequence (CP), *Address 0xB2, [2]*

For certain video sources, the CRC data bits can have an invalid format. In such circumstances the CRC checksum validation procedure is disabled. The CGMSD bit goes high if the rising edge of the start bit is detected within a time window.

Function

CRC_ENABLE	Description
0	No CRC check performed. The CGMSD bit goes high if the rising edge of the start bit is detected within a time window.
1	Uses CRC checksum to validate the CGMS-A sequence. CGMSD bit goes high for valid checksum, ADI recommended setting.

7.16.1.1 CGMS Data Registers

CGMS1[7:0] (CP), *Address 0x96, [7:0]*
CGMS2[7:0] (CP), *Address 0x97, [7:0]*
CGMS3[7:0] (CP), *Address 0x98, [7:0]*

Refer to Figure 33, Figure 34, Figure 35, and Figure 36 to see the bit correspondence between the analogue video waveform and the CGMS1/2/3 registers. CGMS3[7:4] are undetermined and should be masked out by software.

Access Information					
Signal Name	**Block**	**Register Location**	**Address**		**Register Default Value**
CGMS1[7:0]	SDP/CP	CGMS 1 [7:0]	150_d	0x96	(Readback only)
CGMS2[7:0]	SDP/CP	CGMS 2 [7:0]	151_d	0x97	(Readback only)
CGMS3[3:0]	SDP/CP	CGMS 3 [3:0]	152_d	0x98	(Readback only)

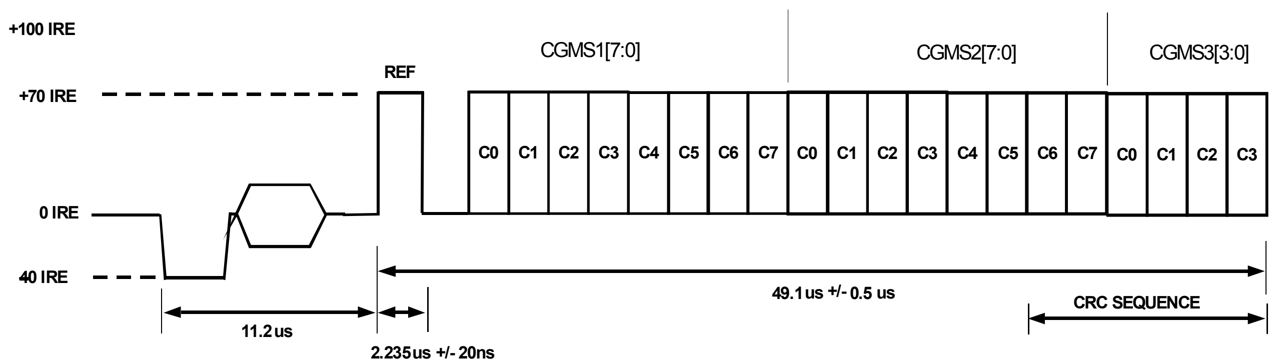


Figure 33: CGMS-A Waveform 480i

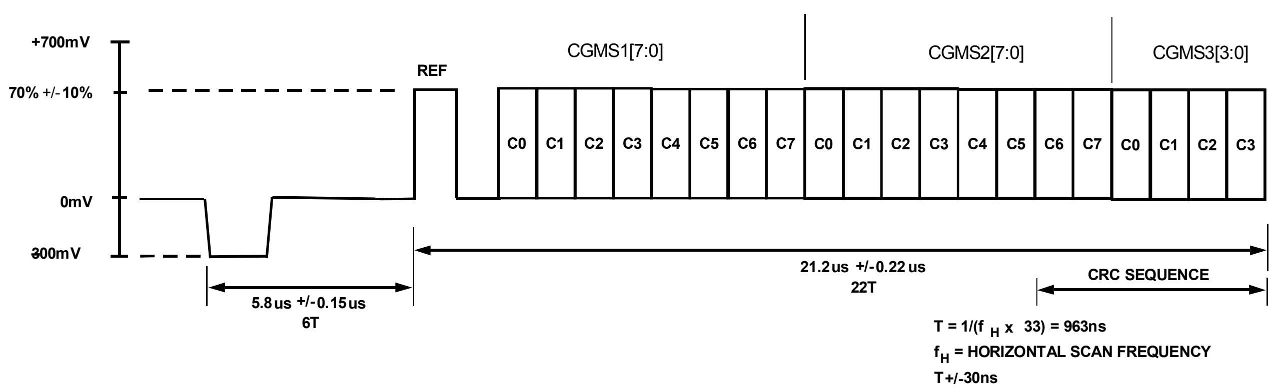


Figure 34: CGMS-A Waveform 480P

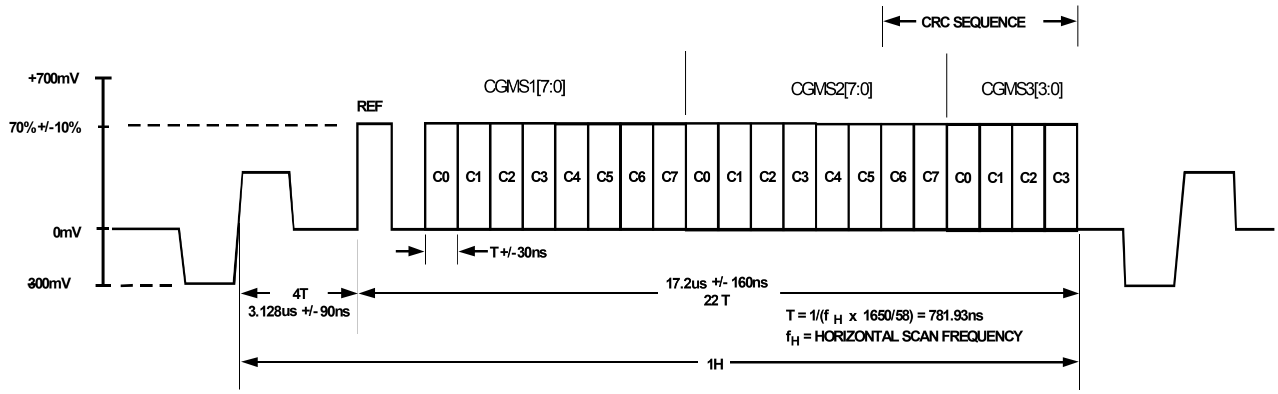


Figure 35: CGMS-A Waveform 720P

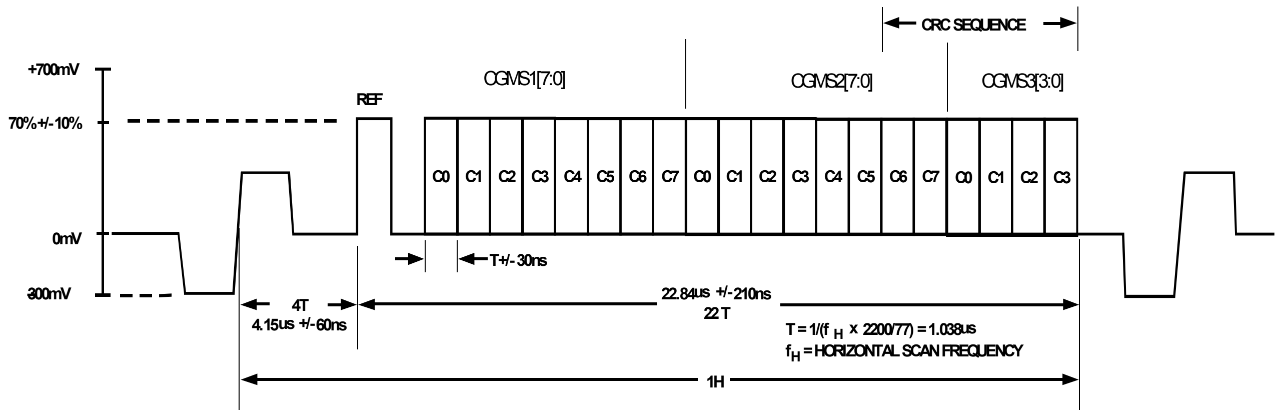


Figure 36: CGMS-A Waveform 1080i

8 Standard Definition Processor

A block diagram of the ADV7181C Standard Definition Processor (SDP) is provided in Figure 37.

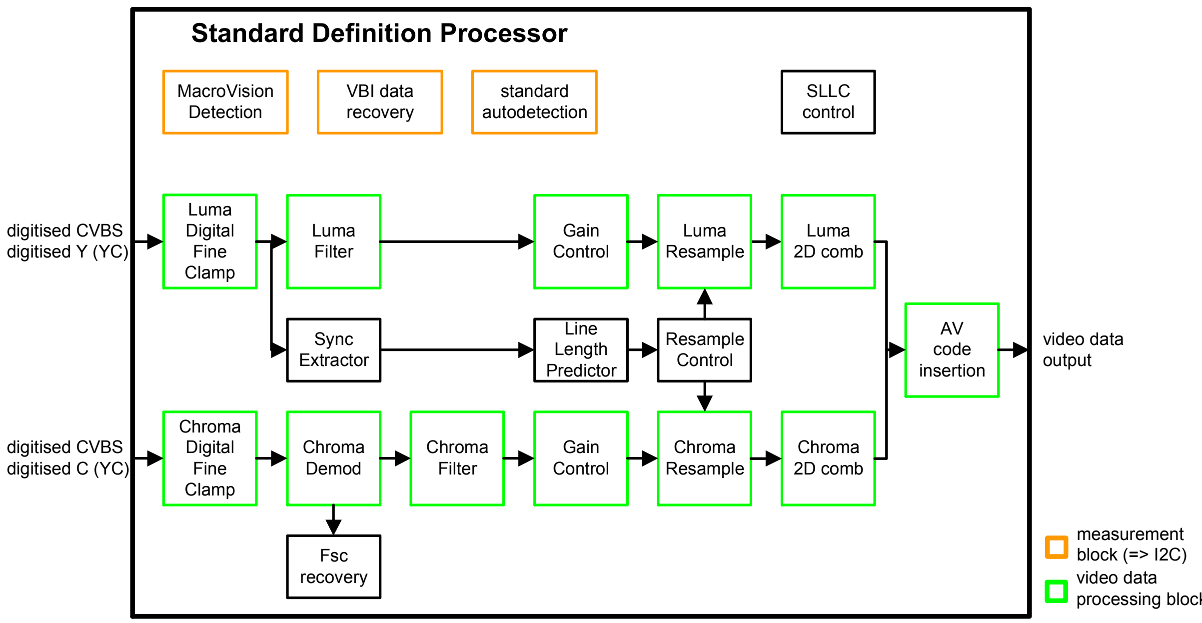


Figure 37: Block Diagram of Standard Definition Processor

The SDP block can handle standard definition video in CVBS, YC and YPbPr formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

8.1 SD Luma Path

The input signal is processed by the following blocks:

- **Digital Fine Clamp**.
  This block uses a high precision algorithm to clamp the video signal.
- **Luma Filter Block**.
  This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- **Luma Gain Control**.
  The automatic gain control (AGC) can operate on a variety of different modes including gain based on the depth of the horizontal sync pulse, peak white mode and fixed manual gain.
- **Luma Resample**.
  To correct for line length errors as well as for dynamic line length changes, the data is digitally resampled.
- **Luma 2D Comb**.
  The two-dimensional comb filter provides YC separation.

- **AV Code Insertion**.
  At this point, the decoded luma (Y) signal is merged with the retrieved chroma values; AV codes (as per ITU-R. BT-656) can be inserted.

8.2 SD Chroma Path

The input signal is processed by the following blocks:

- **Digital Fine Clamp**.
  This block uses a high precision algorithm to clamp the video signal.
- **Chroma Demodulation**.
  This block employs a color subcarrier (Fsc) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC and an FM demodulation for SECAM.
- **Chroma Filter Block**.
  This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- **Gain Control**.
  The automatic gain control (AGC) can operate on a variety of different modes including gain based on the amplitude of the color subcarrier, based on the depth of the horizontal sync pulse on the Luma channel or fixed manual gain.
- **Chroma Resample**.
  The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line length errors of the incoming video signal.
- **Chroma 2D Comb**.
  The 2-dimensional 5-line super adaptive comb filter provides high quality YC separation if the input signal is CVBS.
- **AV Code Insertion**.
  At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values; AV codes (as per ITU-R. BT-656) can be inserted.

8.3 SDP Synchronization Processing

The SDP extracts syncs that are embedded in the video data stream. There is currently no support for external HS/VS inputs. The sync extraction has been optimized to support imperfect video sources, e.g. Video Cassette Recorders with head switches, etc. The actual algorithm used employs a coarse detection based on a threshold crossing followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output is then used to drive the digital resampling section to ensure 720 active pixels per line are output by the SDP.

The sync processing on the ADV7181C also includes two specialized post-processing blocks, which filter and condition the raw sync information as retrieved from the digitized analogue video.

1. VSYNC Processor: provides extra filtering of the detected Vsyncs to give improved vertical lock.

2. HSYNC PLL: designed to filter incoming H Syncs that have been corrupted by noise, providing much improved performance for video signals with stable timebase but poor signal to noise ratio (SNR).

8.4 SDP VBI Data Recovery

The SDP can retrieve the following information from the input video:

- Wide Screen Signaling (WSS)
- Copy Generation Management System (CGMS)
- Closed Caption (CC)
- Macrovision Protection Presence
- EDTV Data
- Gemstar-compatible data slicing

The SDP is also capable of automatically detecting the incoming video standard with respect to:

- Color subcarrier frequency
- Field rate
- Line rate

It can configure itself to support PAL-BGHID, PAL-M/N, PAL-combination N, NTSC-M, NTSC-J, SECAM 50Hz/60Hz, NTSC4.43 and PAL60.

8.5 SDP General Setup

8.5.1 Video Standard Selection (SDP)

The VID_SEL[3:0] register allows the user to force the digital core into a specific video standard. Under normal circumstances, however, this should not be necessary. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM and variants thereof.

Refer to Section 8.5.2 for more information on the autodetection system.

VID_SEL[3:0] Video Standard Selection (SDP), *Address 0x00, [7:4]*

Function

VID_SEL[3:0]	Description
0000 ⊂	Autodetect all PAL standards without pedestal Autodetect all NTSC standards without pedestal Autodetect SECAM
0001	Autodetect all PAL standards without pedestal Autodetect NTSC-M standards (with pedestal) Autodetect SECAM
0010	Autodetect PAL-N (with pedestal) Autodetect NTSC-J (without pedestal) Autodetect SECAM.

Function

VID_SEL[3:0]	Description
0011	Autodetect PAL-N (with pedestal) Autodetect NTSC-M (with pedestal) Autodetect SECAM.
0100	NTSC J ①
0101	NTSC M ①
0110	PAL 60
0111	NTSC 4.43 ①
1000	PAL BGHID
1001	PAL N (= PAL BGHID (with pedestal))
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL combination N
1101	PAL combination N (with pedestal)
1110	SECAM
1111	SECAM (with pedestal)

8.5.2 Autodetection of SDP Modes

In order to guide the autodetect system of the SDP block, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system picks the closest of the remaining enabled standards. The results of the SDP autodetection can be read back via the status registers. Refer to Section 6.1, Section 6.2, and Section 6.3 for more information.

AD_SEC525_EN Enable Autodetection of SECAM 525 line video (SDP), *0x07, [7]*

Function

AD_SEC525_EN	Description
0 ⊂	Disables the autodetection of a 525 line system with a SECAM style, fm-modulated color component
1	Enables the detection

AD_SECAM_EN Enable Autodetection of SECAM (SDP), *Address 0x07, [6]*

Function

AD_SECAM_EN	Description
0	Disables the autodetection of SECAM
1 ⊂	Enables the detection

AD_N443_EN Enable Autodetection of NTSC 443 (SDP), *0 07, [5]*

Function

AD_N443_EN	Description
0	Disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier
1 ⊂	Enables the detection

AD_P60_EN Enable Autodetection of PAL60 (SDP), *Address 0x07, [4]*
Function

AD_P60_EN	Description
0	Disables the autodetection of PAL systems with a 60Hz field rate
1 ⊂	Enables the detection

AD_PALN_EN Enable Autodetection of PAL N (SDP), *Address 0x07, [3]*
Function

AD_PALN_EN	Description
0	Disables the detection of PAL N standard
1 ⊂	Enables the detection

AD_PALM_EN Enable Autodetection of PAL M (SDP), *Address 0x07, [2]*
Function

AD_PALM_EN	Description
0	Disables the autodetection of PAL M
1 ⊂	Enables the detection

AD_NTSC_EN Enable Autodetection of NTSC (SDP), *Address 0x07, [1]*
Function

AD_NTSC_EN	Description
0	Disables the detection of standard NTSC
1 ⊂	Enables the detection

AD_PAL_EN Enable Autodetection of PAL (SDP), *Address 0x07, [0]*
Function

AD_PAL_EN	Description
0	Disables the detection of standard PAL
1 ⊂	Enables the detection

8.5.3 SFL_INV Subcarrier Frequency Lock Inversion (SDP)

This bit controls the behavior of the PAL switch bit in the SFL (GenLock Telegram) data stream. It was implemented to solve some compatibility issues with video encoders.

It solves the following two problems:

1. The PAL switch bit is only meaningful in PAL. Some encoders (including Analog Devices), however, do look at the state of this bit in NTSC too.
2. There was a design change in Analog Devices encoders from ADV717x to ADV719x. The older versions used the SFL (GenLock Telegram) bit directly, the latter ones invert the bit prior to using it. The reason for this was that the inversion compensated for the one line delay of an SFL (GenLock Telegram) transmission.

As a result:

- ADV717x encoders need the PAL switch bit in the SFL (GenLock Telegram) to be 0 for NTSC to work
- ADV7190/91/94 encoders need the PAL switch bit in the SFL to be 1 to work in NTSC

If the state of the PAL switch bit is wrong, a phase shift of 180 degrees occurs.

In a decoder/encoder back-to-back system where SFL is used, this bit needs to be set up properly for the specific encoder used.

SFL_INV Subcarrier Frequency Lock Inversion (SDP), *Address 0x41, [6]*

Function

SFL_INV	Description
0⊂	SFL compatible with ADV717x/7173x encoders
1	SFL compatible with ADV7190/91/94 encoders

8.5.4 Lock Related Controls (SDP)

Lock information is presented to the user in the form of bits [1:0] of the Status 1 register. Refer also to information on STATUS_1[7:0] on page 34. Figure 38 outlines the signal flow and the controls available to influence the way the lock status information is generated.

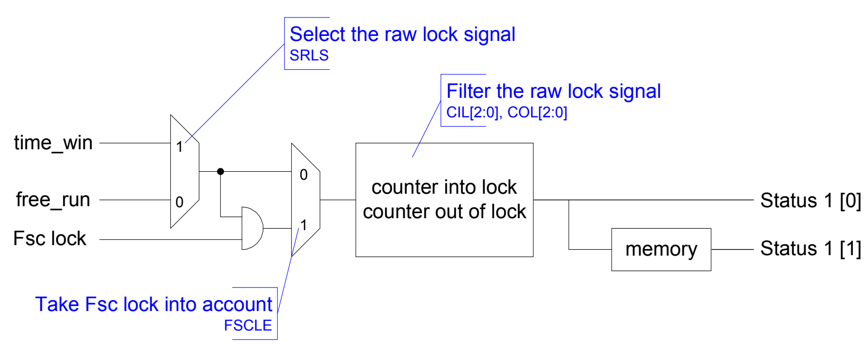


Figure 38: SDP Lock Related Signal Path

SRLS Select Raw Lock Signal (SDP), *0x51, [6]*

Using the SRLS bit, the user can choose between the following two sources for the determination of the lock status (as per bits [1:0] in the Status 1 register):

1. The **time_win** signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
2. The **free_run** signal evaluates the properties of the incoming video over several fields and takes vertical synchronization information into account.

Function

SRLS	Description
0 ⊂	Selects the free_run signal
1	Selects the time_win signal

FSCLE Fsc Lock Enable (SDP), *Address 0x51, [7]*

The FSCLE bit allows the user to choose if the status of the color subcarrier loop is to be taken into account when the overall lock status is determined and presented via bits [1:0] in the Status Register 1. Note this bit must be set to 0 when operating the SDP in YPbPr component mode in order to generate a reliable HLOCK status bit.

Function

FSCLE	Description
0	Overall lock status only dependent on horizontal sync lock
1 ⊂	Overall lock status dependent on horizontal sync lock AND Fsc Lock

VS_COAST (SDP), *Address 0xF9, [3:2]*

These bits are used to set VS free run (coast) frequency when using the SDP.

Function

VS_COAST[1:0]	Description
00⊂	Autocoast mode- follows VS frequency from last video input
01	Forces 50 Hz coast mode
10	Forces 60 Hz coast mode
11	Reserved

CIL[2:0] Count Into Lock (SDP), *Address 0x51, [2:0]*

CIL[2:0] determines the number of consecutive lines for which the 'into lock' condition has to be true before the system switches into the 'locked' state and reports this via Status_0 [1:0].

Function

CIL[2:0]	Description (Count Value in Lines of Video)
000	1
001	2
010	5
011	10
100 ⊂	100
101	500
110	1000
111	100000

COL[2:0] Count Out of Lock (SDP), *Address 0x51, [5:3]*

COL[2:0] determines the number of consecutive lines for which the ‘out of lock’ condition has to be true before the system switches into the ‘unlocked’ state and reports this via Status_0 [1:0].

Function

COL[2:0]	Description (Count Value in Lines of Video)
000	1
001	2
010	5
011	10
100 ⊂	100
101	500
110	1000
111	100000

ST_NOISE_VLD, HS Tip Noise Measurement Valid (SDP), *Address 0xDE, [3], Read only*

This bit indicates whether or not the ST_NOISE[10:0] measurement is valid.

Function

ST_NOISE_VLD	Description
0	ST_NOISE[10:0] measurement is not valid
1 ⊂	ST_NOISE[10:0] measurement is valid

ST_NOISE[10:0] HS Tip Noise Measurement (SDP), *Address 0xDE, [2:0], 0xDF, [7:0]*

The ST_NOISE[10:0] measures, over 4 fields, a readback value of the average of the noise in the HSYNC tip. ST_NOISE_VLD must be 1 for this measurement to be valid.

1 bit of ST_NOISE[10:0] = 1 ADC code.

1 bit of ST_NOISE[10:0] = 1.6V/4096 = 390.625uV

Function

ST_NOISE[10:0]	Description
xxx xxxx xxxx	HS tip noise measurement readback

8.6 SDP Color Controls

The following registers provide user control over the picture appearance, including control of the active data in the event of video being lost. They are independent of any other controls. For instance, the brightness control is independent from the picture clamping, although both controls affect the DC level of the signal.

CON[7:0] Contrast Adjust (SDP), *0x08, [7:0]*

This is the user control for contrast adjustment for the SDP block only.

Function

CON[7:0]	Description
0x80 ⊂	Adjusts the contrast of the picture Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0] SD Saturation Cb Channel (SDP), *Address 0xE3, [7:0]*

This register allows the user to control the gain of the Cb channel only. This register affects the SDP core only.

Function

SD_SAT_Cb[7:0]	Description
0x80 ⊂	Gain on Cb channel = 0dB
0x00	Gain on Cb channel = -42dB
0xFF	Gain on Cb channel = +6dB

SD_SAT_Cr[7:0] SD Saturation Cr Channel (SDP), *Address 0xE4, [7:0]*

This register allows the user to control the gain of the Cr channel only. This register affects the SDP core only.

Function

SD_SAT_Cr[7:0]	Description
0x80 ⊂	Gain on Cr channel = 0dB
0x00	Gain on Cr channel = -42dB
0xFF	Gain on Cr channel = +6dB

SD_OFF_Cb[7:0] SD Offset Cb Channel (SDP), *0xE1, [7:0]*

This register allows the user to select an offset for the Cb channel only. This register affects the SDP core only. There is a functional overlap with HUE[7:0] register.

Function

SD_OFF_Cb[7:0]	Description
0x80 ⊂	0 offset applied to the Cb channel
0x00	-312 mV applied to Cb channel
0xFF	+312 mV applied to Cb channel

SD_OFF_Cr[7:0] SD Offset Cr Channel (SDP), *Address 0xE2, [7:0]*

This register allows the user to select an offset for the Cb channel only. This register affects the SDP core only. There is a functional overlap with HUE[7:0] register.

Function

SD_OFF_Cr[7:0]	Description
0x80 ⊂	0 offset applied to the Cr channel
0x00	-312mV applied to Cr channel
0xFF	+312mV applied to Cr channel

BRI[7:0] Brightness Adjust (SDP), *Address 0x0A, [7:0]*

This register controls the brightness of the video signal through the SDP core.

Function

BRI[7:0]	Description
0x00 ⊂	Adjusts the brightness of the picture Offset of the luma channel = 0IRE
0x7F	Offset of the luma channel = 100IRE
0x80	Offset of the luma channel = -100IRE

HUE[7:0] Hue Adjust (SDP), *Address 0x0B, [7:0]*

This register contains the value for color hue adjustment.

HUE[7:0] has a range of ± 90° with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°

Note: The hue adjustment value is fed into the AM color demodulation block. It applies only to video signals that contain chroma information in the form of an AM modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video input (YUV).

Function

HUE[7:0]	Description
0x00 ⊂	Adjusts the hue of the picture Phase of the chroma signal = 0 degree
0x7F	Phase of the chroma signal = -90 degree
0x80	Phase of the chroma signal = +90 degree

DEF_Y[5:0] Default Value Y (SDP) , *Address 0x0C, [7:2]*

If the ADV7181C lost lock on the incoming video signal or if there is no input signal at all, the DEF_Y[5:0] register allows the user to specify a default luma value to be output.

This value is used under the following conditions:

- DEF_VAL_AUTO_EN bit set to high **and** the ADV7181C lost lock to the input video signal.
  This is the intended mode of operation (automatic mode).
- DEF_VAL_EN bit is set, regardless of the lock status of the video decoder. This is a forced mode and can be useful during configuration.

The DEF_Y[5:0] values define the six MSBs of the output video. The remaining LSBs will be padded with 0's.

Example: In 8-bit mode the output is Y[9:0] = {DEF_Y[5:0], 0, 0})

Function

DEF_Y[5:0]	Description
001101'b (blue)	Default value of Y

DEF_C[7:0] Default Value C (SDP), *0x0D, [7:0]*

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if:

- DEF_VAL_AUTO_EN bit is set to high **and** the ADV7181C cannot lock to the input video (automatic mode)
- DEF_VAL_EN bit is set to high (forced output)

The following data is finally output from the ADV7181C for the chroma side:

- Cr[7:0] = {DEF_C[7:4], 0, 0, 0, 0}
- Cb[7:0] = {DEF_C[3:0], 0, 0, 0, 0}

Function

DEF_C[7:0]	Description
0x7C (blue)	Default values for Cr and Cb

DEF_VAL_EN Default Value Enable (SDP), *Address 0x0C, [0]*

This bit **forces** the usage of the default values for Y, Cr and Cb. Refer to the descriptions of DEF_Y[5:0] and DEF_C[7:0] on page 101 for additional information. The decoder outputs a stable 27 MHz clock, HS and VS also in this mode.

Function

DEF_VAL_EN	Description
0	Do not force the use of default Y, Cr and Cb values. Output colors dependent on DEF_VAL_AUTO_EN.
1	Always use default Y, Cr and Cb values, override picture data even if video decoder is locked.

DEF_VAL_AUTO_EN Default Value Automatic Enable (SDP), *Address 0x0C, [1]*

This bit enables the **automatic** usage of the default values for Y, Cr and Cb in cases where the ADV7181C cannot lock to the input video signal.

Function

DEF_VAL_AUTO_EN	Description
0	Do not use default Y, Cr and Cb values, if unlocked, output noise – snow picture
1	Use default Y, Cr and Cb values when lost lock

8.7 SDP Clamp Operation

Since the input video is AC coupled into the ADV7181C, its DC value needs to be restored. This process is referred to as 'clamping the video'. This section explains the general process of clamping on the ADV7181C for the SDP and shows the different ways in which a user can configure its behavior.

The SDP block uses a combination of current sources and a digital processing block for clamping, as shown in Figure 39. The analogue processing channel shown is replicated three times inside the IC. While only one single channel (and only one ADC) would be needed for a CVBS signal, two independent channels are needed for YC (S-VHS) type signals, and three independent channels allow component signals (YPbPr) to be processed too.

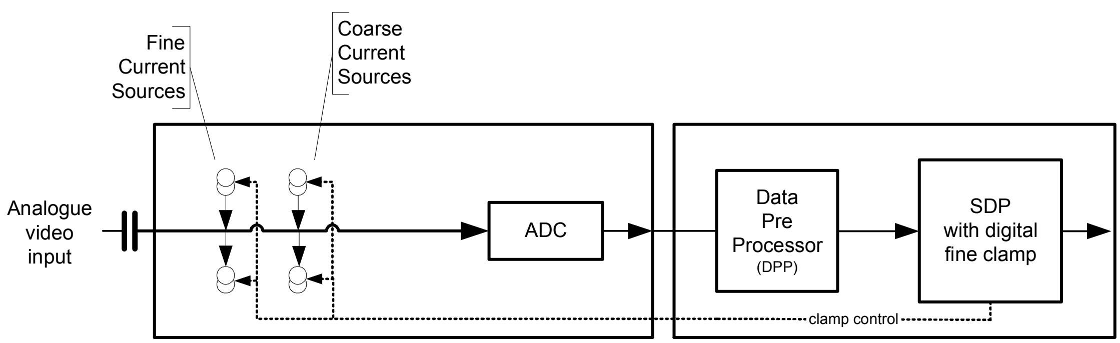


Figure 39: SDP Clamping Overview

The clamping can be divided into two sections:

1. Clamping before the ADC (analogue domain): current sources.
2. Clamping after the ADC (digital domain): digital processing block.

The ADCs can digitize an input signal if it resides within the ADCs input voltage range of 1.6 V. An input signal with a DC level that is too large or too small will be clipped at the top or bottom of the ADC range.

The primary task of the analogue clamping circuits is to ensure that the video signal stays within the valid ADC input window so that the analogue to digital conversion can take place. It is not necessary to clamp the input signal with a very high accuracy in the analogue domain as long as the video signal fits the ADC range.

After digitization, the digital fine clamp block corrects for any remaining variations in DC level. Since the DC level of an input video signal refers directly to the brightness of the picture transmitted, it is important to perform a fine clamp with high accuracy, otherwise brightness variations can occur. Furthermore, dynamic changes in the DC level will almost certainly lead to visually objectionable artifacts and must, therefore, be prohibited.

The clamping scheme has to complete two tasks. Firstly, it has to be able to acquire a newly connected video signal with a completely unknown DC level. Secondly, it has to maintain the DC level during normal operation.

For a fast acquiring of an unknown video signal, the large current clamps can be activated[1]. After the initial acquisition of the video signal, the voltage clamp is switched off and is not used again (SDP only!).

Standard definition video signals can have excessive noise on them, especially CVBS signals transmitted by terrestrial broadcast and demodulated using a tuner. These usually show very large levels of noise (> 100 mV). A voltage clamp would be unsuitable for this type of video signal. Instead, the ADV7181C employs a set of four current sources that can cause coarse (>0.5 mA) and fine (<0.1 mA) currents to flow into and away from the high impedance node that carries the video signal (refer to Figure 39).

The remainder of this section describes the I^2C signals used to influence the behavior of the SDP clamping.

CCLEN Current Clamp Enable (SDP), *Address 0x14, [4]*

The Current Clamp Enable bit allows the user to switch off the current sources in the analogue front end altogether. This can be useful if the incoming analogue video signal is clamped externally (blank level to the voltage given out on the Reference pin) and, therefore, interference from the internal clamp sources is undesirable.

Function

CCLEN	Description
0	Current sources switched off
1	Current sources enabled

DCT[1:0] Digital Clamp Timing (SDP), *Address 0x15, [6:5]*

The Clamp Timing register determines the time constant of the digital fine clamp circuitry. It is important to realize that the digital fine clamp reacts very fast since it is supposed to correct immediately any residual DC level error for the active line. The time constant of the digital fine clamp must be a lot quicker than the one from the analogue blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

[1] It is assumed that the amplitude of the video signal at this point is of a nominal value.

Function

DCT[1:0]	Description
00	Slow (TC: 1 sec)
01	Medium (TC: 0.5sec)
10 ⮌	Fast (TC: 0.1 sec)
11	Determined by ADV7181C dependent on video parameters

DCFE Digital Clamp Freeze Enable (SDP), *Address 0x15, [4]*

This register bit allows the user to freeze the digital clamp loop at any point in time. It is intended mainly for users who like to do their own clamping. They should disable the current sources for analogue clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

Function

DCFE	Description
0 ⮌	Digital clamp operational
1	Digital clamp loop frozen

8.8 SDP Luma Filter

Data[1] from the digital fine clamp block is processed by three sets of filters:

1. **Luma Anti Alias Filter (YAA)**.
   The SDP receives video at a rate of 27 MHz[2]. The ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The Luma anti alias filter decimates the oversampled video using a high quality, linear phase low pass filter that preserves the luma signal while at the same time attenuating out-of-band components. The Luma anti alias filter (YAA) has a fixed response.

2. **Luma Shaping Filters (YSH)**.
   The shaping filter block is a programmable low pass filter with a wide variety of responses. It can be used to reduce selectively the bandwidth of the luma video signal (as is needed prior to scaling, for instance). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. A follow-on video compression stage can work more efficiently if the video is low pass filtered.

   The ADV7181C allows the user to select two responses for the shaping filter: one that will be used for good quality CVBS for component and S-VHS type sources, and a second for non-standard CVBS signals.

   The YSH filter responses also include a set of notches for PAL and NTSC. It is

[1] The data format at this point is CVBS for CVBS input or luma only for Y/C or YUV input formats.
[2] In the case of 4X oversampled video the ADCs sample at 54 MHz, the first decimation is performed inside the DPP filters. Hence the data rate into the SDP core is always 27 MHz.

recommended, however, to use the comb filters for YC separation.

3. **Digital Resampling Filter**.
   This block is used to allow the dynamic resampling of the video signal to alter parameters, such as the time base of a line of video. Fundamentally, the resampler is a set of low pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 41 shows the overall response of all filters together. If not explicitly mentioned, filters are set into a typical wide band mode.

8.8.1 Y Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. YC separation must aim for the best possible crosstalk reduction while still retaining as much bandwidth as possible, especially on the luma component.

High quality YC separation can be achieved by using the internal comb filters of the ADV7181C. Comb filtering relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier (Fsc). For good quality CVBS signals, this relationship is known and the comb filter algorithms can be used to separate out luma and chroma with high accuracy.

In the case of non-standard video signals, the frequency relationship can be disturbed and the comb filters may not be able to remove all crosstalk artifacts in an optimum fashion without the assistance of the shaping filter block.

An automatic mode is provided. Here the ADV7181C evaluates the quality of the incoming video signal and selects the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR and WYSFM allow the user to override manually the automatic decisions in part or in full.

The luma shaping filter has three control registers:

- YSFM[4:0] − allows the user to select manually a shaping filter mode (applied to all video signals) or to enable an automatic selection (dependent on video quality and video standard).
- WYSFMOVR − allows the user to override manually the WYSFM decision.
- WYSFM[4:0] − allows the user to select a different shaping filter mode for good quality CVBS, component (YUV) and S-VHS (YC) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources since they can be combed successfully, as well as for luma components of YUV and YC sources since they need not be combed. For poor quality signals, the system selects from a set of proprietary shaping filter responses that complement the comb filter operation in order to reduce visual artifacts.

The decisions of the control logic are shown in Figure 40.

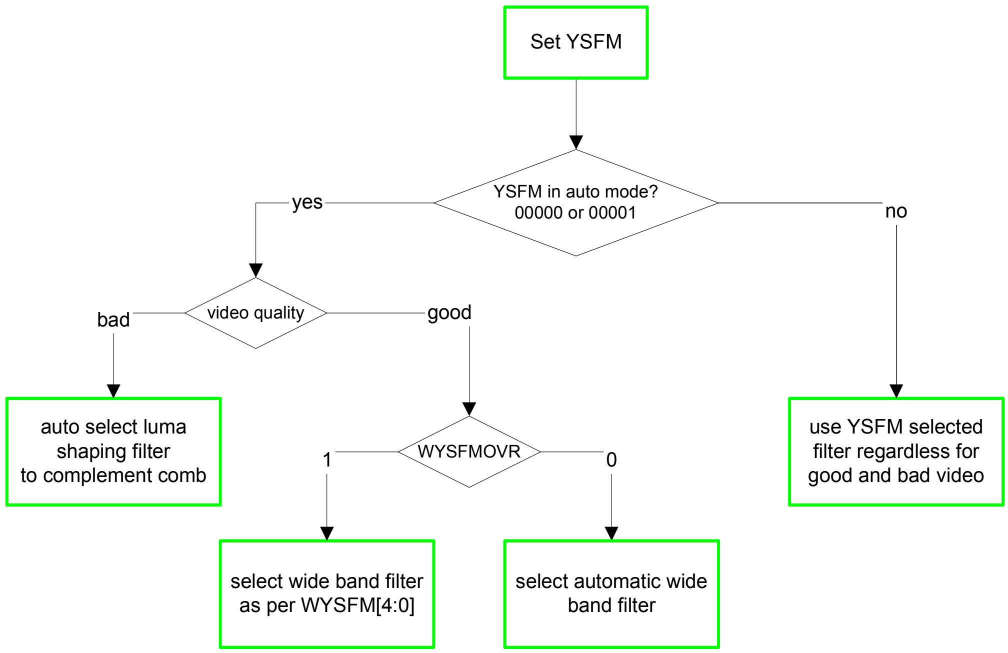


Figure 40: YSFM and WYSFM Control Flowchart

YSFM[4:0] Y Shaping Filter Mode (SDP), *Address 0x17, [4:0]*

The Y Shaping Filter Mode bits allow the user to select from a wide range of low pass and notch filters. When switched in automatic mode, the filter is selected based on other register selections, e.g. detected video standard, as well as based on properties extracted from the incoming video itself, e.g. quality, time base stability, etc. The automatic selection will always pick the widest possible bandwidth for the video input encountered.

Notes:

- If the YSFM settings specify a filter, e.g. YSFM is set to values other than 00000 or 00001, the chosen filter is applied to **all** video, regardless of its quality.
- In automatic selection mode, the notch filters are only used for bad quality video signals. For all other video signals, wide band filters are used.

Function

YSFM[4:0]	Description
0'0000	Automatic selection including a **wide** notch response (PAL/NTSC/SECAM)
0'0001	Automatic selection including a **narrow** notch response (PAL/NTSC/SECAM)
0'0010	SVHS 1
0'0011	SVHS 2
0'0100	SVHS 3
0'0101	SVHS 4
0'0110	SVHS 5
0'0111	SVHS 6

Function

YSFM[4:0]	Description
0'1000	SVHS 7
0'1001	SVHS 8
0'1010	SVHS 9
0'1011	SVHS 10
0'1100	SVHS 11
0'1101	SVHS 12
0'1110	SVHS 13
0'1111	SVHS 14
1'0000	SVHS 15
1'0001	SVHS 16
1'0010	SVHS 17
1'0011	SVHS 18 (CCIR 601)
1'0100	PAL NN 1
1'0101	PAL NN 2
1'0110	PAL NN 3
1'0111	PAL WN 1
1'1000	PAL WN 2
1'1001	NTSC NN 1
1'1010	NTSC NN 2
1'1011	NTSC NN 3
1'1100	NTSC WN 1
1'1101	NTSC WN 2
1'1110	NTSC WN 3
1'1111	Reserved

WYSFMOVR Wide Band Y Shaping Filter Override (SDP), *Address 0x18, [7]*

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information, refer to the general discussion of the luma shaping filters in Section 8.8 and the flowchart in Figure 40.

Function

WYSFMOVR	Description
0	Automatic selection of shaping filter for good quality video signals
1 ⊂	Enables manual override via WYSFM[4:0]

WYSFM[4:0] Wide Band Y Shaping Filter Mode (SDP), *Address 0x18, [4:0]*

The WYSFM[4:0] bits allow the user to select manually a shaping filter for good quality video signals, e.g. CVBS with stable time base, luma component of YUV, luma component of YC. The WYSFM bits are only active if the WYSFMOVR bit is set to 1. Refer also to the general discussion of the setting of the shaping filters in Section 8.8.

Function

WYSFM[4:0]	Description
0'0000	**Do not use**
0'0001	**Do not use**
0'0010	SVHS 1
0'0011	SVHS 2
0'0100	SVHS 3
0'0101	SVHS 4
0'0110	SVHS 5
0'0111	SVHS 6
0'1000	SVHS 7
0'1001	SVHS 8
0'1010	SVHS 9
0'1011	SVHS 10
0'1100	SVHS 11
0'1101	SVHS 12
0'1110	SVHS 13
0'1111	SVHS 14
1'0000	SVHS 15
1'0001	SVHS 16
1'0010	SVHS 17
1'0011 ⊂	SVHS 18 (CCIR 601)
1'0100 – 1'1111	**Do not use**

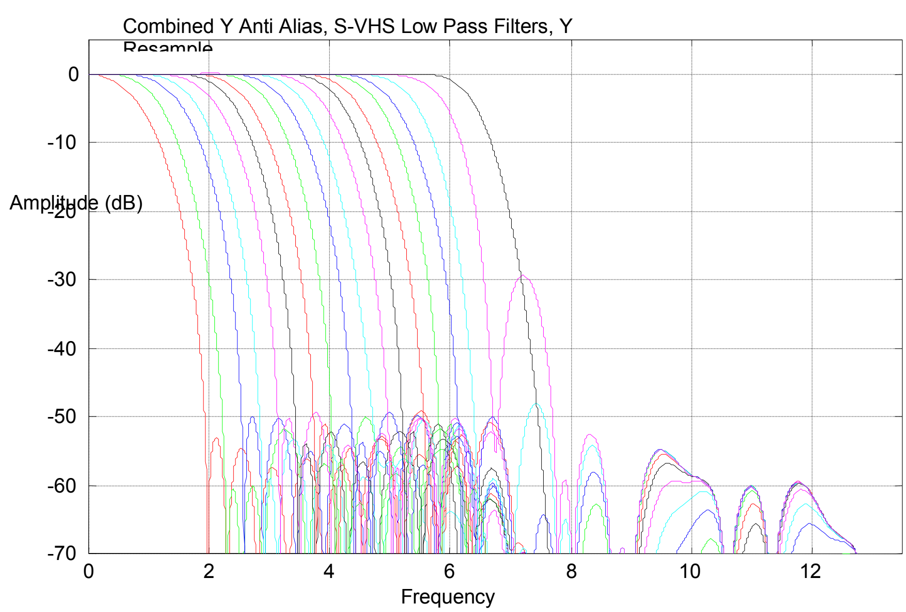


Figure 41: SDP Y S-VHS Combined Responses

The filter plots in Figure 41 show the S-VHS 1 (narrowest) to S-VHS 18 (widest) shaping filter settings.

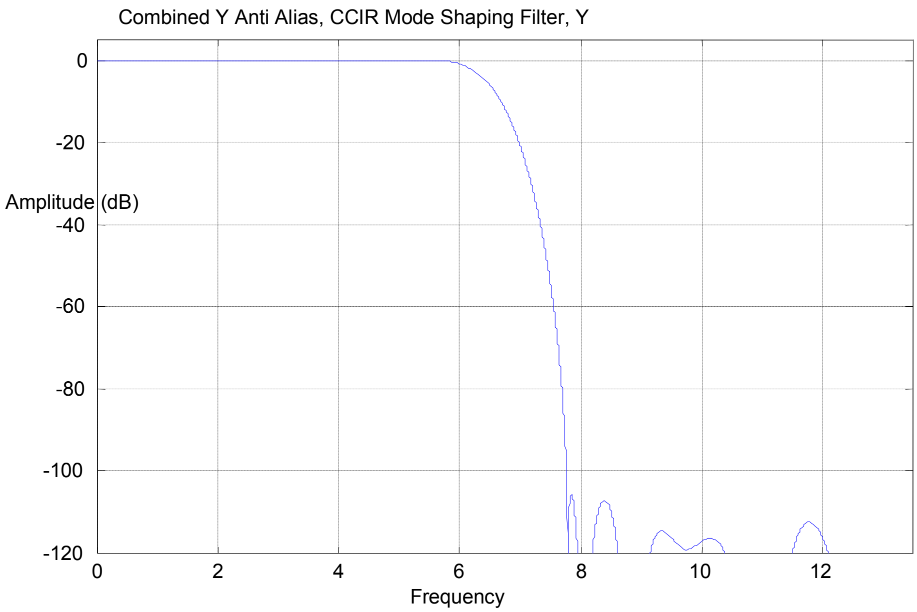


Figure 42: SDP Y S-VHS 18 Extra Wideband Filter (CCIR 601 compliant)

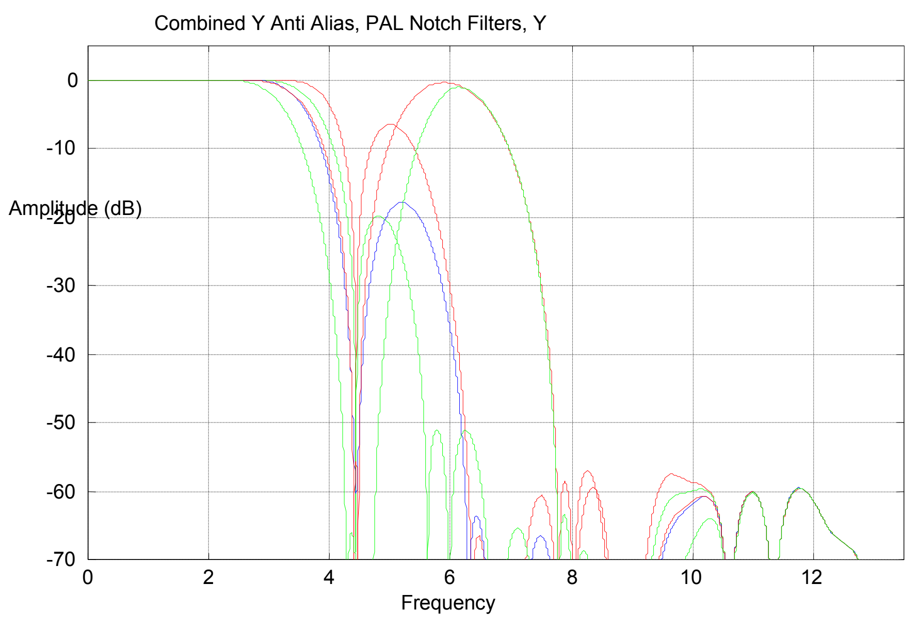


Figure 43: PAL Notch Filter Responses

Figure 43 shows the PAL notch filter responses.

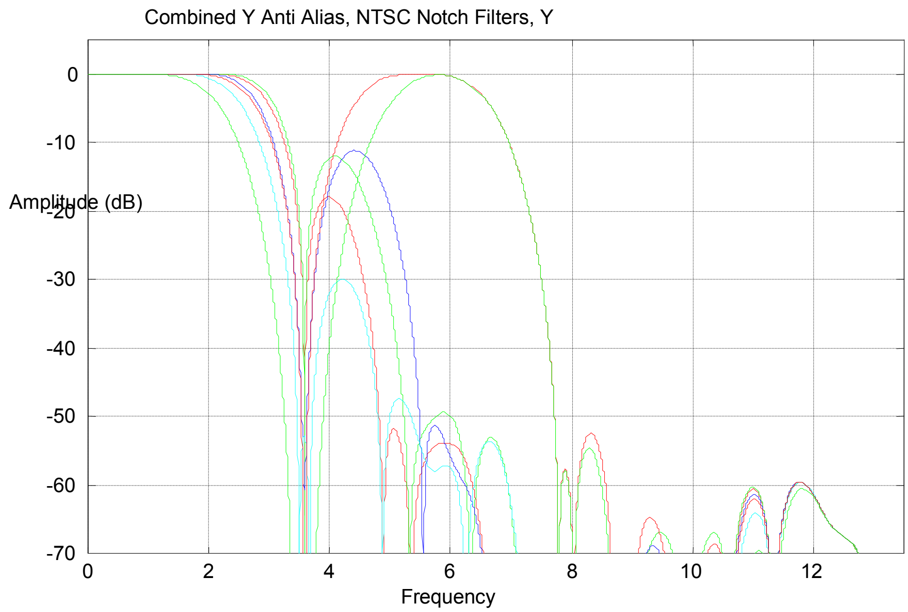


Figure 44: NTSC Notch Filter Responses

Figure 44 shows the NTSC compatible notches.

8.9 SDP Chroma Filter

Data[1] from the digital fine clamp block is processed by three sets of filters:

1. **Chroma Anti Alias Filter (CAA)**.
   The ADV7181C oversamples CVBS by a factor of 2 and Chroma/UV by a factor of 4. A decimating filter (CAA) is used to preserve the active video band and remove any out-of-band components. The CAA filter has a fixed response.

2. **Chroma Shaping Filters (CSH)**.
   The shaping filter block (CSH) can be programmed to perform a variety of low pass responses. It can be used to reduce selectively the bandwidth of the chroma signal for scaling or compression.

3. **Digital Resampling Filter**.
   This block is used to allow dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low pass filters. The actual response is chosen by the system with no requirement for user intervention.

The plots below always show the overall response of all filters together.

[1] The data format at this point is CVBS for CVBS input or chroma only for Y/C or U/V interleaved for YUV input formats.

CSFM[2:0] C Shaping Filter Mode (SDP), *Address 0x17, [7]*

The C Shaping Filter Mode bits allow the user to select from a range of low pass filters for the chrominance signal.

Function

CSFM[2:0]	Description
000	1.5 MHz bandwidth
001	2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wide Band Mode

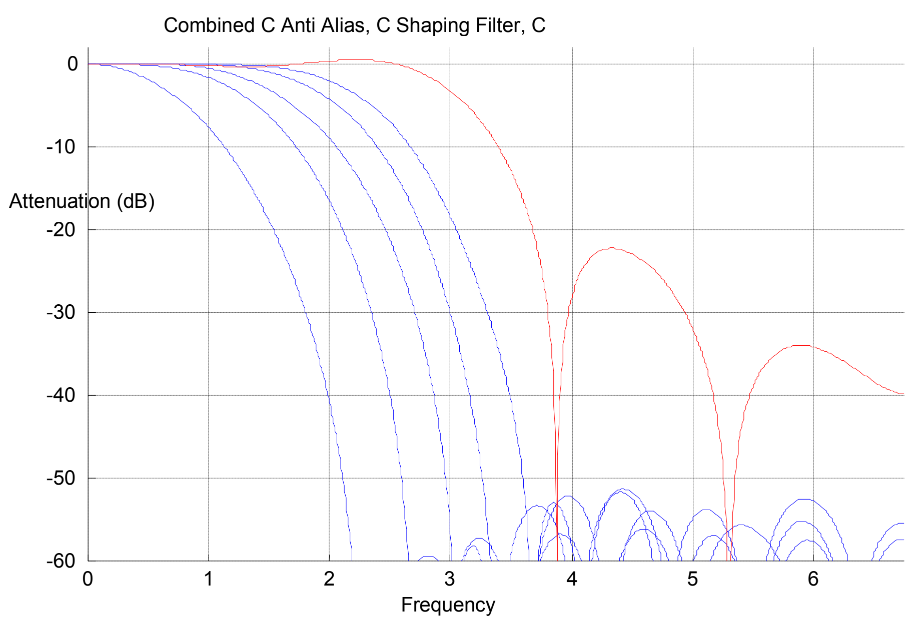


Figure 45: SDP Chroma Shaping Filter Responses

Figure 45 shows the responses of SH1 (narrowest) to SH5 (widest) and, in addition, the Wide Band Mode (red).

8.10 SDP Gain Operation

8.10.1 Description

The gain control within the ADV7181C is done on a purely digital basis. The input ADCs support a 12-bit range, mapped into an analogue voltage range of 1.6 V. Gain correction takes place after digitization in the form of a digital multiplier.

The advantages of this architecture over the commonly used PGA (programmable gain amplifier) **before** the ADCs are manifold; amongst them is the fact that now the gain is completely independent of supply, temperature and process variations.

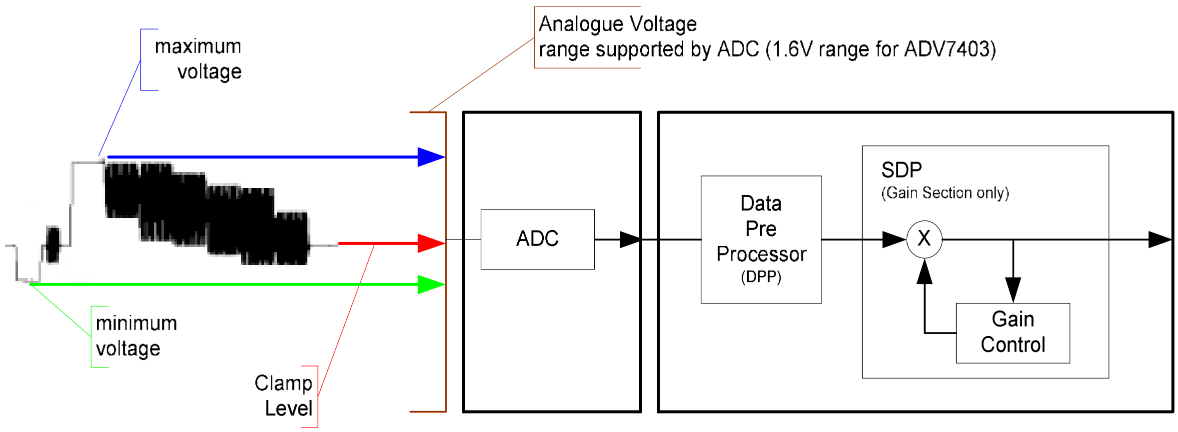


Figure 46: SDP Gain Control Overview

As shown in Figure 46, the ADV7181C can decode a video signal as long as it fits into the ADC window. There are two components to this: the amplitude of the input signal, and the DC level it resides on. The DC level is set by the clamping circuitry (refer to Section 8.7).

If the amplitude of the analogue video signal is too high, clipping can occur and visual artifacts appear. The analogue input range of the ADC, together with the clamp level, determine the maximum supported amplitude of the video signal.

The minimum supported amplitude of the input video is determined by the SDP core's ability to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are two gain control units, for luma and for chroma data. Both can operate independently of each other. The chroma unit can also take its gain value from the luma path. Several AGC modes are possible, as summarized by Table 17.

Table 17: SDP AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth	Dependent on color burst amplitude
		Taken from luma path
	Peak white	Dependent on color burst amplitude
		Taken from luma path
Y/C	Dependent on horizontal sync depth	Dependent on color burst amplitude
		Taken from luma path
	Peak white	Dependent on color burst amplitude
		Taken from luma path
YPbPr	Dependent on horizontal sync depth	Taken from luma path

It is possible to freeze the automatic gain control loops. This causes the loops to stop updating and the AGC determined gain at the time of the freeze stays active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Refer to the descriptions of the dual function manual gain registers, LG[11:0] on page 114, and CG[11:0] on page 116.

8.10.2 SDP Luma Gain

LAGC[2:0] Luma Automatic Gain Control (SDP), *Address 0x30, [7:0]*
The Luma Automatic Gain Control mode bits select the mode of operation for the gain control in the luma path.

Notes:

- The entries 011, 100, 101 and 110 are for the internal evaluation of ADI **and must not be used by customers.**
- There are ADI internal parameters to customize the peak white gain control. These can be obtained by contacting ADI for more information.

Function

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0])
001	AGC (blank level to sync tip): no override through white peak
010	AGC (blank level to sync tip): automatic override through white peak
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

LAGT[1:0] Luma Automatic Gain Timing (SDP), *Address 0x2F, [7:6]*

The Luma Automatic Gain Timing register allows the user to influence the tracking speed of the luminance automatic gain control. Note that this register has an effect only if the LAGC[2:0] register is set to 001, 010, 011 or 100 (automatic gain control modes).

Notes:

- If peak white AGC is enabled and active (refer to STATUS_1[7:0] on page 34 also), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the part leaves peak white, AGC and LAGT become relevant again.
- The update speed for the peak white algorithm can be customized by the use of internal parameters. Contact ADI if further details are required.

Function

LAGT[1:0]	Description
00	Slow (TC: 2 sec)
01	Medium (TC: 1sec)
10	Fast (TC: 0.2 sec)
11 ⮌	Adaptive

LG[11:0] Luma Gain (SDP), *Address 0x2F, [3:0]; Address 0x30, [7:0]*
LMG[11:0] Luma Manual Gain (SDP), *Address 0x2F, [3:0]; Address 0x30, [7:0]*

Luma gain[11:0] is a **dual function** register:

- If written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to Manual fixed gain. Equation 8 shows how to calculate a desired gain.

- If read back, this register returns the **current gain** value. Depending on the setting in the LAGC[2:0] bits, this will be either one of the following values:

    - Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
    - Luma automatic gain value (LAGC[2:0] set to any of the automatic modes)

Function

LG[11:0]/LMG[11:0]	Read/ Write	Description
LMG[11:0] = X	Write	Manual gain for luma path
LG[11:0]	Read	Actually used gain

$$Luma\_Gain(525i) = \frac{1024 < LMG[11:0] \leq 4095}{1128} = 0.9...3.63$$

Equation 8: NTSC SDP Luma Gain Formula

$$Luma\_Gain(625i) = \frac{1024 < LMG[11:0] \leq 4095}{1222} = 0.83...3.35$$

Equation 9: PAL SDP Luma Gain Formula

Example:

Program the ADV7181C into manual fixed gain mode with a desired gain of 0.89:

- Use Equation 8 to convert the gain:
  0.89 * 1128 = 1003.92
- Truncate to integer value:
  1003.92 → 1003

- Convert to hexadecimal:
  1003_d → 0x3E6
- Split into two registers and program:
  Luma Gain Control 1[3:0] = 0x3
  Luma Gain Control 2[7:0] = 0xE6
- Enable Manual Fixed Gain Mode:
  Set LAGC[2:0] to 000

BETACAM Enable Betacam Levels (SDP), *Address 0x01, [5]*

If YUV data is routed through the SDP core, the automatic gain control modes can target different video input levels, as outlined in Table 18. Note that the BETACAM bit is only valid if the input mode is YUV (component) and if the data is routed through the SDP core. The BETACAM bit basically sets the target value for the AGC operation.

A review of the following sections of this manual is useful:

- Section 4 for activating the SDP core initially
- INSEL[3:0] on page 16 to find out how component video (YPbPr) can be routed through the SDP core
- VID_SEL[3:0] on page 93 for the various standards, e.g. with and without pedestal

Table 18: Betacam Levels

Name	**Betacam**	**Betacam Variant**	**SMPTE**	**MII**
Y Range	0 - 714mV (incl. 7.5% pedestal)	0 – 714 mV	0 – 700 mV	0 – 700 mV (incl. 7.5% pedestal)
U and V Range	-467mV - +467mV	-505 mV - +505 mV	-350 mV - +350 mV	-324 mV - +324 mV
Sync Depth	286mV	286 mV	300 mV	300 mV

The automatic gain control (AGC) algorithms adjust the levels based on the setting of the BETACAM bit as outlined below.

Function

BETACAM	Description
0 ⊂	Assuming YUV is selected as input format Selecting PAL with pedestal selects MII Selecting PAL without pedestal selects SMPTE Selecting NTSC with pedestal selects MII Selecting NTSC without pedestal selects SMPTE
1	Assuming YUV is selected as input format Selecting PAL with pedestal selects BETACAM Selecting PAL without pedestal selects BETACAM variant Selecting NTSC with pedestal selects BETACAM Selecting NTSC without pedestal selects BETACAM variant

PW_UPD Peak White Update (SDP), *Address 0x2B, [0]*

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change.

Notes:

- LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place.
- Refer to information on LAGC[2:0] on page 113.

Function

PW_UPD	Description
0	Updates gain once per video line
1 ⊂	Updates gain once per field

8.10.3 Chroma Gain

CAGC[1:0] Chroma Automatic Gain Control (SDP), *Address 0x2C, [1:0]*

The two bits of Color Automatic Gain Control mode select the basic mode of operation for the automatic gain control in the chroma path.

Function

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0])
01	Uses luma gain for chroma
10 ⊂	Automatic gain (based on color burst)
11	Freezes chroma gain

CAGT[1:0] Chroma Automatic Gain Timing (SDP), *Address 0x2D, [7:6]*
The Chroma Automatic Gain Timing register allows the user to influence the tracking speed of the chroma automatic gain control. Note that this register has an effect only if the CAGC[1:0] register is set to 10 (automatic gain).

Function

CAGT[1:0]	Description
00	Slow (TC: 2 sec)
01	Medium (TC: 1sec)
10	Fast (TC: 0.2 sec)
11 ⊂	Adaptive

CG[11:0] Chroma Gain (SDP), *Address 0x2D, [3:0]; Address 0x2E, [7:0]*
CMG[11:0] Chroma Manual Gain (SDP), *Address 0x2D, [3:0]; Address 0x2E, [7:0]*

Chroma gain[11:0] is a dual function register:

- If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] mode is switched to Manual fixed gain. Refer to Equation 10 on how to calculate a desired gain.

- If read back, this register returns the **current gain** value. Depending on the setting in the CAGC[1:0] bits this will be either one of the following values:

  - Chroma manual gain value (CAGC[1:0] set to chroma manual gain mode)
  - Chroma automatic gain value (CAGC[1:0] set to any of the automatic modes)

Function

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma\_Gain = \frac{(0 < CG \leq 4095)}{650} = 0...6.29$$

Equation 10: SDP Chroma Gain Formula

Example:

Freezing the automatic gain loop and reading back the CG[11:0] register resulted in a value of 0x47A.

- Convert the readback value to decimal:
  0x47A ➔ 1146_d
- Apply Equation 10 to convert the readback value:
  1146/650 = 1.76

CKE Color Kill Enable (SDP), *Address 0x2B, [6]*

The Color Kill Enable bit allows the optional color kill function to be switched on or off. For QAM based video standards (PAL and NTSC), as well as for FM based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled, color processing will be switched off (black and white output) if the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines. To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

Note: The color kill option only works for input signals with a modulated chroma part. For component input (YUV) there is no color kill.

Function

CKE	Description
0	Color kill disabled
1 ⇐	Color kill enabled

CKILLTHR[2:0] Color Kill Threshold (SDP), *Address 0x3D, [6:4]*

The CKILLTHR[2:0] bits allow to the user select a threshold for the color kill function. The threshold only applies to QAM based video standards (NTSC and PAL) or FM modulated ones (SECAM).

To enable the color kill function, the CKE bit must be set.

Note: For settings 000, 001, 010 and 011, chroma demodulation inside the ADV7181C may not work satisfactorily for poor input video signals.

Function

CKILLTHR[2:0]	Description	
	SECAM	NTSC, PAL
000	No color kill	Kill at < 0.5%
001	Kill at < 5%	Kill at < 1.5%
010	Kill at < 7%	Kill at < 2.5%
011	Kill at < 8%	Kill at < 4.0%
100	Kill at < 9.5%	Kill at < 8.5%
101	Kill at < 15%	Kill at < 16.0%
110	Kill at < 32%	Kill at < 32.0%
111	Reserved, ADI internal use only. Do not select	

8.11 SDP Chroma Transient Improvement

The signal bandwidth allocated for chroma is typically a lot smaller than the one for luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth since the human eye is a lot less sensitive to chrominance than to luminance.

The uneven bandwidth, however, can lead to some visual artifacts when it comes to sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (refer to Figure 47). Due to the higher bandwidth, the signal transition of the luma component is usually a lot sharper than that of the chroma component. The color edge is not sharp, but, in the worst case, blurred over several pixels.

The Chroma Transient Improvement (CTI) block examines the input video data. It detects transitions of chroma and can be programmed to steepen the chroma edges in an attempt to restore artificially lost color bandwidth. The CTI block, however, only operates on edges above a certain threshold to ensure that noise is not emphasized. Care was taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Note: Chroma transient improvements are needed primarily for signals experiencing severe chroma bandwidth limitation. For these types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

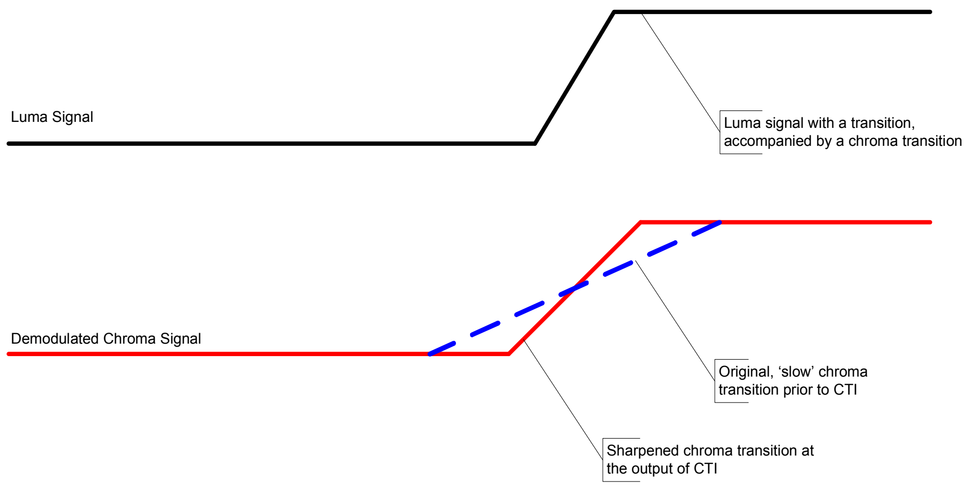


Figure 47: CTI Luma/Chroma Transition

CTI_EN Chroma Transient Improvement Enable (SDP), *Address 0x4D, [0]*

The CTI_EN bit enables the CTI function. If set to 0, the CTI block is inactive and the chroma transients are left untouched.

Function

CTI_EN	Description
0	Disables CTI
1	Enables CTI block

CTI_AB_EN Chroma Transient Improvement Alpha Blend Enable (SDP), *Address 0x4D, [1]*

The CTI_AB_EN bit enables an alpha-blend function within the CTI block. If set to 1, the alpha-blender mixes the transient improved chroma with the original signal. The sharpness of the alpha-blending is configured via the CTI_AB[1:0] bits.

Note: For the alpha-blender to be active, the CTI block must be enabled via the CTI_EN bit.

Function

CTI_AB_EN	Description
0	Disables CTI alpha blender
1	Enables CTI alpha blend mixing function

CTI_AB[1:0] Chroma Transient Improvement Alpha Blend (SDP), *Address 0x4D, [3:2]*

The CTI_AB[1:0] controls the behavior of alpha-blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

Notes:

- For CTI_AB[1:0] to become effective, the CTI block must be enabled via the CTI_EN bit and the alpha blender must be switched on via CTI_AB_EN.

- Sharp blending maximizes the effect of CTI on the picture, but can also increase the visual impact of small amplitude high frequency chroma noise.

Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing
10	Smooth mixing
11 ⊂	Smoothest alpha blend function

CTI_C_TH[7:0] CTI Chroma Threshold (SDP), *Address 0x4E, [7:0]*

The CTI_C_TH[7:0] value is an unsigned 8-bit number specifying how big the amplitude step in a chroma transition has to be in order to be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block only to improve large transitions.

Function

CTI_C_TH[7:0]	Description
0x08⊂	Threshold for chroma edges prior to CTI

8.12 Digital Noise Reduction and Luma Peaking Filter (SDP)

Digital Noise Reduction (DNR) is based on the assumption that high frequency signals with low amplitude are probably noise and that, therefore, their removal improves picture quality. There are two DNR blocks in the ADV7181C: the DNR1 block before the luma peaking filter and the DNR2 block after the luma peaking filter, as shown in Figure 48.

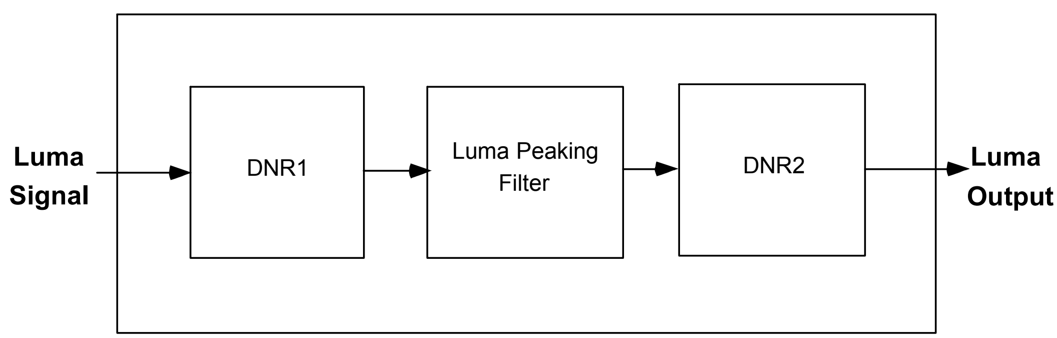


Figure 48: DNR and Peaking Block Diagram

DNR_EN Digital Noise Reduction Enable (SDP), *Address 0x4D, [5]*

The DNR_EN bit enables the DNR block or bypasses it.

Function

DNR_EN	Description
0	Bypasses DNR (disable)
1 ⊂	Enables digital noise reduction on the luma data

DNR_TH[7:0] DNR Noise Threshold, *Address 0x50, [7:0]*

The DNR1 block is positioned before the luma peaking block. The DNR_TH[7:0] value is an unsigned 8-bit number, which determines the maximum edge that will still be interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH[7:0] will cause the DNR block to interpret even large transients as noise and will remove them. As a result, the effect on the video data will be more visible. Programming a small value will cause only small transients to be seen as noise and to be removed.

Function

DNR_TH[7:0]	Description
0x08 ⊂	Threshold for maximum luma edges to be interpreted as noise

PEAKING_GAIN[7:0], Luma Peaking Gain, *Address 0xFB, [7:0]*

This filter can be manually enabled. The user can select to boost or attenuate the mid region of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The default value on this register passes through the Luma data unaltered. A lower value will attenuate the signal and a higher value will gain the Luma signal. A plot of the filters responses is shown in Figure 49.

Function

PEAKING_GAIN[7:0]	Description
0x40 ⊂	0db response

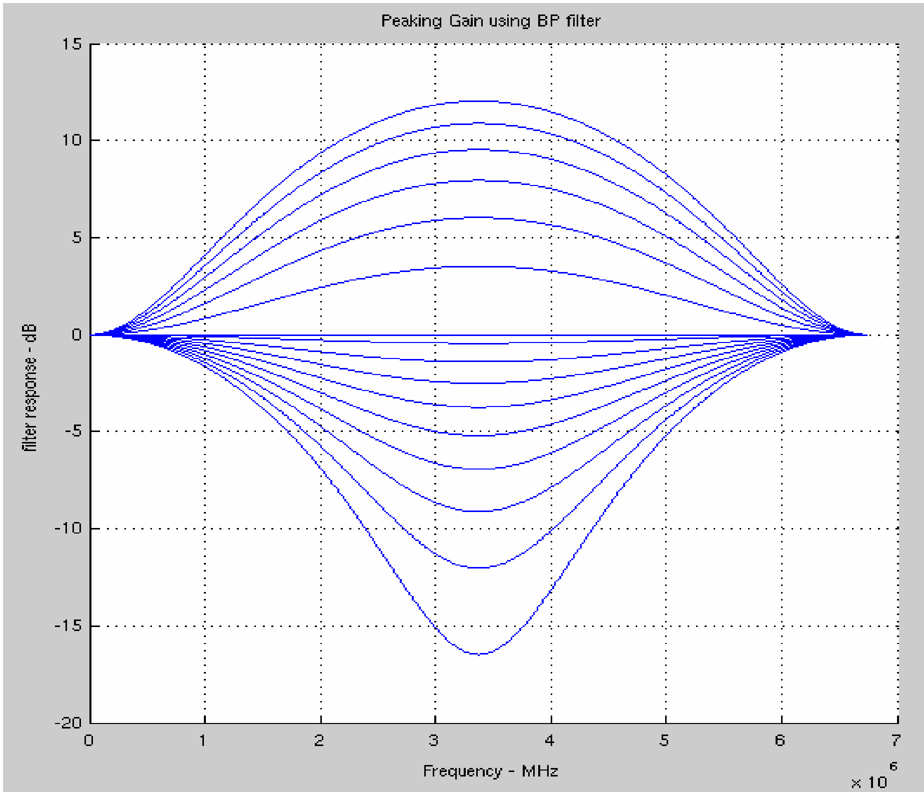


Figure 49: Peaking Filter Responses

DNR_TH2[7:0] DNR Noise Threshold 2, *Address 0xFC, [7:0]*

The DNR2 block is positioned after the luma peaking block, so it affects the gained luma signal. It operates in the same way as the DNR1 block, but there is an independent threshold control for this block, DNR_TH2[7:0]. This value is an unsigned 8-bit number, which determines the maximum edge that will still be interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH2[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data will be more visible. Programming a small value will cause only small transients to be seen as noise and to be removed.

Function

DNR_TH2[7:0]	Description
0x04 ⊂	Threshold for maximum luma edges to be interpreted as noise

8.13 SDP Comb Filters

Registers are available to customize the comb filter operation.

Depending on the video standard detected (by autodetection) or selected (by manual programming), the NTSC or the PAL configuration registers are used. In addition to the bits listed in this section, there are some further ADI internal controls. Contact ADI if further details are required.

8.13.1.1 NTSC Comb Filter Settings

These are used for NTSC-M/J CVBS inputs.

NSFSEL[1:0] Split Filter Selection NTSC (SDP), *Address 0x19, [3:2]*

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection gives better performance on diagonal lines, but leaves more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

Function

NSFSEL[1:0]	Description
00	Narrow
01	Medium
10	Medium
11	Wide

8.13.1.2 PAL Comb Filter Settings

This is used for PAL-B/G/H/I/D, PAL-M, PAL-Combinational N, PAL-60 and NTSC443 CVBS inputs.

PSFSEL[1:0] Split Filter Selection PAL (SDP), *Address 0x19, [1:0]*

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection will eliminate dot crawl, but will show imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Function

PSFSEL[1:0]	Description
00	Narrow
01	Medium
10	Wide
11	Widest

8.13.2 Comb Filter Vertical Blank Control

NVBIOLCM[1:0] NTSC VBI Odd Field Luma Comb Mode (SDP), *Address 0xEB, [7:6]*

NVBIOLCM controls the first combed line after VBI on NTSC odd field (luma comb).

Function

NVBIOLCM[1:0]	Description
00	Early by 1 line
01	0: SMPTE170 compliant, blank lines 1-20, 264-282, comb half lines
10	Delay by 1 line
11	Delay by 2 lines

NVBIELCM[1:0] NTSC VBI Even Field Luma Comb Mode (SDP), *Address 0xEB, [5:4]*

NVBIELCM controls the first combed line after VBI on NTSC even field (luma comb).

Function

NVBIELCM[1:0]	Description
00	Early by 1 line
01 ⊃	0: SMPTE170 compliant, blank lines 1-20, 264-282, comb half lines
10	Delay by 1 line
11	Delay by 2 lines

PVBIOLCM[1:0] PAL VBI Odd Field Luma Comb Mode (SDP), *Address 0xEB, [3:2]*

PVBIOLCM controls the first combed line after VBI on PAL odd field (luma comb).

Function

PVBIOLCM[1:0]	Description
00	Early by 1 line
01 ⊃	0: BT470 compliant, blank lines 624-22, 311-335, comb half lines
10	Delay by 1 line
11	Delay by 2 lines

PVBIELCM[1:0] PAL VBI Even Field Luma Comb Mode (SDP), *Address 0xEB, [1:0]*

PVBIELCM controls the first combed line after VBI on PAL even field (luma comb).

Function

PVBIELCM[1:0]	Description
00	Early by 1 line
01 ⊃	0: BT470 compliant, blank lines 624-22, 311-335, comb half lines
10	Delay by 1 line
11	Delay by 2 lines

NVBIOCCM[1:0] NTSC VBI Odd Field Chroma Comb Mode (SDP), *Address 0xEC, [7:6]*

NVBIOCCM controls the first combed line after VBI on NTSC odd field (chroma comb).

Function

NVBIOCCM[1:0]	Description
00	Early by 1 line
01 ⊃	0: SMPTE170 compliant, no color on lines 1 to 20, 264 to 282, chroma present on half lines
10	Delay by 1 line
11	Delay by 2 lines

NVBIECCM[1:0] NTSC VBI Even Field Chroma Comb Mode (SDP), *Address 0xEC, [5:4]*

NVBIECCM controls the first combed line after VBI on NTSC even field (chroma comb).

Function

NVBIECCM[1:0]	Description
00	Early by 1 line
01 ⊂	0: SMPTE170 compliant, no color on lines 1 to 20, 264 to 282, chroma present on half lines
10	Delay by 1 line
11	Delay by 2 lines

PVBIOCCM[1:0] PAL VBI Odd Field Chroma Comb Mode (SDP), *Address 0xEC, [3:2]*

PVBIOCCM controls the first combed line after VBI on PAL odd field (chroma comb).

Function

PVBIOCCM[1:0]	Description
00	Early by 1 line
01 ⊂	0: SMPTE170 compliant, no color on lines 1 to 20, 264 to 282, chroma present on half lines
10	Delay by 1 line
11	Delay by 2 lines

PVBIECCM[1:0] PAL VBI Even Field Chroma Comb Mode (SDP), *Address 0xEC, [1:0]*

PVBIECCM controls the first combed line after VBI on PAL even field (chroma comb).

Function

PVBIECCM[1:0]	Description
00	Early by 1 line
01 ⊂	0: SMPTE170 compliant, no color on lines 1 to 20, 264 to 282, chroma present on half lines
10	Delay by 1 line
11	Delay by 2 lines

8.14 SDP AV Code Insertion and Controls

This section describes the I^{2}C based controls that affect:

- Insertion of AV codes into the data stream
- Data blanking during the vertical blank interval (VBI)
- The range of data values permitted in the output data stream
- The relative delay of luma versus chroma signals

Note that some of the decoded VBI data is being inserted during the horizontal blanking interval. Refer to Section 8.19.1 for more information.

BT656-4 ITU Standard BT-R.656-4 Enable (SDP), *Address 0x04, [7]*

The ITU has changed the position for toggling the V bit within the SAV EAV codes for NTSC only between revisions 3 and 4. The BT656-4 standard bit allows the user to select an output mode that is compliant either with the previous or the new standard. For further information, review the standard at http://www.itu.ch.

Note: The standard change affects NTSC only and has no bearing on PAL.

Function

BT656-4	Description
0	BT656-3 spec: V bit goes low at EAV of lines 10 and 273
1	BT656-4 spec: V bit goes low at EAV of lines 20 and 283

SD_DUP_AV SDP Duplicate AV codes (SDP), *Address 0x03, [0]*

Depending on the output interface width, it may be necessary to duplicate the AV codes from the luma path into the chroma path.

In an 8/10-bit wide output interface (Cb/Y/Cr/Y interleaved data), the AV codes are defined as (FF/00/00/AV), with AV being the actually transmitted word containing information about H/V/F. In this output interface mode, the following assignment takes place: Cb = FF, Y = 00, Cr = 00 and Y = AV.

In a 16-/20-bit output interface where Y and Cr/Cb are delivered via separate data buses, the AV code would be over the whole 20 bits. The SD_DUP_AV bit allows the doubling up of the AV codes so that the full sequence can be found on the Y bus as well as (i.e. duplicated) on the Cr/Cb bus. Figure 50 illustrates this information.

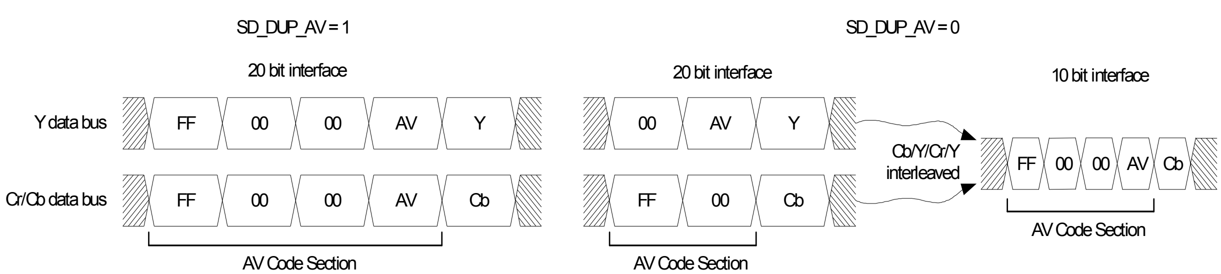


Figure 50: SDP AV Code Duplication Control

Function

SD_DUP_AV	Description
0	AV codes in single fashion to suit 8-/10-bit interleaved data output
1	AV codes duplicated for 16-/20-bit interfaces

VBI_EN Vertical Blanking Interval Data Enable (SDP), *Address 0x03, [7]*

The VBI enable bit allows data such as Intercast and CC data to be passed through the luma channel of the SDP decoder with only a minimum amount of filtering performed. All data for VBI lines are passed through and available at the output port. (Refer to Table 92 for information on the control of VBI end positions.) The ADV7181C does not blank the luma data and it switches all filters along the luma data path automatically into their widest bandwidth. For active video, the filter settings for YSH and YPK are restored.

Refer also to the description of BL_C_VBI for information on the chroma path.

Function

VBI_EN	Description
0	All video lines are filtered/scaled
1	Only active video region is filtered/scaled

BL_C_VBI Blank Chroma during VBI (SDP), *Address 0x04, [2]*

Setting BL_C_VBI high, the Cr and Cb values of all VBI lines get blanked. This is done so that any data that comes during VBI is not decoded as 'color' and output through Cr and Cb. As a result, it should be possible to send VBI lines into the decoder, then output them through an encoder again and they should appear undistorted. Without this blanking, any wrongly decoded color would get encoded by the video encoder and, therefore, the VBI lines would be distorted.

Function

BL_C_VBI	Description
0	Decodes and outputs color during VBI
1	Blank Cr and Cb value during VBI (no color, 0x80)

RANGE Range Selection (SDP), *Address 0x04, [0]*

AV codes (as per ITU-R BT-656, formerly known as CCIR-656) consist of a fixed header made up of 0xFF and 0x00 values. These two values are reserved and are not to be used for active video. In addition, the ITU specifies that the nominal range for video should be restricted to values between 16 and 235 for luma, and 16 to 240 for chroma.

The RANGE bit allows the user to limit the range of values output by the ADV7181C to the recommended value range. It is ensured in any case that the reserved values of 255_d (0xFF) and 00_d (0x00) are not presented on the output pins unless they are part of an AV code header.

Function

RANGE	Description	
0	$16 \leq Y \leq 235$	$16 \leq C/P \leq 240$
1	$1 \leq Y \leq 254$	$1 \leq C/P \leq 254$

AUTO_PDC_EN Automatic Programmed Delay Control (SDP), *Address 0x27, [6]*

Enabling the AUTO_PDC_EN function activates a function within the ADV7181C that automatically programs the LTA[1:0] and CTA[2:0] to have the chroma and luma data match delays for all modes of operation. If set, the manual registers LTA[1:0] and CTA[2:0] are not used by the system. If the automatic mode is disabled via setting the AUTO_PDC_EN bit to 0, the values programmed into the LTA[1:0] and CTA[2:0] registers take effect.

Function

AUTO_PDC_EN	Description
0 ⊂	Uses LTA[1:0] and CTA[2:0] values for delaying luma and chroma samples. Refer to the following descriptions of LTA[1:0] and CTA[2:0].
1	ADV7181C automatically determines the LTA and CTA values to have luma and chroma aligned at the output.

LTA[1:0] Luma Timing Adjust (SDP), *Address 0x27, [1:0]*

The Luma Timing Adjust register allows the user to specify a timing difference between chroma and luma samples.

Note: There is a certain functionality overlap with the CTA[2:0] register.

Function

LTA[1:0]	Description
00 ⊂	No delay
01	Luma 1 clk (37 ns) delayed
10	Luma 2 clk (74 ns) early
11	Luma 1 clk (37 ns) early

CTA[2:0] Chroma Timing Adjust (SDP), *Address 0x27, [5:3]*

The Chroma Timing Adjust register allows the user to specify a timing difference between chroma and luma samples. This can be used to compensate for external filter group delay differences in the luma versus chroma path, and to allow for a different number of pipeline delays while processing the video downstream. Review this functionality together with the LTA[1:0] register.

Note: The chroma can only be delayed/advanced in chroma pixel steps. One chroma pixel step is equal to 2 luma pixels. The programmable delay happens after demodulation where you cannot delay any more by luma pixel steps.

Function

CTA[2:0]	Description
000	Not used
001	Chroma + 2 chroma pixel (early)
010	Chroma + 1 chroma pixel (early)
011 ⊂	No delay
100	Chroma - 1 chroma pixel (late)
101	Chroma - 2 chroma pixel (late)
110	Chroma - 3 chroma pixel (late)
111	Not used

8.15 SDP Synchronization Output Signals

8.15.1 HS Configuration

The following controls allow the user to configure the behavior of the HS output pin only:

- Begin of HS signal via HSB[10:0]
- End of HS signal via HSE[10:0]
- Polarity of HS using PHS

HSB[10:0] HS Begin, *Address 0x34, [6:4], Address 0x35, [7:0]*

The HS Begin and HS End registers allow the user to freely position the HS output (pin) within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HS. Using both values, the user can program both the position and the length of the HS output signal.

The position of this edge is controlled by placing a binary number into HSB[10:0]. The number applied offsets the edge with respect to an internal counter reset to zero [0] immediately after EAV code FF,00,00,XY (refer to Figure 51). HSB is set to 00000000010b, which is 2 LLC1 clock cycles from count[0].

Function

HSB[10:0]	Description
0x002 ⊂	HS pulse starts after HSB[10:0] pixel after falling edge of HS

HSE[10:0] HS End, *Address 0x34, [2:0], Address 0x36, [7:0]*

The HS Begin and HS End registers allow the user to freely position the HS output (pin) within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HS. Using both values, the user can program both the position and the length of the HS output signal.

The position of this edge is controlled by placing a binary number into HSE[10:0]. The number applied offsets the edge with respect to an internal counter reset to zero immediately after EAV code FF,00,00,XY (refer to Figure 51). HSE is set to 00000000000b, which is 0 LLC1 clock cycles from count[0].

Function

HSE[9:0]	Description
0x000 ⊂	HS pulse ends after HSE[10:0] pixel after falling edge of HS

Example:

1. To shift the HS towards active video by 20 LLCs, add 20 LLCs to both HSB and HSE.
   i.e. HSB[10:0] = [00000010110]
   HSE[10:0] = [00000010100]

2. To shift the HS away from active video by 20 LLCs, add 1696* LLCs to both HSB and HSE (for NTSC).
   i.e. HSB[10:0] = [11010100010]
   HSE[10:0] = [11010100000]

   *1696 is derived from NTSC total number of Pixels = 1716

To move 20 LLC away from active video is equal to subtracting 20 from 1716 and adding the result in binary to both HSB[10:0] and HSE[10:0]

Table 19: HS Timing Parameters

Refer to Figure 50.

<table>
<tr><td rowspan="3"></td><td>Characteristic</td><td>HS Begin Adjust</td><td>HS End Adjust</td><td>HS to Active Video (LLC Clock Cycles)</td><td>Active Video Samples/Line</td><td>Total LLC Clock Cycles</td></tr>
<tr><td>Symbol</td><td>HSB[10:0]</td><td>HSE[10:0]</td><td>c</td><td>d</td><td>e</td></tr>
<tr><td>Note</td><td>Default</td><td>Default</td><td>Default</td><td></td><td></td></tr>
<tr><td rowspan="3">Standard</td><td>NTSC</td><td rowspan="3">00000000010b</td><td rowspan="3">00000000000b</td><td>272</td><td>720Y+720C =1440</td><td>1716</td></tr>
<tr><td>NTSC Square Pixel</td><td>276</td><td>640Y+640C =1280</td><td>1560</td></tr>
<tr><td>PAL</td><td>284</td><td>720Y+720C =1440</td><td>1728</td></tr>
</table>

PHS Polarity HS (SDP), *Address 0x37, [7]*

The polarity of the HS pin as it comes from the SDP block can be inverted using the PHS bit.

Function

PHS	Description
0	HS active high
1	HS active low

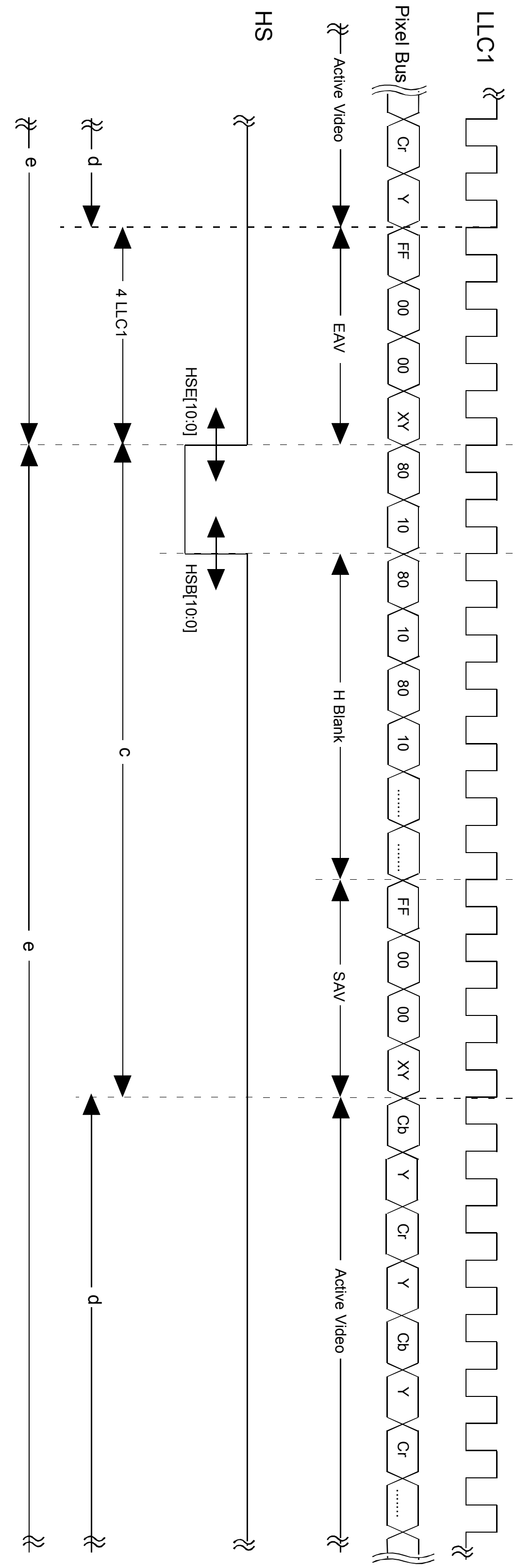


Figure 51: HS Timing (SDP)

8.15.2 VS and FIELD Configuration

The following controls allow the user to configure the behavior of the VS and FIELD output pins, as well as the generation of embedded AV codes:

- ADV encoder compatible signals via NEWAVMODE
- PVS, PF
- HVSTIM
- VSBHO, VSBHE
- VSEHO, VSEHE
- For NTSC control:
  - NVBEGDELO, NVBEGDELE, NVBEGSIGN, NVBEG[4:0],
  - NVENDDELO, NVENDDELE, NVENDSIGN, NVEND[4:0],
  - NFTOGDELO, NFTOGDELE, NFTOGSIGN, NFTOG[4:0].
- For PAL control:
  - PVBEGDELO, PVBEGDELE, PVBEGSIGN, PVBEG[4:0],
  - PVENDDELO, PVENDDELE, PVENDSIGN, PVEND[4:0],
  - PFTOGDELO, PFTOGDELE, PFTOGSIGN, PFTOG[4:0].

NEWAVMODE New AV Mode, *Address 0x31, [4]*

Function

NEWAVMODE	Description
0	EAV/SAV codes generated to suit ADI Encoders. No adjustments possible.
1	Enables Manual Position of VSYNC, Field, and AV codes using registers 0x34 to 0x37 and 0xE5 to 0xEA. Default register settings are CCIR656 Compliant (refer to Figure 52 (NTSC), Figure 57 (PAL)). For recommended manual user settings for NTSC, refer to Table 20 and Figure 53; for PAL, refer to Table 21 and Figure 58.

HVSTIM Horizontal VS Timing (SDP), *Address 0x31, [3]*

The HVSTIM bit allows the user to select where the VS signal is being asserted within a line of video. Some interface circuitry can require VS to go low while HS is low.

Function

HVSTIM	Description
0	Start of line relative to HSE
1	Start of line relative to HSB

VSBHO VS Begin Horizontal Position Odd (SDP), *Address 0x32, [7]*

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

Function

VSBHO	Description
0 ⊂	VS pin goes high at the middle of a line of video (odd field)
1	VS pin changes state at the start of a line (odd field)

VSBHE VS Begin Horizontal Position Even (SDP), *Address 0x32, [6]*

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

Function

VSBHE	Description
0	VS pin goes high at the middle of a line of video (even field)
1⊂	VS pin changes state at the start of a line (even field)

VSEHO VS End Horizontal Position Odd (SDP), *Address 0x33, [7]*

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

Function

VSEHO	Description
0	VS pin goes low (inactive) at the middle of a line of video (odd field)
1⊂	VS pin changes state at the start of a line (odd field)

VSEHE VS End Horizontal Position Even (SDP), *Address 0x33, [6]*

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

Function

VSEHE	Description
0 ⊂	VS pin goes low (inactive) at the middle of a line of video (even field)
1	VS pin changes state at the start of a line (even field)

PVS Polarity VS (SDP), *Address 0x37, [5]*

The polarity of the VS pin as it comes from the SDP block can be inverted using the PVS bit.

Function

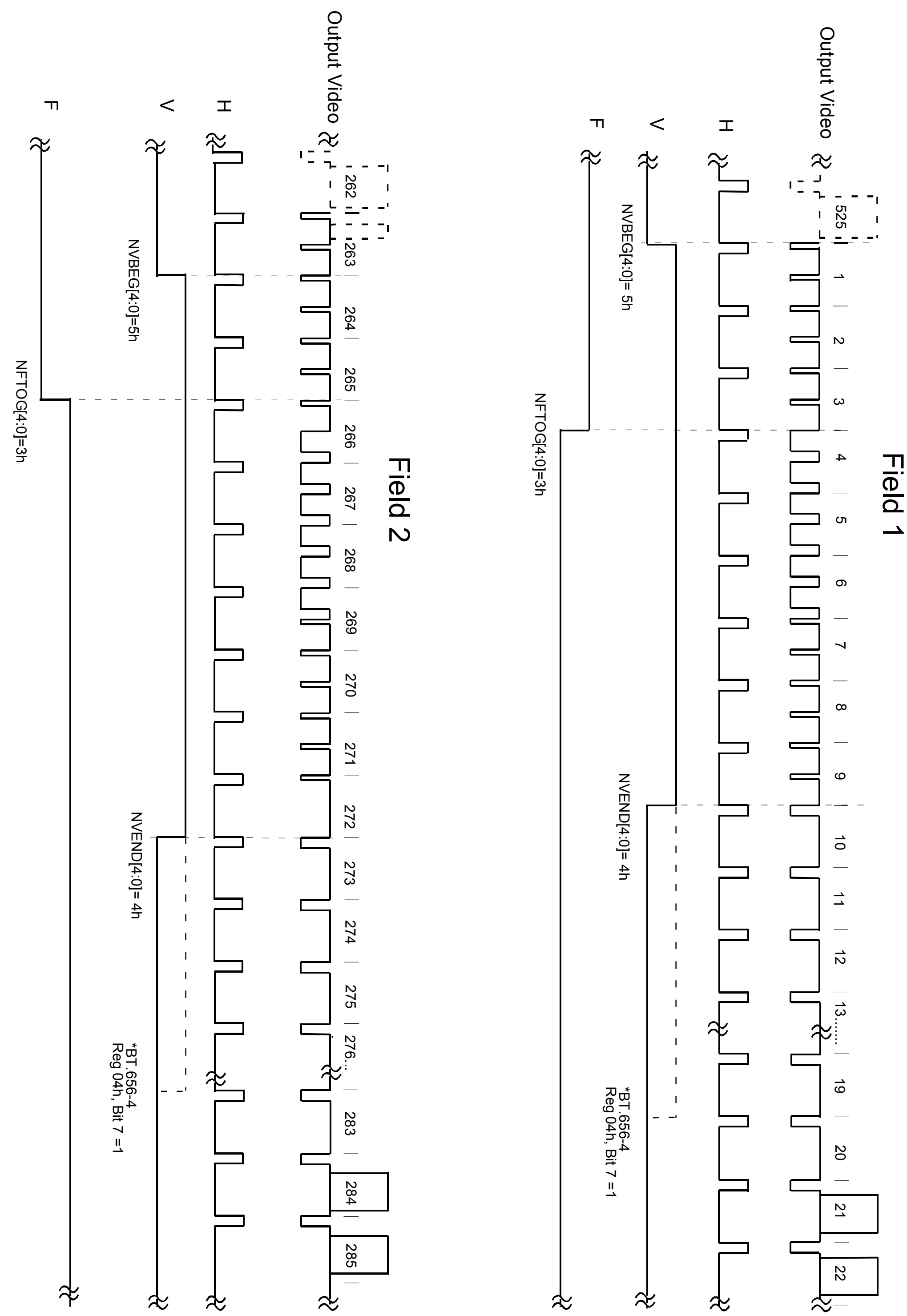
PVS	Description
0 ⊂	VS active high
1	VS active low

PF Polarity FIELD (SDP), *Address 0x37, [3]*

The polarity of the FIELD pin as it comes from the SDP block can be inverted using the PF bit.

Function

PF	Description
0 ⊃	FIELD active high
1	FIELD active low



* Applies if NEMAVMODE = 0
Must be manually shifted if NEWAVMODE = 1.

Figure 52: NTSC Default (BT.656) (Polarity of H, V, and F Embedded in Data)

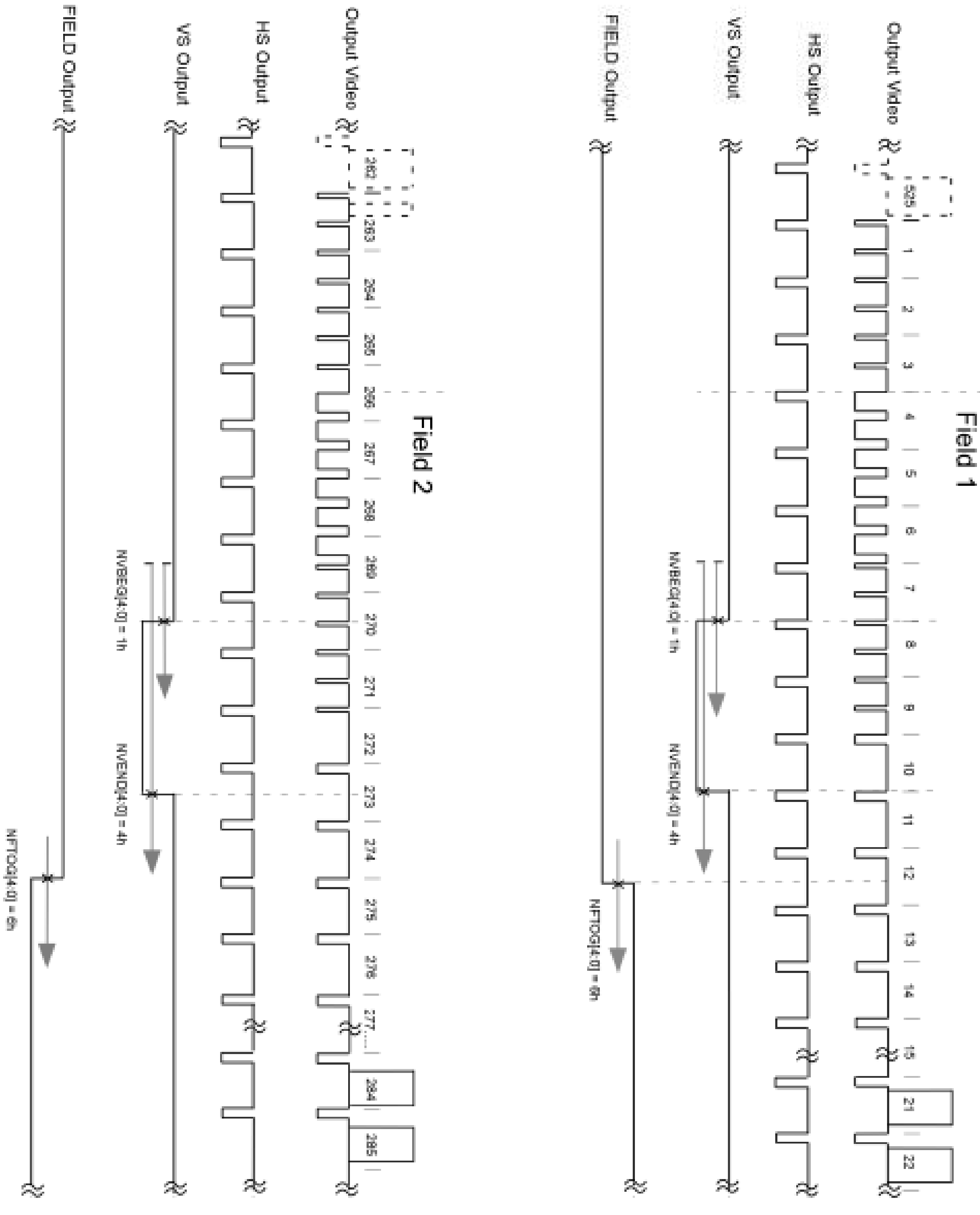


Figure 53: NTSC Typical VSYNC/Field Positions Using Register Writes in Table 20

Table 20: Recommended User Settings for NTSC

Refer to Figure 52.

Register (Hex)	Register Name	Write (Hex)
31	Vsync Field Control 1	1A
32	Vsync Field Control 2	81
33	Vsync Field Control 3	84
34	Hsync Pos. Control 1	00
35	Hsync Pos. Control 2	00
36	Hsync Pos. Control 3	7D
37	Polarity	A1
E5	NTSC_V_Bit_Beg	41
E6	NTSC_V_Bit_End	84
E7	NTSC_F_Bit_Tog	06

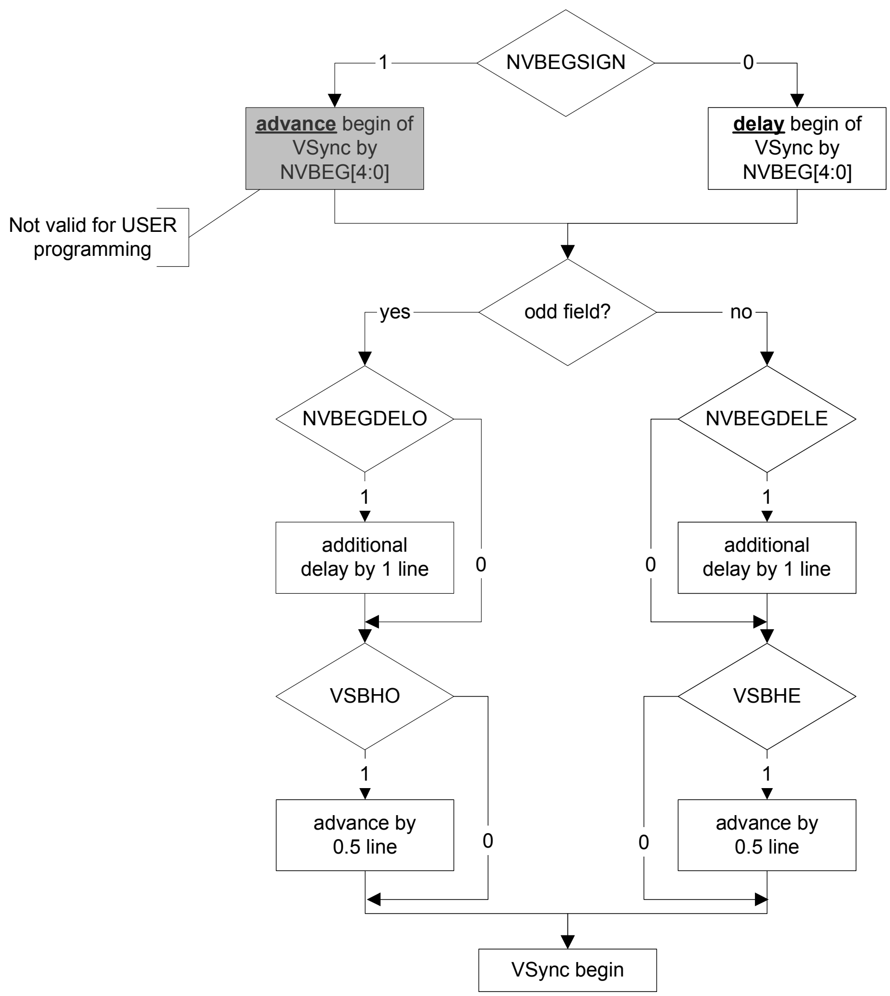


Figure 54: NTSC VSYNC Begin

NVBEGDELO NTSC VSync Begin Delay on Odd Field, *Address 0xE5, [7]*
Function

NVBEGDELO	Description
0 ⊂	No delay
1	Delays VSYNC going high on Odd Field by a line relative to NVBEG

NVBEGDELE NTSC Vsync Begin Delay on Even Field, *Address 0xE5, [6]*
Function

NVBEGDELE	Description
0 ⊂	No delay
1	Delays VSYNC going high on Even Field by a line relative to NVBEG

NVBEGSIGN NTSC Vsync Begin Sign, *Address 0xE5, [5]*
Function

NVBEGSIGN	Description
0	Delays Start of VSYNC: set for user manual programming
1⊂	Advances Start of VSYNC: not recommended for user programming

NVBEG[4:0] NTSC Vsync Begin, *Address 0xE5, [4:0]*
Function

NVBEG	Description
00101 ⊂	NTSC VSYNC begin position

Note: For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC on the VS pin are modified.

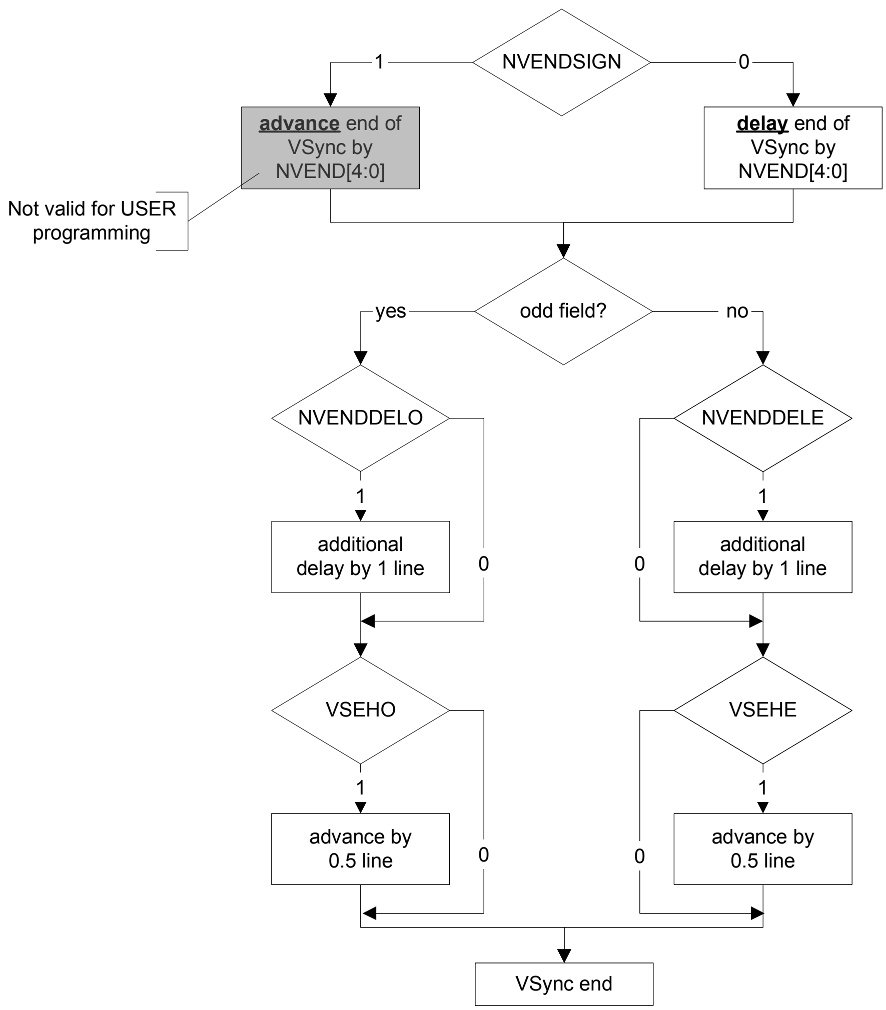


Figure 55: NTSC VSYNC End

NVENDDELO NTSC Vsync End Delay on Odd Field, *Address 0xE6, [7]*

Function

NVENDDELO	Description
0 ⊂	No delay
1	Delays VSYNC going low on Odd Field by a line relative to NVEND

NVENDDELE NTSC Vsync End Delay on Even Field, *Address 0xE6, [6]*

Function

NVENDDELE	Description
0 ⊂	No delay
1	Delays VSYNC going low on Even Field by a line relative to NVEND

NVENDSIGN NTSC Vsync End Sign, *Address 0xE6, [5]*

Function

NVENDSIGN	Description
0 ⊂	Delays End of VSYNC: set for user manual programming
1	Advances End of VSYNC: not recommended for user programming

NVEND NTSC[4:0] Vsync End, *Address 0xE6, [4:0]*

Function

NVEND	Description
00100 ⊂	NTSC VSYNC end position

Note: For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC on the VS pin are modified.

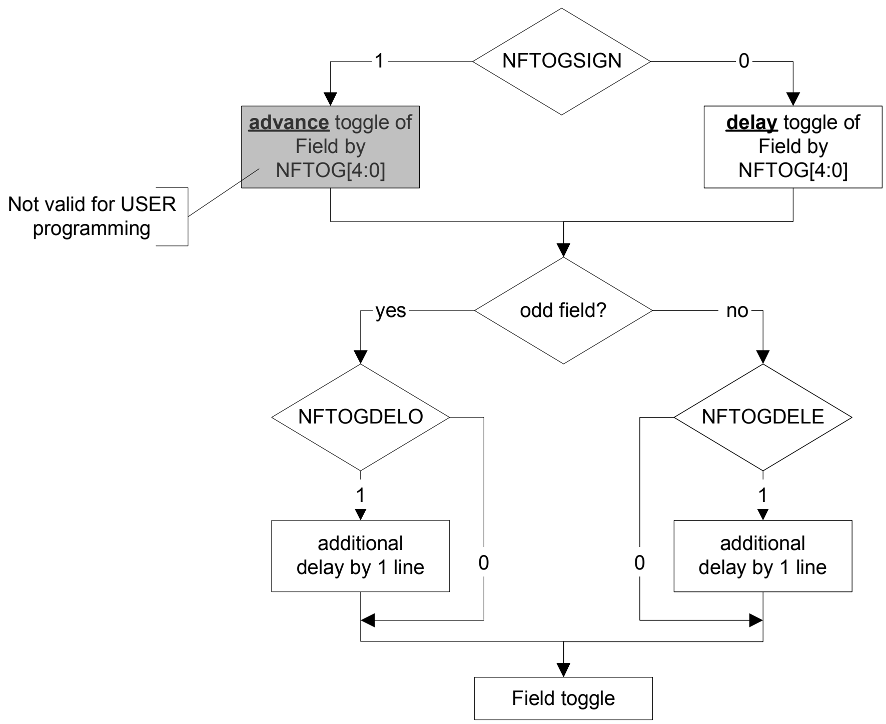


Figure 56: NTSC F Toggle

NFTOGDELO NTSC Field Toggle Delay on Odd Field, *Address 0xE7, [7]*

Function

NFTOGDELO	Description
0 ⊂	No delay
1	Delays F toggle/transition on Odd field by a line relative to NFTOG

NFTOGDELE NTSC Field Toggle Delay on Even Field, *Address 0xE7, [6]*

Function

NFTOGDELE	Description
0	No delay
1⊂	Delays F toggle/transition on Even field by a line relative to NFTOG

NFTOGSIGN NTSC Field Toggle Sign, *Address 0xE7, [5]*

Function

NFTOGSIGN	Description
0	Delays Field transition: set for user manual programming
1⊂	Advances Field transition: not recommended for user programming

NFTOG[4:0] NTSC Field Toggle, *Address 0xE7, [4:0]*

Function

NFTOG	Description
00011 ⊂	NTSC Field toggle position

Note: For all NTSC/PAL Field timing controls, both the F bit in the AV code and the Field signal on the FIELD/DE pin are modified.

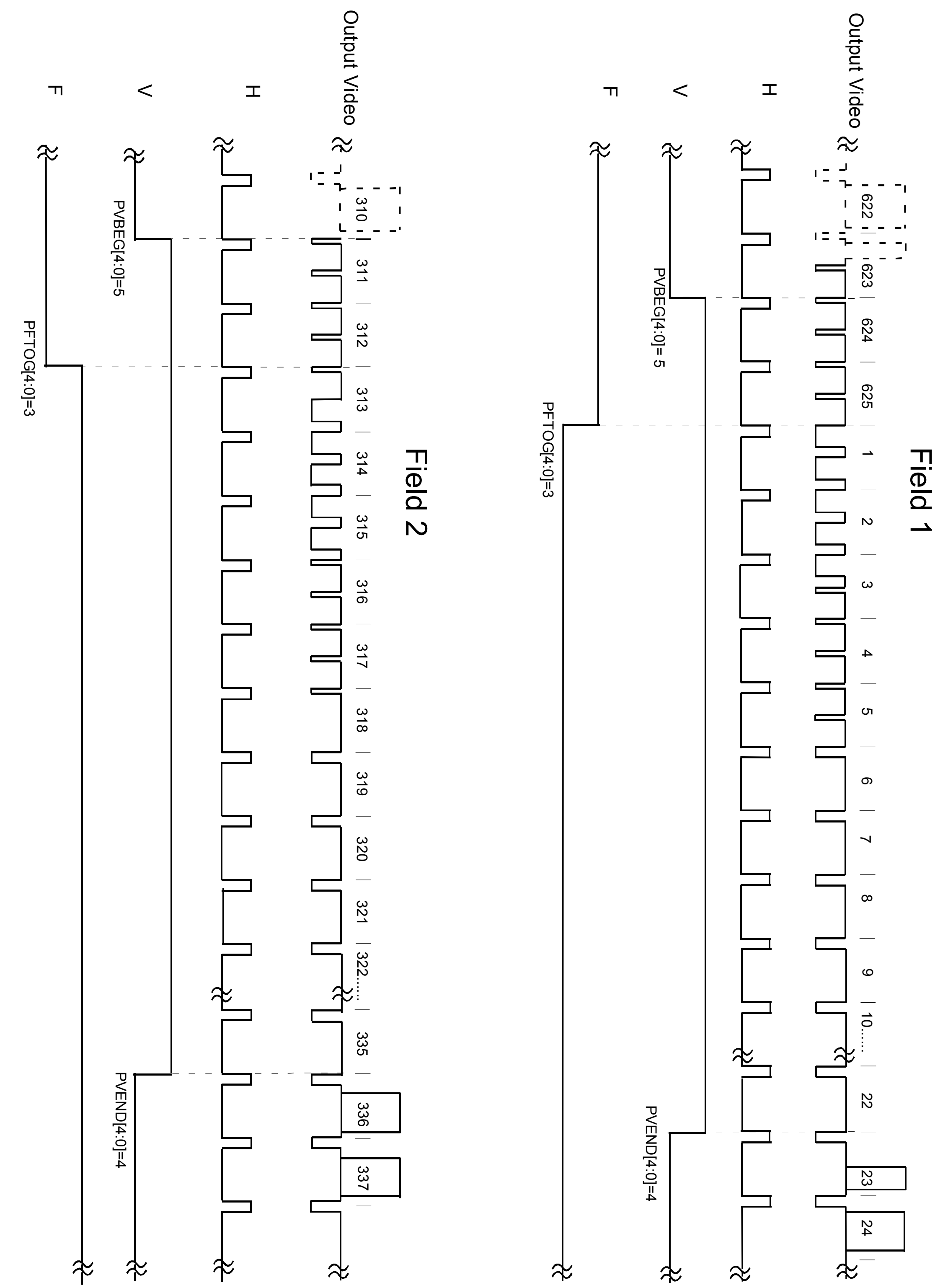


Figure 57: PAL Default (BT.656) (Polarity of H, V and F Embedded in Data)

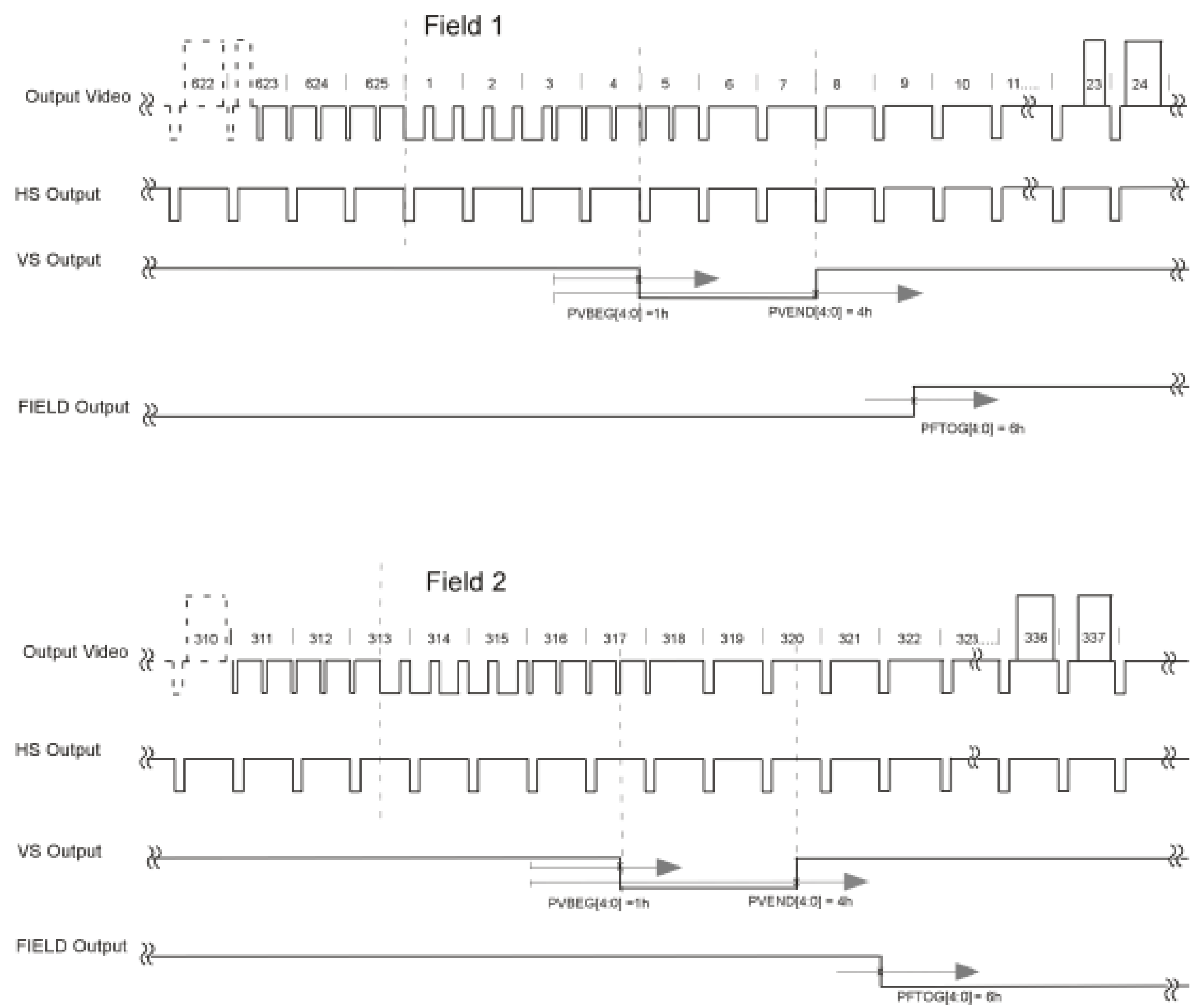


Figure 58: PAL Typical VSYNC/Field Positions Using Register Writes in Table 21

Table 21: Recommended User Settings for PAL

Refer to Figure 57.

Register (Hex)	Register Name	Write (Hex)
0x31	VSYNC Field Control 1	0x1A
0x32	VSYNC Field Control 2	0x81
0x33	VSYNC Field Control 3	0x84
0x34	HSYNC Pos. Control 1	0x00
0x35	HSYNC Pos. Control 2	0x00
0x36	HSYNC Pos. Control 3	0x7D
0x37	Polarity	0xA1
0xE8	NTSC_V_Bit_Beg	0x41
0xE9	NTSC_V_Bit_End	0x84
0xEA	NTSC_F_Bit_Tog	0x06

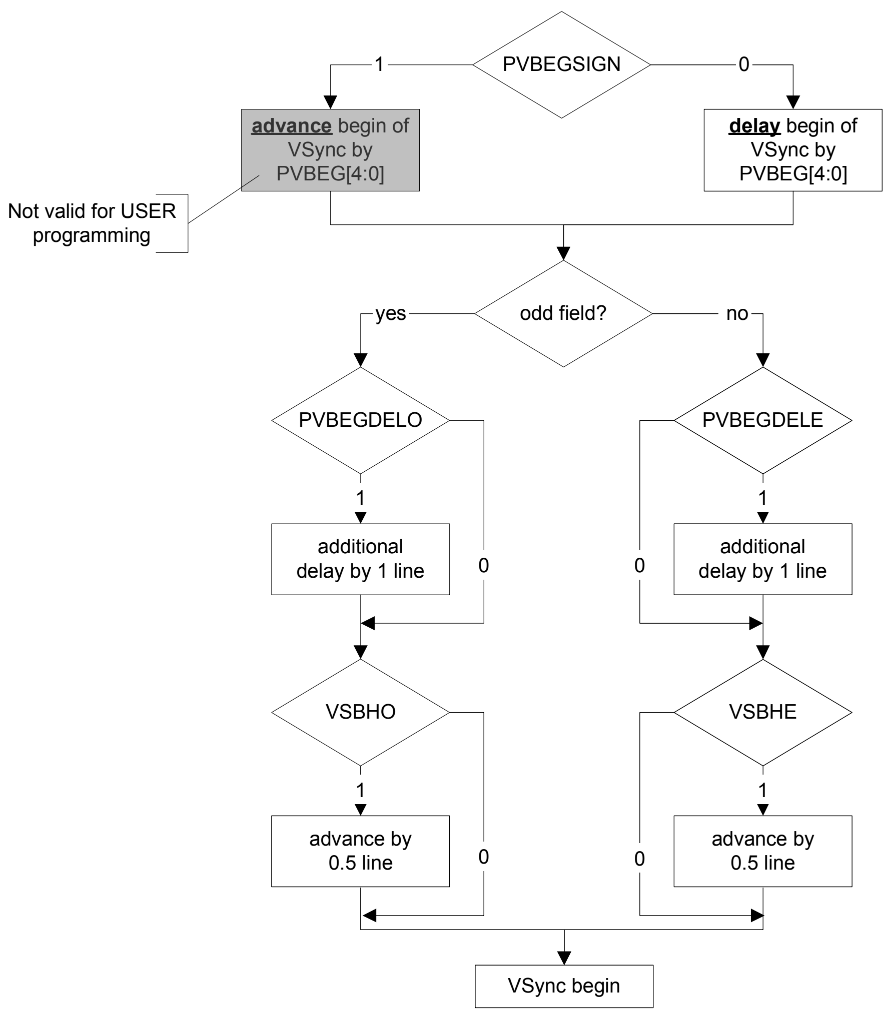


Figure 59: PAL VSYNC Begin

PVBEGDELO PAL Vsync Begin Delay on Odd Field, *Address 0xE8, [7]*

Function

PVBEGDELO	Description
0	No delay
1	Delays VSYNC going high on Odd Field by a line relative to PVBEG

PVBEGDELE PAL Vsync Begin Delay on Even Field, *Address 0xE8, [6]*

Function

PVBEGDELE	Description
0	No delay
1	Delays VSYNC going high on Even Field by a line relative to PVBEG

PVBEGSIGN PAL Vsync Begin Sign, *Address 0xE8, [5]*

Function

PVBEGSIGN	Description
0	Delays begin of VSYNC: set for user manual programming
1	Advances begin of VSYNC: not recommended for user programming

PVBEG[4:0] PAL Vsync Begin, *Address 0xE8, [4:0]*

Function

PVBEG	Description
00101	PAL VSYNC begin position

Note: For all NTSC/PAL Field timing controls, both the F bit in the AV code and the Field signal on the FIELD/DE pin are modified.

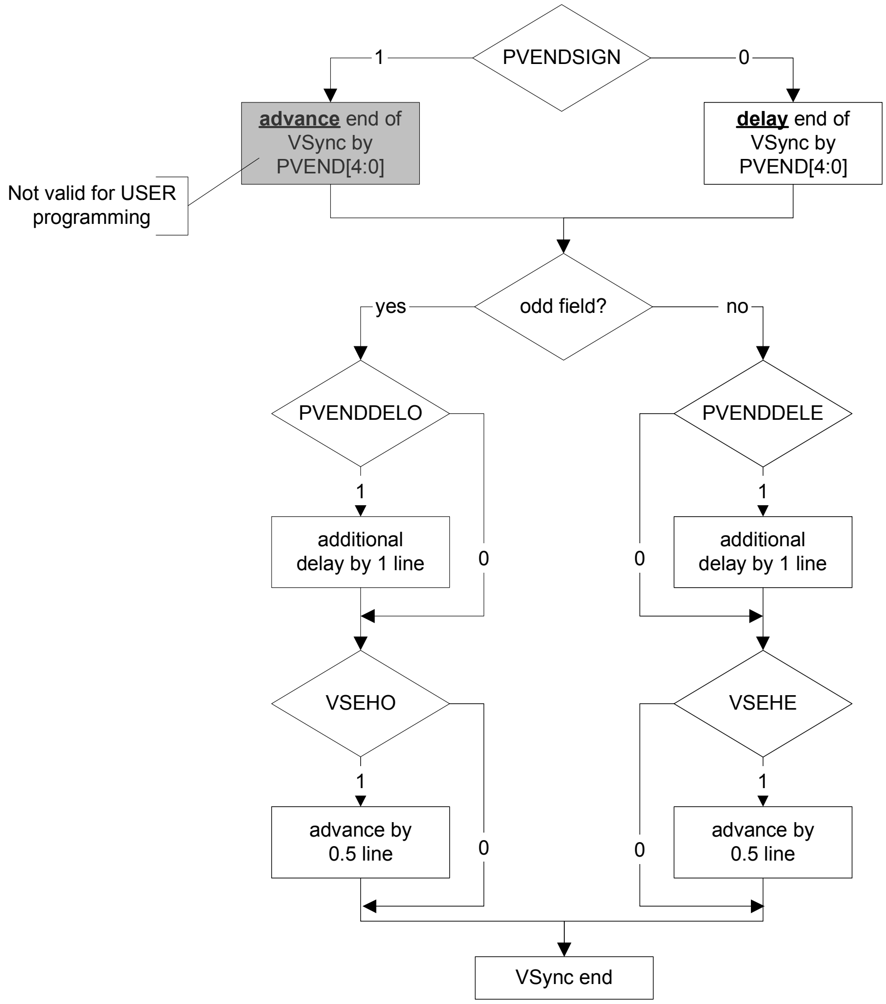


Figure 60: PAL VSYNC End

PVENDDELO PAL Vsync End Delay on Odd Field, *Address 0xE9,[7]*

Function

PVENDDELO	Description
0 ⊂	No delay
1	Delays VSYNC going low on Odd Field by a line relative to PVEND

PVENDDELE PAL Vsync End Delay on Even Field, *Address 0xE9,[6]*

Function

PVENDDELE	Description
0 ⊂	No delay
1	Delays VSYNC going low on Even Field by a line relative to PVEND

PVENDSIGN PAL Vsync End Sign, *Address 0xE9, [5]*

Function

PVENDSIGN	Description
0 ⊂	Delays End of VSYNC: set for user manual programming
1	Advances End of VSYNC: not recommended for user programming

PVEND[4:0] PAL Vsync End, *Address 0xE9, [4:0]*

Function

PVEND	Description
10100 ⊂	PAL VSYNC end position

Note: For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC on the VS pin are modified.

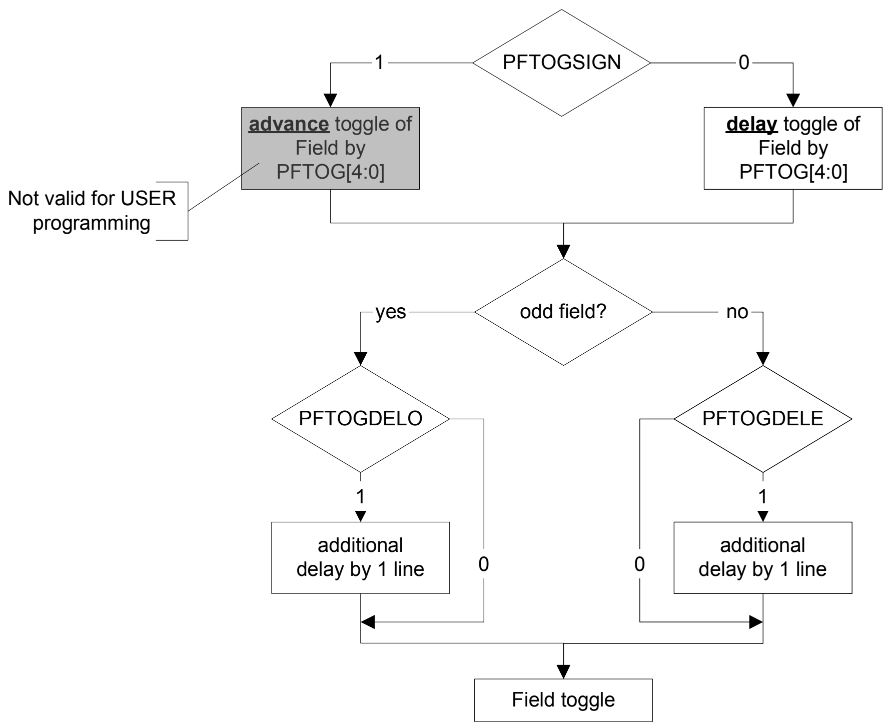


Figure 61: PAL F Toggle

PFTOGDELO PAL Field Toggle Delay on Odd Field, *Address 0xEA, [7]*

Function

PFTOGDELO	Description
0 ⊂	No delay
1	Delays F toggle/transition on Odd field by a line relative to PFTOG

PFTOGDELE PAL Field Toggle Delay on Even Field, *Address 0xEA, [6]*

Function

PFTOGDELE	Description
0	No delay
1⊂	Delays F toggle/transition on Even field by a line relative to PFTOG

PFTOGSIGN PAL Field Toggle Sign, *Address 0xEA, [5]*

Function

PFTOGSIGN	Description
0	Delays Field transition: set for user manual programming
1⊂	Advances Field transition: not recommended for user programming

PFTOG PAL Field Toggle, *Address 0xEA, [4:0]*

Function

PFTOG	Description
00011 ⊂	PAL Field toggle position

Note: For all NTSC/PAL Field timing controls, both the F bit in the AV code and the Field signal on the FIELD/DE pin are modified.

8.16 SDP Synchronization Processing

The ADV7181C has two additional sync processing blocks that post-process the raw synchronization information extracted from the digitized input video. If desired, the blocks can be disabled via the following two I^2C bits.

ENHSPLL Enable HSync PLL (SDP), *Address 0x01, [6]*

The HSYNC PLL is designed to filter incoming H Syncs corrupted by noise, providing much improved performance for video signals with stable timebase but poor SNR.

Notes:

- For CVBS PAL/NTSC, YC PAL/NTSC enable HSYNC PLL
- For SECAM, disable HSYNC PLL
- For YPbPr, through SDP, disable HSYNC PLL

Function

ENHSPLL	Description
0	Disables HSYNC PLL
1⊂	Enables HSYNC PLL

ENVSPROC Enable VSync Processor (SDP), *Address 0x01, [3]*

This block provides extra filtering of the detected Vsyncs to give improved vertical lock.

Function

ENVSPROC	Description
0	Disables VSYNC Processor
1⊂	Enables VSYNC Processor

8.17 SDP VBI Data Decode

There are two VBI data slicers in the ADV7181C. The first is called the VBI data processor (VDP) and the second is called the VBI system 2. System 2 can slice Gemstar and Closed Caption data only.

The VDP can slice both low bandwidth and high bandwidth standards such as Teletext.

8.18 SDP VDP VBI Data Slicer

The VBI Data Processor (VDP) of the ADV7181C is capable of slicing multiple VBI data standards on SD video. The VDP decodes the VBI data on the incoming CVBS/YC or YUV data processed by the SDP core. The VDP cannot decode VBI data on the YUV data processed through the CP core.
The decoded results are available as ancillary data in output 656 data stream. For low data rate VBI standards like CC/WSS/CGMS user can read the decoded data bytes from I^2C registers.

The VBI data standards that can be decoded by the VDP are:

PAL

• Teletext System A or C or D	ITU-BT-653
• Teletext System B/WST	ITU-BT-653
• VPS (Video Programming System)	ETSI EN 300 231 V 1.3.1
• VITC (Vertical Interval Time Codes)	
• WSS (Wide Screen Signaling)	BT.1119-1/ETSI.EN.300294
• CCAP (Closed Captioning)	

NTSC

• Teletext System B and D	ITU-BT-653
• Teletext System C/NABTS	ITU-BT-653/EIA-516
• VITC (Vertical Interval Time Codes)	
• CGMS (Copy Generation management System)	EIA-J CPR-1204/IEC 61880
• Gemstar	
• CCAP (Closed Captioning)	EIA-608

The VBI data standard that the VDP decodes on a particular line of incoming video has been set by default as described in Table 22. This can be over-ridden manually and any VBI data can be decoded on any line. The details of manual programming are described in Table 23 and Table 24.

8.18.1 VDP Default Configuration

The VDP can decode different VBI data standards on a line-to-line basis. The various standards supported by default on different lines of VBI are explained in Table 22.

Table 22: Default Standards on Lines for PAL and NTSC

PAL – 625/50				NTSC – 525/60			
Line No.	Default VBI DATA Decoded	Line No.	Default VBI DATA Decoded	Line no	Default VBI DATA Decoded	Line no.	Default VBI DATA Decoded
6	WST	318	VPS	23	Gemstar-1x	-	-
7	WST	319	WST	24	Gemstar-1x	286	Gemstar-1x
8	WST	320	WST	25	Gemstar-1x	287	Gemstar-1x
9	WST	321	WST	-	-	288	Gemstar-1x
10	WST	322	WST	-	-	-	-
11	WST	323	WST	-	-	-	-
12	WST	324	WST	10	NABTS	272	NABTS
13	WST	325	WST	11	NABTS	273	NABTS
14	WST	326	WST	12	NABTS	274	NABTS
15	WST	327	WST	13	NABTS	275	NABTS
16	VPS	328	WST	14	VITC	276	NABTS
17	-	329	VPS	15	NABTS	277	VITC
18	-	330	-	16	VITC	278	NABTS
19	VITC	331	-	17	NABTS	279	VITC
20	WST	332	VITC	18	NABTS	280	NABTS
21	WST	333	WST	19	NABTS	281	NABTS
22	CCAP	334	WST	20	CGMS	282	NABTS
23	WSS	335	CCAP	21	CCAP	283	CGMS
24 + Full ODD Field	WST	336	WST	22 + Full ODD Field	NABTS	284	CCAP
		337 + Full EVEN Field	WST			285 + Full EVEN Field	NABTS

MAN_LINE_PGM (VDP), *Address 0x64, [7] User Sub Map*

The user can configure the VDP to decode different standards on a line-to-line basis through manual line programming. For this, the user has to set MAN_LINE_PGM bit. The user needs to write into all the line programming registers, VBI_DATA_Px_Ny (User Sub Map, Registers 0x64 to 0x77)

Function

MAN_LINE_PGM	Description
0	Decode default standards on lines as in Table 22
1	Manually program the VBI standards to be decoded

VBI_DATA_Px_Ny[3:0] (VDP), *Address 0x64-0x77, User Sub Map*

These are related 4-bit clusters contained from register 0x64 to register 0x77 in the User Sub Map. VBI_DATA_Px_Ny, which is the 4-bit line programming register, identifies the VBI data standard to be decoded. If the SDP is in PAL mode, it is decoded on line number X. If the SDP is in NTSC mode, it is decoded on line number Y. The different types of VBI standards decoded by VBI_DATA_Px_Ny are shown in Table 23. Note that the interpretation of its value depends on whether the SDP is in PAL or NTSC mode.

Table 23: VBI Data Standards

VBI_DATA_Px_Ny[3:0]	625/50 – PAL	525/60 – NTSC
0000	Disable VDP	Disable VDP
0001	Teletext system identified by VDP_TTXT_TYPE	Teletext system identified by VDP_TTXT_TYPE
0010	VPS – ETSI EN 300 231 V 1.3.1	Reserved
0011	VITC	VITC
0100	WSS BT.1119-1/ETSI.EN.300294	CGMS EIA-J CPR-1204/IEC 61880
0101	Reserved	Gemstar_1X
0110	Reserved	Gemstar_2X
0111	CCAP	CCAP EIA-608
1000 - 1111	Reserved	Reserved

Table 24: VBI_DATA_Px_Ny [3:0] Values Indicating VBI Data Standard to be Decoded on Line x (for PAL) or y (for NTSC)

Signal Name	Register Location	Address	
		Dec	Hex
Vbi_data_p6_n23	VDP_Line_00F[7:4]	101	0x65
Vbi_data_p7_n24	VDP_Line_010[7:4]	102	0x66
Vbi_data_p8_n25	VDP_Line_011[7:4]	103	0x67
Vbi_data_p9	VDP_Line_012[7:4]	104	0x68
Vbi_data_p10	VDP_Line_013[7:4]	105	0x69
Vbi_data_p11	VDP_Line_014[7:4]	106	0x6A
Vbi_data_p12_n10	VDP_Line_015[7:4]	107	0x6B
Vbi_data_p13_n11	VDP_Line_016[7:4]	108	0x6C
Vbi_data_p14_n12	VDP_Line_017[7:4]	109	0x6D
Vbi_data_p15_n13	VDP_Line_018[7:4]	110	0x6E
Vbi_data_p16_n14	VDP_Line_019[7:4]	111	0x6F
Vbi_data_p17_n15	VDP_Line_01A[7:4]	112	0x70
Vbi_data_p18_n16	VDP_Line_01B[7:4]	113	0x71
Vbi_data_p19_n17	VDP_Line_01C[7:4]	114	0x72
Vbi_data_p20_n18	VDP_Line_01D[7:4]	115	0x73
Vbi_data_p21_n19	VDP_Line_01E[7:4]	116	0x74
Vbi_data_p22_n20	VDP_Line_01F[7:4]	117	0x75
Vbi_data_p23_n21	VDP_Line_020[7:4]	118	0x76
Vbi_data_p24_n22	VDP_Line_021[7:4]	119	0x77
Vbi_data_p318	VDP_Line_00E[3:0]	100	0x64
Vbi_data_p319_n286	VDP_Line_00F[3:0]	101	0x65
Vbi_data_p320_n287	VDP_Line_010[3:0]	102	0x66
Vbi_data_p321_n288	VDP_Line_011[3:0]	103	0x67
Vbi_data_p322	VDP_Line_012[3:0]	104	0x68
Vbi_data_p323	VDP_Line_013[3:0]	105	0x69
Vbi_data_p324_n272	VDP_Line_014[3:0]	106	0x6A

Signal Name	Register Location	Address	
		Dec	Hex
Vbi_data_p325_n273	VDP_Line_015[3:0]	107	0x6B
Vbi_data_p326_n274	VDP_Line_016[3:0]	108	0x6C
Vbi_data_p327_n275	VDP_Line_017[3:0]	109	0x6D
Vbi_data_p328_n276	VDP_Line_018[3:0]	110	0x6E
Vbi_data_p329_n277	VDP_Line_019[3:0]	111	0x6F
Vbi_data_p330_n278	VDP_Line_01A[3:0]	112	0x70
Vbi_data_p331_n279	VDP_Line_01B[3:0]	113	0x71
Vbi_data_p332_n280	VDP_Line_01C[3:0]	114	0x72
Vbi_data_p333_n281	VDP_Line_01D[3:0]	115	0x73
Vbi_data_p334_n282	VDP_Line_01E[3:0]	116	0x74
Vbi_data_p335_n283	VDP_Line_01F[3:0]	117	0x75
Vbi_data_p336_n284	VDP_Line_020[3:0]	118	0x76
Vbi_data_p337_n285	VDP_Line_021[3:0]	119	0x77

Notes:

- Full field detection (lines other than VBI lines) of any standard can also be enabled by writing into the registers VBI_data_p24_n22 [3:0] and Vbi_data_p337_n285 [3:0]. So, if VBI_data_p24_n22 [3:0] is programmed with any Teletext standard, then Teletext is decoded off the whole of the ODD field. The corresponding register for the EVEN field is Vbi_data_p337_n285 [3:0].

- Teletext System Identification
  VDP assumes that if Teletext is present in a video channel, all the Teletext lines will comply with a single standard system. Thus, the line programming using VBI_DATA_Px_Ny registers identifies whether the data in line is Teletext and further the actual standard is identified by the VDP_TTXT_TYPE_MAN bit. To program the VDP_TTXT_TYPE_MAN bit, the VDP_TTXT_TYPE_MAN_ENABLE bit must be set to 1.

VDP_TTXT_TYPE_MAN_ENABLE (VDP), *Address 0x60, [2], User Sub Map*

This bit enables manual selection of Teletext Type

Function

VDP_TTXT_TYPE_MAN_ENABLE	Description
0 ⊂	User Programming of Teletext type is disabled
1	User Programming of Teletext type is enabled

VDP_TTXT_TYPE_MAN[1:0] (VDP), *Address 0x60, [1:0], User Sub Map*

These bits specify the Teletext type to be decoded. These bits are functional only if VDP_TTXT_TYPE_MAN_ENABLE is set to 1.

Function

VDP_TTXT_TYPE_MAN[1:0]	Description	
	625/50 (PAL)	525/60 (NTSC)
00 ⊂	Teletext-ITU-BT.653- 625/50-A	Reserved
01	Teletext-ITU-BT.653- 625/50-B (WST)	Teletext-ITU-BT.653-525/60-B
10	Teletext-ITU-BT.653- 625/50-C	Teletext-ITU-BT.653-525/60-C or EIA516 (NABTS)
11	Teletext-ITU-BT.653- 625/50-D	Teletext-ITU-BT.653-525/60-D

8.18.2 VDP Ancillary Data Output

Reading the data back via I^2C may not be feasible for VBI data standards with high data rates (e.g. Teletext). An alternative is to place the sliced data in a packet in the line blanking of the digital output CCIR656 stream. This is available for all standards sliced by the VDP module.

When data have been sliced on a given line, the corresponding ancillary data packet is placed immediately after the next EAV code that occurs at the output (i.e. sliced data from multiple lines are not buffered up and then emitted in a burst). Note that the line number on which the packet is placed will differ from the line number on which the data was sliced due to the vertical delay through the comb filters.

The user can enable or disable the insertion of VDP decoded results into the 656 Ancillary Streams by using ADF_ENABLE bit.

ADF_ENABLE (VDP), *Address 0x62, [7], User Sub Map*

This bit enables ancillary data output through 656 stream

Function

ADF_ENABLE	Description
0 ⊂	Disable insertion of VBI decoded data into ancillary 656 stream
1	Enable insertion of VBI decoded data into ancillary 656 stream

The user may select the Data Identification Word (DID) and the Secondary Data Identification word (SDID) through programming ADF_DID [4:0] and ADF_SDID [5:0] registers respectively, as explained below.

ADF_DID[4:0] (VDP), *Address 0x62 [4:0], User Sub Map*

This bit selects the Data ID word to be inserted in the Ancillary data stream. The default value of ADF_DID[4:0] is 10101b.

Function

ADF_DID	Description
xxxx	User specified DID sent in the ancillary stream with VDP decoded data

ADF_SDID[5:0] (VDP), *Address 0x63 [5:0], User Sub Map*

This bit selects the Secondary Data ID word to be inserted in the Ancillary data stream. The default value of ADF_SDID[5:0] is 101010b.

Function

ADF_SDID	Description
xxxxx	User specified SDID sent in the ancillary stream with VDP decoded data

DUPLICATE_ADF (VDP), *Address 0x63 [7], User Sub Map*

This bit determines whether the Ancillary data is duplicated over both Y and C buses or if the data packets are spread between the 2 channels.

Function

DUPLICATE_ADF	Description
0 ⊂	Ancillary data packet is spread across the Y and C data streams
1	Ancillary data packet is duplicated on the Y and C data streams

ADF_MODE[1:0] (VDP), *Address 0x62, [6:5], User Sub Map*

These bits determine if the Ancillary data output mode is in Byte Mode or Nibble mode.

Function

ADF_MODE	Description
00 ⊂	Nibble Mode (Default)
01	Byte Mode, no code restrictions
10	Byte Mode but 00_h and FF_h prevented (00_h -> 01_h, FF_h -> FE_h)
11	Reserved

The ancillary data packet sequence is explained in Table 25. The "Nibble Output Mode" is the default mode of output from Ancillary stream when ancillary stream output is enabled. This format is in compliance with ITU-R BT.1364.

Definitions of the abbreviations used in Table 25 and Table 26 are provided below.

- **EP**
  Even parity for bits B8-B2. This means that the parity bit EP is set so that there is an even number of 1s in bits in B8-B2. This means that the parity bit EP is set so that there is an even number of 1s in bits in B8-B2, including the parity bit, D8.

- **CS**
  Checksum word. The CS word is used to increase confidence of the integrity of the ancillary data packet from the DID, SDID, DC through the UDWs. It consists of 10 bits, a 9-bit calculated value and B9 as the inverse of B8. The checksum value B8-B0 is equal to the 9 least significant bits of sum of the 9 least significant bits of the DID, SDID, DC and all UDWs in the packet. Prior to the start of the checksum count cycle all checksum and carry bits are preset to zero. Any carry out resulting from the checksum count cycle is ignored.

- $\overline{\textbf{EP}}$
  The MSB B9 is the inverse EP and this ensures that restricted codes 0x00 and 0xFF will not occur.

- **Line_number[9:0]**
  The line number of the line that immediately precedes the Ancillary Data Packet. The line number is as per the numbering system in ITU-R BT.470. The line number runs from 1-625 in a 625 line system and from 1-263 in a 525 line system. Note the line number on which the packet is output will differ from the line number on which the VBI data were sliced due to the vertical delay through the comb filters.

- **Data Count**
  The data count specifies the number of User data words in the Ancillary stream for the standard. The *total number of user data words = 4 * Data Count.* Padding words may be introduced to make the total number of user data words divisible by four.

Table 25: Ancillary Data in Nibble Output Format

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	0	0	0	Ancillary Data Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	$\overline{EP}$	EP		I2c_did6_2[4:0]					0	0	DID- Data identification word
4	$\overline{EP}$	EP	I2c_sdid7_2[5:0]						0	0	SDID- Secondary data identification word
5	$\overline{EP}$	EP	0	DC[4:0]					0	0	Data Count
6	$\overline{EP}$	EP	padding[1:0]		VBI_DATA_STD[3:0]				0	0	ID0 – user data word 1
7	$\overline{EP}$	EP	0	Line_number[9:5]					0	0	ID1 – user data word 2
8	$\overline{EP}$	EP	Even_Field	Line_number[4:0]					0	0	ID2 – user data word 3
9	$\overline{EP}$	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0	ID3 – user data word 4
10	$\overline{EP}$	EP	0	0	Vbi_word_1[7:4]				0	0	User data word 5
11	$\overline{EP}$	EP	0	0	Vbi_word_1[3:0]				0	0	User data word 6
12	$\overline{EP}$	EP	0	0	Vbi_word_2[7:4]				0	0	User data word 7
13	$\overline{EP}$	EP	0	0	Vbi_word_2[3:0]				0	0	User data word 8
14	$\overline{EP}$	EP	0	0	Vbi_word_3[7:4]				0	0	User data word 9
.	.	.	.	.	.	.	.	.	.	.	(Pad 0x200, these padding words may or may not be present depending on ancillary data type.) User data word.
.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	
n-3	1	0	0	0	0	0	0	0	0	0	
n-2	1	0	0	0	0	0	0	0	0	0	
n-1	$\overline{B8}$	Checksum							0	0	

Table 26: Ancillary Data in Byte Output Format

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	0	0	0	Ancillary Data Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	$\overline{\text{EP}}$	EP		I2c_did6_2[4:0]					0	0	DID - Data identification word
4	$\overline{\text{EP}}$	EP	I2c_sdid7_2[5:0]						0	0	SDID- Secondary data identification word
5	$\overline{\text{EP}}$	EP	0	DC[4:0]					0	0	Data Count
6	$\overline{\text{EP}}$	EP	padding[1:0]		VBI_DATA_STD[3:0]				0	0	ID0 – user data word 1
7	$\overline{\text{EP}}$	EP	0	Line_number[9:5]					0	0	ID1 – user data word 2
8	$\overline{\text{EP}}$	EP	Even_Field	Line_number[4:0]					0	0	ID2 – user data word 3
9	$\overline{\text{EP}}$	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0	ID3 – user data word 4
10	Vbi_word_1[7:0]								0	0	User data word 5
11	Vbi_word_2[7:0]								0	0	User data word 6
12	Vbi_word_3[7:0]								0	0	User data word 7
13	Vbi_word_4[7:0]								0	0	User data word 8
14	Vbi_word_5[7:0]								0	0	User data word 9
.	.	.	.	.	.	.	.	.	.	.	(Pad 0x200, these padding words may or may not be present depending on ancillary data type.) User data word
.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	
n-3	1	0	0	0	0	0	0	0	0	0	
n-2	1	0	0	0	0	0	0	0	0	0	
n-1	$\overline{\text{B8}}$	Checksum							0	0	

Note that the Byte output mode does **not** fully comply with ITU-R BT.1364.S

Structure of VBI Words in Ancillary Data Stream

Each VBI data standard has been split into a clock-run-in (CRI), a framing code (FC) and a number of data-bytes (n). The data packet in the ancillary stream will include only the FC and data bytes. Table 27 shows the format of the Vbi_word_x in the ancillary data stream.

Table 27: Structure of VBI Data Words in Ancillary Stream

Vbi_word_1	FC0	Framing code [23:16]
Vbi_word_2	FC1	Framing Code [15:8]
Vbi_word_3	FC2	Framing Code [7:0]
Vbi_word_4	DB1	1st data byte
…	...	…
Vbi_word_n+3	DBn	Last (nth) Data byte

Framing Code

The length of the actual framing code depends on the VBI data standard. For uniformity, the length of the framing code reported in the ancillary data stream is always 24 bits. For standards with a lesser framing code length, the extra LSB bits would be set to 0. The valid length of the framing code can be decoded from the VBI_DATA_STD bit available in ID0 (User Data Word 1). The framing code is always reported in the inverse-transmission order. Table 28 shows the framing code and its valid length for VBI data standards supported by the VDP.

Table 28: Framing Code Sequence for Different VBI Standards

VBI Standard	**Framing code length in bits**	**Error Free Framing Code bits (In the order of Transmission)**	**Error Free Framing Code given out by VDP (In the reversed order of transmission)**
TTXT_SYSTEM_A (PAL)	8	1110_0111	1110_0111
TTXT_SYSTEM_B (PAL)	8	1110_0100	0010_0111
TTXT_SYSTEM_B (NTSC)	8	1110_0100	0010_0111
TTXT_SYSTEM_C (PAL and NTSC)	8	1110_0111	1110_0111
TTXT_SYSTEM_D (PAL and NTSC)	8	1110_0101	1010_0111
VPS (PAL)	16	1000_1010_10001_1001	1001_1001_0101_0001
VITC (NTSC and PAL)	1	0	0
WSS (PAL)	24	0001_1110_0011_1100_0001_1111	1111_1000_0011_1100_0111_1000
GEMSTAR_1X (NTSC)	3	001	100
GEMSTAR_2X (NTSC)	11	1001_1011_101	101_1101_1001
CCAP (NTSC and PAL)	3	001	100
CGMS (NTSC)	1	0	0

Example:

For Teletext (B-WST), the Framing code byte is 1110_0100$_b$ (0xE4) (bits shown in the order of transmission). Thus, Vbi_word_1 = 0x27, vbi_word_2 = 0x00 and vbi_word_3 = 0x00. Translating them into UDWs in ancillary data stream,

For the nibble mode:

UDW5 [5:2] = 0010
UDW6 [5:2] = 0111
UDW7 [5:2] = 0000 (undefined bits made zeros)
UDW8 [5:2] = 0000 (undefined bits made zeros)
UDW9 [5:2] = 0000 (undefined bits made zeros)
UDW10 [5:2] = 0000 (undefined bits made zeros)

For the byte mode:

UDW5 [9:2] = 0010_0111
UDW6 [9:2] = 0000_0000 (undefined bits made zeros)
UDW7 [9:2] = 0000_0000 (undefined bits made zeros)

Data Bytes

The vbi_word_4 to vbi_word_n+3 contains the data words that were decoded by the VDP in the transmission order. The position of bits in bytes is in the inverse transmission order.
For example, closed caption has two user data bytes, as shown in Table 29. The data bytes in the ancillary data stream would be as follows:

Vbi_word_4 = Byte1 [7:0]
Vbi_word_5 = Byte2 [7:0]

The number of vbi_words for each VBI data standard and the total number of UDWs in the ancillary data stream is shown in Table 29.

Table 29: Total User Data Words for Different VBI Standards

VBI Standard	ADF Mode	4 ID user data words	Framing_ code UDWs	VBI data words	Number of Padding words	Total Number of User Data words
TTXT_SYSTEM_A (PAL)	00 (Nibble Mode)	4	6	74	0	84
	01,10 (Byte Mode)	4	3	37	0	44
TTXT_SYSTEM_B (PAL)	00 (Nibble Mode)	4	6	84	2	96
	01,10 (Byte Mode)	4	3	42	3	52
TTXT_SYSTEM_B (NTSC)	00 (Nibble Mode)	4	6	68	2	80
	01,10 (Byte Mode)	4	3	34	3	44
TTXT_SYSTEM_C (PAL and NTSC)	00 (Nibble Mode)	4	6	66	0	76
	01,10 (Byte Mode)	4	3	33	2	42
TTXT_SYSTEM_D (PAL and NTSC)	00 (Nibble Mode)	4	6	68	2	80
	01,10 (Byte Mode)	4	3	34	3	44
VPS (PAL)	00 (Nibble Mode)	4	6	26	0	36
	01,10 (Byte Mode)	4	3	13	0	20
VITC (NTSC and PAL)	00 (Nibble Mode)	4	6	18	0	28
	01,10 (Byte Mode)	4	3	9	0	16
WSS (PAL)	00 (Nibble Mode)	4	6	4	2	16
	01,10 (Byte Mode)	4	3	2	3	12
GEMSTAR_1X (NTSC)	00 (Nibble Mode)	4	6	4	2	16
	01,10 (Byte Mode)	4	3	2	3	12
GEMSTAR_2X (NTSC)	00 (Nibble Mode)	4	6	8	2	20
	01,10 (Byte Mode)	4	3	4	1	12
CCAP (NTSC and PAL)	00 (Nibble Mode)	4	6	4	2	16
	01,10 (Byte Mode)	4	3	2	3	12
CGMS (NTSC)	00 (Nibble Mode)	4	6	6	0	16
	01,10 (Byte Mode)	4	3	3 + 3	2	12

8.18.3 I^2C Interface

Dedicated I^2C readback registers are available for CCAP, CGMS, WSS, Gemstar, VPS, PDC/UTC and VITC. Teletext, being a high data rate standard, is supported only through the ancillary data packet. The details of these registers and their access procedure are described below.

User Interface for I^2C **Readback Registers**

The VDP decodes all enabled VBI data standards in real time. The I^2C access speed being much lower than the decoded rate, it is possible that when the registers are being accessed, they get updated with data from the next line. In order to avoid this, VDP has a self-clearing CLEAR bit and an AVAILABLE status bit accompanying all the I^2C readback registers.

The user has to clear the I^2C readback register by writing a HIGH to the CLEAR bit. This will reset the state of AVAILABLE bit to LOW and indicate that the data in the associated readback registers are not valid. After the VDP decodes the next line of the corresponding VBI data, the decoded data would be placed in the I^2C readback register and the AVAILABLE bit would be set to HIGH to indicate that valid data is now available.
Though the VDP will decode this VBI data in subsequent lines, if present, the decoded data will not be updated to the readback registers until the CLEAR bit is set HIGH again. However, this data will be available through the 656 ancillary data packets.

The CLEAR and AVAILABLE bits are in VDP_CLEAR (0x78, User Sub Map – write only register) and VDP_STATUS (0x78, User Sub Map – read only register) registers.

Example I^2C **Readback Procedure**

The following tasks have to be performed to read one packet (line) of PDC data from the decoder.

1. Write “10” to I2C_GS_VPS_PDC_UTC[1:0] (0x9C, User Sub Map) to specify that PDC data has to be updated to I^2C registers.

2. Write HIGH to the GS_PDC_VPS_UTC_CLEAR bit (0x78, User Sub Map) bit to enable I^2C register update.

3. Poll the GS_PDC_VPS_UTC_AVL bit (0x78, User Sub Map) bit going HIGH to check the availability of the PDC packets.

4. Read the data bytes from the PDC I^2C registers. To read another line or packet of data, repeat the above steps.

To read a packet of CC, CGMS, and WSS, steps 2, 3, and 4 only are required since they have dedicated registers.

Content Based Data Update

For certain standards like WSS, CGMS, Gemstar, PDC, UTC, and VPS the information content in the signal transmitted remains the same over numerous lines and the user may want to be notified only when there is a change in the information content or loss of the information content. The user needs to enable content based update for the required standard through the GS_VPS_PDC_UTC_CB_CHANGE and

WSS_CGMS_CB_CHANGE bits. Thus the AVAILABLE bit will show the availability of that standard only when there has been any change in its content.

The content based update also applies to loss of data at the lines where some data was present before. Thus for standards like VPS, Gemstar, CGMS, and WSS if there is no data arrival in their next 4 lines programmed, then the corresponding AVAILABLE bit in the VDP_STATUS register is set HIGH and the content in the I^2C registers for that standard is set to zero. The user has to write HIGH to the CLEAR bit so that whenever a valid line is decoded after some time, the decoded results are available into the I^2C registers, with AVAILABLE status bit set HIGH.

If content based updating is enabled, the AVAILABLE bit will be set HIGH (assuming the CLEAR bit was written) in the following cases:

- The data contents change
- There was some data being decoded and four lines with no data have been detected.
- There was no data being decoded and new data is being decoded.

GS_VPS_PDC_UTC_CB_CHANGE (VDP), *Address 0x9C, [5], User Sub Map*

This bit enables content based update for Gemstar, VPS, PDC, and UTC.

Function

GS_VPS_PDC_UTC_ CB_CHANGE	Description
0	Disable content based update of Gemstar, VPS, PDC, and UTC data
1	Enable content based update of Gemstar, VPS, PDC, and UTC data

WSS_CGMS_CB_CHANGE (VDP), *Address 0x9C, [4], User Sub Map*

This bit enables content based update for WSS and CGMS.

Function

WSS_CGMS_CB_ CHANGE	Description
0	Disable content based update of WSS and CGMS data
1	Enable content based update of WSS and CGMS data

8.18.4 Interrupt Based Reading of I^2C Registers

Some VDP status bits are also linked to the Interrupt Request Controller so that the user does not have to poll the AVAILABLE status bit. The user can configure the Video Decoder to trigger an interrupt request on the $\overline{\text{INT}}$ pin in response to the valid data available in I^2C registers. This function is available for the following data types:

CGMS or WSS: The user can select between triggering an interrupt request each time sliced data are available or triggering an interrupt request only when the sliced data have changed. Selection is via WSS_CGMS_CB_CHANGE bit.

Gemstar, PDC, VPS or UTC: The user can select between triggering an interrupt request each time sliced data are available or triggering an interrupt request only when the sliced data have changed. Selection is via GS_VPS_PDC_UTC_CB_CHANGE bit.

The sequence for the Interrupt based reading of the VDP I^{2}C data registers is the following for the CCAP standard.

1. User unmasks the CCAP interrupt bit (0x50 bit0, User Sub Map = 1). CCAP data occurs on the incoming video. VDP slices CCAP data and places it in the VDP readback registers.
2. The VDP CCAP available bit goes high and the VDP module signals to the interrupt controller to stimulate an interrupt request (for CCAP in this case).
3. The user reads the interrupt status bits in the Interrupt I^{2}C space (User Sub Map) and sees that new CCAP data is available (0x4E bit0, User Sub Map = 1).
4. The user writes 1 to the CCAP interrupt clear bit (0x4F bit0, User Sub Map = 1) in the Interrupt I^{2}C space (this is a self clearing bit). This clears the interrupt on the $\overline{\text{INT}}$ pin but does NOT have an effect in the VDP I^{2}C area.
5. The user reads the CCAP data from the VDP I^{2}C area.
6. The user writes to a bit, CCAP_CLEAR in the VDP_STATUS register, (0x78 bit0, User Sub Map = 1), in the VDP area to signify that the CCAP data was read (=> the VDP CCAP can be updated at the next occurrence of CCAP).
7. Return to step 2.

Interrupt Mask Register Details

The following bits set the interrupt mask on the signal from the VDP VBI data slicer.

VDP_CCAPD_MSKB (VDP), *Address 0x50, [0], User Sub Map*
Function

VDP_CCAPD_MSKB	Description
0 ⊂	Disable interrupt on VDP_CCAPD_Q signal
1	Enable interrupt on VDP_CCAPD_Q signal

VDP_CGMS_WSS_CHNGD_MSKB (VDP), *Address 0x50, [2], User Sub Map*
Function

VDP_CGMS_WSS_ CHNGD_MSKB	Description
0 ⊂	Disable interrupt on VDP_CGMS_WSS_CHNGD_Q signal
1	Enable interrupt on VDP_CGMS_WSS_CHNGD_Q signal

VDP_GS_VPS_PDC_UTC_CHNG_MSKB (VDP), *Address 0x50, [4], User Sub Map*
Function

VDP_GS_VPS_PDC_UTC _CHNG_MSKB	Description
0 ⊂	Disable interrupt on VDP_GS_VPS_PDC_UTC_CHNG_Q signal
1	Enable interrupt on VDP_GS_VPS_PDC_UTC_CHNG_Q signal

VDP_VITC_MSKB (VDP), *Address 0x50, [6], User Sub Map*

Function

VDP_VITC_MSKB	Description
0 ⊂	Disable interrupt on VDP_VITC_Q signal
1	Enable interrupt on VDP_VITC_Q signal

Interrupt Status Register Details

The following read only bits contain data detection information from the VDP module from the time the status bit has last been cleared or unmasked.

VDP_CCAPD_Q (VDP), *Address 0x4E, [0], User Sub Map, Read only*

Function

VDP_CCAPD_Q	Description
0 ⊂	CCAP data has not been detected
1	CCAP data has been detected

VDP_CGMS_WSS_CHNGD_Q (VDP), *Address 0x4E, [2], User Sub Map, Read only*

Function

VDP_CGMS_WSS_CHNGD_Q	Description
0 ⊂	CGMS/WSS data has not been detected
1	CGMS/WSS data has been detected

VDP_GS_VPS_PDC_UTC_CHNG_Q (VDP), *Address 0x4E, [4], User Map, Read only*

Function

VDP_GS_VPS_PDC_UTC_CHNG_Q	Description
0 ⊂	Gemstar, PDC, UTC, VPS data has not been detected
1	Gemstar, VPS, PDC, UTC data has been detected

VDP_VITC_Q (VDP), *Address 0x4E, [6], User Sub Map, Read only*

Function

VDP_VITC_Q	Description
0 ⊂	VITC data has not been detected
1	VITC data has been detected

Interrupt Status Clear Register Details

VDP_CCAPD_CLR (VDP), *Address 0x4F, [0], User Sub Map, write only*

It is not necessary to write 0 to this bit as the bit automatically resets when it is set.

Function

VDP_CCAPD_CLR	Description
0 ⊂	Self clearing bit
1	Clears VDP_CCAP_Q bit

VDP_CGMS_WSS_CHNGD_CLR (VDP), *Address 0x4F, [2], User Sub Map, write only*

It is not necessary to write 0 to this bit as the bit automatically resets when it is set.

Function

VDP_CGMS_WSS_CHNGD_CLR	Description
0 ⊂	Self clearing bit
1	Clears VDP_CGMS_WSS_CHNGD_Q bit

VDP_GS_VPS_PDC_UTC_CHNG_CLR (VDP), *Address 0x4F, [4], User Sub Map, write only*

It is not necessary to write 0 to this bit as the bit automatically resets when it is set.

Function

VDP_GS_VPS_PDC_UTC_CHNG_CLR	Description
0 ⊂	Self clearing bit
1	Clears VDP_GS_VPS_PDC_UTC_CHNG_Q bit

VDP_VITC_CLR (VDP), *Address 0x4F, [6], User Sub Map, write only*

It is not necessary to write 0 to this bit as the bit automatically resets when it is set.

Function

VDP_VITC_CLR	Description
0 ⊂	Self clearing bit
1	Clears VDP_VITC_Q bit

8.18.5 I^{2}C Readback Registers

Teletext

Teletext, being a high data rate standard, the decoded bytes are available only as Ancillary data. However, a TTX_AVL bit has been provided in I^{2}C so that the user can check whether the VDP has detected Teletext or not. Note that the TTX_AVL bit is a plain status bit and does not use the protocol identified in the I^{2}C interface section.

TTX_AVL (VDP), *Address 0x78, [7], User Sub Map*

Function

TTX_AVL	Description
0 ⊂	Teletext not detected
1	Teletext detected

WST Packet Decoding

For WST ONLY, the VDP will decode the Magazine and Row address of WST Teletext packets and further decode the packet's 8x4 hamming coded words. This feature can be disabled using WST_PKT_ DECOD_ DISABLE bit (Bit 3, register 0x60, User Sub Map). This feature is valid for WST ONLY.

WST_PKT_DECOD_DISABLE (VDP), *Address 0x60 [3], User Sub Map*

Function

WST_PKT_DECOD_DISABLE	Description
0 ⊂	Enable hamming decoding of WST packets
1	Disable hamming decoding of WST packets

For hamming coded bytes, the dehammed nibbles are output along with some error information from the hamming decoder as follows.

- Input hamming coded byte: {D3, P3, D2, P2, D1, P1, D0, P0} (bits in decoded order)
- Output dehammed byte: {E1, E0, 0, 0, D3', D2', D1', D0'} (Di' – corrected bits, Ei error information).

Table 30: Explanation of Error Bits in Dehammed Output Byte

E[1:0]	Error Information	Output Data bits in Nibble
00	No errors detected	OK
01	Error in P4	OK
10	Double error	BAD
11	Single error found and corrected	OK

The different WST packets that will be decoded are described in Table 31.

Table 31: WST Packet Description

Header Packet (X/00)	1Pst Byte	Mag No. - Dehammed Byte4
	2Pnd Byte	Row No. - Dehammed Byte5
	3rd Byte	Page No. - Dehammed Byte6
	4th Byte	Page No. - Dehammed Byte7
	5th to 10th Byte	Control Bytes - Dehammed bytes 8 to 13
	11th to 42nd Byte	Raw data bytes
Text Packets (X/01 to X/25)	1st Byte	Mag No. - Dehammed Byte4
	2nd Byte	Row No. - Dehammed Byte5
	3rd to 42nd Byte	Raw data bytes
8/30 (Format 1) packet Desig Code = 0000 or 0001 UTC	1st Byte	Mag No. - Dehammed Byte4
	2nd Byte	Row No. - Dehammed Byte5
	3rd Byte	Desig Code. - Dehammed Byte6
	4th Byte to 10th Byte	Dehammed Initial Teletext Page Bytes 7 to 12
	11th to 23rd Byte	UTC bytes - Dehammed bytes 13 to 25
	24th to 42nd Byte	Raw Status bytes
8/30 (Format 2) packet Desig Code = 0010 or 0011 PDC	1st Byte	Mag No. - Dehammed Byte4
	2nd Byte	Row No. - Dehammed Byte5
	3rd Byte	Desig Code. - Dehammed Byte6
	4th Byte to 10th Byte	Dehammed Initial Teletext Page Byte 7 to 12
	11th to 23rd Byte	PDC bytes - Dehammed bytes 13 to 25
	24th to 42nd Byte	Raw Status bytes
X/26 , X/27, X/28, X/29, X/30, X/31 (X/26, X/28 and M/29 further decoding needs 24x18 hamming decoding. Not supported at present.)	1st Byte	Mag No. - Dehammed Byte4
	2nd Byte	Row No. - Dehammed Byte5
	3rd Byte	Desig Code. - Dehammed Byte6
	4th to 42nd Byte	Raw Data bytes

8.18.6 CGMS and WSS

The CGMS and WSS data packets convey the same type of information for different video standards. WSS is for PAL and CGMS is for NTSC and hence the CGMS and WSS readback registers are shared. WSS is bi-phase coded and the VDP does a bi-phase decoding to produce the 14 raw WSS bits to be available in the CGMS/WSS readback I^{2}C registers and CGMS_WSS_AVL bit is set.

CGMS_WSS_CLEAR (VDP), *Address 0x78, [2], User Sub Map, Write only*

This is the CGMS/WSS clear bit.

Function

CGMS_WSS_CLEAR	Description
0	Not necessary to write 0 since CGMS_WSS_CLEAR is a self clearing bit
1	Re-initializes the CGMS/WSS readback registers

CGMS_WSS_AVL (VDP), *Address 0x78, [2], User Sub Map, Read only*

This is the CGMS/WSS available bit.

Function

CGMS_WSS_AVL	Description
0	CGMS/WSS not detected
1	CGMS/WSS detected

CGMS_WSS_DATA[19:0] (VDP), *Address 0x7D, [3:0], 0x7E, [7:0], 0x7F, [7:0], User Sub Map, Read only*

These bits hold the decoded CGMS or WSS data.

Function

CGMS_WSS_DATA[19:0]	Description
xxxx xxxx xxxx xxxx xxxx	Decoded CGMS[19:0] (NTSC)/WSS[13:0] (PAL) data

Table 32: CGMS/WSS Readback Registers

Signal Name	Register Location	Address (User Sub Map)	
CGMS_WSS_DATA_0[3:0]	VDP_CGMS_WSS_DATA_0 [3:0]	125	0x7D
CGMS_WSS_DATA_1[7:0]	VDP_CGMS_WSS_DATA_1 [7:0]	126	0x7E
CGMS_WSS_DATA_2[7:0]	VDP_CGMS_WSS_DATA_2 [7:0]	127	0x7F

Refer to Figure 62 and Figure 63 for the I²C bit to WSS/CGMS bit mapping.

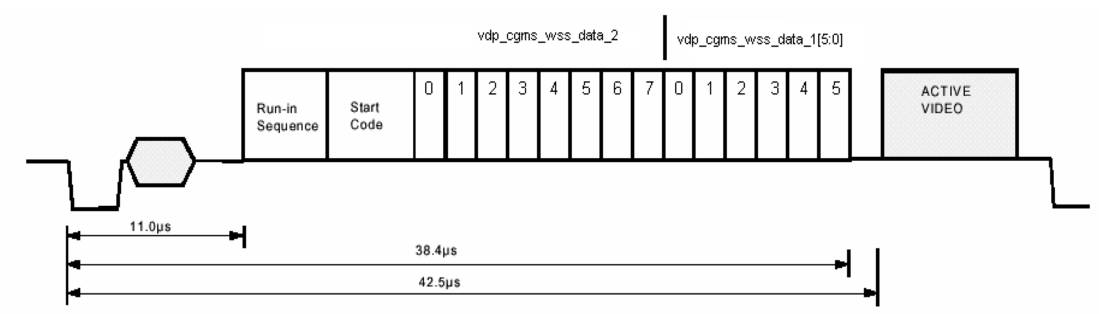


Figure 62: WSS Waveform

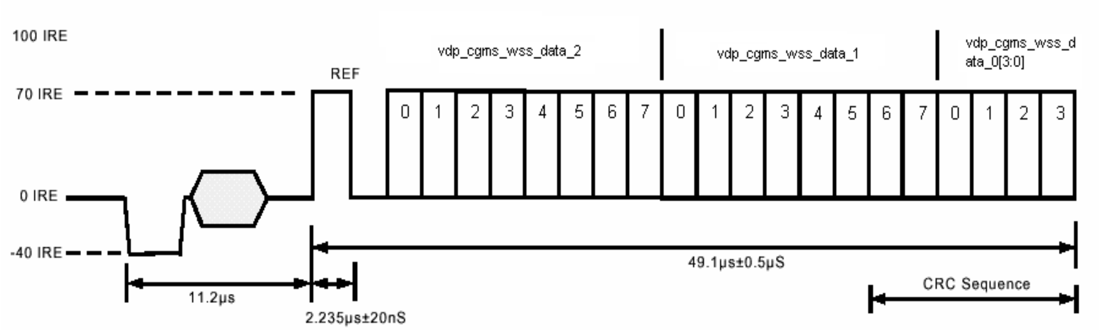


Figure 63: CGMS Waveform

CCAP

Two bytes of decoded closed caption data are available in the I^{2}C registers. The field information of the decoded CCAP data can be obtained from the CC_EVEN_FIELD bit (bit 1, register 0x78, user sub map).

CC_CLEAR (VDP), *Address 0x78, [0], User Sub Map, Write only*

This is the Closed Caption CLEAR bit

Function

CC_CLEAR	Description
0 ⊂	Not necessary to write 0 since CGMS_WSS_CLEAR is a self clearing bit
1	Re-initializes the CGMS/WSS readback registers

CC_AVL (VDP), *Address 0x78, [0], User Sub Map*

This is the Closed Caption AVAILABLE bit

Function

CC_AVL	Description
0 ⊂	Closed Captioning not detected
1	Closed Captioning detected

CC_EVEN_FIELD (VDP), *Address 0x78, [1], User Sub Map*

Identifies the field from which the CCAP data was decoded.

Function

CC_EVEN_FIELD	Description
0 ⊂	CC on odd field
1	CC on even field

Table 33: Closed Caption Readback Registers

Signal Name	Register Location	Address (User Sub Map) Dec	Hex
CCAP_BYTE_1[7:0]	VDP_CCAP_DATA_0[7:0]	121	0x79
CCAP_BYTE_2[7:0]	VDP_CCAP_DATA_1[7:0]	122	0x7A

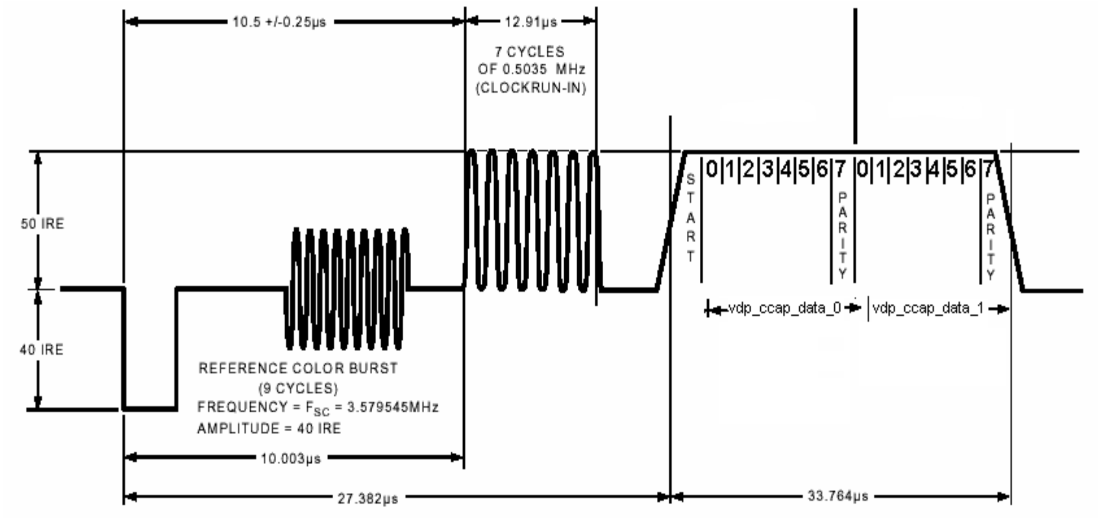


Figure 64: CCAP Waveform and Decoded Rata Correlation

VITC

VITC has a sync sequence of "10" in between each data byte. The VDP strips these syncs from the data stream to give out only the data bytes. The VITC results are available in VDP_VITC_DATA_0 to VDP_VITC_DATA_8 registers (Registers 0x92 to 0x9A, User Sub Map).

The VITC has a CRC byte at the end and the in-between syncs are also used in this CRC calculation. Since, the in-between syncs are not given out, the CRC is also calculated internally and the calculated CRC is also available for the user in the VITC_CALC_CRC register 0x9B, User Sub Map. Once the VDP completes decoding the VITC line, the VITC_DATA and VITC_CALC_CRC registers are updated and VITC_AVL bit is set.

VITC_AVL (VDP), *Address 0x78, [6], User Sub Map*

VITC AVAILABLE bit

Function

VITC_AVL	Description
0	VITC not detected
1	VITC detected

Table 34: VITC Readback Registers

Signal Name	Register Location		Address (User Sub Map)	
VITC_DATA_0[7:0]	VDP_VITC_DATA_0[7:0]	(VITC bits [9:2)	146	0x92
VITC_DATA_1[7:0]	VDP_VITC_DATA_1[7:0]	(VITC bits [19:12)	147	0x93
VITC_DATA_2[7:0]	VDP_VITC_DATA_2[7:0]	(VITC bits [29:22)	148	0x94
VITC_DATA_3[7:0]	VDP_VITC_DATA_3[7:0]	(VITC bits [39:32)	149	0x95
VITC_DATA_4[7:0]	VDP_VITC_DATA_4[7:0]	(VITC bits [49:42)	150	0x96
VITC_DATA_5[7:0]	VDP_VITC_DATA_5[7:0]	(VITC bits [59:52)	151	0x97
VITC_DATA_6[7:0]	VDP_VITC_DATA_6[7:0]	(VITC bits [69:62)	152	0x98
VITC_DATA_7[7:0]	VDP_VITC_DATA_7[7:0]	(VITC bits [79:72)	153	0x99
VITC_DATA_8[7:0]	VDP_VITC_DATA_8[7:0]	(VITC bits [89:82)	154	0x9A
VITC_CALC_CRC[7:0]	VDP_VITC_CALC_CRC[7:0]		155	0x9B

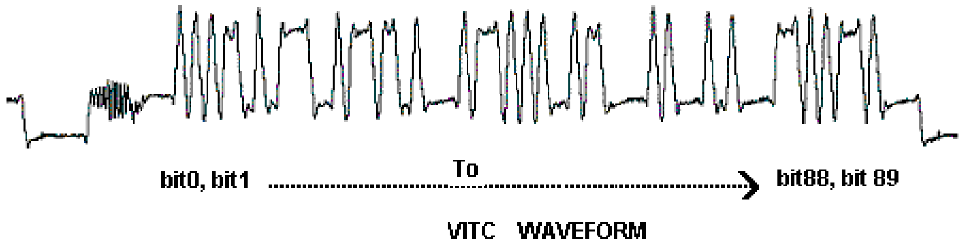


Figure 65: VITC Waveform and Decoded Rata Correlation

VPS, PDC, UTC, and Gemstar

The readback registers for VPS, PDC, and UTC have been shared. The Gemstar is a high data rate standard and so is available only through Ancillary Stream, however, for evaluation purposes any one line of Gemstar is available through I^2C registers sharing the same register space as PDC, UTC, and VPS. Thus only one standard out of VPS, PDC, UTC, and Gemstar can be read through the I^2C at a time.

To identify the data that should be made available in the I^2C registers, the user has to program i2c_gs_vps_pdc_utc [1:0] (register address 0x9C, User Sub Map).

I2C_GS_VPS_PDC_UTC (VDP), *Address 0x9C, [6:5], User Sub Map*

This specifies which standard result is to be available for I^2C readback.

Function

I2C_GS_VPS_PDC_UTC	Description
00	Gemstar 1x/2x
01	VPS
10	PDC
11	UTC

GS_PDC_VPS_UTC_AVL, *Address 0x78, [4], User Sub Map, Read only*

This is the GS, PDC, VPS, or UTC AVAILABLE bit.

Function

GS_PDC_VPS_UTC_AVL	Description
0	VPS not detected
1	VPS detected

Table 35: VDP_GS_VPS_PDC_UTC Readback Registers

Signal Name	Register Location	Address (User Sub Map)	
		Dec	Hex
GS_VPS_PDC_UTC_BYTE_0[7:0]	VDP_GS_VPS_PDC_UTC_0[7:0]	132d	0x84
GS_VPS_PDC_UTC_BYTE_1[7:0]	VDP_GS_VPS_PDC_UTC_1[7::0]	133d	0x85
GS_VPS_PDC_UTC_BYTE_2[7:0]	VDP_GS_VPS_PDC_UTC_2[7:0]	134d	0x86
GS_VPS_PDC_UTC_BYTE_3[7:0]	VDP_GS_VPS_PDC_UTC_3[7:0]	135d	0x87
VPS_PDC_UTC_BYTE_4[7:0]	VDP_VPS_PDC_UTC_4[7:0]	136d	0x88
VPS_PDC_UTC_BYTE_5[7:0]	VDP_VPS_PDC_UTC_5[7:0]	137d	0x89
VPS_PDC_UTC_BYTE_6[7:0]	VDP_VPS_PDC_UTC_6[7:0]	138d	0x8A
VPS_PDC_UTC_BYTE_7[7:0]	VDP_VPS_PDC_UTC_7[7:0]	139d	0x8B
VPS_PDC_UTC_BYTE_8[7:0]	VDP_VPS_PDC_UTC_8[7:0]	140d	0x8C
VPS_PDC_UTC_BYTE_9[7:0]	VDP_VPS_PDC_UTC_9[7:0]	141d	0x8D
VPS_PDC_UTC_BYTE_10[7:0]	VDP_VPS_PDC_UTC_10[7:0]	142d	0x8E
VPS_PDC_UTC_BYTE_11[7:0]	VDP_VPS_PDC_UTC_11[7:0]	143d	0x8F
VPS_PDC_UTC_BYTE_12[7:0]	VDP_VPS_PDC_UTC_12[7:0]	144d	0x90

VPS

The VPS data bits are bi-phase decoded by the VDP. The decoded data is available in both the Ancillary Stream and in the I^2C register. VPS decoded data is available in the VDP_GS_VPS_PDC_UTC_0 to VPS_PDC_UTC_12 registers (addresses 0x84 – 0x90, User Sub Map). The GS_VPS_PDC_UTC_AVL bit is set if the user had programmed I2C_GS_VPS_PDC_UTC to 01.

Gemstar

The Gemstar decoded data is made available in the Ancillary Stream and any one line of Gemstar is also available in I^2C registers for evaluation purposes. In order to get Gemstar results in I^2C registers, the user has to program I2C_GS_VPS_PDC_UTC to 00.

Autodetection of Gemstar

VDP supports autodetection of Gemstar standard between Gemstar 1x or Gemstar 2x and decodes accordingly. For this autodetection mode to work the user has to set AUTO_DETECT_GS_TYPE I2C bit (register 0x61, User Sub Map) and program the decoder to decode GEMSTAR_2x on the required lines through line programming. The type of Gemstar decoded can be found out by observing the bit GS_DATA_TYPE bit (register 0x78, User Sub Map).

AUTO_DETECT_GS_TYPE, *Address 0x61, [4], User Sub Map*

Enable auto identification of Gemstar type

Function

AUTO_DETECT_GS_TYPE	Description
0	Disable Autodetection of Gemstar type
1 ⊂	Enable Autodetection of Gemstar type

GS_DATA_TYPE, *Address 0x78, [5], User Sub Map*

Identifies the decoded Gemstar data type

Function

GS_DATA_TYPE	Description
0	Gemstar 1x detected – Read 2 data bytes from 0x84
1	Gemstar 2x detected – Read 4 data bytes from 0x84

The Gemstar data that is available in the I^2C register could be from any line of the input video on which Gemstar was decoded. In case the user wants to read the Gemstar data on a particular video line, the user should use the Manual Configuration as described in Table 24, and enable Gemstar decoding on ONLY the required line.

PDC/UTC

PDC and UTC are data transmission through Teletext packet 8/30 format2 – (magazine 8, row 30, desig_code being 2 or 3); and packet 8/30 format 1 – (magazine 8, row 30, desig_code being 0 or 1). Hence, if PDC/UTC data is to be read through I^2C, the corresponding Teletext standard (WST – PAL System B) should be decoded by VDP. The whole Teletext decoded packet is output on the ancillary data stream and hence the user can look for the Magazine number, row number and desig_code and qualify the data as PDC/UTC or none of these.

If PDC/UTC packets have been identified, bytes 0 to 12 will be updated to GS_VPS_PDC_UTC_0 to VPS_PDC_UTC_12 registers, and GS_VPS_PDC_UTC_AVL bit is set. The full packet data is also available in the ancillary data format.

Note that the data available in the I^2C register will depend on the status of the WST_PKT_DECODE_DISABLE bit (bit 3, subaddress 0x60, User Sub Map).

8.19 VBI System 2

The user has an option of using a different VBI data slicer called 'VBI system 2'. This data slicer is used to decode Gemstar and Closed Caption VBI signals only.

Using this system, the Gemstar data is available only in the ancillary data stream. There is a special mode that enables one line of data to be read back via I^2C. For further details, refer to the ADI applications note on the ADV7181C VBI processing.

8.19.1 Gemstar Data Recovery – VBI System 2

The Gemstar compatible data recovery block (GSCD) supports 1X and 2X data transmissions. In addition, it can also serve as a CC decoder. Gemstar compatible data transmissions only occur in NTSC. CC data can be decoded in both PAL and NTSC.

The block is configured via I^2C in the following way:

- GDECEL[15:0] allows the user to enable and disable the data recovery on selected video lines on even fields
- GDECOL[15:0] enables the data recovery on selected lines for odd fields
- GDECAD configures the way in which data is being embedded in the video data stream
- GEMD informs the user if Gemstar Data was detected.

The recovered data is **not** available through I^2C, but is inserted into the horizontal blanking period of a ITU-R. BT656 compatible data stream. The data format is intended to comply with the recommendation by the International Telecommunications Union ITU-R BT.1364[1]. Refer also to Figure 66.

GDE_SEL_OLD_ADF (CP), *Address 0x4C, [3]*

The ADV7181C has a new ancillary data output block that can be used by the VDP data slicer and the System 2 data slicer. The new ancillary data formatter is used by selecting GDE_SEL_OLD_ADF = 0 (default setting). If this bit is set low, refer to Table 25 and Table 26 for information about how the data is packaged in the ancillary data stream

If customers wish to use the old ancillary data formatter (to be backward compatible with the ADV7402a), then GDE_SEL_OLD_ADF should be set to 1. The ancillary data format in this section refers to the ADV7402a ancillary data formatter.

Function

GDE_SEL_OLD_ADF	Description
0 ⊂	Enables new ancillary data system (VDP) recommended.
1	Enables ancillary data system compatible with ADV7402a

The format of the data packet depends on the following criteria:

- Transmission is 1X or 2X
- Data is output in 8-bit or 4-bit format (refer to the description of GDECAD on page 180).
- Data is Closed Caption (CCAP) or Gemstar compatible

Data packets are output if the corresponding enable bit is set **and** if the decoder detects the presence of data. Refer to the descriptions for GDECEL[15:0] and GDECOL[15.0] on page 180. This means that for video lines where no data was decoded, no data packet is output even if the corresponding line enable bit is set.

Each data packet starts immediately after the EAV code of the preceding line. Refer to Figure 66 and Table 36, which shows the overall structure of the data packet. The entries within the packet are as follows:

- Fixed preamble sequence of 0x00, 0xFF, 0xFF.
- Data Identification Word (DID). The value for the DID marking a Gemstar or CCAP data packet is 0x140 (10-bit value).
- Secondary Data Identification Word (SDID), which contains information about the video line from which data was retrieved, whether the Gemstar transmission was of 1X or 2X format and whether it was retrieved from an even or odd field.
- Data Count byte, giving the number of user data words that follow.
- User data section.
- Optional padding to ensure that the user data word section of a packet has length of a multiple of 4 bytes[2]

[1] For more information, refer to their website at http://www.itu.ch
[2] Requirement as set in ITU-R BT.1364

- Checksum byte.

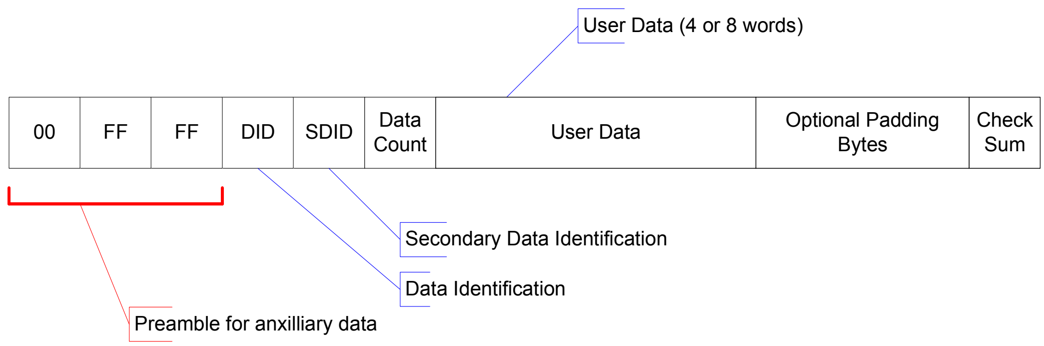


Figure 66: Gemstar and CCAP Embedded Data Packet (Generic)

Table 36 lists the values within a generic data packet output by the ADV7181C in a 10-bit format.

Table 36: Generic Data Output Packet

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	2X	Line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	DC[1]	DC[0]	0	0	Data Count (DC)
6	$\overline{EP}$	EP	0	0	word1[7:4]				0	0	User Data Words
7	$\overline{EP}$	EP	0	0	word1[3:0]				0	0	
8	$\overline{EP}$	EP	0	0	word2[7:4]				0	0	
9	$\overline{EP}$	EP	0	0	word2[3:0]				0	0	
10	$\overline{EP}$	EP	0	0	word3[7:4]				0	0	
11	$\overline{EP}$	EP	0	0	word3[3:0]				0	0	
12	$\overline{EP}$	EP	0	0	word4[7:4]				0	0	
13	$\overline{EP}$	EP	0	0	word4[3:0]				0	0	
14	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	0	0	Checksum

Notes:

- **DID**
  The Data Identification value is 0x140. (10-bit value). Care has been taken so that in 8-bit systems the 2 LSBs do not carry vital information.
- **EP and $\overline{EP}$**
  The EP bit is set to ensure even parity on the data word D[8:0]. Even parity means that there is always an even number of 1s within the D[8:0] bit arrangement, including the EP bit. The $\overline{EP}$ describes the logic inverse of EP and is output on D[9]. The $\overline{EP}$ is output to ensure that the reserved codes of 00 and FF cannot happen.

- **EF**
  Even Field identifier. EF = 1 indicates that the data was recovered from a video line on an even field.
- **2X**
  This bit indicates whether the data sliced was in Gemstar 1X or 2X format. A high indicates 2X format.
- **line[3:0]**
  This entry provides a code that is unique for each of the possible 16 source lines of video from which Gemstar data can be retrieved. Refer to Table 46.
- **DC[1:0]**
  Data count value. The number of User Data Words (UDW) in the packet divided by 4. The number of UDW in any packet must be an integral number of 4. Padding is required at the end if necessary[1] (refer to Table 37). The 2X bit determines whether the raw information retrieved from the video line was 2 or 4 bytes. The state of the GDECAD bit affects whether the bytes are transmitted straight (i.e. 2 bytes transmitted as 2 bytes) or split into nibbles (i.e. 2 bytes transmitted as 4 half bytes). Padding bytes are then added where necessary.
- **CS[8:2]**
  The Checksum is provided to determine the integrity of the ancillary data packet. It is calculated by summing up D[8:2] of DID, SDID, the Data Count byte and all UDWs and ignoring any overflow during the summation. Since all the data bytes used to calculate the Checksum have their two least significant bits set to 0, the CS[1:0] bits are also always 0. $\overline{CS[8]}$ describes the logic inversion of CS[8]. The value $\overline{CS[8]}$ is included in the Checksum entry of the data packet to ensure that the reserved values of 0x00 and 0xFF do not occur.

Table 37: Data Byte Allocation

2X	No. Raw Information Bytes as Retrieved from Video Line	GDECAD	No. User Data Words (Including Padding)	No. Padding Bytes	DC[1:0]
1	4	0	8	0	10
1	4	1	4	0	01
0	2	0	4	0	01
0	2	1	4	2	01

Table 38, Table 39, Table 40, and Table 41 outline the various data packages possible.

8.19.1.1 Gemstar 2X Format, Half-Byte Output Mode

Half-Byte output mode is selected by setting GDECAD = 0, full-byte output mode is selected by setting CDECAD = 1. Refer to the description of GDECAD on page 180.

[1] Requirement as set in ITU-R BT.1364

Table 38: Gemstar 2X Data, Half-byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	**1**	line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	**1**	**0**	0	0	Data Count
6	$\overline{EP}$	EP	0	0	Gemstar word1[7:4]				0	0	User Data Words
7	$\overline{EP}$	EP	0	0	Gemstar word1[3:0]				0	0	
8	$\overline{EP}$	EP	0	0	Gemstar word2[7:4]				0	0	
9	$\overline{EP}$	EP	0	0	Gemstar word2[3:0]				0	0	
10	$\overline{EP}$	EP	0	0	Gemstar word3[7:4]				0	0	
11	$\overline{EP}$	EP	0	0	Gemstar word3[3:0]				0	0	
12	$\overline{EP}$	EP	0	0	Gemstar word4[7:4]				0	0	
13	$\overline{EP}$	EP	0	0	Gemstar word4[3:0]				0	0	
14	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 39: Gemstar 2X Data, Full-byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	**1**	line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	Gemstar word1[7:0]								0	0	User Data Words
7	Gemstar word2[7:0]								0	0	
8	Gemstar word3[7:0]								0	0	
9	Gemstar word4[7:0]								0	0	
10	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

8.19.1.2 Gemstar 1X Format

Half-Byte output mode is selected by setting GDECAD = 0, full-byte output mode is selected by setting GDECAD = 1. Refer to the description of GDECAD on page 180.

Table 40: Gemstar 1X Data, Half-byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{\text{EP}}$	EP	EF	**0**	line[3:0]				0	0	SDID
5	$\overline{\text{EP}}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	$\overline{\text{EP}}$	EP	0	0	Gemstar word1[7:4]				0	0	User Data Words
7	$\overline{\text{EP}}$	EP	0	0	Gemstar word1[3:0]				0	0	
8	$\overline{\text{EP}}$	EP	0	0	Gemstar word2[7:4]				0	0	
9	$\overline{\text{EP}}$	EP	0	0	Gemstar word2[3:0]				0	0	
10	$\overline{\text{CS[8]}}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 41: Gemstar 1X Data, Full-byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{\text{EP}}$	EP	EF	**0**	line[3:0]				0	0	SDID
5	$\overline{\text{EP}}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	Gemstar word1[7:0]								0	0	User Data Words
7	Gemstar word2[7:0]								0	0	
8	1	0	0	0	0	0	0	0	0	0	UDW Padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW Padding 0x200
10	$\overline{\text{CS[8]}}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

8.19.1.3 NTSC CCAP Data

Half-Byte output mode is selected by setting GDECAD = 0, the full-byte mode is enabled by GDECAD = 1.

Refer to the description of GDECAD on page 180. The data packet formats are shown in Table 42 and Table 43.

Notes:

- Only Closed Caption data from the SDP core can be embedded in the output data stream. NTSC Closed Caption data is sliced on line 21_d on even and odd fields. The corresponding enable bit has to be set high.
- Refer to the information on GDECEL[15:0] and GDECOL[15.0] on page 180.

Table 42: NTSC CCAP Data, Half-byte Mode

Byte	**D[9]**	**D[8]**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Description**
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	**0**	**1**	**0**	**1**	**1**	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	$\overline{EP}$	EP	0	0	CCAP word1[7:4]				0	0	User Data Words
7	$\overline{EP}$	EP	0	0	CCAP word1[3:0]				0	0	
8	$\overline{EP}$	EP	0	0	CCAP word2[7:4]				0	0	
9	$\overline{EP}$	EP	0	0	CCAP word2[3:0]				0	0	
10	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 43: NTSC CCAP Data, Full-byte Mode

Byte	**D[9]**	**D[8]**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**Description**
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	**0**	**1**	**0**	**1**	**1**	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	CCAP word1[7:0]								0	0	User Data Words
7	CCAP word2[7:0]								0	0	
8	1	0	0	0	0	0	0	0	0	0	UDW Padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW Padding 0x200
10	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

8.19.1.4 PAL CCAP Data

Half-Byte output mode is selected by setting GDECAD = 0, full-byte output mode is selected by setting GDECAD = 1.

Refer to the information about GDECAD on page 180. Table 44 and Table 45 list the bytes of the data packet.

Notes:

- Only Closed Caption data from the SDP core can be embedded in the output data stream. PAL Closed Caption data is sliced from lines 22 and 335. The corresponding enable bits have to be set.
- Refer to the information about GDECOL[15.0] and GDECEL[15:0] on page 179.

Table 44: PAL CCAP Data, Half-byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	**0**	**1**	**0**	**1**	**0**	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	$\overline{EP}$	EP	0	0	CCAP word1[7:4]				0	0	User Data Words
7	$\overline{EP}$	EP	0	0	CCAP word1[3:0]				0	0	
8	$\overline{EP}$	EP	0	0	CCAP word2[7:4]				0	0	
9	$\overline{EP}$	EP	0	0	CCAP word2[3:0]				0	0	
10	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 45: PAL CCAP Data, Full-byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed Preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	**0**	**1**	**0**	**1**	**0**	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	**0**	**1**	0	0	Data Count
6	CCAP word1[7:0]								0	0	User Data Words
7	CCAP word2[7:0]								0	0	
8	1	0	0	0	0	0	0	0	0	0	UDW Padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW Padding 0x200
10	$\overline{CS[8]}$	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

GDECEL[15:0] Gemstar Decoding Even Lines (SDP), *0x48, [7:0]; Address 0x49, [7:0]*

The 16 bits of GDECEL[15:0] are interpreted as a collection of 16 individual line decode enable signals. Each of them refers to a line of video in an even field. Setting the bit enables the decoder block trying to find Gemstar or Closed Caption compatible data on that particular line. Setting the bit to 0 prevents the decoder from trying to retrieve data. (Refer to Table 46 and Table 47.) Users should only enable slicing on lines where VBI data is expected to occur as this minimizes the chances of false detections.

Notes:

- To retrieve Closed Caption data services on NTSC (line 284), GDECEL[11] must be set
- To retrieve Closed Caption data services on PAL (line 335), GDECEL[14] must be set

Function

GDECEL[15:0]	Description
0x0000	Do not attempt to decode Gemstar compatible data or CCAP on any line (even field)

GDECOL[15.0] Gemstar Decoding Odd Lines (SDP), *Address 0x4A, [7.0]: Address 0x4B, [7.0]*

The 16 bits of the GDECOL[15:0] form a collection of 16 individual line decode enable signals. (Refer to Table 46 and Table 47.) Users should only enable slicing on lines where VBI data is expected to occur as this minimizes the chances of false detections.

Notes:

- To retrieve Closed Caption data services on NTSC (line 21), GDECOL[11] must be set
- To retrieve Closed Caption data services on PAL (line 22), GDECOL[14] must be set

Function

GDECOL[15:0]	Description
0x0000	Do not attempt to decode Gemstar compatible data or CCAP on any line (odd field)

GEMD Gemstar Detected status bit (SDP) , *Address 0x13, [1]*

The Gemstar detected status bit will go high when the window of lines for which Gemstar data could occur is passed and Gemstar data was detected on a line that was enabled using GDECEL[15:0] and GDECOL[15:0]. If GEMD goes high in a given field, it will remain high until the end of the active video lines in that field (i.e. until the start of the next VBI region).

Function

GEMD	Description
0	No Gemstar Data detected
1	Gemstar Data detected

GDECAD Gemstar Decode Ancillary Data Format (SDP), *Address 0x4C, [0]*
The decoded data from Gemstar compatible transmissions or from Closed Caption is inserted into the horizontal blanking period of the respective line of video. There is a potential problem if the retrieved data bytes have the value 0x00 or 0xFF. In an ITU-R BT.656 compatible data stream, those values are reserved and only used to form a fixed preamble.

The GDECAD bit allows the data to be inserted into the horizontal blanking period in two ways:

1. Inserts all data **straight** into the data stream, even the reserved values of 0x00 and 0xFF if they happen. This can violate the output data format specification ITU-R BT.1364.

2. Splits all data into nibbles and insert the half bytes over double the number of cycles in a 4-bit format.

Function

GDECAD	Description
0	Splits data into half-bytes and insert
1	Outputs data straight in 8-bit format

Table 46: NTSC Line Enable Bits and Corresponding Line Numbering

line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
0	10	GDECOL[0]	Gemstar
1	11	GDECOL[1]	Gemstar
2	12	GDECOL[2]	Gemstar
3	13	GDECOL[3]	Gemstar
4	14	GDECOL[4]	Gemstar
5	15	GDECOL[5]	Gemstar
6	16	GDECOL[6]	Gemstar
7	17	GDECOL[7]	Gemstar
8	18	GDECOL[8]	Gemstar
9	19	GDECOL[9]	Gemstar
10	20	GDECOL[10]	Gemstar
11	21	GDECOL[11]	Gemstar or Closed Caption
12	22	GDECOL[12]	Gemstar
13	23	GDECOL[13]	Gemstar
14	24	GDECOL[14]	Gemstar
15	25	GDECOL[15]	Gemstar
0	273 (10)	GDECEL[0]	Gemstar
1	274 (11)	GDECEL[1]	Gemstar
2	275 (12)	GDECEL[2]	Gemstar
3	276 (13)	GDECEL[3]	Gemstar
4	277 (14)	GDECEL[4]	Gemstar
5	278 (15)	GDECEL[5]	Gemstar
6	279 (16)	GDECEL[6]	Gemstar
7	280 (17)	GDECEL[7]	Gemstar
8	281 (18)	GDECEL[8]	Gemstar
9	282 (19)	GDECEL[9]	Gemstar
10	283 (20)	GDECEL[10]	Gemstar
11	284 (21)	GDECEL[11]	Gemstar or Closed Caption
12	285 (22)	GDECEL[12]	Gemstar
13	286 (23)	GDECEL[13]	Gemstar
14	287 (24)	GDECEL[14]	Gemstar
15	288 (25)	GDECEL[15]	Gemstar

Table 47: PAL Line Enable Bits and Corresponding Line Numbering

line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
12	8	GDECOL[0]	Not valid
13	9	GDECOL[1]	Not valid
14	10	GDECOL[2]	Not valid
15	11	GDECOL[3]	Not valid
0	12	GDECOL[4]	Not valid
1	13	GDECOL[5]	Not valid
2	14	GDECOL[6]	Not valid
3	15	GDECOL[7]	Not valid
4	16	GDECOL[8]	Not valid
5	17	GDECOL[9]	Not valid

line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
6	18	GDECOL[10]	Not valid
7	19	GDECOL[11]	Not valid
8	20	GDECOL[12]	Not valid
9	21	GDECOL[13]	Not valid
10	**22**	**GDECOL[14]**	**Closed Caption**
11	23	GDECOL[15]	Not valid
12	321 (8)	GDECEL[0]	Not valid
13	322 (9)	GDECEL[1]	Not valid
14	323 (10)	GDECEL[2]	Not valid
15	324 (11)	GDECEL[3]	Not valid
0	325 (12)	GDECEL[4]	Not valid
1	326 (13)	GDECEL[5]	Not valid
2	327 (14)	GDECEL[6]	Not valid
3	328 (15)	GDECEL[7]	Not valid
4	329 (16)	GDECEL[8]	Not valid
5	330 (17)	GDECEL[9]	Not valid
6	331 (18)	GDECEL[10]	Not valid
7	332 (19)	GDECEL[11]	Not valid
8	333 (20)	GDECEL[12]	Not valid
9	334 (21)	GDECEL[13]	Not valid
10	**335 (22)**	**GDECEL[14]**	**Closed Caption**
11	336 (23)	GDECEL[15]	Not valid

8.19.2 Letterbox Detection

Incoming video signals can conform to different aspect ratios (16:9 wide screen of 4:3 standard). For transmissions in the wide screen format, a digital sequence (WSS) is transmitted with the video signal. If a WSS sequence is provided, the aspect ratio of the video can be derived from digitally decoded bits contained within it.

In the absence of a WSS sequence, the letterbox detection can be used to find wide screen signals. The detection algorithm examines the active video content of lines at the start and the end of a field. If the presence of black lines is detected, this can serve as an indication that the currently shown picture is in wide screen format.

The active video content (luminance magnitude) over a line of video is summed together. At the end of a line, this accumulated value is compared with a threshold and a decision is made whether or not a particular line is considered to be black. The threshold value needed can depend on the type of input signal and some control is provided via LB_TH[4:0].

8.19.2.1 Detection at Start of Field

At the top of a field, the ADV7181C expects a section of at least six consecutive black lines of video. Once those lines are detected, the register LB_LCT[7:0] reports back the number of black lines actually found. By default, the ADV7181C starts looking for those black lines in sync with the beginning of active video, e.g. straight after the last VBI video line. LB_SL[3:0] allows the user to set the start of letterbox detection from the beginning of a frame on a line by line basis. The detection window closes in the middle of the field.

8.19.2.2 Detection at End of Field

The ADV7181C again expects at least six continuous lines of black video at the bottom of a field before reporting back the number of lines actually found via the LB_LCB[7:0] value. The activity window for the letterbox detection (end of field) starts in the middle of the active field. Its end is programmable via LB_EL[3:0].

8.19.2.3 Detection at Mid Range

Some transmissions of wide screen video include subtitles within the lower black box. If the ADV7181C finds at least two black lines, followed by some more non-black video (e.g. the subtitle), and finally followed by the remainder of the bottom black block, it reports back a mid-count via LB_LCM[7:0]. If no subtitles are found, LB_LCM[7:0] reports the same number as LB_LCB[7:0].

Notes:

- There is a two field delay in the reporting of any line count parameters.
- There is no letterbox detected bit. The user is requested to read the LB_LCT[7:0] and LB_LCB[7:0] register values and come to a conclusion about the presence of letterbox type video in the software.

LB_LCT[7:0] Letterbox Line Count Top (SDP), *0x9B, [7:0]*
LB_LCM[7:0] Letterbox Line Count Mid (SDP), *Address 0x9C, [7:0]*
LB_LCB[7:0] Letterbox Line Count Bottom (SDP), *Address 0x9D, [7:0]*

Access Information			
Signal Name	**Block**	**Address**	**Register Default Value**
LB_LCT[7:0]	SDP	0x9BB	(Readback only)
LB_LCM[7:0]	SDP	0x9CB$_{0B}$	(Readback only)
LB_LCB[7:0]	SDP	0x9DB	(Readback only)

LB_TH[4:0] Letterbox Threshold Control (SDP), *Address 0xDC, [4:0]*
Function

LB_TH[4:0]	Description
01100	Default threshold for detection of black lines
01101 - 10000	Increases threshold (need larger active video content before identifying non-black)
00000 - 01011	Decreased threshold (even small noise level scan cause the detection of non-black lines)

LB_SL[3:0] Letterbox Start Line (SDP), *0xDD, [7:4]*
Function

LB_SL[3:0]	Description
0100	Letterbox detection aligned with active video. Window starts after EDTV VBI data line. Example: 0100: 23/286 (NTSC)
0001, 0010	Example: 0101: 24/287 (NTSC) etc.

LB_EL[3:0] Letterbox End Line (SDP), *Address 0xDD, [3:0]*
Function

LB_EL[3:0]	Description
1101	Letterbox detection ends with the last active line of video on a field. Example: 1101: 262/ 525 (NTSC)
0001,0010	Example: 1100: 261/ 524 (NTSC)

8.20 IF Filter Compensation

IFFILTSEL[2:0] IF Filter Select *Address 0xF8, [2:0]*
The IFFILTSEL[2:0] register allows the user to compensate for SAW filter characteristics on a composite input as would be observed on a tuner output. Figure 67 and Figure 68 show IF Filter compensation for NTSC and PAL respectively.

The options for this feature are as follows:

- Bypass Mode
- NTSC: consists of three filter characteristics
- PAL: consists of three filter characteristics

Refer to Table 94 for programming details.

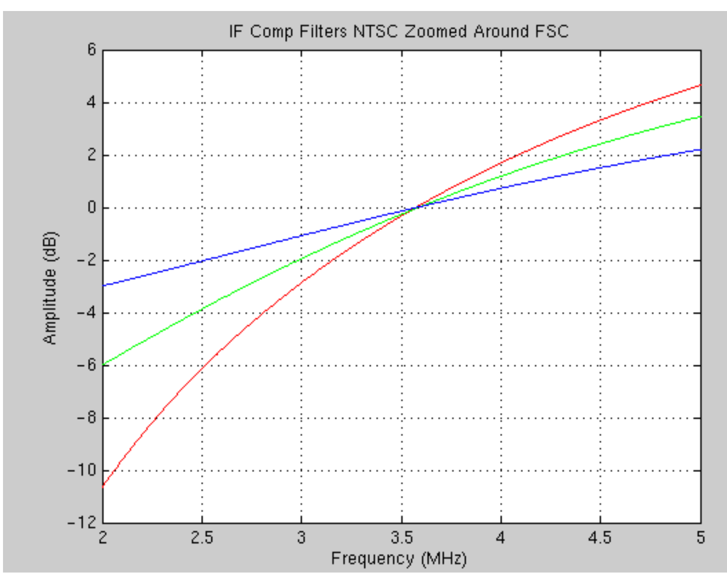


Figure 67: NTSC IF Filter Compensation

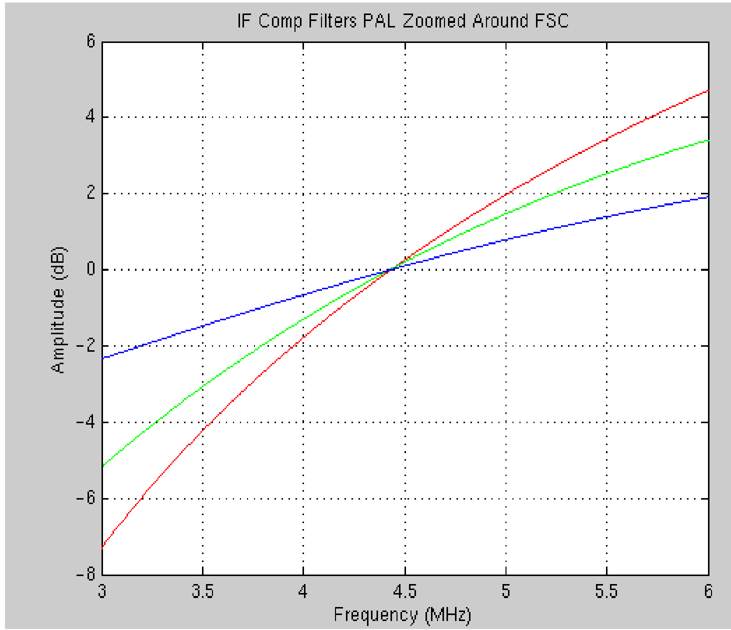


Figure 68: PAL IF Filter Compensation

9 Pixel Port Configuration

The ADV7181C has a very flexible pixel port; it can be configured in a variety of formats to accommodate downstream ICs. Table 48 summarizes the various functions that pins can have on the ADV7181C in different modes of operation. Refer to Table 50 and Table 80 (CP), and Table 49 and Table 63 (SDP) for programming the various configurations.

Notes:

- The ordering of components (e.g. Cr versus Cb, CHA/B/C) can be changed. Refer to the information in the SDP and CP pixel output modes sections of this manual. Table 48 indicates the default positions for the components.
- Not all modes shown in Table 48 are available in either CP or SDP modes of operation. Refer to the information in section 9.1 and 9.2 for more details.

Table 48: SDP and CP Pixel Input/Output Pin Map

<table>
<tr><th colspan="2" rowspan="2">Processor, Format, and Mode</th><th colspan="20">Pixel Port Pins [P19:0]</th></tr>
<tr><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>SDP</td><td>Video out 8-bit 4:2:2</td><td colspan="8">YCrCb[7:0]OUT</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>SDP</td><td>Video out 10-bit 4:2:2</td><td colspan="10">YCrCb [9:0]OUT</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>SDP</td><td>Video out 16-bit 4:2:2</td><td colspan="8">Y[7:0] OUT</td><td>-</td><td>-</td><td colspan="8">CrCb[7:0]OUT</td><td>-</td><td>-</td></tr>
<tr><td>SDP</td><td>Video out 20-bit 4:2:2</td><td colspan="10">Y[9:0] OUT</td><td colspan="10">CrCb[7:0]OUT</td></tr>
<tr><td>CP</td><td>Video out 12-bit 4:4:4 RGB DDR</td><td>D7
B[7]↑
R[3]↓</td><td>D6
B[6]↑
R[2]↓</td><td>D5
B[5]↑
R[1]↓</td><td>D4
B[4]↑
R[0]↓</td><td>D3
B[3]↑
G[7]↓</td><td>D2
B[2]↑
G[6]↓</td><td>D1
B[1]↑
G[5]↓</td><td>D0
B[0]↑
G[4]↓</td><td>-</td><td>-</td><td>D11
G[3]↑
R[7]↓</td><td>D10
G[2]↑
R[6]↓</td><td>D9
G[1]↑
R[5]↓</td><td>D8
G[0]↑
R[4]↓</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>CP</td><td>Video out 16-bit 4:2:2</td><td colspan="8">CHA[7:0] OUT (for example, Y[7:0])</td><td>-</td><td>-</td><td colspan="8">CHB/C[7:0] OUT (for example, Cr/Cb[7:0])</td><td>-</td><td>-</td></tr>
<tr><td>CP</td><td>Video out 20-bit 4:2:2</td><td colspan="10">CHA[9:0] OUT (for example, Y[9:0])</td><td colspan="10">CHB/C[9:0] OUT (for example, Cr/Cb[9:0])</td></tr>
</table>

9.1 SDP Pixel Port Output Modes

There are several modes in which the ADV7181C pixel port can be configured when the SD Processor core is enabled; these modes are under the control of OF_SEL[3:0]. Refer to Table 49 for more details. The default value is shaded.

Table 49: Standard Definition Pixel Port Modes

<table>
<tr><th rowspan="3">OF_SEL[3:0]</th><th rowspan="3">Format</th><th colspan="4">Pixel Port Pins P[19:0]</th></tr>
<tr><th colspan="2">P[19:10]</th><th colspan="2">P9[9:0]</th></tr>
<tr><th>P[19:12]</th><th>P[11:10]</th><th>P[9:2]</th><th>P[1:0]</th></tr>
<tr><td>0000</td><td>10 bit @LLC1 4:2:2 ITU656</td><td colspan="2">YCrCb[9:0]</td><td>Tristate</td><td>Tristate</td></tr>
<tr><td>0001</td><td>20 bit @LLC2 4:2:2</td><td colspan="2">Y[9:0]</td><td colspan="2">CrCb[9:0]</td></tr>
<tr><td>0010</td><td>16 bit @LLC2 4:2:2</td><td>Y[7:0]</td><td>Tristate</td><td>CrCb[7:0]</td><td>Tristate</td></tr>
<tr><td>0011</td><td>8 bit @LLC1 4:2:2 CCIR656656</td><td>YCrCb[7:0]</td><td>Tristate</td><td>Tristate</td><td>Tristate</td></tr>
<tr><td>0100-1111</td><td>Reserved</td><td colspan="4">Reserved: Do not use</td></tr>
</table>

Note: The default LLC frequency output on the LLC pin is approximately 27 MHz. For modes that operate with a nominal data rate of 13.5 MHz (0010 and 0101), the clock frequency on the output pin stays at the higher rate of 27 MHz. To output the nominal 13.5 MHz clock on the LLC pin, refer to the information in Section 9.1.1.

SWPC Swap Pixel Cr/Cb (SDP), *Address 0x27, [7]*

This bit allows the user to swap Cr and Cb samples of the SDP block only.

Function

SWPC	Description
0 ⊂	No swapping
1	Swaps Cr and Cb values

9.1.1 LLC Output Selection

LLC_PAD_SEL[2:0] (SDP), *0x8F, [6:4]*

The following I^2C write allows the user to select between the LLC (nominally at 27 MHz) and LLC2 (nominally at 13.5 MHz).

The LLC2 signal is useful for LLC2 compatible wide bus (20-bit) output modes. Refer to Table 49 for additional information.

Notes:

- It is important to set the LLC_PAD_SEL[2:0] control back to its default when leaving the SDP mode of operation.
- The LLC2 signal and data on the data bus are synchronized. By default, the rising edge of LLC2 is aligned with the Y data, and the falling edge occurs when the data bus holds C data. The polarity of the clock and, hence, the Y/C assignments to the clock edges can be altered by using the PCLK bit. Refer to the *Polarity LLC Pin* section of this manual for a description.

Function

LLC_PAD_SEL[2:0]	Description
000 ⊂	Output clock as per PRIM_MODE and VID_STD
101	Output LLC2 (valid setting in SDP mode only) on LLC pin
111	Output clock at twice data rate for data processed through the CP core only

9.2 CP Pixel Port Output Modes

There are several modes in which the ADV7181C pixel port can be configured when the CP core is enabled. These modes are under the control of CPOP_SEL[3:0] (refer to Table 50).

CPOP_SEL[3:0] (CP), *Address 0x6B, [3:0]*

Table 50: CP Mode Pixel Port Configuration

DDR_ EN	CPOP_SEL [3:0]	Output Format	Pixel Port Pins P[29:0]			
			P[19:10]		P9[9:0]	
			P[19:12]	P[11:10]	P[9:2]	P[1:0]
0	0001	20 bit @LLC1 4:2:2 SDR	Y[9:0]		CrCb[9:0]	
0	0011	16 bit @LLC1 4:2:2 SDR	Y[7:0]	Tristate	CrCb[7:0]	Tristate
1	0001	10 bit DDR Mode	Refer to Table 51			
1	0011	8 bit DDR Mode				
1	0100	12- bit DDR Mode				

CPOP_INV_Crb Invert Cr/Cb in 4:2:2 Output Mode (CP), *Address 0x86, [4]*

This bit swaps the order in which Cr and Cb are interleaved in the output data stream. It caters for cases in which the data on channels B and C are swapped.

It is only effective if:

- CP is active
- CPOP_SEL[3:0] is set to a 4:2:2 compatible output mode
- Decimation filters in the DPP block are set to downsampling chroma

Function

CPOP_INV_Crb	Description
0	Output Cr/Cb interleaved as per standard
1	Inverts the order of Cr and Cb in the interleaved data stream

9.3 CP DDR Output Interface

The ADV7181C allows data to be output in a double data rate (DDR) mode up to a clock rate of 75 MHz. In DDR mode, a new data value is presented on the positive and the negative edge of the LLC (line-locked clock) and, hence, double the amount of data is transferred.

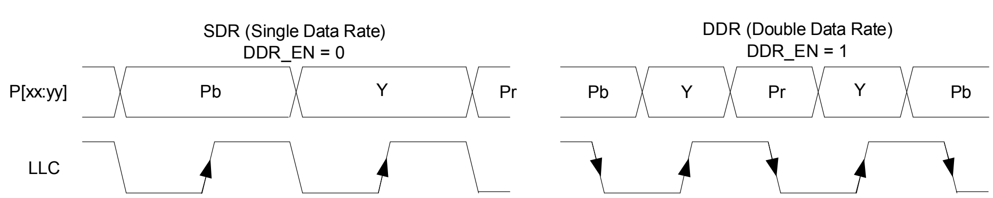


Figure 69: DDR Principle of Operation

The DDR is based on a two-stage interleaving (refer to Figure 70).

1. The Pr and Pb values must be interleaved via selecting the appropriate CPOP_SEL mode. For more information, refer to the description of CPOP_SEL[3:0] on page 188 and CPOP_INV_Crb Invert Cr/Cb in 4:2:2 Output Mode (CP) on page 188. Select the 4:2:2 output mode.
2. The PrPb stream is interleaved with the Y stream in a secondary interleave stage.

As a result, DDR mode can only work if both interleaving stages are enabled.

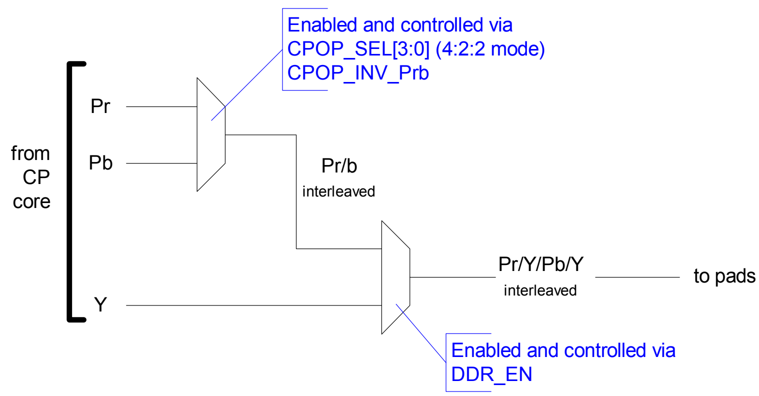


Figure 70: DDR Interleave Stages

As can be seen from Figure 69 in SDR mode, the clock is aligned with the data. Data changes with the negative edge of the clock and is stable for the user during the positive edge.

The following controls are in place to allow some flexibility for the DDR interface:

- **DDR mode enable via DDR_EN**.
  This control enables the second interleaving stage, thus producing the data stream shown in Figure 69. It also enables the clock delay block as described in DDR_CLK_DEL[3:0].

- **Clock polarity via PCLK**.
  The clock can be inverted, thus allowing the assignment of positive and negative edge with Y and Pr/b data to be changed.

- **Adjustable delay via DDR_CLK_DEL[3:0]**.
  The ADV7181C provides a digital control, which allows a delay to the output clock edges (DDR mode only) with respect to the data.

Important: On the ADV7181C, the DDR interface is supported for clock frequencies up to 75 MHz

DDR_EN Enable DDR Mode (CP), *Address 0xC9, [3]*

Function

DDR_EN	Description
0 ⊂	Output in 4:2:2 or 4:4:4 format (as determined by CPOP_SEL[3:0]).
1	Enables second interleaving stage and clock delay block. **Note:** As a prerequisite, the first interleaving stage must be enabled via CPOP_SEL[3:0]. Select 4:2:2 output mode and refer to the information on CPOP_SEL[3:0] on page 188.

DDR_CLK_DEL[3:0] DDR Clock Delay (CP), *Address 0x89, [3:0]*

The setup and hold time of the DDR clock versus data on the bus can be influenced by setting the DDR_CLK_DEL[3:0] control bits. The delay figure of data versus clock is absolute and does not scale with the LLC clock frequency. It must be noted that this delay figure depends on operating temperature, voltage supply levels and the IC manufacturing process variations. Therefore, care must be taken to ensure the DDR interface works on all corners.

It is expected that the current DDR interface architecture will work reliably up to HD rates. For faster data transmission (GR modes), the interface can be made work for a specific temperature/supply/process range. However, it is not expected to be able to achieve reliable operation over all corners.

Note: It depends on the downstream ICs whether the SAV and EAV code words are supposed to last one full LLC cycle (AV code lasts 4 clocks) or whether they too should be output at DDR rate (AV code lasts 2 clocks).

Refer to the description of CP_DUP_AV on page 61 for information on how to control the duplication of AV codes after the first interleaving stage.

9.3.1 Pin Assignment

Table 51: DDR Bus Assignment

		8-Bit DDR		**10-Bit DDR**		**12-Bit DDR**		**12-Bit DDR**	
Pixel Port ID	**D[x]**	**Comp ↑**	**Comp ↓**	**Comp ↑**	**Comp ↓**	**RGB ↑**	**RGB ↓**	**YCrCb ↑**	**YCrCb ↓**
P[9]	11	N/A	N/A	N/A	N/A	G[3]	R[7]	Y[3]	Cr[7]
P[8]	10	N/A	N/A	N/A	N/A	G[2]	R[6]	Y[2]	Cr[6]
P[7]	9	N/A	N/A	N/A	N/A	G[1]	R[5]	Y[1]	Cr[5]
P[6]	8	N/A	N/A	N/A	N/A	G[0]	R[4]	Y[0]	Cr[4]
P[19]	7	Y[7]	C_B/C_R[7]	Y[9]	C_B/C_R[9]	B[7]	R[3]	Cb[7]	Cr[3]
P[18]	6	Y[6]	C_B/C_R[6]	Y[8]	C_B/C_R[8]	B[6]	R[2]	Cb[6]	Cr[2]
P[17]	5	Y[5]	C_B/C_R[5]	Y[7]	C_B/C_R[7]	B[5]	R[1]	Cb[5]	Cr[1]
P[16]	4	Y[4]	C_B/C_R[4]	Y[6]	C_B/C_R[6]	B[4]	R[0]	Cb[4]	Cr[0]
P[15]	3	Y[3]	C_B/C_R[3]	Y[5]	C_B/C_R[5]	B[3]	G[7]	Cb[3]	Y[7]
P[14]	2	Y[2]	C_B/C_R[2]	Y[4]	C_B/C_R[4]	B[2]	G[6]	Cb[2]	Y[6]
P[13]	1	Y[1]	C_B/C_R[1]	Y[3]	C_B/C_R[3]	B[1]	G[5]	Cb[1]	Y[5]
P[12]	0	Y[0]	C_B/C_R[0]	Y[2]	C_B/C_R[2]	B[0]	G[4]	Cb[0]	Y[4]
P[11]		N/A	N/A	Y[1]	C_B/C_R[1]	N/A	N/A	N/A	N/A
P[10]		N/A	N/A	Y[0]	C_B/C_R[0]	N/A	N/A	N/A	N/A

Table 51 shows the bus assignment in DDR mode. The top row in the table provides clock polarity information. Table 48 relates D[x] to the actual data port pins.

9.4 Default Color Output (CP)

In the event of loss of input signal, the ADV7181C can be configured to output a default color rather than noise. The default color values are given in Table 52.

The times at which the default colors are inserted can be set as follows:

- Output is forced: default colors are always output
- Automatic mode: default colors are output when the system detects a loss of video signal
- Default colors disabled

Table 52: Default Color Output Values (CP)

Mode	BLANK_RGB_SEL	CP_DEF_COL_MAN_VAL	Signal	Value
Default – GR	1	0	CH_A (G)	0
			CH_B (R)	0
			CH_C (B)	135_d
Default – COMP	0	0	CH_A (Y)	35_d
			CH_A (Pr)	114_d
			CH_A (Pb)	212_d
Man. Override	x	1	CH_A	DEF_COL_CHA[7:0]
			CH_B	DEF_COL_CHB[7:0]
			CH_C	DEF_COL_CHC[7:0]

CP_DEF_COL_FORCE Force Output of Default Colors (CP), *Address 0xBF, [0]*

Setting this bit high forces the permanent output of default colors. Refer to Table 52 for information about the actual colors output.

Note: The CP_DEF_COL_FORCE bit has highest priority. It overrides the CP_DEF_COL_AUTO bit.

Function

CP_DEF_COL_FORCE	Description
0	Do not force default color output
1	Forces the permanent output of default colors (and thus overwrites video data)

CP_DEF_COL_AUTO Automatic Output of Default Colors (CP), *Address 0xBF, [1]*

Setting this bit high enables the automatic output of default colors. For information about the actual colors output, refer to Table 52 and the relevant discussion. The data is inserted when CP looses lock to the input video. The state in which this happens can be monitored via the STATUS_2[6] (CP_FREE_RUN). Refer to Section 6.2 for more information.

The decision whether or not lock is lost depends primarily on the measured length of the incoming video line being compared with the line length as decoded from PRIM_MODE and VID_STD. If the two values differ by more than a certain threshold, the ADV7181C enters free run mode, outputs the default color (if enabled via CP_DEF_COL_AUTO), and updates the status register.

Notes:

- The CP_DEF_COL_AUTO bit has lower priority than the CP_DEF_COL_FORCE bit. If in FORCE mode, default colors are output regardless of the lock status of the CP block.
- Internal parameters, e.g. the threshold for entering free-run mode, can be overwritten by internal parameters. Contact ADI for further details, if required.

Function

CP_DEF_COL_AUTO	Description
0	Disables automatic insertion of default color
1 ⊂	Outputs default colors when the CP core looses sync to the input video

CP_DEF_COL_MAN_VAL Enable Manual Selection of Default Colors (CP), *Address 0xBF, [2]*

Table 52 shows the default colors for component and graphics based video. The values describe the color blue. Setting the CP_DEF_COL_MAN_VAL bit high enables the user to overwrite the default colors with values given in DEF_COL_CHA[7:0], DEF_COL_CHB[7:0] and DEF_COL_CHC[7:0].

Function

CP_DEF_COL_MAN_VAL	Description
0 ⊂	Uses default color blue (refer to Table 52 for values)
1	Outputs default colors as given in CP_DEF_COL_CHA/B/C[7:0]

DEF_COL_CHA/B/C[7:0] Manual Default Color Channel A/B/C (CP), *Address 0xC0, [7:0]; Address 0xC1, [7:0]; Address 0xC2, [7:0]*

The three parameters DEF_COL_CHA[7:0], DEF_COL_CHB[7:0] and DEF_COL_CHC[7:0] allow the user to specify their own default values.

Note: CP_DEF_COL_MAN_VAL must be set high for the three parameters to be used.

Refer to Table 52 for more information on the automatic values.

Function

DEF_COL_CHA[7:0]	Description
xxxx xxxx ⊂	Manual default color for channel A

Function

DEF_COL_CHB[7:0]	Description
xxxx xxxx ⊂	Manual default color for channel B

Function

DEF_COL_CHC[7:0]	Description
xxxx xxxx ⊂	Manual default color for channel C

9.5 Free Run Mode (CP)

Free Run mode is intended to provide the user with a stable clock and predictable data if the input signal cannot be decoded, e.g. input video is not present. It controls the default color insertion and it causes the ADV7181C to generate a default clock.

CP_F_RUN_TH[2:0] CP Free Run Threshold Select, *Address 0xB3, [2:0]*

The CP_F_RUN_TH[2:0] parameter determines the conditions under which free-run mode is entered or left.

The length of the incoming video line is measured based on the 28.63636 MHz crystal clock. This value is compared with an internally stored parameter and the magnitude of the difference decides whether or not CP will enter free-run mode. The CP_F_RUN_TH[2:0] bits allow the user to select the threshold.

The internally stored parameter (the 'ideal' line length) is usually decoded off PRIM_MODE and VID_STD. For video standards other than the preprogrammed settings of PRIM_MODE and VID_STD, the ideal line length can be manually set via **FR_LL[10:0] Free Run Line Length (CP)**

Function

CP_F_RUN_TH[2:0]	Description	
	Minimum Difference to Switch **into** Free-run	Maximum Error to Switch **out** of Free-run
000	2	1
001	256	200
010	128	112
011	64	48
100 ⊂	32	24
101	16	12
110	8	6
111	4	3

FR_LL[10:0] Free Run Line Length (CP), *Address 0x8F, [2:0], Address 0x90, [7:0]*

This parameter holds the ideal line length for a given video standard. It affects the way CP handles the unlocked state. If set to 0, the internally used free-run line length value is decoded from the current setting of PRIM_MODE and VID_STD. For standards not covered by the preprogrammed values, the FR_LL[10:0] parameter must be set to the ideally expected length of one line of input video.

Refer also to information on CP_F_RUN_TH[2:0] on page 193.

Notes:

- The register locations where FR_LL[10:8] and FR_LL[7:0] reside are WRITE_ONLY.

- The FR_LL[10:0] parameter has **no** effect on the video decoding.

Function

FR_LL[10:0]	Description
0x000 ⊂	Actually used internal free-run line length is decoded of PRIM_MODE and VID_STD
All other values	Use as ideal line length to enter and leave free-run mode

10 Specifications and Characteristics

10.1 Electrical Characteristics

The temperature range is T_{MIN} to T_{MAX}, -40°C to +85°C. The minimum/maximum specifications are guaranteed over this range. All specifications obtained using programming scripts with the following sequence included: Address 0x0E – data 0x80, Address 0x54 – data 0x00, and Address 0x0E – data 0x00.

At AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V, nominal input range 1.6 V. Operating temperature range, unless otherwise noted.

Table 53: Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[1, 2]						
Resolution (each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 27 MHz (10-bit level)		±0.6	±2.5	LSB
Integral Nonlinearity	INL	BSL at 54 MHz (10-bit level)		−0.6/+0.7		LSB
Integral Nonlinearity	INL	BSL at 74 MHz (10-bit level)		±1.4		LSB
Integral Nonlinearity	INL	BSL at 110 MHz (8-bit level)		±0.9		LSB
Differential Nonlinearity	DNL	At 27 MHz (10-bit level)		−0.2/+0.25	−0.99/+2.5	LSB
Differential Nonlinearity	DNL	At 54 MHz (10-bit level)		−0.2/+0.25		LSB
Differential Nonlinearity	DNL	At 74 MHz (10-bit level)		±0.9		LSB
Differential Nonlinearity	DNL	At 110 MHz (8-bit level)		−0.2/+1.5		LSB
DIGITAL INPUTS[3]						
Input High Voltage[4]	V_{IH}		2			V
Input Low Voltage[5]	V_{IL}				0.8	V
Input High Voltage	V_{IH}	HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage	V_{IL}	HS_IN, VS_IN low trigger mode			0.3	V
Input Current	I_{IN}		−10		+10	μA
Input Capacitance[3]	C_{IN}				10	pF

[1] All ADC linearity tests performed at input range of full scale – 12.5%, and at zero scale + 12.5%.
[2] Maximum INL and DNL specifications obtained with part configured for component video input.
[3] Guaranteed by characterization.
[4] To obtain specified V_{IH} level on Pin 22, register 0x13 (wo) must be programmed with value 0x04. If register 0x13 is programmed with value 0x00, then V_{IH} on Pin 22 = 1.2 V.
[5] To obtain specified V_{IL} level on Pin 22, register 0x13 (wo) must be programmed with value 0x04. If register 0x13 is programmed with value 0x00, then V_{IL} on Pin 22 = 0.4 V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUTS						
Output High Voltage[1]	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage[1]	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pin 1			60	µA
		All other output pins			10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS						
Digital Core Power Supply	DVDD		1.65	1.8	2	V
Digital I/O Power Supply	DVDDIO		3.0	3.3	3.6	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		3.15	3.3	3.45	V
Digital Core Supply Current	IDVDD	CVBS input sampling at 54 MHz		105		mA
		Graphics RGB sampling at 110 MHz		113		mA
		SCART RGB FB sampling at 54 MHz		106		mA
Digital I/O Supply Current	IDVDDIO	CVBS input sampling at 54 MHz		4		mA
		Graphics RGB sampling at 110 MHz		16		mA
PLL Supply Current	IPVDD	CVBS input sampling at 54 MHz		11		mA
		Graphics RGB sampling at 110 MHz		12		mA
Analog Supply Current[2]	IAVDD	CVBS input sampling at 54 MHz		99		mA
		Graphics RGB sampling at 110 MHz		198		mA
		SCART RGB FB sampling at 54 MHz		269		mA
Power-Down Current	IPWRDN			2.25		mA
Green Mode Power-Down	IPWRDNG	Synchronization bypass function		16		mA
Power-Up Time	TPWRUP			20		ms

[1] V_{OH} and V_{IL} levels obtained using default drive strength value (0xD5) in register subaddress 0xF4.
[2] Analog current measurements for CVBS made with ADC0 powered up only, For RGB, ADC0, ADC1 and ADC2 powered up only, for SCART FB, all ADCs powered up.

10.2 Video Specifications

Temperature range: T_{MIN} to T_{MAX}, -40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.

Guaranteed by characterization. At A_{VDD} = 3.15V to 3.45V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0V to 3.6V, P_{VDD} = 1.71V to 1.89V, nominal input range =1.6V (operating temperature range, unless otherwise noted).

Table 54: Video Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulated 5 step		0.5		degree
Differential Gain	DG	CVBS input, modulated 5 step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5 step		0.5		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	54	56		dB
SNR Unweighted		Luma flat field	58	60		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
F_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock in Time				60		line
Sync Depth Range[1]			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		field
Horizontal Lock Time				100		line
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		degree
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		degree
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

10.3 Timing Specifications

Temperature range: T_{MIN} to T_{MAX}, -40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0V to 3.6 V, P_{VDD} = 1.71 V to 1.89 V, nominal input range =1.6 V (operating temperature range, unless otherwise noted).

[1] Nominal synchronization depth is 300 mV at 100% synchronization depth range.

Table 55: Timing Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
LLC1 Frequency Range[1]			12.825		110	MHz
I^2C PORT[2]						
SCLK Frequency					400	kHz
SCLK Min Pulse Width High	t_1		0.6			µs
SCLK Min Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC1 Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA and CONTROL OUTPUTS						
Data Output Transition Time SDR (SDP)[3]	t_{11}	Negative clock edge to start of valid data			3.6	ns
Data Output Transition Time SDR (SDP)[3]	t_{12}	End of valid data to negative clock edge			2.4	ns
Data Output Transition Time SDR (CP)[4]	t_{13}	End of valid data to negative clock edge			2.8	ns
Data Output Transition Time SDR (CP)[4]	t_{14}	Negative clock edge to start of valid data			0.1	ns
Data Output Transition Time DDR (CP)[4, 5]	t_{15}	Positive clock edge to end of valid data	−4 + TLLC/4			ns
Data Output Transition Time DDR (CP)[4, 5]	t_{16}	Positive clock edge to start of valid data	0.25 + TLLC/4			ns
Data Output Transition Time DDR (CP)[4, 5]	t_{17}	Negative clock edge to end of valid data	−2.95 + TLLC/4			ns
Data Output Transition Time DDR (CP)[4, 5]	t_{18}	Negative clock edge to start of valid data	−0.5 + TLLC/4			ns

[1] Maximum LLC frequency is 110 MHz.
[2] TTL input values are 0 V to 3 V, with rise/fall times ≤3 ns, measured between the 10% and 90% points.
[3] SDP timing figures obtained using default drive strength value (0xD5) in register subaddress 0xF4.
[4] CP timing figures obtained using maximum drive strength value (0xFF) in register subaddress 0xF4.
[5] DDR timing specifications dependent on LLC output pixel clock; TLCC/4 = 9.25 ns at LLC = 27 MHz.

10.4 Analog Specifications

Temperature range: T_{MIN} to T_{MAX}, -40°C to +85°C. The minimum/maximum specifications are guaranteed over this range.

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.71 V to 1.89 V, nominal input range =1.6 V (operating temperature range, unless otherwise noted).

Table 56: Analog Specifications

Parameter	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance[1]	Clamps switched off		10		MΩ
Input Impedance of Pin 34 (FB)			20		kΩ
CML			1.86		V
ADC Full-Scale Level			CML + 0.8 V		V
ADC Zero-Scale level			CML − 0.8 V		V
ADC Dynamic Range			1.6		V
Clamp Level (When Locked)	CVBS input		CML – 0.292 V		V
	SCART RGB input (R, G, B signals)		CML – 0.4 V		V
	S-Video input (Y signal)		CML – 0.292 V		V
	S-Video input (C signal)		CML – 0 V		V
	Component input (Y, Pr, Pb signals)		CML – 0.3 V		V
	PC RGB input (R, G, B signals)		CML – 0.3 V		V
Large Clamp Source Current	SDP only		0.75		mA
Large Clamp Sink Current	SDP only		0.9		mA
Fine Clamp Source Current	SDP only		17		µA
Fine Clamp Sink Current	SDP only		17		µA

10.5 Thermal Specifications

Table 57: Thermal Specifications

Thermal Characteristics	Symbol	Test Conditions	Typ	Unit
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane	7	°C/W
Junction-to-Ambient Thermal Resistance	θ_{JA}	4-layer PCB with solid ground plane (still air)	30	°C/W

[1] Except Pin 34 (FB).

10.5.1 Package Thermal Performance

To reduce power consumption when using the part, the user is advised to turn off any unused ADC's . The junction temperature must at all times stay below the maximum junction temperature ($T_{J\ MAX}$) of 125°C. The following equation shows how to calculate this junction temperature:

$$T_J = T_{AmbMax} + (\Theta_{JA} \times W_{\max})$$

where:

$T_{AmbMax} = 85°C$

$\Theta_{JA} = 45.5°C/W$

$W_{\max} = ((A_{VDD} x\ I_{AVDD}) + (D_{VDD}\ x\ I_{DVDD}) + (D_{VDDIO}\ x\ I_{DVDDIO}) + (P_{VDD}\ x\ I_{PVDD}))$

10.6 Timing Diagrams

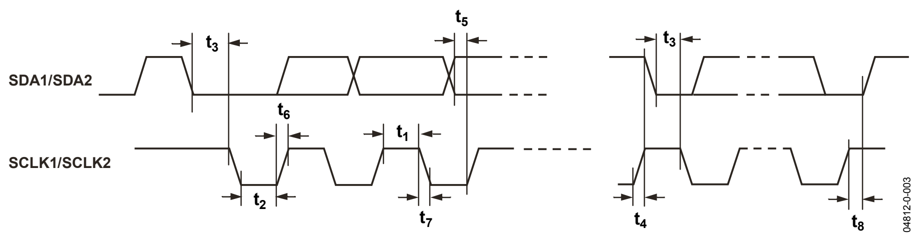


Figure 71: I²C Timing

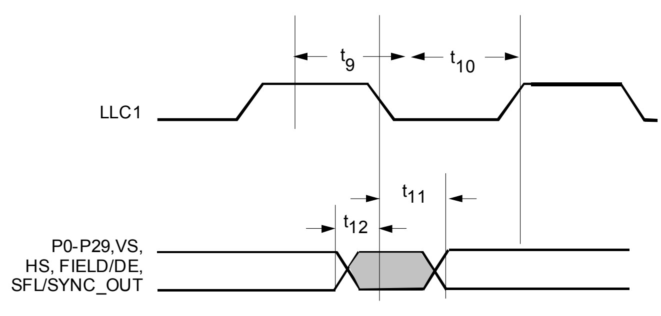


Figure 72: Pixel Port and Control Output SDR Timing (SD Core)

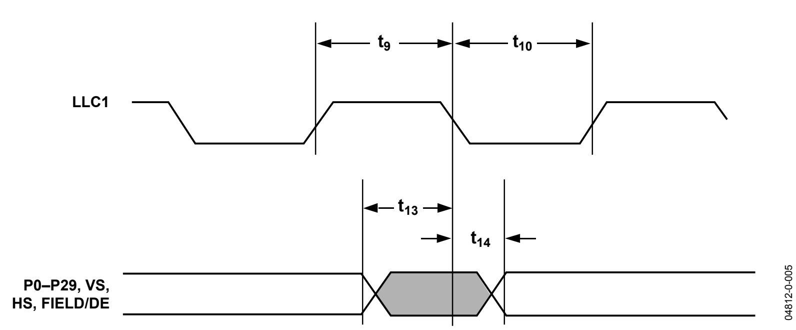


Figure 73: Pixel Port SDR Timing (CP Core)

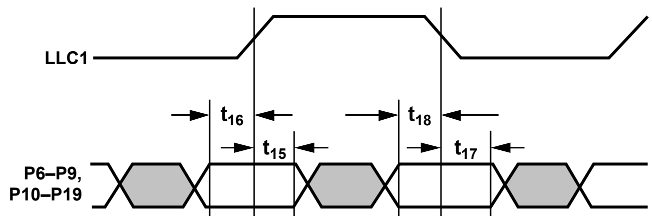


Figure 74: Pixel Port DDR Timing (CP Core)

11 MPU Port Description

The ADV7181C supports a 2-wire serial (I^2C compatible) interface. Four inputs, Serial Data (SDA1 and SDA2) and Serial Clock (SCLK1 and SCLK2), carry information between the ADV7181C and the system I^2C master controller. Each slave device is recognized by a unique address. The ADV7181C has two ports; the first port is called the Control port, which allows the user to set up and configure the decoder. The second port is called the VBI data readback port, which allows the user to readback captured VBI data over this port. Note that the VBI readback port is used only for backward compatibility with the ADV7402a decoder, and is not recommended for use with the ADV7181C.

Both the Control and VBI port have four possible slave addresses for both read and write operations, depending on the logic level on the ALSB pin. These four unique addresses are illustrated in Table 58. The ALSB pin of the ADV7181C controls bit 1 of the slave address. By altering the ALSB, it is possible to control two ADV7181Cs in an application without having a conflict with the same slave address. The LSB (bit 0) sets either a read or write operation. Logic level ‘1’ corresponds to a read operation while logic level ‘0’ corresponds to a write operation.

Table 58: I^2C Address for ADV7181C

ALSB	R/W	Slave Address Control Port	Slave Address VBI Port
0	0	0x40	0x20
0	1	0x41	0x21
1	0	0x42	0x22
1	1	0x43	0x23

To control the device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a Start condition, defined by a high to low transition on SDA1/SDA2 while SCLK1/SCLK2 remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-bit address + R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition.

The idle condition is where the device monitors the SDA1/SDA2 and SCLK1/SCLK2 lines waiting for the Start condition and the correct transmitted address. The R/W bit determines the direction of the data. A logic ‘0’ on the LSB of the first byte means that the master will write information to the peripheral. A logic ‘1’ on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7181C acts as a standard slave device on the bus. The data on the SDA pin is 8-bits long supporting the 7-bit addresses plus the R/W bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, these cause an immediate jump to the idle condition. During a given SCLK high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7181C will not issue an acknowledge and will return to the idle condition.

If in auto-increment mode the user exceeds the highest subaddress, the following actions are taken:

- In Read Mode, the highest subaddress register contents continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
- In Write Mode, the data for the invalid byte is not loaded into any subaddress register. A no-acknowledge is issued by the ADV7181C, and the part returns to the idle condition.

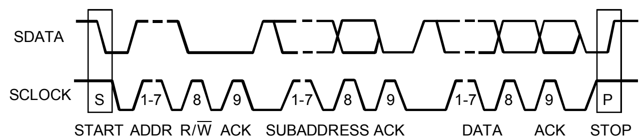


Figure 75: Bus Data Transfer

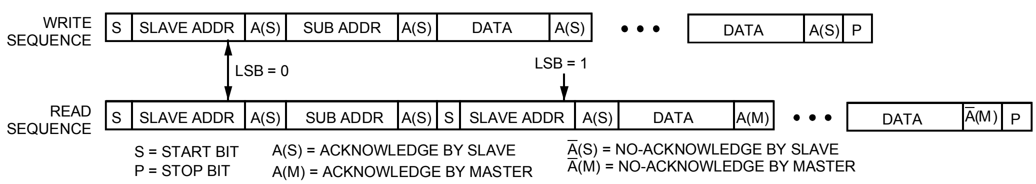


Figure 76: Read and Write Sequence

11.1 Register Access

The MPU can write to or read from all of the registers of the ADV7181C except those subaddress registers that are read only or write only. The subaddress register determines the register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. Then a read/write operation is performed from/to the target address, which increments to the next address until a Stop command on the bus is performed.

11.2 Register Programming

As can be seen in Table 59 and Table 60, the registers in the ADV7181C are arranged into two maps: the "User Map" (enabled by default) and the "User Sub Map". The User Sub Map has controls for the interrupt and VDP functionality on the ADV7181C and the User Map controls everything else. The User Map and the User Sub Map consist of a "Common Space" from address 0x00 to 0x3F. Depending on how bit 5 in register 0x0E (SUB_USR_EN) is set, the register map then splits in two sections.

11.2.1 SUB_USR_EN, Address 0x0E, [5]

This bit splits the register map at register 0x40.

Function

SUB_USR_EN	Description
0 ⊂	The Register map does not split – User Map Enabled.
1	The Register map splits – User Sub Map Enabled

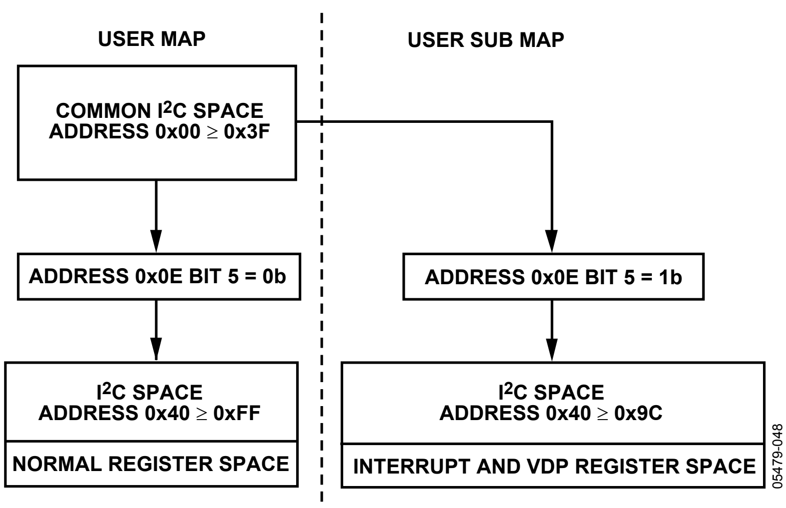


Figure 77: Register Access - User Map and User Sub Map

11.3 I²C Sequencer

An I²C sequencer is employed in cases where a parameter exceeds 8 bits and thus is distributed over two or more I²C registers, e.g. **A_OFFSET[9:0]** in the *Component Processor Offset Block* section of this manual.

When such a parameter is changed using two or more I²C writes operations, the parameter may hold an invalid value for the time between the first I²C finishing and the last I²C being completed. In other words, the top bits of the parameter can already hold the new value while the remaining bits of the parameter still hold the previous value.

To avoid this problem, the I^2C sequencer holds the already updated bits of the parameter in a local memory and only updates all bits of the parameter together once the last register write operation has completed.

The correct operation of the I^2C sequencer relies on:

- All I^2C registers for the parameter in question are written to in order of ascending addresses, e.g. for A_OFFSET[9:0]: write to address *0x77* first, followed by *0x78*.
- No other I^2C to take place between the two (or more) I^2C writes for the sequence, e.g. for A_OFFSET[9:0]: write to address *0x77* first, immediately followed by *0x78*.

11.4 I²C Register Map

Table 59: User Map

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex)
Dec	Hex												
0	00	Input Control	rw	VID_SEL.3	VID_SEL.2	VID_SEL.1	VID_SEL.0	INSEL.3	INSEL.2	INSEL.1	INSEL.0	00000000	00
1	01	Video Selection	rw		ENHSPLL	BETACAM		ENVSPROC				11001000	C8
3	03	Output Control	rw	VBI_EN	TOD	OF_SEL.3	OF_SEL.2	OF_SEL.1	OF_SEL.0		SD_DUP_AV	00001100	0C
4	04	Extended Output Control	rw	BT656-4				TIM_OE	BL_C_VBI	EN_SFL_PIN	RANGE	01xx0101	45
5	05	Primary Mode	rw					PRIM_MODE.3	PRIM_MODE.2	PRIM_MODE.1	PRIM_MODE.0	00000000	00
6	06	Video Standard	rw					VID_STD.3	VID_STD.2	VID_STD.1	VID_STD.0	00000010	02
7	07	Autodetect Enable	rw	AD_SEC525_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN	01111111	7F
8	08	Contrast	rw	CON.7	CON.6	CON.5	CON.4	CON.3	CON.2	CON.1	CON.0	10000000	80
10	0A	Brightness	rw	BRI.7	BRI.6	BRI.5	BRI.4	BRI.3	BRI.2	BRI.1	BRI.0	00000000	00
11	0B	Hue	rw	HUE.7	HUE.6	HUE.5	HUE.4	HUE.3	HUE.2	HUE.1	HUE.0	00000000	00
12	0C	Default Value Y	rw	DEF_Y.5	DEF_Y.4	DEF_Y.3	DEF_Y.2	DEF_Y.1	DEF_Y.0	DEF_VAL_AUTO_EN	DEF_VAL_EN	00110110	36
13	0D	Default Value C	rw	DEF_C.7	DEF_C.6	DEF_C.5	DEF_C.4	DEF_C.3	DEF_C.2	DEF_C.1	DEF_C.0	01111100	7C
14	0E	ADI Control	rw	HIDI2CEN	SUB_USR_EN.1	SUB_USR_EN.0						00000000	00
15	0F	Power Management	rw	RES		PWRDN[1]	PWRSAV	CP_PWRDN	PWRDN[0]	FB_PWRDN		00000000	00
16	10	Status 1	r	COL_KILL	AD_RESULT.2	AD_RESULT.1	AD_RESULT.0	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK	---	---
17	11	Ident	r	IDENT.7	IDENT.6	IDENT.5	IDENT.4	IDENT.3	IDENT.2	IDENT.1	IDENT.0	---	---
18	12	Status 2	r	TLLC PLL LOCK	CP FREE RUN	FSC NSTD	LL NSTD	MV AGC DET	MV PS DET	MVCS T3	MVCS DET	---	---
19	13	Status 3	r	PAL SW LOCK	INTERLACE	STD FLD LEN	FREE_RUN_ACT	CVBS	SD_OP_50Hz	GEMD	INST_HLOCK	---	---
19	13	Analogue Control Internal	w						XTAL_TTL_SEL			00000000	00
20	14	Analogue Clamp Control	rw				CCLEN					00010010	12
21	15	Digital Clamp Control 1	rw		DCT.1	DCT.0						0000xxxx	00
23	17	Shaping Filter Control	rw	CSFM.2	CSFM.1	CSFM.0	YSFM.4	YSFM.3	YSFM.2	YSFM.1	YSFM.0	00000001	01
24	18	Shaping Filter Control 2	rw	WYSFMOVR			WYSFM.4	WYSFM.3	WYSFM.2	WYSFM.1	WYSFM.0	10010011	93
25	19	Comb Filter Control	rw					NSFSEL.1	NSFSEL.0	PSFSEL.1	PSFSEL.0	11110001	F1
29	1D	Vertical Scale Value 1	rw	TRI_LLC	EN28XTAL							00000xxx	00
39	27	Pixel Delay Control	rw	SWPC	AUTO_PDC_EN	CTA.2	CTA.1	CTA.0		LTA.1	LTA.0	01011000	58
43	2B	Misc Gain Control	rw		CKE						PW_UPD	11100001	E1
44	2C	AGC Mode Control	rw		LAGC.2	LAGC.1	LAGC.0			CAGC.1	CAGC.0	10101110	AE
45	2D	Chroma Gain Control 1	w	CAGT.1	CAGT.0			CMG.11	CMG.10	CMG.9	CMG.8	11110100	F4
46	2E	Chroma Gain Control 2	w	CMG.7	CMG.6	CMG.5	CMG.4	CMG.3	CMG.2	CMG.1	CMG.0	00000000	00
47	2F	Luma Gain Control 1	w	LAGT.1	LGAT.0			LMG.11	LMG.10	LMG.9	LMG.8	1111xxxx	F0
48	30	Luma Gain Control 2	w	LMG.7	LMG.6	LMG.5	LMG.4	LMG.3	LMG.2	LMG.1	LMG.0	xxxxxxxx	00
49	31	VSync Field Control 1	rw				NEWAVMODE	HVSTIM				00010010	12
50	32	VSync Field Control 2	rw	VSBHO	VSBHE							01000001	41
51	33	VSync Field Control 3	rw	VSEHO	VSEHE							10000100	84
52	34	HSync Position Control 1	rw		HSB.10	HSB.9	HSB.8		HSE.10	HSE.9	HSE.8	00000000	00

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex)
Dec	Hex												
53	35	HSync Position Control 2	rw	HSB.7	HSB.6	HSB.5	HSB.4	HSB.3	HSB.2	HSB.1	HSB.0	00000010	02
54	36	HSync Position Control 3	rw	HSE.7	HSE.6	HSE.5	HSE.4	HSE.3	HSE.2	HSE.1	HSE.0	00000000	00
55	37	Polarity	rw	PHS		PVS		PF			PCLK	00000001	01
56	38	NTSC Comb Control	rw	CTAPSN.1	CTAPSN.0	CCMN.2	CCMN.1	CCMN.0	YCMN.2	YCMN.1	YCMN.0	10000000	80
57	39	PAL Comb Control	rw	CTAPSP.1	CTAPSP.0	CCMP.2	CCMP.1	CCMP.0	YCMP.2	YCMP.1	YCMP.0	11000000	C0
58	3A	ADC Control	rw	LATCH_CLK .3	LATCH_CLK .2	LATCH_CLK .1	LATCH_CLK .0	PDN_ADC0	PDN_ADC1	PDN_ADC2	PDN_ADC3	00010001	11
59	3B	Bias Control	rw	IBIAS_SET.4	IBIAS_SET.3	IBIAS_SET.2	IBIAS_SET.1	IBIAS_SET.0			EN_INTERN AL_RES	10000101	85
60	3C	TLLC Control Analogue	rw	SOG_SYNC _LEV.4	SOG_SYNC _LEV.3	SOG_SYNC _LEV.2	SOG_SYNC _LEV.1	SOG_SYNC _LEV.0	PLL_QPUM P.2	PLL_QPUM P.1	PLL_QPUM P.0	01011000	58
61	3D	Manual Window Control	rw		CKILLTHR.2	CKILLTHR.1	CKILLTHR.0					01000011	43
65	41	Resample Control	rw		SFL_INV							00000001	01
72	48	GemStar Ctrl 1	rw	GDECEL.15	GDECEL.14	GDECEL.13	GDECEL.12	GDECEL.11	GDECEL.10	GDECEL.9	GDECEL.8	00000000	00
73	49	GemStar Ctrl 2	rw	GDECEL.7	GDECEL.6	GDECEL.5	GDECEL.4	GDECEL.3	GDECEL.2	GDECEL.1	GDECEL.0	00000000	00
74	4A	GemStar Ctrl 3	rw	GDECOL.15	GDECOL.14	GDECOL.13	GDECOL.12	GDECOL.11	GDECOL.10	GDECOL.9	GDECOL.8	00000000	00
75	4B	GemStar Ctrl 4	rw	GDECOL.7	GDECOL.6	GDECOL.5	GDECOL.4	GDECOL.3	GDECOL.2	GDECOL.1	GDECOL.0	00000000	00
76	4C	GemStar Ctrl 5	rw								GDECAD	xxxx0000	00
77	4D	CTI DNR Ctrl 1	rw			DNR_EN		CTI_AB.1	CTI_AB.0	CTI_AB_EN	CTI_EN	11101111	EF
78	4E	CTI DNR Ctrl 2	rw	CTI_C_TH.7	CTI_C_TH.6	CTI_C_TH.5	CTI_C_TH.4	CTI_C_TH.3	CTI_C_TH.2	CTI_C_TH.1	CTI_C_TH.0	00001000	08
80	50	CTI DNR Ctrl 4	rw	DNR_TH.7	DNR_TH.6	DNR_TH.5	DNR_TH.4	DNR_TH.3	DNR_TH.2	DNR_TH.1	DNR_TH.0	00001000	08
81	51	Lock Count	rw	FSCLE	SRLS	COL.2	COL.1	COL.0	CIL.2	CIL.1	CIL.0	00100100	24
82	52	CSC_1	rw	CSC_scale			A4.12	A4.11	A4.10	A4.9	A4.8	10000000	80
83	53	CSC_2	rw	A4.7	A4.6	A4.5	A4.4	A4.3	A4.2	A4.1	A4.0	00000000	00
84	54	CSC_3	rw		A3.12	A3.11	A3.10	A3.9	A3.8	A3.7	A3.6	00000000	00
85	55	CSC_4	rw	A3.5	A3.4	A3.3	A3.2	A3.1	A3.0	A2.12	A2.11	00000000	00
86	56	CSC_5	rw	A2.10	A2.9	A2.8	A2.7	A2.6	A2.5	A2.4	A2.3	00000000	00
87	57	CSC_6	rw	A2.2	A2.1	A2.0	A1.12	A1.11	A1.10	A1.9	A1.8	00001000	08
88	58	CSC_7	rw	A1.7	A1.6	A1.5	A1.4	A1.3	A1.2	A1.1	A1.0	00000000	00
89	59	CSC_8	rw				B4.12	B4.11	B4.10	B4.9	B4.8	00000000	00
90	5A	CSC_9	rw	B4.7	B4.6	B4.5	B4.4	B4.3	B4.2	B4.1	B4.0	00000000	00
91	5B	CSC_10	rw		B3.12	B3.11	B3.10	B3.9	B3.8	B3.7	B3.6	00000000	00
92	5C	CSC_11	rw	B3.5	B3.4	B3.3	B3.2	B3.1	B3.0	B2.12	B2.11	00000001	01
93	5D	CSC_12	rw	B2.10	B2.9	B2.8	B2.7	B2.6	B2.5	B2.4	B2.3	00000000	00
94	5E	CSC_13	rw	B2.2	B2.1	B2.0	B1.12	B1.11	B1.10	B1.9	B1.8	00000000	00
95	5F	CSC_14	rw	B1.7	B1.6	B1.5	B1.4	B1.3	B1.2	B1.1	B1.0	00000000	00
96	60	CSC_15	rw				C4.12	C4.11	C4.10	C4.9	C4.8	00000000	00
97	61	CSC_16	rw	C4.7	C4.6	C4.5	C4.4	C4.3	C4.2	C4.1	C4.0	00000000	00
98	62	CSC_17	rw		C3.12	C3.11	C3.10	C3.9	C3.8	C3.7	C3.6	00100000	20
99	63	CSC_18	rw	C3.5	C3.4	C3.3	C3.2	C3.1	C3.0	C2.12	C2.11	00000000	00
100	64	CSC_19	rw	C2.10	C2.9	C2.8	C2.7	C2.6	C2.5	C2.4	C2.3	00000000	00
101	65	CSC_20	rw	C2.2	C2.1	C2.0	C1.12	C1.11	C1.10	C1.9	C1.8	00000000	00
102	66	CSC_21	rw	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0	00000000	00
103	67	CSC_22	rw	DLY_A	DLY_B	DLY_C	SOFT_FILT	DS_ONLY	DPP_FILT.2	DPP_FILT.1	DPP_FILT.0	00000011	03
104	68	CSC_23	rw								DPP_AFILT	00000001	01
105	69	Config 1	rw	TRI_LEVEL	SYN_LOTRI G	INV_DINCLK				SDM_SEL.1	SDM_SEL.0	00000x00	00
106	6A	TLLC Phase Adjust	rw			BYP_DLL	DLL_PH.4	DLL_PH.3	DLL_PH.2	DLL_PH.1	DLL_PH.0	0x000000	00
107	6B	CP Output Selection	rw	HS_OUT_SE L	F_OUT_SEL			CPOP_SEL. 3	CPOP_SEL. 2	CPOP_SEL. 1	CPOP_SEL. 0	11000000	C0

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex)
Dec	Hex												
108	6C	CP Clamp 1	rw	CLMP_A_MAN	CLMP_BC_MAN	CLMP_FREEZE		CLMP_A.11	CLMP_A.10	CLMP_A.9	CLMP_A.8	00000000	00
109	6D	CP Clamp 2	rw	CLMP_A.7	CLMP_A.6	CLMP_A.5	CLMP_A.4	CLMP_A.3	CLMP_A.2	CLMP_A.1	CLMP_A.0	00000000	00
110	6E	CP Clamp 3	rw	CLMP_B.11	CLMP_B.10	CLMP_B.9	CLMP_B.8	CLMP_B.7	CLMP_B.6	CLMP_B.5	CLMP_B.4	00000000	00
111	6F	CP Clamp 4	rw	CLMP_B.3	CLMP_B.2	CLMP_B.1	CLMP_B.0	CLMP_C.11	CLMP_C.10	CLMP_C.9	CLMP_C.8	00000000	00
112	70	CP Clamp 5	rw	CLMP_C.7	CLMP_C.6	CLMP_C.5	CLMP_C.4	CLMP_C.3	CLMP_C.2	CLMP_C.1	CLMP_C.0	00000000	00
113	71	CP AGC 1	rw	AGC_TAR.9	AGC_TAR.8	AGC_TAR_MAN	AGC_FREEZE	HS_NORM	AGC_TIM.2	AGC_TIM.1	AGC_TIM.0	xx000000	00
114	72	CP AGC 2	rw	AGC_TAR.7	AGC_TAR.6	AGC_TAR.5	AGC_TAR.4	AGC_TAR.3	AGC_TAR.2	AGC_TAR.1	AGC_TAR.0	xxxxxxxx	00
115	73	CP AGC 3	rw	GAIN_MAN	AGC_MODE_MAN	A_GAIN.9	A_GAIN.8	A_GAIN.7	A_GAIN.6	A_GAIN.5	A_GAIN.4	00010000	10
116	74	CP AGC 4	rw	A_GAIN.3	A_GAIN.2	A_GAIN.1	A_GAIN.0	B_GAIN.9	B_GAIN.8	B_GAIN.7	B_GAIN.6	00000100	04
117	75	CP AGC 5	rw	B_GAIN.5	B_GAIN.4	B_GAIN.3	B_GAIN.2	B_GAIN.1	B_GAIN.0	C_GAIN.9	C_GAIN.8	00000001	01
118	76	CP AGC 6	rw	C_GAIN.7	C_GAIN.6	C_GAIN.5	C_GAIN.4	C_GAIN.3	C_GAIN.2	C_GAIN.1	C_GAIN.0	00000000	00
119	77	CP Offset 1	rw	CP_PREC.1	CP_PREC.0	A_OFFSET.9	A_OFFSET.8	A_OFFSET.7	A_OFFSET.6	A_OFFSET.5	A_OFFSET.4	00111111	3F
120	78	CP Offset 2	rw	A_OFFSET.3	A_OFFSET.2	A_OFFSET.1	A_OFFSET.0	B_OFFSET.9	B_OFFSET.8	B_OFFSET.7	B_OFFSET.6	11111111	FF
121	79	CP Offset 3	rw	B_OFFSET.5	B_OFFSET.4	B_OFFSET.3	B_OFFSET.2	B_OFFSET.1	B_OFFSET.0	C_OFFSET.9	C_OFFSET.8	11111111	FF
122	7A	CP Offset 4	rw	C_OFFSET.7	C_OFFSET.6	C_OFFSET.5	C_OFFSET.4	C_OFFSET.3	C_OFFSET.2	C_OFFSET.1	C_OFFSET.0	11111111	FF
123	7B	CP AV Control	rw	AV_inv_F	AV_inv_V	INTLCD_240P_540P	CP_DUP_AV	AV_BLANK_EN	AV_POS_SEL	AV_CODE_EN	BLANK_RGB_SEL	00011110	1E
124	7C	CP HVF Control 1	rw	PIN_inv_HS	PIN_inv_VS	PIN_inv_F		START_HS.9	START_HS.8	END_HS.9	END_HS.8	110x0000	C0
125	7D	CP HVF Control 2	rw	END_HS.7	END_HS.6	END_HS.5	END_HS.4	END_HS.3	END_HS.2	END_HS.1	END_HS.0	00000000	00
126	7E	CP HVF Control 3	rw	START_HS.7	START_HS.6	START_HS.5	START_HS.4	START_HS.3	START_HS.2	START_HS.1	START_HS.0	00000000	00
127	7F	CP HVF Control 4	rw	START_VS.3	START_VS.2	START_VS.1	START_VS.0	END_VS.3	END_VS.2	END_VS.1	END_VS.0	00000000	00
128	80	CP HVF Control 5	rw	START_FE.3	START_FE.2	START_FE.1	START_FE.0	START_FO.3	START_FO.2	START_FO.1	START_FO.0	00000000	00
131	83	CP Measure Control 3	rw	ISD_THR.7	ISD_THR.6	ISD_THR.5	ISD_THR.4	ISD_THR.3	ISD_THR.2	ISD_THR.1	ISD_THR.0	00000000	00
132	84	CP Measure Control 4	rw	CP_GAIN_FILT.3	CP_GAIN_FILT.2	CP_GAIN_FILT.1	CP_GAIN_FILT.0				IFSD_AVG	00001100	0C
133	85	CP Detection Control 1	rw	POL_MAN_EN	POL_VS	POL_HSCS	SYN_SRC.1	SYN_SRC.0	TRIG_SSPD	SSPD_CONT	DS_OUT	0xx00010	02
134	86	CP Misc Control 1	rw				CPOP_INV_Prb	stdi_line_count_mode	TRIG_STDI	STDI_CONT		00x00011	03
135	87	CP TLLC Control 1	rw	PLL_DIV_MAN_EN			PLL_DLL_UPD_VS_EN	PLL_DIV_RATIO.11	PLL_DIV_RATIO.10	PLL_DIV_RATIO.9	PLL_DIV_RATIO.8	01100011	63
136	88	CP TLLC Control 2	rw	PLL_DIV_RATIO.7	PLL_DIV_RATIO.6	PLL_DIV_RATIO.5	PLL_DIV_RATIO.4	PLL_DIV_RATIO.3	PLL_DIV_RATIO.2	PLL_DIV_RATIO.1	PLL_DIV_RATIO.0	01011010	5A
137	89	CP TLLC Control 3	rw				SWP_CR_CB_WB					00001000	08
138	8A	CP TLLC Control 4	rw	VCO_RANGE_MAN	VCO_RANGE.1	VCO_RANGE.0						00010000	10
143	8F	Free Run Line Length 1	w		LLC_PAD_SEL_MAN	LLC_PAD_SEL.1	LLC_PAD_SEL.0		FR_LL .10	FR_LL.9	FR_LL.8	00000000	00
144	90	Free Run Line Lengh 2	w	FR_LL.7	FR_LL.6	FR_LL.5	FR_LL.4	FR_LL.3	FR_LL.2	FR_LL.1	FR_LL.0	00000000	00
144	90	VBI Info	r					CGMSD				---	---
145	91	DPP_CP_64	w		INTERLACED							0101xxxx	50
150	96	CGMS 1	r	CGMS1.7	CGMS1.6	CGMS1.5	CGMS1.4	CGMS1.3	CGMS1.2	CGMS1.1	CGMS1.0	---	---
151	97	CGMS 2	r	CGMS2.7	CGMS2.6	CGMS2.5	CGMS2.4	CGMS2.3	CGMS2.2	CGMS2.1	CGMS2.0	---	---
152	98	CGMS 3	r	CGMS3.7	CGMS3.6	CGMS3.5	CGMS3.4	CGMS3.3	CGMS3.2	CGMS3.1	CGMS3.0	---	---
153	99	CCAP 1	r	CCAP1.7	CCAP1.6	CCAP1.5	CCAP1.4	CCAP1.3	CCAP1.2	CCAP1.1	CCAP1.0	---	---
154	9A	CCAP 2	r	CCAP2.7	CCAP2.6	CCAP2.5	CCAP2.4	CCAP2.3	CCAP2.2	CCAP2.1	CCAP2.0	---	---
155	9B	Letterbox 1	r	LB_LCT.7	LB_LCT.6	LB_LCT.5	LB_LCT.4	LB_LCT.3	LB_LCT.2	LB_LCT.1	LB_LCT.0	---	---
156	9C	Letterbox 2	r	LB_LCM.7	LB_LCM.6	LB_LCM.5	LB_LCM.4	LB_LCM.3	LB_LCM.2	LB_LCM.1	LB_LCM.0	---	---
157	9D	Letterbox 3	r	LB_LCB.7	LB_LCB.6	LB_LCB.5	LB_LCB.4	LB_LCB.3	LB_LCB.2	LB_LCB.1	LB_LCB.0	---	---
160	A0	RB CP AGC 1	r	0	0	0	0	0	0	CP_AGC_GAIN.9	CP_AGC_GAIN.8	---	---
161	A1	RB CP AGC 2	r	CP_AGC_GAIN.7	CP_AGC_GAIN.6	CP_AGC_GAIN.5	CP_AGC_GAIN.4	CP_AGC_GAIN.3	CP_AGC_GAIN.2	CP_AGC_GAIN.1	CP_AGC_GAIN.0	---	---
163	A3	RB CP Measure 2	r	0	0	0	CALIB.10	CALIB.9	CALIB.8	IFSD.8	ISD.8	---	---

Address Dec	Address Hex	Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex)
164	A4	RB CP Measure 3	r	ISD.7	ISD.6	ISD.5	ISD.4	ISD.3	ISD.2	ISD.1	ISD.0	---	---
165	A5	RB CP Measure 4	r	IFSD.7	IFSD.6	IFSD.5	IFSD.4	IFSD.3	IFSD.2	IFSD.1	IFSD.0	---	---
167	A7	RB CP HSync Depth 1	r	0	0	HSD_CHC.9	HSD_CHC.8	HSD_CHB.9	HSD_CHB.8	HSD_CHA.9	HSD_CHA.8	---	---
168	A8	RB CP HSync Depth 2	r	HSD_CHA.7	HSD_CHA.6	HSD_CHA.5	HSD_CHA.4	HSD_CHA.3	HSD_CHA.2	HSD_CHA.1	HSD_CHA.0	---	---
169	A9	RB CP HSync Depth 3	r	HSD_CHB.7	HSD_CHB.6	HSD_CHB.5	HSD_CHB.4	HSD_CHB.3	HSD_CHB.2	HSD_CHB.1	HSD_CHB.0	---	---
170	AA	RB CP HSync Depth 4	r	HSD_CHC.7	HSD_CHC.6	HSD_CHC.5	HSD_CHC.4	HSD_CHC.3	HSD_CHC.2	HSD_CHC.1	HSD_CHC.0	---	---
171	AB	RB CP HSync Depth 5	r	0	0	0	0	HSD_FB.11	HSD_FB.10	HSD_FB.9	HSD_FB.8	---	---
172	AC	RB CP HSync Depth 6	r	HSD_FB.7	HSD_FB.6	HSD_FB.5	HSD_FB.4	HSD_FB.3	HSD_FB.2	HSD_FB.1	HSD_FB.0	---	---
173	AD	RB CP Peak Video 1	r	0	0	PKV_CHA.9	PKV_CHA.8	PKV_CHB.9	PKV_CHB.8	PKV_CHC.9	PKV_CHC.8	---	---
174	AE	RB CP Peak Video 2	r	PKV_CHA.7	PKV_CHA.6	PKV_CHA.5	PKV_CHA.4	PKV_CHA.3	PKV_CHA.2	PKV_CHA.1	PKV_CHA.0	---	---
175	AF	RB CP Peak Video 3	r	PKV_CHB.7	PKV_CHB.6	PKV_CHB.5	PKV_CHB.4	PKV_CHB.3	PKV_CHB.2	PKV_CHB.1	PKV_CHB.0	---	---
176	B0	RB CP Peak Video 4	r	PKV_CHC.7	PKV_CHC.6	PKV_CHC.5	PKV_CHC.4	PKV_CHC.3	PKV_CHC.2	PKV_CHC.1	PKV_CHC.0	---	---
177	B1	RB Standard Ident 1	r	STDI_DVALID	STDI_INTLCD	BL.13	BL.12	BL.11	BL.10	BL.9	BL.8	---	---
178	B2	DPP_CP_97	w						CRC_ENABLE			00011100	1C
178	B2	RB Standard Ident 2	r	BL.7	BL.6	BL.5	BL.4	BL.3	BL.2	BL.1	BL.0	---	---
179	B3	DPP_CP_98	w						cp_f_run_th.2	cp_f_run_th.1	cp_f_run_th.0	01010100	54
179	B3	RB Standard Ident 3	r	SCVS.4	SCVS.3	SCVS.2	SCVS.1	SCVS.0	SCF.10	SCF.9	SCF.8	---	---
180	B4	RB Standard Ident 4	r	SCF.7	SCF.6	SCF.5	SCF.4	SCF.3	SCF.2	SCF.1	SCF.0	---	---
181	B5	RB Standard Ident 5	r	SSPD_DVALID	VS_ACT	CUR_POL_VS	HS_ACT	CUR_POL_HS		CUR_SYNC_SRC.1	CUR_SYNC_SRC.0	---	---
191	BF	CP DEF COL 1	rw						CP_DEF_COL_MAN_VAL	CP_DEF_COL_AUTO	CP_DEF_COL_FORCE	xxxxx010	02
192	C0	CP DEF COL 2	rw	DEF_COL_CHA.7	DEF_COL_CHA.6	DEF_COL_CHA.5	DEF_COL_CHA.4	DEF_COL_CHA.3	DEF_COL_CHA.2	DEF_COL_CHA.1	DEF_COL_CHA.0	xxxxxxxx	00
193	C1	CP DEF COL 3	rw	DEF_COL_CHB.7	DEF_COL_CHB.6	DEF_COL_CHB.5	DEF_COL_CHB.4	DEF_COL_CHB.3	DEF_COL_CHB.2	DEF_COL_CHB.1	DEF_COL_CHB.0	xxxxxxxx	00
194	C2	CP DEF COL 4	rw	DEF_COL_CHC.7	DEF_COL_CHC.6	DEF_COL_CHC.5	DEF_COL_CHC.4	DEF_COL_CHC.3	DEF_COL_CHC.2	DEF_COL_CHC.1	DEF_COL_CHC.0	xxxxxxxx	00
195	C3	ADC Switch 1	rw	ADC1_SW.3	ADC1_SW.2	ADC1_SW.1	ADC1_SW.0	ADC0_SW.3	ADC0_SW.2	ADC0_SW.1	ADC0_SW.0	xxxxxxxx	00
196	C4	ADC Switch 2	rw	ADC_SW_MAN	SOG_SEL			ADC2_SW.3	ADC2_SW.2	ADC2_SW.1	ADC2_SW.0	0xxxxxxx	00
197	C5	CP Clamp Pos HS Ctrl 1	rw	CP_CLAMP_AVG_FCTR.1	CP_CLAMP_AVG_FCTR.0							10xxx001	81
201	C9	DPP_CP_118	rw					DDR_EN	DDR_I2C_RC_FIRST	DDS_DIN_CLK_EN	DPP_CP_BYPASS	00000100	04
202	CA	Field Length Count 1	r				FCL.12	FCL.11	FCL.10	FCL.9	FCL.8	---	---
203	CB	Field Length Count 2	r	FCL.7	FCL.6	FCL.5	FCL.4	FCL.3	FCL.2	FCL.1	FCL.0	---	---
220	DC	Letterbox Control 1	rw				LB_TH.4	LB_TH.3	LB_TH.2	LB_TH.1	LB_TH.0	10101100	AC
221	DD	Letterbox Control 2	rw	LB_SL.3	LB_SL.2	LB_SL.1	LB_SL.0	LB_EL.3	LB_EL.2	LB_EL.1	LB_EL.0	01001100	4C
222	DE	ST Noise Readback 1	r					ST_NOISE_VLD	ST_NOISE.10	ST_NOISE.9	ST_NOISE.8	---	---
223	DF	ST Noise Readback 2	r	ST_NOISE.7	ST_NOISE.6	ST_NOISE.5	ST_NOISE.4	ST_NOISE.3	ST_NOISE.2	ST_NOISE.1	ST_NOISE.0	---	---
225	E1	SD Offset U	rw	SD_OFF_U.7	SD_OFF_U.6	SD_OFF_U.5	SD_OFF_U.4	SD_OFF_U.3	SD_OFF_U.2	SD_OFF_U.1	SD_OFF_U.0	10000000	80
226	E2	SD Offset V	rw	SD_OFF_V.7	SD_OFF_V.6	SD_OFF_V.5	SD_OFF_V.4	SD_OFF_V.3	SD_OFF_V.2	SD_OFF_V.1	SD_OFF_V.0	10000000	80
227	E3	SD Saturation U	rw	SD_SAT_U.7	SD_SAT_U.6	SD_SAT_U.5	SD_SAT_U.4	SD_SAT_U.3	SD_SAT_U.2	SD_SAT_U.1	SD_SAT_U.0	10000000	80
228	E4	SD Saturation V	rw	SD_SAT_V.7	SD_SAT_V.6	SD_SAT_V.5	SD_SAT_V.4	SD_SAT_V.3	SD_SAT_V.2	SD_SAT_V.1	SD_SAT_V.0	10000000	80
229	E5	NTSC V bit begin	rw	NVBEGDELO	NVBEGDELE	NVBEGSIGN	NVBEG.4	NVBEG.3	NVBEG.2	NVBEG.1	NVBEG.0	00100101	25
230	E6	NTSC V bit end	rw	NVENDDELO	NVENDDELE	NVENDSIGN	NVEND.4	NVEND.3	NVEND.2	NVEND.1	NVEND.0	00000100	04

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex)
Dec	Hex												
231	E7	NTSC F bit toggle	rw	NFTOGDELO	NFTOGDELE	NFTOGSIGN	NFTOG.4	NFTOG.3	NFTOG.2	NFTOG.1	NFTOG.0	01100011	63
232	E8	PAL V bit begin	rw	PVBEGDELO	PVBEGDELE	PVBEGSIGN	PVBEG.4	PVBEG.3	PVBEG.2	PVBEG.1	PVBEG.0	01100101	65
233	E9	PAL V bit end	rw	PVENDDELO	PVENDDELE	PVENDSIGN	PVEND.4	PVEND.3	PVEND.2	PVEND.1	PVEND.0	00010100	14
234	EA	PAL F bit toggle	rw	PFTOGDELO	PFTOGDELE	PFTOGSIGN	PFTOG.4	PFTOG.3	PFTOG.2	PFTOG.1	PFTOG.0	01100011	63
235	EB	Vblank Control 1	rw	NVBIOLCM.1	NVBIOLCM.0	NVBIELCM.1	NVBIELCM.0	PVBIOLCM.1	PVBIOLCM.0	PVBIELCM.1	PVBIELCM.0	01010101	55
236	EC	Vblank Control 2	rw	NVBIOCCM.1	NVBIOCCM.0	NVBIECCM.1	NVBIECCM.0	PVBIOCCM.1	PVBIOCCM.0	PVBIECCM.1	PVBIECCM.0	01010101	55
237	ED	FB_STATUS	r	FB_STATUS.3	FB_STATUS.2	FB_STATUS.1	FB_STATUS.0					---	---
237	ED	FB_CONTROL1	w					FB_INV	CVBS_RGB_SEL	FB_MODE.1	FB_MODE.0	00010000	10
238	EE	FB_CONTROL 2	rw	FB_CSC_MAN	MAN_ALPHA_VAL.6	MAN_ALPHA_VAL.5	MAN_ALPHA_VAL.4	MAN_ALPHA_VAL.3	MAN_ALPHA_VAL.2	MAN_ALPHA_VAL.1	MAN_ALPHA_VAL.0	00000000	00
239	EF	FB_CONTROL 3	rw	FB_SP_ADJUST.3	FB_SP_ADJUST.2	FB_SP_ADJUST.1	FB_SP_ADJUST.0	CNTR_ENABLE	FB_EDGE_SHAPE..2	FB_EDGE_SHAPE.1	FB_EDGE_SHAPE.0	01001010	4A
240	F0	FB_CONTROL 4	rw					FB_DELAY.3	FB_DELAY.2	FB_DELAY.1	FB_DELAY.0	01000100	44
241	F1	FB_CONTROL 5	rw	CNTR_LEVEL.1	CNTR_LEVEL.0	FB_LEVEL.1	FB_LEVEL.0	CNTR_MODE.1	CNTR_MODE.0		RGB_IP_SEL	00001100	0C
243	F3	AFE_CONTROL 1	rw	ADC3_SW.3	ADC3_SW.2	ADC3_SW.1	ADC3_SW.0	AA_FILT_EN.3	AA_FILT_EN.2	AA_FILT_EN.1	AA_FILT_EN.0	00000000	00
244	F4	Drive Strength	rw			DR_STR	DR_STR.0	DR_STR_C	DR_STR_C.0	DR_STR_S	DR_STR_S.0	xx010101	15
248	F8	IF Comp Control	rw						IFFILTSEL.2	IFFILTSEL.1	IFFILTSEL.0	00000000	00
249	F9	VS Mode Control	rw					VS_COAST_MODE.1	VS_COAST_MODE.0	EXTEND_VS_MIN_FREQ	EXTEND_VS_MAX_FREQ	00000000	00
251	FB	Peaking Control	rw	PEAKING_GAIN.7	PEAKING_GAIN.6	PEAKING_GAIN.5	PEAKING_GAIN.4	PEAKING_GAIN.3	PEAKING_GAIN.2	PEAKING_GAIN.1	PEAKING_GAIN.0	01000000	40
252	FC	Coring Threshold 2	rw	DNR_TH_2.7	DNR_TH_2.6	DNR_TH_2.5	DNR_TH_2.4	DNR_TH_2.3	DNR_TH_2.2	DNR_TH_2.1	DNR_TH_2.0	00000100	04

Table 60: User Map 1

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex)
Dec	Hex												
64	40	Interrupt Configuration 0	rw	INTRQ_DUR_SEL.1	INTRQ_DUR_SEL.0	MV_INTRQ_SEL.1	MV_INTRQ_SEL.0		MPU_STIM_INTRQ	INTRQ_OP_SEL.1	INTRQ_OP_SEL.0	0001x000	10
66	42	Interrupt Status 1	r		MV_PS_CS_Q	SD_FR_CHNG_Q	STDI_DVALID_Q	CP_UNLOCK_Q	CP_LOCK_Q	SD_UNLOCK_Q	SD_LOCK_Q	---	---
67	43	Interrupt Clear 1	w		MV_PS_CS_CLR	SD_FR_CHNG_CLR	STDI_DVALID_CLR	CP_UNLOCK_CLR	CP_LOCK_CLR	SD_UNLOCK_CLR	SD_LOCK_CLR	x0000000	00
68	44	Interrupt Maskb 1	rw		MV_PS_CS_MSKB	SD_FR_CHNG_MSKB	STDI_DVALID_MSKB	CP_UNLOCK_MSKB	CP_LOCK_MSKB	SD_UNLOCK_MSKB	SD_LOCK_MSKB	x0000000	00
69	45	Raw Status 2	r	MPU_STIM_INTRQ			EVEN_FIELD				CCAPD	---	---
70	46	Interrupt Status 2	r	MPU_STIM_INTRQ_Q			SD_FIELD_CHNGD_Q	WSS_CHNGD_Q	CGMS_CHNGD_Q	GEMD_Q	CCAPD_Q	---	---
71	47	Interrupt Clear 2	w	MPU_STIM_INTRQ_CLR			SD_FIELD_CHNGD_CLR	WSS_CHNGD_CLR	CGMS_CHNGD_CLR	GEMD_CLR	CCAPD_CLR	0xx00000	00
72	48	Interrupt Maskb 2	rw	MPU_STIM_INTRQ_MSKB			SD_FIELD_CHNGD_MSKB	WSS_CHNGD_MSKB	CGMS_CHNGD_MSKB	GEMD_MSKB	CCAPD_MSKB	0xx00000	00
73	49	Raw Status 3	r				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_50Hz	---	---
74	4A	Interrupt Status 3	r			PAL_SW_LK_CHNG_Q	SCM_LOCK_CHNG_Q	SD_AD_CHNG_Q	SD_H_LOCK_CHNG_Q	SD_V_LOCK_CHNG_Q	SD_OP_CHNG_Q	---	---
75	4B	Interrupt Clear 3	w			PAL_SW_LK_CHNG_CLR	SCM_LOCK_CHNG_CLR	SD_AD_CHNG_CLR	SD_H_LOCK_CHNG_CLR	SD_V_LOCK_CHNG_CLR	SD_OP_CHNG_CLR	xx000000	00
76	4C	Interrupt Maskb 3	rw			PAL_SW_LK_CHNG_MSKB	SCM_LOCK_CHNG_MSKB	SD_AD_CHNG_MSKB	SD_H_LOCK_CHNG_MSKB	SD_V_LOCK_CHNG_MSKB	SD_OP_CHNG_MSKB	xx000000	00
78	4E	Interrupt Status 4	r		VDP_VITC_Q		VDP_GS_VPS_PDC_UTC_CHNG_Q		VDP_CGMS_WSS_CHNGD_Q		VDP_CCAPD_Q	---	---
79	4F	Interrupt Clear 4	w		VDP_VITC_CLR		VDP_GS_VPS_PDC_UTC_CHNG_CLR		VDP_CGMS_WSS_CHNGD_CLR		VDP_CCAPD_CLR	00x0x0x0	00
80	50	Interrupt Maskb 4	rw		VDP_VITC_MSKB		VDP_GS_VPS_PDC_UTC_CHNG_MSKB		VDP_CGMS_WSS_CHNGD_MSKB		VDP_CCAPD_MSKB	00x0x0x0	00
96	60	VDP_Config_1	rw						Vdp_ttxt_type_man_enable	Vdp_ttxt_type_man.1	Vdp_ttxt_type_man.0	10001000	88
97	61	VDP_Config_2	rw				AUTO_DETECT_GS_TYPE					0001xx00	10
98	62	VDP_ADF_Config_1	rw	ADF_ENABLE	ADF_MODE.1	ADF_MODE.0	ADF_DID.4	ADF_DID.3	ADF_DID.2	ADF_DID.1	ADF_DID.0	00010101	15
99	63	VDP_ADF_Config_2	rw	DUPLICATE ADF		ADF_SDID.5	ADF_SDID.4	ADF_SDID.3	ADF_SDID.2	ADF_SDID.1	ADF_SDID.0	0x101010	2A
100	64	VDP_Line_00E	rw	MAN_LINE_PGM				Vbi_data_p318.3	Vbi_data_p318.2	Vbi_data_p318.1	Vbi_data_p318.0	0xxx0000	00
101	65	VDP_Line_00F	rw	Vbi_data_p6_n23.3	Vbi_data_p6_n23.2	Vbi_data_p6_n23.1	Vbi_data_p6_n23.0	Vbi_data_p319_n286.3	Vbi_data_p319_n286.2	Vbi_data_p319_n286.1	Vbi_data_p319_n286.0	00000000	00
102	66	VDP_Line_010	rw	Vbi_data_p7_n24.3	Vbi_data_p7_n24.2	Vbi_data_p7_n24.1	Vbi_data_p7_n24.0	Vbi_data_p320_n287.3	Vbi_data_p320_n287.2	Vbi_data_p320_n287.1	Vbi_data_p320_n287.0	00000000	00
103	67	VDP_Line_011	rw	Vbi_data_p8_n25.3	Vbi_data_p8_n25.2	Vbi_data_p8_n25.1	Vbi_data_p8_n25.0	Vbi_data_p321_n288.3	Vbi_data_p321_n288.2	Vbi_data_p321_n288.1	Vbi_data_p321_n288.0	00000000	00
104	68	VDP_Line_012	rw	Vbi_data_p9.3	Vbi_data_p9.2	Vbi_data_p9.1	Vbi_data_p9.0	Vbi_data_p322.3	Vbi_data_p322.2	Vbi_data_p322.1	Vbi_data_p322.0	00000000	00
105	69	VDP_Line_013	rw	Vbi_data_p10.3	Vbi_data_p10.2	Vbi_data_p10.1	Vbi_data_p10.0	Vbi_data_p323.3	Vbi_data_p323.2	Vbi_data_p323.1	Vbi_data_p323.0	00000000	00
106	6A	VDP_Line_014	rw	Vbi_data_p11.3	Vbi_data_p11.2	Vbi_data_p11.1	Vbi_data_p11.0	Vbi_data_p324_n272.3	Vbi_data_p324_n272.2	Vbi_data_p324_n272.1	Vbi_data_p324_n272.0	00000000	00
107	6B	VDP_Line_015	rw	Vbi_data_p12_n10.3	Vbi_data_p12_n10.2	Vbi_data_p12_n10.1	Vbi_data_p12_n10.0	Vbi_data_p325_n273.3	Vbi_data_p325_n273.2	Vbi_data_p325_n273.1	Vbi_data_p325_n273.0	00000000	00
108	6C	VDP_Line_016	rw	Vbi_data_p13_n11.3	Vbi_data_p13_n11.2	Vbi_data_p13_n11.1	Vbi_data_p13_n11.0	Vbi_data_p326_n274.3	Vbi_data_p326_n274.2	Vbi_data_p326_n274.1	Vbi_data_p326_n274.0	00000000	00
109	6D	VDP_Line_017	rw	Vbi_data_p14_n12.3	Vbi_data_p14_n12.2	Vbi_data_p14_n12.1	Vbi_data_p14_n12.0	Vbi_data_p327_n275.3	Vbi_data_p327_n275.2	Vbi_data_p327_n275.1	Vbi_data_p327_n275.0	00000000	00
110	6E	VDP_Line_018	rw	Vbi_data_p15_n13.3	Vbi_data_p15_n13.2	Vbi_data_p15_n13.1	Vbi_data_p15_n13.0	Vbi_data_p328_n276.3	Vbi_data_p328_n276.2	Vbi_data_p328_n276.1	Vbi_data_p328_n276.0	00000000	00
111	6F	VDP_Line_019	rw	Vbi_data_p16_n14.3	Vbi_data_p16_n14.2	Vbi_data_p16_n14.1	Vbi_data_p16_n14.0	Vbi_data_p329_n277.3	Vbi_data_p329_n277.2	Vbi_data_p329_n277.1	Vbi_data_p329_n277.0	00000000	00
112	70	VDP_Line_01A	rw	Vbi_data_p17_n15.3	Vbi_data_p17_n15.2	Vbi_data_p17_n15.1	Vbi_data_p17_n15.0	Vbi_data_p330_n278.3	Vbi_data_p330_n278.2	Vbi_data_p330_n278.1	Vbi_data_p330_n278.0	00000000	00
113	71	VDP_Line_01B	rw	Vbi_data_p18_n16.3	Vbi_data_p18_n16.2	Vbi_data_p18_n16.1	Vbi_data_p18_n16.0	Vbi_data_p331_n279.3	Vbi_data_p331_n279.2	Vbi_data_p331_n279.1	Vbi_data_p331_n279.0	00000000	00

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex) Dec
Dec	Hex												
114	72	VDP_Line_01C	rw	Vbi_data_p19_n17.3	Vbi_data_p19_n17.2	Vbi_data_p19_n17.1	Vbi_data_p19_n17.0	Vbi_data_p332_n280.3	Vbi_data_p332_n280.2	Vbi_data_p332_n280.1	Vbi_data_p332_n280.0	00000000	00
115	73	VDP_Line_01D	rw	Vbi_data_p20_n18.3	Vbi_data_p20_n18.2	Vbi_data_p20_n18.1	Vbi_data_p20_n18.0	Vbi_data_p333_n281.3	Vbi_data_p333_n281.2	Vbi_data_p333_n281.1	Vbi_data_p333_n281.0	00000000	00
116	74	VDP_Line_01E	rw	Vbi_data_p21_n19.3	Vbi_data_p21_n19.2	Vbi_data_p21_n19.1	Vbi_data_p21_n19.0	Vbi_data_p334_n282.3	Vbi_data_p334_n282.2	Vbi_data_p334_n282.1	Vbi_data_p334_n282.0	00000000	00
117	75	VDP_Line_01F	rw	Vbi_data_p22_n20.3	Vbi_data_p22_n20.2	Vbi_data_p22_n20.1	Vbi_data_p22_n20.0	Vbi_data_p335_n283.3	Vbi_data_p335_n283.2	Vbi_data_p335_n283.1	Vbi_data_p335_n283.0	00000000	00
118	76	VDP_Line_020	rw	Vbi_data_p23_n21.3	Vbi_data_p23_n21.2	Vbi_data_p23_n21.1	Vbi_data_p23_n21.0	Vbi_data_p336_n284.3	Vbi_data_p336_n284.2	Vbi_data_p336_n284.1	Vbi_data_p336_n284.0	00000000	00
119	77	VDP_Line_021	rw	Vbi_data_p24_n22.3	Vbi_data_p24_n22.2	Vbi_data_p24_n22.1	Vbi_data_p24_n22.0	Vbi_data_p337_n285.3	Vbi_data_p337_n285.2	Vbi_data_p337_n285.1	Vbi_data_p337_n285.0	00000000	00
120	78	VDP_Status	rw	TTXT_AVL	VITC_AVL	GS_DATA_TYPE	GS_PDC_VPS_UTC_AVL		CGMS_WSS_AVL	CC_EVEN_FIELD	CC_AVL	00000000	00
121	79	VDP_CCAP_DATA_0	r	CCAP_BYTE_1.7	CCAP_BYTE_1.6	CCAP_BYTE_1.5	CCAP_BYTE_1.4	CCAP_BYTE_1.3	CCAP_BYTE_1.2	CCAP_BYTE_1.1	CCAP_BYTE_1.0	---	---
122	7A	VDP_CCAP_DATA_1	r	CCAP_BYTE_2.7	CCAP_BYTE_2.6	CCAP_BYTE_2.5	CCAP_BYTE_2.4	CCAP_BYTE_2.3	CCAP_BYTE_2.2	CCAP_BYTE_2.1	CCAP_BYTE_2.0	---	---
125	7D	CGMS_WSS_DATA_0	r	zero	zero	zero	zero	CGMS_CRC.5	CGMS_CRC.4	CGMS_CRC.3	CGMS_CRC.2	---	---
126	7E	CGMS_WSS_DATA_1	r	CGMS_CRC.1	CGMS_CRC.0	CGMS_WSS.13	CGMS_WSS.12	CGMS_WSS.11	CGMS_WSS.10	CGMS_WSS.9	CGMS_WSS.8	---	---
127	7F	CGMS_WSS_DATA_2	r	CGMS_WSS.7	CGMS_WSS.6	CGMS_WSS.5	CGMS_WSS.4	CGMS_WSS.3	CGMS_WSS.2	CGMS_WSS.1	CGMS_WSS.0	---	---
132	84	VDP_GS_VPS_PDC_UTC_0	r	GS_VPS_PDC_UTC_BYTE_0.7	GS_VPS_PDC_UTC_BYTE_0.6	GS_VPS_PDC_UTC_BYTE_0.5	GS_VPS_PDC_UTC_BYTE_0.4	GS_VPS_PDC_UTC_BYTE_0.3	GS_VPS_PDC_UTC_BYTE_0.2	GS_VPS_PDC_UTC_BYTE_0.1	GS_VPS_PDC_UTC_BYTE_0.0	---	---
133	85	VDP_GS_VPS_PDC_UTC_1	r	GS_VPS_PDC_UTC_BYTE_1.7	GS_VPS_PDC_UTC_BYTE_1.6	GS_VPS_PDC_UTC_BYTE_1.5	GS_VPS_PDC_UTC_BYTE_1.4	GS_VPS_PDC_UTC_BYTE_1.3	GS_VPS_PDC_UTC_BYTE_1.2	GS_VPS_PDC_UTC_BYTE_1.1	GS_VPS_PDC_UTC_BYTE_1.0	---	---
134	86	VDP_GS_VPS_PDC_UTC_2	r	GS_VPS_PDC_UTC_BYTE_2.7	GS_VPS_PDC_UTC_BYTE_2.6	GS_VPS_PDC_UTC_BYTE_2.5	GS_VPS_PDC_UTC_BYTE_2.4	GS_VPS_PDC_UTC_BYTE_2.3	GS_VPS_PDC_UTC_BYTE_2.2	GS_VPS_PDC_UTC_BYTE_2.1	GS_VPS_PDC_UTC_BYTE_2.0	---	---
135	87	VDP_GS_VPS_PDC_UTC_3	r	GS_VPS_PDC_UTC_BYTE_3.7	GS_VPS_PDC_UTC_BYTE_3.6	GS_VPS_PDC_UTC_BYTE_3.5	GS_VPS_PDC_UTC_BYTE_3.4	GS_VPS_PDC_UTC_BYTE_3.3	GS_VPS_PDC_UTC_BYTE_3.2	GS_VPS_PDC_UTC_BYTE_3.1	GS_VPS_PDC_UTC_BYTE_3.0	---	---
136	88	VDP_VPS_PDC_UTC_4	r	VPS_PDC_UTC_BYTE_4.7	VPS_PDC_UTC_BYTE_4.6	VPS_PDC_UTC_BYTE_4.5	VPS_PDC_UTC_BYTE_4.4	VPS_PDC_UTC_BYTE_4.3	VPS_PDC_UTC_BYTE_4.2	VPS_PDC_UTC_BYTE_4.1	VPS_PDC_UTC_BYTE_4.0	---	---
137	89	VDP_VPS_PDC_UTC_5	r	VPS_PDC_UTC_BYTE_5.7	VPS_PDC_UTC_BYTE_5.6	VPS_PDC_UTC_BYTE_5.5	VPS_PDC_UTC_BYTE_5.4	VPS_PDC_UTC_BYTE_5.3	VPS_PDC_UTC_BYTE_5.2	VPS_PDC_UTC_BYTE_5.1	VPS_PDC_UTC_BYTE_5.0	---	---
138	8A	VDP_VPS_PDC_UTC_6	r	VPS_PDC_UTC_BYTE_6.7	VPS_PDC_UTC_BYTE_6.6	VPS_PDC_UTC_BYTE_6.5	VPS_PDC_UTC_BYTE_6.4	VPS_PDC_UTC_BYTE_6.3	VPS_PDC_UTC_BYTE_6.2	VPS_PDC_UTC_BYTE_6.1	VPS_PDC_UTC_BYTE_6.0	---	---
139	8B	VDP_VPS_PDC_UTC_7	r	VPS_PDC_UTC_BYTE_7.7	VPS_PDC_UTC_BYTE_7.6	VPS_PDC_UTC_BYTE_7.5	VPS_PDC_UTC_BYTE_7.4	VPS_PDC_UTC_BYTE_7.3	VPS_PDC_UTC_BYTE_7.2	VPS_PDC_UTC_BYTE_7.1	VPS_PDC_UTC_BYTE_7.0	---	---
140	8C	VDP_VPS_PDC_UTC_8	r	VPS_PDC_UTC_BYTE_8.7	VPS_PDC_UTC_BYTE_8.6	VPS_PDC_UTC_BYTE_8.5	VPS_PDC_UTC_BYTE_8.4	VPS_PDC_UTC_BYTE_8.3	VPS_PDC_UTC_BYTE_8.2	VPS_PDC_UTC_BYTE_8.1	VPS_PDC_UTC_BYTE_8.0	---	---
141	8D	VDP_VPS_PDC_UTC_9	r	VPS_PDC_UTC_BYTE_9.7	VPS_PDC_UTC_BYTE_9.6	VPS_PDC_UTC_BYTE_9.5	VPS_PDC_UTC_BYTE_9.4	VPS_PDC_UTC_BYTE_9.3	VPS_PDC_UTC_BYTE_9.2	VPS_PDC_UTC_BYTE_9.1	VPS_PDC_UTC_BYTE_9.0	---	---
142	8E	VDP_VPS_PDC_UTC_10	r	VPS_PDC_UTC_BYTE_10.7	VPS_PDC_UTC_BYTE_10.6	VPS_PDC_UTC_BYTE_10.5	VPS_PDC_UTC_BYTE_10.4	VPS_PDC_UTC_BYTE_10.3	VPS_PDC_UTC_BYTE_10.2	VPS_PDC_UTC_BYTE_10.1	VPS_PDC_UTC_BYTE_10.0	---	---
143	8F	VDP_VPS_PDC_UTC_11	r	VPS_PDC_UTC_BYTE_11.7	VPS_PDC_UTC_BYTE_11.6	VPS_PDC_UTC_BYTE_11.5	VPS_PDC_UTC_BYTE_11.4	VPS_PDC_UTC_BYTE_11.3	VPS_PDC_UTC_BYTE_11.2	VPS_PDC_UTC_BYTE_11.1	VPS_PDC_UTC_BYTE_11.0	---	---
144	90	VDP_VPS_PDC_UTC_12	r	VPS_PDC_UTC_BYTE_12.7	VPS_PDC_UTC_BYTE_12.6	VPS_PDC_UTC_BYTE_12.5	VPS_PDC_UTC_BYTE_12.4	VPS_PDC_UTC_BYTE_12.3	VPS_PDC_UTC_BYTE_12.2	VPS_PDC_UTC_BYTE_12.1	VPS_PDC_UTC_BYTE_12.0	---	---
146	92	VDP_VITC_DATA_0	r	VITC_DATA_1.7	VITC_DATA_1.6	VITC_DATA_1.5	VITC_DATA_1.4	VITC_DATA_1.3	VITC_DATA_1.2	VITC_DATA_1.1	VITC_DATA_1.0	---	---
147	93	VDP_VITC_DATA_1	r	VITC_DATA_2.7	VITC_DATA_2.6	VITC_DATA_2.5	VITC_DATA_2.4	VITC_DATA_2.3	VITC_DATA_2.2	VITC_DATA_2.1	VITC_DATA_2.0	---	---
148	94	VDP_VITC_DATA_2	r	VITC_DATA_3.7	VITC_DATA_3.6	VITC_DATA_3.5	VITC_DATA_3.4	VITC_DATA_3.3	VITC_DATA_3.2	VITC_DATA_3.1	VITC_DATA_3.0	---	---
149	95	VDP_VITC_DATA_3	r	VITC_DATA_4.7	VITC_DATA_4.6	VITC_DATA_4.5	VITC_DATA_4.4	VITC_DATA_4.3	VITC_DATA_4.2	VITC_DATA_4.1	VITC_DATA_4.0	---	---
150	96	VDP_VITC_DATA_4	r	VITC_DATA_5.7	VITC_DATA_5.6	VITC_DATA_5.5	VITC_DATA_5.4	VITC_DATA_5.3	VITC_DATA_5.2	VITC_DATA_5.1	VITC_DATA_5.0	---	---
151	97	VDP_VITC_DATA_5	r	VITC_DATA_6.7	VITC_DATA_6.6	VITC_DATA_6.5	VITC_DATA_6.4	VITC_DATA_6.3	VITC_DATA_6.2	VITC_DATA_6.1	VITC_DATA_6.0	---	---
152	98	VDP_VITC_DATA_6	r	VITC_DATA_7.7	VITC_DATA_7.6	VITC_DATA_7.5	VITC_DATA_7.4	VITC_DATA_7.3	VITC_DATA_7.2	VITC_DATA_7.1	VITC_DATA_7.0	---	---
153	99	VDP_VITC_DATA_7	r	VITC_DATA_8.7	VITC_DATA_8.6	VITC_DATA_8.5	VITC_DATA_8.4	VITC_DATA_8.3	VITC_DATA_8.2	VITC_DATA_8.1	VITC_DATA_8.0	---	---

Address		Register Name	rw	7	6	5	4	3	2	1	0	Reset Value (binary)	(Hex) Dec
Dec	Hex												
154	9A	VDP_VITC_ DATA_8	r	VITC_DATA_ 9.7	VITC_DATA_ 9.6	VITC_DATA_ 9.5	VITC_DATA_ 9.4	VITC_DATA_ 9.3	VITC_DATA_ 9.2	VITC_DATA_ 9.1	VITC_DATA_ 9.0	---	---
155	9B	VDP_VITC_ CALC_CRC	r	VITC_CRC.7	VITC_CRC.6	VITC_CRC.5	VITC_CRC.4	VITC_CRC.3	VITC_CRC.2	VITC_CRC.1	VITC_CRC.0	---	---
156	9C	VDP_OUTP UT_SEL	rw	I2C_GS_VPS _PDC_UTC.1	I2C_GS_VP S_PDC_UTC .0	GS_VPS_PD C_UTC_CB_ CHANGE	WSS_CGMS _CB_CHAN GE					00110000	30

To access the User Sub Map in Table 60, the SUB_USR_EN bit in *Address 0x0E* must be programmed to 1b.

11.5 I²C Register Map Details (User Map)

Grayed out sections in the following tables mark the reset value of the register.

Table 61: Register 0x00

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x00	Input Control	**INSEL [3:0]** The INSEL bits allow the user to select an input channel as well as the input format					0	0	0	0	CVBS in on AIN1	Composite
							0	0	0	1	CVBS in on AIN2	
							0	0	1	1	CVBS in on AIN4	
							0	1	0	0	CVBS in on AIN5	
							0	1	0	1	CVBS in on AIN6	
							0	1	1	0	Y on AIN1, C on AIN4	S-Video
							0	1	1	1	Y on AIN2, C on AIN5	
							1	0	0	1	Y on AIN1, Pr on AIN4, Pb on AIN5	YPbPr
							1	1	1	0	CVBS in on AIN3	Composite
		VID_SEL [3:0] The VID_SEL bits allow the user to select the input video standard	0	0	0	0					Auto detect PAL (BGHID), NTSC (without pedestal)	
			0	0	0	1					Auto detect PAL (BGHID), NTSC (M) (with pedestal)	
			0	0	1	0					Auto detect PAL (N), NTSC (M) (without pedestal)	
			0	0	1	1					Auto detect PAL (N), NTSC (M) (with pedestal)	
			0	1	0	0					NTSC (J)	
			0	1	0	1					NTSC (M)	
			0	1	1	0					PAL 60	
			0	1	1	1					NTSC 4.43	
			1	0	0	0					PAL BGHID	
			1	0	0	1					PAL N (BGHID without pedestal)	
			1	0	1	0					PAL M (without pedestal)	
			1	0	1	1					PAL M	
			1	1	0	0					PAL combination N	
			1	1	0	1					PAL combination N (with Pedestal)	
			1	1	1	0					SECAM	
			1	1	1	1					SECAM (with pedestal)	

Table 62: Register 0x01 to 0x03

Subaddress	Register	Bit Desciption	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x01	Video selection	Reserved						0	0	0	Set to Default	
		ENVSPROC					0				Disable VSync Processor	
							1				Enable VSync Processor	
		Reserved				0					Set to Default	
		BETACAM			0						Standard video input	
					1						Betacam input enable	
		ENHSPLL		0							Disable HSync PLL	
				1							Enable HSync PLL	
		Reserved										
			1								Set to Default	
0x02	Reserved	Reserved										
0x03	Output Control	**SD_DUP_AV** duplicate the AV codes from the Luma into the chroma path								0	AV codes to suit 8-bit interleaved data output	
										1	AV codes duplicated (for 16-bit interfaces)	
		Reserved							0		Set as default	
		OF_SEL [3:0] Allows the user to choose from a set of output formats.			0	0	0	0			10-bit @ LLC1 4:2:2 ITU-R BT.656	
					0	0	0	1			20-bit @ LLC2 4:2:2	
					0	0	1	0			16-bit @ LLC2 4:2:2	
					0	0	1	1			8-bit@LLC1 4:2:2 ITU-R BT.656	
					0	1	0	0			Not Used	
					0	1	0	1			Not Used	
					0	1	1	0			Not Used	
					0	1	1	1			Not Used	
					1	0	0	0			Not Used	
					1	0	0	1			Not Used	
					1	0	1	0			Not Used	
					1	0	1	1			Not Used	
					1	1	0	0			Not Used	
					1	1	0	1			Not Used	
					1	1	1	0			Not Used	
					1	1	1	1			Not Used	
		TOD Tri-State Output Drivers. This bit allows the user to tri-state the output drivers: P[19:12], P[9:2], HS, VS, FIELD, SFL.		0							Output pins enabled	See also TIM_OE; TRI_LLC
				1							Drivers tri-stated.	
		VBI_EN Allows VBI data (lines 1 to 21) to be passed through with only a mininum amount of filtering performed.	0								All lines filtered and scaled	
			1								Only active video region filtered	

Table 63: Register 0x04

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x04	Extended Output Control	**RANGE** Allows the user to select the range of output values. Can be BT656 compliant or fill the whole accessible number range.								0	16<Y<235,16<C<240	ITU-R BT.656
										1	1<Y<254,1<C<254	Extended Range
		EN_SFL_PIN							0		SFL output is disabled	SFL output enables
									1		SFL information output on the SFL pin	
		BL_C_VBI Blank Chroma During VBI. If set will enable data in the VBI region to be passed through the decoder undistorted						0			Decode and Output colour	During VBI
								1			Blank Cr and Cb	
		TIM_OE Timing Signals Output Enable					0				HS,VS,F tri-stated	Controlled by TOD
							1				HS,VS,F forced active	
		Reserved			x	x					Set to default	
		Reserved		1							Set to default	
		BT656-4 Allows the user to select an output mode that is compatible with ITU-R BT656-3/4	0								BT656-3 compatible	
			1								BT656-4 compatible	

Table 64: Register 0x05

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Processor	Comment
0x05	Primary Mode	**PRIM_MODE[3:0]** Selects the primary mode of operation of the decoder. Used with **VID_STD[3:0]**					0	0	0	0	Standard Definition	SDP	CVBS,Y/C,YPbPr
							0	0	0	1	Component Video (YPbPr/RGB)	CP	SD,HD and PR
							0	0	1	0	RGB Graphics mode		VGA to XGA
							0	0	1	1	Reserved		
							0	1	0	0	Reserved		
							0	1	0	1	Reserved		
							0	1	1	0	Reserved		
							0	1	1	1	Reserved		
							1	0	0	0	Reserved		
							1	0	0	1	Reserved		
							1	0	1	0	Reserved		
							1	0	1	1	Reserved		
							1	1	0	0	Reserved		
							1	1	0	1	Reserved		
							1	1	1	0	Reserved		
							1	1	1	1	Reserved		
		Reserved	0	0	0	0					Set to Default		

Table 65: Register 0x06

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Processor	Comment
0x06	Video Standard	**VID_STD[3:0]** Sets the input and output Video standards dependant on **PRIM_MODE[2:0]**					0	0	0	0	Reserved		PRIM_MODE= 0000 (SD-M)
							0	0	1	0	SD 4X1 (54MHz sampling)	SDP	
							0	1	0	1	Reserved		
							0	1	1	0	Reserved		
							0	1	1	1	Reserved		
							1	0	1	0	525i 4X1 (720x480)	CP	
							1	0	1	1	625i 4X1 (720x576)	CP	
							1	1	1	0	525i 2X1 (720x480)	CP	
							1	1	1	1	625i 2X1 (720x576)	CP	
							0	0	0	0	525i 2X2 (1440x480)	CP	PRIM_MODE= 0001 (COMP SD/HD/PR)
							0	0	0	1	625i 2X2 (1440x576)	CP	
							0	0	1	0	525i 4X2 (1440x480)	CP	
							0	0	1	1	625i 4X2 (1440x576)	CP	
							0	1	1	0	525P 2X1 (720x480)	CP	
							0	1	1	1	625P 2X1 (720x576)	CP	
							1	0	0	0	525P 2X2 (1440x480)	CP	
							1	0	0	1	625P 2X2 (1440x576)	CP	
							1	0	1	0	HD 720P 1X1 (1280x720)	CP	
							1	1	0	0	HD 1125 1X1 (1920x1080)	CP	
							1	1	0	1	HD 1125 1X1 (1920x1035)	CP	
							1	1	1	0	HD 1250 1X1 (1920x1080)	CP	
							1	1	1	1	HD 1250 1X1 (1920x1152)	CP	
							0	0	0	0	SVGA (800x600@56)	CP	PRIM_MODE= 0010 (Analog Graphics)
							0	0	0	1	SVGA (800x600@60)	CP	
							0	0	1	0	SVGA (800x600@72)	CP	
							0	0	1	1	SVGA (800x600@75)	CP	
							0	1	0	0	SVGA (800x600@85)	CP	
							0	1	0	1	Reserved		
							1	0	0	0	VGA (640x480@60)	CP	
							1	0	0	1	VGA (640x480@72)	CP	
							1	0	1	0	VGA (640x480@75)	CP	
							1	0	1	1	VGA (640x480@85)	CP	
							1	1	0	0	XVGA (1024x768@60)	CP	
							1	1	0	1	XVGA (1024x768@70)	CP	
							1	1	1	0	Reserved		
							1	1	1	1	Reserved		

Table 66: Register 0x07 to 0x0C

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x07	Auto Detect Enable	**AD_PAL_EN** PAL B/G/I/H autodetect enable								0	Disable	
										1	Enable	
		AD_NTSC_EN NTSC autodetect enable							0		Disable	
									1		Enable	
		AD_PALM_EN PAL M autodetect enable						0			Disable	
								1			Enable	
		AD_PALN_EN PAL N autodetect enable					0				Disable	
							1				Enable	
		AD_P60_EN PAL 60 autodetect enable				0					Disable	
						1					Enable	
		AD_N443_EN NTSC443 autodetect enable			0						Disable	
					1						Enable	
		AD_SECAM_EN SECAM autodetect enable		0							Disable	
				1							Enable	
		AD_SEC525_EN SECAM 525 autodetect enable	0								Disable	
			1								Enable	
0x08	Contrast register	**CON[7:0]** Contrast Adjust. This is the user control for contrast adjustment	1	0	0	0	0	0	0	0	Luma gain = 1	00h Gain = 0 80h Gain = 1 FFh Gain = 2
0x09	Reserved	Reserved	1	0	0	0	0	0	0	0		
0x0A	Brightness register	**BRI[7:0]** This register controls the brightness of the video signal.	0	0	0	0	0	0	0	0		00h = 0IRE 7Fh = 100IRE 80h = -100IRE
0x0B	Hue Register	**HUE[7:0]** This register contains the value for the colour hue adjustment.	0	0	0	0	0	0	0	0		Hue Range = -90 degree to +90 degree
0x0C	Default Value Y	**DEF_ VAL_ EN** Default Value Enable								0	Free Run mode dependent on DEF_ VAL_ AUTO_EN	
										1	Force SDP Free Run mode on and output Blue Screen	
		DEF_ VAL_ AUTO_EN Default Value Auto Enable. In the case of lost lock enables/disables default Y & C values.							0		Disable SDP Free Run mode	When lock is lost Free Run mode can be enabled to output stable timing, clock and a set color
									1		Enable Automatic Free Run Mode (Blue Screen)	
		DEF_Y[5:0] Default Value Y. This register holds the Y default value	0	0	1	1	0	1			Default Y value output in free-run mode Y[7:0]={DEF_Y[5:0], 0,0}	

Table 67: Register 0x0D to 0x11

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Comment
0x0D	Default Value C	**DEF_C[7:0]** Default Value C. Cr and Cb default values are defined in this register. User can control SDP Free output color from a reset default of blue to any other color	0	1	1	1	1	1	0	0	Cr[7:0]={DEF_C[7:4],0,0,0,0} Cb[7:0]={DEF_C[3:0],0,0,0,0}	Default values give blue screen output
0x0E	ADI Control	Reserved				0	0	0	0	0	Set as default	
		SUB_USR_EN			0						User Map	See Section 10.2.1 for further information
					1						User Sub Map 1	
		Reserved	0	0							Set as default	
0x0F	Power Management	Reserved								0	Set to default	
		FB_PWRDN							0		FB input operational	
									1		FB input in power save mode	
		Reserved						0				
		CP_PWRDN					0				CP Operational	
							1				CP in Power save	
		PWRSAV Power save mode powers down the clock generator.				0					System functional	Allows SSPD & STDI to run while
						1					Enable PWRSAV	
		PWRDN Power Down places the decoder in a full power down mode.			0						System functional	
					1						Powered Down	
		Reserved		0							Set to default	
		RESET Chip Reset will load all I2C bits with default values.	0								Normal orperation	Executing reset takes approx. 2ms.
			1								Start reset sequence	
0x10	Status 1 Read only	**IN_LOCK** (STATUS_1[0])								x	In Lock (right now) =1	
		LOST_LOCK (STATUS_1[1])							x		Lost Lock (Since last read) =1	
		FSC_LOCK (STATUS_1[2])						x			Fsc Lock (right now)	
		FOLLOW_PW (STATUS_1[3])					x				Peak White AGC mode active =1	
		AD_RESULT[2:0], (STATUS_1[6:4] **)** AutoDetection Result reports the findings from the autodetection block.		0	0	0					NTSM-MJ	Detected Standard
				0	0	1					NTSC-443	
				0	1	0					PAL-M	
				0	1	1					PAL-60	
				1	0	0					PAL-BGHID	
				1	0	1					SECAM	
				1	1	0					PAL Combination N	
				1	1	1					SECAM 525	
		COL_KILL (STATUS_1[7] **)** Colour Kill	x								Colour Kill is active =1	
0x11	Info Register Read Only	**IDENT[7:0]** Provides identification on the revision of the part.	0	0	0	1	1	0	0	1	ident = 19h	

Table 68: Register 0x12 to 0x15

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Setting	
0x12	Status Register 2 Read only	**MCVS DET** (STATUS_2[0])								x	MV Colour striping detected	1= detected
		MCVS T3 (STATUS_2[1])							x		MV Colour striping type	0=type2, 1=type3
		MV PS DET (STATUS_2[2])						x			MV Pseudo Sync detected	1= detected
		MV AGC (STATUS_2[3])					x				MV AGC pulses detected	1= detected
		LL NSTD (STATUS_2[4])				x					Non Standard line length	1= detected
		FSC NSTD (STATUS_2[5])			x						Fsc Frequency non standard	1= detected
		CP_FREE_RUN (STATUS_2[6]) Component processor is free running.		x							0=Valid Video signal found. 1=CP free running	
		TLLC PLL LOCK (STATUS_2[7]) True Line Lock clock PLL in lock	x								1=PLL Locked	Locked to input H_Syncs
0x13	Status Register 3 Read only	**INST_HLOCK** (STATUS_3[0])								x	1=Horizontal lock achieved	Unfiltered
		GEMD (STATUS_3[1])							x		1= Gemstar data detected	
		SD_OP_50Hz (STATUS_3[2])						0			SD 60Hz detected	SD Field Rate Detect
								1			SD 50Hz detected	
		CVBS (STATUS_3[3])					x				Result of CVBS / Y/C autodetection	0 = Y/C 1 = CVBS signal
		FREE_RUN_ACT (STATUS_3[4])				x					1=Free Run mode Active	`Blue Screen` o/p
		STD FLD LEN (STATUS_3[5])			x						1=Field length standard	
		INTERLACE (STATUS_3[6])		x							1=Interlaced Video detected	
		PAL SW LOCK	x								1=Swinging Burst Detected	Reliable sequence
0x13	Analogue Control Internal Write Only	Reserved							0	0		
		XTAL_TTL_SEL						0			Crystal cct operation	
								1			TTL level clock operation	External Clock
		Reserved	0	0	0	0	0					
0x14	Analogue Clamp Control	Reserved					0	0	1	0	Reserved set to default	
		CCLEN Current Clamp Enable				0					Current sources switched off	
						1					Current sources enabled	
		Reserved	0	0	0						Reserved set to default	
0x15	Digital Clamp	Reserved				0	x	x	x	x	Set to Default	
		DCT[1:0] Digital Clamp Timing		0	0						Slow (TC: 1sec)	
				0	1						Medium (TC: 0.5sec)	
				1	0						Fast (TC:0.1sec)	
				1	1						TC dependant on Video	
		Reserved	0								Set to default	

Table 69: Register 0x17

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x17	Shaping Filter Control	**YSFM[4:0]** Selects Y Shaping Filter Mode when in CVBS only mode. It allows the user to select a wide range of low pass and notch filters. If either Auto mode is selected the decoder selects the optimum Y filter depending on the CVBS video source quality (good v's bad).				0	0	0	0	0	Auto Wide notch for poor quality sources or wide band filter with Comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality.
						0	0	0	0	1	Auto narrow notch for poor quality sources or wide band filter with Comb for good quality input	
						0	0	0	1	0	SVHS 1	If one of these modes is selected the deocder does not change filter modes depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video.
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR601)	
						1	0	1	0	0	PAL NN1	
						1	0	1	0	1	PAL NN2	
						1	0	1	1	0	PAL NN3	
						1	0	1	1	1	PAL WN 1	
						1	1	0	0	0	PAL WN 2	
						1	1	0	0	1	NTSC NN1	
						1	1	0	1	0	NTSC NN2	
						1	1	0	1	1	NTSC NN3	
						1	1	1	0	0	NTSC WN1	
						1	1	1	0	1	NTSC WN2	
						1	1	1	1	0	NTSC WN3	
						1	1	1	1	1	Reserved	
		CSFM[2:0] C Shaping Filter Mode allows the selection from a range of low pass chrominance filters. If either Auto mode is selected the decoder selects the optimum C filter depending on the CVBS video source quality (good v's bad). Non auto settings force a C filter for all standards and quality of CVBS video	0	0	0						Auto selection 1.5Mhz	Automatically selects a C filter based on video standard and
			0	0	1						Auto selection 2.17Mhz	
			0	1	0						SH1	Selects a C filter for all video standards and for good and bad video.
			0	1	1						SH2	
			1	0	0						SH3	
			1	0	1						SH4	
			1	1	0						SH5	
			1	1	1						Wide Band Mode	

Table 70: Register 0x18 to 0x1D

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x18	Shaping Filter Control 2	**WYSFM[4:0]** Wideband Y Shaping Filter Mode allows the user to select which Y Shaping filter is used for the Y component of Y/C, YPbPr, B/W input signals and is also used when good quality input CVBS signal is detected. For all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0].				0	0	0	0	0	Reserved Do Not Use	
						0	0	0	0	1	Reserved Do Not Use	
						0	0	0	1	0	SVHS 1	
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	Reserved Do Not Use	
						~	~	~	~	~	Reserved Do Not Use	
						1	1	1	1	1	Reserved Do Not Use	
		Reserved										
				0	0						Set to default	
		WYSFMOVR enables the use of automatic WYSFN filter selection.	0								Auto selection of best filter	
			1								Manual select filter using WYSFM[4:0]	
0x19	Comb Filter Control	**PSFSEL[1:0]** Control the signal bandwidth which is fed to the comb filters (PAL)							0	0	Narrow	
									0	1	Medium	
									1	0	Wide	
									1	1	Widest	
		NSFSEL[1:0] Control the signal bandwidth which is fed to the comb filters (NTSC)					0	0			Narrow	
							0	1			Medium	
							1	0			Medium	
							1	1			Wide	
		Reserved	1	1	1	1					Set as default	
0x1A to 0x1C	Reserved	Reserved										
0x1D	ADI Control 2	Reserved			0	0	0	x	x	x		
		28MHz Crystal Mode		0							Use 27MHz Crystal	
				1							Use 28MHz Crystal	
		LLC Tristate	0								LLC Pin Active	
			1								LLC Pin Tristated	

Table 71: Register 0x27 to 0x2C

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x27	Pixel Delay Control	**LTA[1:0]** Luma timing adjust allows the user to specify a timing difference between chroma and luma samples.							0	0	No Delay	CVBS mode LTA[1:0] = 00b, S-Video mode LTA[1:0]= 01b, YPrPb mode LTA[1:0] = 01b
									0	1	Luma 1 clk(37nS) delayed	
									1	0	Luma 2 clk(74nS) early	
									0	1	Luma 1 clk(37nS) early	
		Reserved						0			Set to Zero	
		CTA[2:0] Chroma Timing Adjust allows a specified timing defference between the Luma and Chroma samples			0	0	0				Not valid setting	CVBS mode CTA[2:0] = 011b, S-Video mode CTA[2:0]= 101b, YPrPb mode CTA[2:0] = 110b
					0	0	1				Chroma+2 pixel (early)	
					0	1	0				Chroma+1 pixel (early)	
					0	1	1				No Delay	
					1	0	0				Chroma-1 pixel (late)	
					1	0	1				Chroma-2 pixel (late)	
					1	1	0				Chroma-3 pixel (late)	
					1	1	1				Not valid setting	
		AUTO_PDC_EN Automatically programs the LTA / CTA values so that luma and chroma aligned at output for all modes of operation.		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma samples.	
				1							LTA and CTA values determined automatically	
		SWPC This bit allows the Cr and Cb samples to be swapped.	0								No swapping	See; SWAP_CR_CB_WB; Addr. 0x89
			1								Swap the Cr and Cb values	
0x28 to 0x2A	Reserved	Reserved										
0x2B	Misc Gain Control	**PW_UPD** Peak white update								0	Update once per video line	Peak white must be enabled see
										1	Update once per field	
		Reserved			1	0	0	0	0		Set to default	
		CKE Colour kill enable allows the colour kill function to be switched on and off.		0							Colour kill disabled	For SECAM colour kill threshold is set at 8%
				1							Colour kill enabled	see CKILLTHR[2:0]
		Reserved	1								Set to Default	
0x2C	AGC Mode Control	**CAGC[1:0]** Chroma Automatic							0	0	Manual Fixed gain	Use CMG[11:0]
									0	1	Use luma gain for chroma	
									1	0	Automatic gain	Based on colour
									1	1	Freeze chroma gain	
		Reserved					1	1			Set to One	
		LAGC[2:0] Luma Automatic		0	0	0					Manual Fixed gain	Use LMG[11:0]
				0	0	1					AGC no override through white peak. Man IRE control	Blank level to sync tip
				0	1	0					AGC auto override through white peak. Man IRE control	Blank level to sync tip
				0	1	1					AGC no override through white peak. Auto IRE control	Blank level to sync tip
				1	0	0					AGC auto override through white peak. Auto IRE control	Blank level to sync tip
				1	0	1					AGC active video with white peak	
				1	1	0					AGC active video with average video.	
				1	1	1					Freeze gain	
		Reserved	1								Set to One	

Table 72: Register 0x2D to 0x33

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x2D	Chroma Gain Control 1 Write Only	**CMG[11:8]** Chroma Manual Gain can be used to program a desired manual chroma gain. Reading back from this register in AGC mode gives the current gain setting					0	1	0	0	CAGC[1:0] settings will decide what mode CMG[11:0] operates in	
		Reserved			1	1					Set to One	
		CAGT[1:0] Chroma Automatic Gain Timing allows adjustment of the Chroma AGC tracking speed	0	0							Slow (TC: 2 sec)	Will only have effect if CAGC[1:0] is set to auto gain (`10`)
			0	1							Medium (TC: 1 sec)	
			1	0							Fast (TC: 0.2 sec)	
			1	1							Adaptive	
0x2E	Chroma Gain Control 2 Write Only	**CMG[7:0]** Chroma Manual Gain lower 8-bits, see CMG[11:8] for discription	0	0	0	0	0	0	0	0	CMG[11:0] = 750dec the gain is 1 in NTSC CMG[11:0] = 741dec the gain is 1 in PAL	Min value is 0dec(G=-60db) Max value is 3750(Gain = 5)
0x2F	Luma Gain Control 1 Write Only	**LMG[11:8]** Luma Manual Gain can be used program a desired manual chroma gain or read back the actual used gain value					x	x	x	x	LAGC[1:0] settings will decide what mode LMG[11:0] operates in	
		Reserved			1	1					Set to One	
		LAGT[1:0] Luma Automatic Gain Timing allows adjustment of the Luma AGC tracking speed	0	0							Slow (TC: 2 sec)	Will only have effect if LAGC[1:0] is set to auto gain (001,010,011or 100)
			0	1							Medium (TC: 1 sec)	
			1	0							Fast (TC: 0.2 sec)	
			1	1							Dependent on VID_QUAL	
0x30	Luma Gain Control 2 Write Only	**LMG[7:0]** Luma Manual Gain can be used to program a desired manual chroma gain or read back the actual used gain value	x	x	x	x	x	x	x	x	LMG[11:0] =1234dec the gain is 1 in NTSC LMG[11:0] = 1266dec the gain is 1 in PAL	Min value NTSC 1024 (G= 0.85) PAL (G=0.81) Max value NTSC = 2468(G = 2) & PAL = 2532 (G = 2)
0x31	VS & FIELD control 1	Reserved						0	1	0	Set to Default	
		HVSTIM selects where within a line of video the VS signal is asserted.					0				Start of line relative to HSE	HSE=Hsync end
							1				Start of line relative to HSB	HSB=Hsync begin
		NEWAVMODE Sets the EAV/SAV mode				0					EAV/SAV codes generated to suit ADV Encoders	
						1					Manual VS/Field position controlled by registers 32h,33h,E5h-EAh	
		Reserved	0	0	0						Set to Default	
0x32	Vsync Field control 2	Reserved			0	0	0	0	0	1	Set to default	
		VSBHE		0							VS goes high in middle of line (even field)	NEWAVMODE bit must be set high
				1							VS changes state at start of line (even field)	
		VSBHO	0								VS goes high in middle of line (odd field)	
			1								VS changes state at start of line (odd field)	
0x33	Vsync Field control 3	Reserved			0	0	0	1	0	0	Set to default	
		VSEHE		0							VS goes low in middle of line (even field)	
				1							VS changes state at start of line (even field)	
		VSEHO	0								VS goes low in middle of line (odd field)	
			1								VS changes state at start of line (odd field)	

Table 73: Register 0x34 to 0x38

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x34	HS Position Control 1	**HSE[10:8]** HS End allows the positioning of the HS output within the video line						0	0	0	HS output ends HSE[10:0] pixels after falling edge of HSync	Using HSB and HSE the user can program the position and length of the output Hsync
		Reserved					0				Set to Zero	
		HSB[10:8] HS begin allows the positioning of HS output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSync	
		Reserved	0								Set to Zero	
0x35	HS Position Control 2	**HSB[7:0]** See above, using HSB[9:0] and HSE[9:0] the user can program the position and length of HS output signal	0	0	0	0	0	0	1	0		
0x36	HS Position Control 3	**HSE[7:0]** See above.	0	0	0	0	0	0	0	0		
0x37	Polarity	**PCLK** Sets the polarity of LLC1								0	Invert Polarity	
										1	Normal polarity as per timing diagrams	
		Reserved						0	0		Set to Zero	
		PF sets the FIELD polarity					0				Active High	
							1				Active Low	
		Reserved				0					Set to Zero	
		PVS sets the VS Polarity			0						Active High	
					1						Active Low	
		Reserved		0							Set to Zero	
		PHS sets HS Polarity	0								Active High	
			1								Active Low	
0x38	NTSC comb control	**YCMN[2:0]** Luma Comb Mode						0	0	0	Adaptive 3 Line 3 tap luma	
								1	0	0	Use Low pass notch	
								1	0	1	Fixed Luma Comb (2 Line)	Top lines of memory
								1	1	0	Fixed Luma Comb (3 Line)	All lines of memory
								1	1	1	Fixed Luma Comb (2 Line)	Bottom lines of memory
		CCMN[2:0] Chroma Comb Mode NTSC			0	0	0				3 line adaptive for CTAPSN =01 4 line adaptive for CTAPSN =10 5 line adaptive	
					1	0	0				Disable Chroma Comb	
					1	0	1				Fixed 2 line for CTAPSN =01 Fixed 3 line for CTAPSN =10 Fixed 4 line for CTAPSN =11	Top lines of memory
					1	1	0				Fixed 3 line for CTAPSN =01 Fixed 4 line for CTAPSN =10 Fixed 5 line for CTAPSN =11	All lines of memory
					1	1	1				Fixed 2 line for CTAPSN =01 Fixed 3 line for CTAPSN =10 Fixed 4 line for CTAPSN =11	Bottom lines of memory
		CTAPSN[1:0] Chroma Comb	0	0							Not Used	
			0	1							Adapts 3 lines ---2 lines	
			1	0							Adapts 5 lines ---3 lines	
			1	1							Adapts 5 lines ---4 lines	

Table 74: Register 0x39 to 0x3B

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x39	PAL comb control	**YCMP[2:0]** Luma Comb Mode PAL						0	0	0	Adaptive 5 Line 3 tap luma comb	
								1	0	0	Use Low pass notch	
								1	0	1	Fixed Luma Comb (3 Line)	Top lines of memory
								1	1	0	Fixed Luma Comb (5 Line)	All lines of memory
								1	1	1	Fixed Luma Comb (3 Line)	Bottom lines of mem
		CCMP[2:0] Chroma Comb Mode PAL			0	0	0				3 line adaptive for CTAPSN =01 4 line adaptive for CTAPSN =10 5 line adaptive for CTAPSN =11	
					1	0	0				Disable Chroma Comb	
					1	0	1				fixed 2 line for CTAPSN =01 fixed 3 line for CTAPSN =10 fixed 4 line for CTAPSN =11	Top lines of memory
					1	1	0				fixed 3 line for CTAPSN =01 fixed 4 line for CTAPSN =10 fixed 5 line for CTAPSN =11	All lines of memory
					1	1	1				fixed 2 line for CTAPSN =01 fixed 3 line for CTAPSN =10 fixed 4 line for CTAPSN =11	Bottom lines of mem
		CTAPSP[1:0] Chroma Comb Taps PAL	0	0							Not Used	
			0	1							adapts 5 lines ---2 lines (2 taps)	
			1	0							adapts 5 lines ---3 lines (3 taps)	
			1	1							adapts 5 lines ---4 lines (4 taps)	
0x3A	ADC Control	**PWRDN_ADC_3** Enable powerdown of ADC3.								0	ADC3 normal operation	
										1	Powerdown ADC3	
		PWRDN_ADC_2 Enable powerdown of ADC2.							0		ADC2 normal operation	
									1		Powerdown ADC2	
		PWRDN_ADC_1 Enable powerdown of ADC1						0			ADC1 normal operation	
								1			Powerdown ADC1	
		PWRDN_ADC_0 Enable powerdown of ADC0					0				ADC0 normal operation	
							1				Powerdown ADC0	
		LATCH_CLK[3:0] Internal ADC parameter which controls the data acquisition stage of the A/D conversion.	0	0	0	1					Recommended LLC range [13.5MHz – 55MHz]	
			0	0	1	0					Recommended LLC range [55MHz – 111MHz]	
			0	1	1	0					Reserved	
0x3B	BIAS CONTROL	**EN_INTERNAL_RES** enable internal resistor. Allows the user to switch between internal and external bias								0	Use external resistor	
										1	Use internal resistor	
		Reserved							0		Set to zero	
		Reserved						1			Set to one	
		IBIAS_SET[4:0] this value sets the raw bias current value. This value muntiplies the fundemental bias value of 37.5uA to generate the overall bias current for the entire chip	1	0	0	0	0				Default 600uA bias current	

Table 75: Register 0x3C to 0x49

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x3C	TLLC CONTROL	**PLL_QPUMP[2:0]** PLL charge pump current settings						0	0	0	50uA	PLL_QPUMP must be set for each CP mode as described in this document.
								0	0	1	100uA	
								0	1	0	150uA	
								0	1	1	250uA	
								1	0	0	350uA	
								1	0	1	500uA	
								1	1	0	750uA	
								1	1	1	1500uA	
		SOG_SYNC_LEVEL[4:0] embedded sync trigger level. Allows the setting of the analogue trigger threshold for the sync detection Vth=300mVxSOG_S_L[4:0] /32	0	1	0	1	1				Slice level set at 103mV above the lowest analog voltage level within the input video line	
0x3D	Manual Window	Reserved					0	0	1	1	Set to Default	
		CKILLTHR[2:0] Sets the threshold at which color kill is enabled for PAL and NTSC. SECAM is fixed at 8%		0	0	0					kill at .5%	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1					kill at 1.5%	
				0	1	0					kill at 2.5%	
				0	1	1					kill at 4%	
				1	0	0					kill at 8.5%	
				1	0	1					kill at 16%	
				1	1	0					kill at 32%	
				1	1	1					Reserved	
		Reserved	0								Set to Default	
0x3E to 0x40	Reserved	Reserved										
0x41	Resample Control	Reserved			0	0	0	0	0	1	Set to default	
		SFL_INV Controls the behaviour of the PAL switch bit		0							SFL compatible with ADV717x / ADV73xx encoders	
				1							SFL compatible with ADV7190/91/94 encoders	
		Reserved	0								Set to default	
0x42 to 0x47	Reserved	Reserved										
0x48	Gemstar Control 1	GDECEL[15:0] 16 individual enable bits that select the lines of video (even field lines 10-25) that the decoder checks for Gemstar compatible data										LSB= Line 10 MSB= Line 25 Default = Do not check for gemstar compatible data on any lines [10-25] in even fields
		GDECEL[15:8] see above	0	0	0	0	0	0	0	0		
0x49	Gemstar Control 2	**GDECEL[7:0]** see above	0	0	0	0	0	0	0	0		

Table 76: Register 0x4A to 0x50

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x4A	Gemstar Control 3	**GDECOL[15:0]** 16 individual enable bits that select the lines of video (odd field lines 10-25) that the decoder checks for Gemstar compatible data										LSB= Line 10 MSB= Line 25 Default = Do not check for gemstar compatible data on any lines [10-25] in odd fields
		GDECOL[15:8] see above	0	0	0	0	0	0	0	0		
0x4B	Gemstar Control 4	**GDECOL[7:0]** see above	0	0	0	0	0	0	0	0		
0x4C	Gemstar Control 5	**GDECAD** Controls the manor in which decoded Gemstar data is inserted into the horizontal blanking period								0	Split data into half byte	To avoid 00/ FF code
										1	Output in straight 8-bit format	
		Reserved	x	x	x	x	0	0	0			
0x4D	CTI DNR control 1	**CTI_EN** CTI enable								0	Disable CTI	
										1	Enable CTI	
		CTI_AB_EN enables the mixing of the transient improved chroma with the origional signal							0		Disable CTI alpha blender	
									1		Enable CTI alpha blender	
		CTI_AB[1:0] controls the behaviour of the alpha-blend circuitry					0	0			Sharpest mixing	
							0	1			Sharp mixing	
							1	0			Smooth	
							1	1			Smoothest	
		Reserved				0					Set to Default	
		DNR_EN Enable or bypass the DNR block			0						Bypass the DNR block	
					1						Enable the DNR block	
		Reserved		1							Set to default	
		Reserved	1								Set to default	
0x4E	CTI DNR control 2	**CTI_CTH[7:0]** Specifies how big the amplitude step must be to be steepened by the CTI block	0	0	0	0	1	0	0	0		
0x4F	Reserved	Reserved										
0x50	CTI DNR control 4	**DNR_TH[7:0]** specifies the max. edge that will be interpreted as noise and therefore blanked	0	0	0	0	1	0	0	0		

Table 77: Register 0x51 to 0x58

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x51	Lock Count	**CIL[2:0]** Count into Lock determines the number of lines that the system has to remain in lock before the system shows a locked status						0	0	0	1 Line of Video	Only operational for SDP modes
								0	0	1	2 Line of Video	
								0	1	0	5 Line of Video	
								0	1	1	10 Line of Video	
								1	0	0	100 Line of Video	
								1	0	1	500 Line of Video	
								1	1	0	1000 Line of Video	
								1	1	1	100000 Line of Video	
		COL[2:0] Count out of Lock determines the number of lines that the system has to remain out of lock before the system shows a lost locked status			0	0	0				1 Line of Video	
					0	0	1				2 Lines of Video	
					0	1	0				5 Lines of Video	
					0	1	1				10 Lines of Video	
					1	0	0				100 Lines of Video	
					1	0	1				500 Lines of Video	
					1	1	0				1000 Lines of Video	
					1	1	1				100000 Lines of Video	
		SRLS Select Raw Lock Signal selects the determination of the		0							Over field with verticle info	
				1							Line to Line evaluation	
		FSCLE Fsc Lock Enable	0								Lock Status set only by horizontal lock	FSCLE must be set to 0 in YPrPb mode if a reliable
			1								Lock Status set by horizontal	
0x52	CSC_1	A4[12:0] Contains the 13-bit offset for the A channel										CSC only available in CP modes See CSC section in this document for more details and programming examples
		A4[12:8] see A4[12:0] above				0	0	0	0	0		
		Reserved		0	0							
		CSC_SCALE bit allows to cater for coefficients which extend the supported range	0								No Scaling	
			1								2x scaling	
0x53	CSC_2	**A4[7:0]** see A4[12:0] above	0	0	0	0	0	0	0	0		
0x54	CSC_3	A3[12:0] Contains the 13-bit A3 coefficient for channel A										
		A3[12:6] see A3[12:0] above		0	0	0	0	0	0	0		
		Reserved	0									
0x55	CSC_4	A2[12:0] Contains the 13-bit A2 coefficient for channel A										
		A2[12:11] see A2[12:0] above							0	0		
		A3[5:0] see A3[12:0] above	0	0	0	0	0	0				
0x56	CSC_5	**A2[10:3]** see A2[12:0] above										
		A2[10:3] see A2[12:0] above	0	0	0	0	0	0	0	0		
0x57	CSC_6	A1[12:0] Contains the 13-bit A1 coefficient for channel A										
		A1[12:8] see A1[12:0] above				0	1	0	0	0		
		A2[2:0] see A2[12:0] above	0	0	0							
0x58	CSC_7	**A1[7:0]** see A1[12:0] above	0	0	0	0	0	0	0	0		

Table 78: Register 0x59 to 0x66

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x59	CSC_8	B4[12:0] Contains the 13-bit offset for the B channel										CSC only available in CP modes See CSC section in this document for more details and programming examples
		B4[12:8] see B4[12:0] above				0	0	0	0	0		
		Reserved	0	0	0							
0x5A	CSC_9	**B4[7:0]** see B4[12:0] above	0	0	0	0	0	0	0	0		
0x5B	CSC_10	B3[12:0] Contains the 13-bit B3 coefficient for channel B										
		B3[12:6] see B3[12:0] above		0	0	0	0	0	0	0		
		Reserved	0									
0x5C	CSC_11	B2[12:0] Contains the 13-bit B2 coefficient for channel B										
		B2[12:11] see B2[12:0] above							0	1		
		B3[5:0] see B3[12:0] above	0	0	0	0	0	0				
0x5D	CSC_12	**B2[10:3]** see B2[12:0] above	0	0	0	0	0	0	0	0		
0x5E	CSC_13	B1[12:0] Contains the 13-bit B1 coefficient for channel B										
		B1[12:8] see B1[12:0] above				0	0	0	0	0		
		B2[2:0] see B2[12:0] above	0	0	0							
0x5F	CSC_14	**B1[7:0]** see B1[12:0] above	0	0	0	0	0	0	0	0		
0x60	CSC_15	C4[12:0] Contains the 13-bit offset for the C channel										
		C4[12:8] see C4[12:0] above				0	0	0	0	0		
		Reserved	0	0	0							
0x61	CSC_16	**C4[7:0]** see C4[12:0] above	0	0	0	0	0	0	0	0		
0x62	CSC_11	C3[12:0] Contains the 13-bit C3 coefficient for channel C										
		C3[12:6] see C3[12:0] above		0	1	0	0	0	0	0		
		Reserved	0									
0x63	CSC_17	C2[12:0] Contains the 13-bit C2 coefficient for channel C										
		C2[12:11] see C2[12:0] above							0	1		
		C3[5:0] see C3[12:0] above	0	0	0	0	0	0				
0x64	CSC_18	**C2[10:3]** see C2[12:0] above	0	0	0	0	0	0	0	0		
0x65	CSC_19	C1[12:0] Contains the 13-bit C1 coefficient for channel C										
		C1[12:8] see C1[12:0] above				0	0	0	0	0		
		C2[2:0] see C2[12:0] above	0	0	0							
0x66	CSC_20	**C1[7:0]** see C1[12:0] above	0	0	0	0	0	0	0	0		

Table 79: Register 0x67 to 0x69

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x67	CSC_22	**DPP_FILT[2:0]** Data Preprocessor Decimation Filters						0	0	0	No oversampling and no decimation, 4:4:4 output	Only applicable in CP modes
								0	0	1	No oversampling, CH A no decimation, CHB & CHC decimate by 2, 4:2:2 output	
								0	1	0	CH A, CHB & CHC oversampled by 2 & decimate by 2, 4:4:4 output	
								0	1	1	CHA, CHB & CHC oversampling by 2, CHA decimated by 2 CHB & CHC decimated by 4, 4:2:2 output	
								1	0	0		
								1	0	1		
								1	1	0		
								1	1	1		
		DS_ONLY Enables downsampling (data dropping)					0				filter and downsanple	
							1				downsample only (no filtering)	
		SOFT_FILT DPP ChB/ChC decimation filter transition band selection				0					Steep roll-off in transition band	
						1					Shallow roll-off in transition band	
		DLY_C Enables the delay of data through the C channel by one clock cycle			0						Pass data	
					1						Delay data by one clock cycle	
		DLY_B Enables the delay of data through the B channel by one clock cycle		0							Pass data	
				1							Delay data by one clock cycle	
		DLY_A Enables the delay of data through the A channel by one clock cycle	0								Pass data	
			1								Delay data by one clock cycle	
0x68	CSC_23	**DPP_AFILT[1:0]** DPP Decimation filter configuration control								0	Manual selection of DPP filters as per DPP_FILT[1:0]	
										1	Automatic selection of DPP filters	Selection based on PRIM_MODE, VID_STD, CPOP_SEL
		Reserved	0	0	0	0	0	0	0		Set to default	
0x69	Configure 1	**SDM_SEL[1:0]** Standard definition mode selection							0	0	As per INSEL[3:0]	
									1	1	Y/C on AIN2 and AIN3	
		Reserved				0	0	0			Set to Default	
		INV_DINCLK Inverts the Digital input clock			0						Invert	
					1						Normal	
		SYN_LOTRIG External Sync Input Trigger Level		0							3.3V trigger for HS/VS	Threshold approx.1.5V
				1							1V trigger for HS/VS	Threshold approx.0.6V
		TRI_LEVEL	0								Sync detection for bi-level sync	
			1								Sync detection for tri level sync	

Table 80: Register 0x6A to 0x6C

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6A	TLLC Phase Adjust	**DLL_PH[4:0]** sets the ADC sampling point into 32 evenly spaced sampling points				0	0	0	0	0	Select Phase 0	Only use in CP RGB graphics modes. Backend IC should be used to determines optimum sampling phase
						~	~	~	~	~		
						1	1	1	1	1	Select Pase 31	
		BYP_DLL allows the user to bypass the DLL block			0						ADC clock through DLL block	
					1						Bypass DLL block	
		Reserved	0	x							Undefined	
0x6B	CP output selection	**CPOP_SEL[0:3]** controls the format of the output data from the CP core					0	0	0	0	Reserved	
							0	0	0	1	20-bit out, Y=P19-P10, PrPb=P9-P0	PrPb interleaved
							0	0	1	0	Reserved	
							0	0	1	1	16-bit out, Y=P19-P12, PrPb=P9-P2	PrPb interleaved
							0	1	0	0	12-bit DDR	
							~	~	~	~	Reserved	
							1	1	1	1	Reserved	
		Reserved			0	0					Set to Default	
		F_OUT_SEL allows the switching of an active window output on the F pin		0							DE (Data Enable) output on the FIELD pin	DE signal can be used to drive the DE signal on a DVI Tx
				1							Field signal o/p on FIELD pin	
		HS_OUT_SEL allows the switching of a CSync output on the HS pin	0								CSync o/p on the HS pin	
			1								HSync o/p on the HS pin	
0x6C	CP Clamp1	CLMP_A[11:0] Manual Clamp for channel A, 12-bit value to be subtracted from the incoming video signal.										
		CLMP_A[11:8] see CLMP_A[11:0] above					0	0	0	0		
		Reserved				0					Reserved	
		CLMP_FREEZE stops the digital fine clamp loops, A, B & C from updating										
		CLMP_FREEZE stops the			0						Clamp loop operational	update every line
					1						Clamps stopped	No update
		CLMP_BC_MAN manual or automatic control of channels B and C. No individual control		0							Auto-determined by clamp loop	CLMP_BC_MAN bit must to set for CLMP_B[11:0] & CLMP_C[11:0] to be active.
				1							Manual-determined by CLMP_B[11:0] and CLMP_C[11:0]	
		CLMP_A_MAN manual or automatic control of channel A	0								Auto-determined by clamp loop	CLMP_A_MAN bit must to set for CLMP_A[11:0] to be active.
			1								Manual-determined by CLMP_A[11:0]	

Table 81: Register 0x6D to 0x72

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6D	CP Clamp2	**CLMP_A[7:0]** see CLMP_A[11:0] above	0	0	0	0	0	0	0	0		
0x6E	CP Clamp3	CLMP_B[11:0] Manual Clamp for channel B, 12-bit value to be subtracted from the incoming video signal.										
		CLMP_B[11:4] see CLMP_B[11:0] above	0	0	0	0	0	0	0	0		
0x6F	CP Clamp4	CLMP_C[11:0] Manual Clamp for channel C, 12-bit value to be subtracted from the incoming video signal.										
		CLMP_C[11:8] see CLMP_C[11:0] above					0	0	0	0		
		CLMP_B[3:0] see CLMP_B[11:0] above	0	0	0	0						
0x70	CP Clamp5	**CLMP_C[7:0]** see CLMP_C[11:0] above	0	0	0	0	0	0	0	0		
0x71	CP AGC 1	**AGC_TIM[2:0]** AGC time constant						0	0	0	100 Lines	
								0	0	1	1 frame	
								0	1	0	.5 seconds	
								0	1	1	1 seconds	
								1	0	0	2 seconds	
								1	0	1	3 seconds	
								1	1	0	5 seconds	
								1	1	1	7 seconds	
		HS_NORM nominal Hsync depth					0				Scale as per 300mV Hsync	
							1				Scale as per 286mV Hsync	
		AGC FREEZE agc freeze enable				0					AGC loop operational	
						1					Freeze AGC loop	
		AGC_TAR_MAN manual target level enable			0						AGC scales to 300/286mV HSync	
					1						AGC scales to value AGC_TAR[9:0]	
		AGC_TAR[9:0] Manual target level set the target value for Sync depth after gain has been applied										
		AGC_TAR[9:8] see AGC_TAR[9:0]	x	x								
0x72	CP AGC 2	**AGC_TAR[7:0]** see AGC_TAR[9:0]	x	x	x	x	x	x	x	x		

Table 82: Register 0x73 to 0x7A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x73	CP AGC 3	A_GAIN[9:0] manual gain value for channel A										
		A_GAIN[9:4] see A_GAIN[9:0] next page			0	1	0	0	0	0		
		AGC_MODE_MAN switch control of gain operation mode from SSPD block to GAIN_MAN parameter.		0							Enable AGC based on SSPD decision	
				1							Gain operation controlled by GAIN_MAN	
		GAIN_MAN enable the gain factor to be set by the AGC or manually	0								Automatic Gain mode enabled	
			1								Manual gain mode set by A_GAIN[9:0], B_GAIN[9:0] and C_GAIN[9:0]	
0x74	CP AGC 4	B_GAIN[9:0] manual gain value for channel B										
		B_GAIN[9:6] see B_GAIN[9:0] above					0	1	0	0		
		A_GAIN[3:0] see A_GAIN[9:0] on previous page	0	0	0	0						
0x75	CP AGC 5	C_GAIN[9:0] manual gain value for channel C										
		C_GAIN[9:8] see C_GAIN[9:0] above							0	1		
		B_GAIN[5:0] see B_GAIN[9:0] above	0	0	0	0	0	0				
0x76	CP AGC 6	**C_GAIN[7:0]** see C_GAIN[9:0]	0	0	0	0	0	0	0	0		
0x77	CP OFFSET1	A_OFFSET[9:0]Channel A offset										Set offsets accordingly for YPrPb or RGB mode. When A/B/C_OFFSET= 3FFh then that offset is determined automatically.
		A_OFFSET[9:4]			1	1	1	1	1	1		
		CP_PREC[1:0]	0	0							Rounds and Truncates data in Channels A, B & C to 10-bit precision	
			0	1							Rounds and Truncates data in Channels A, B & C to 9-bit precision	
			1	0							Rounds and Truncates data in Channels A, B & C to 8-bit precision	
			1	1							Rounds and Truncates data in Channels A, B & C to 8-bit precision	
0x78	CP OFFSET2	B_OFFSET[9:0] Channel B offset										
		B_OFFSET[9:6]					1	1	1	1		
		A_OFFSET[3:0]	1	1	1	1						
0x79	CP OFFSET3	C_OFFSET[9:0] Channel C offset										
		C_OFFSET[9:8]							1	1		
		B_OFFSET[5:0]	1	1	1	1	1	1				
0x7A	CP OFFSET4	**C_OFFSET[7:0]**	1	1	1	1	1	1	1	1		

Table 83: Register 0x7B to 0x7C

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x7B	CP AV CONTROL	**BLANK_RGB_SEL** allow the blank values for channels A,B and C to be changed.								0	A = 64dec, B & C = 512dec, use for YPrPb i/p's	
										1	A, B & C = 64dec, use for RGB i/p's	
		AV_CODE_EN allows the insertion of AV codes into the data stream							0		Do not insert AV codes	
									1		Insert AV codes in the data stream	
		AV_POS_SEL allows the selection of the AV code position						0			SAV at falling edge of Hsync, EAV at rising edge of Hsync	Dependant on HSync polarity
								1			Default position for SAV & EAV	
		AV_BLANK_ENABLE sets the data output during blanking					0				Output clamped and gained data during the horizontal and vertical blanking periods	
							1				Replace data during the horizontal and vertical blanking periods with default data (see also AV_RGB_EN)	
		CP_DUP_AV Duplicate AV code				0					Spread AV code over ch. A & ch. B	
						1					AV code duplicated on ch A & ch. B	
		INTLCD_240P_540P Interlaced 240P/540P			0						Disable free running field	Progressive timing o/p
					1						Enable Free running field	Interlaced timing o/p
		AV_INV_V Invert V bit in AV		0							Insert V bit with default polarity	
				1							Invert V bit before Inserting	
		AV_INV_F Invert F bit in AV	0								Insert F bit with default polarity	
			1								Invert F bit before Inserting	
7Ch	CP HVF CONTROL 1	END_HS[9:0] End HS signal 10-bit 2`s complement number controlling the end of Hsync										e.g. 3F0=HS ends 16 llc early, 100h= HS ends 256 LLC1 late
		END_HS[9:8] see END_HS[9:0] above							0	0		
		START_HS[9:0] Start HS signal 10-bit 2`s complement number controlling the start of HS										e.g. 3FF=HSstarts 1 LLC1 early, 005h= HS starts 5 LLC1 late
		START_HS[9:8] see START_HS[9:0] above					0	0				
		Reserved				x						
		PIN_INV_F Invert polarity of FIELD/DE signal			0						Interlaced-low for odd, high for even.	FIELD/DE active high
					1						Interlaced-high for odd, high for even.	FIELD/DE active low
		PIN_INV_VS Invert polarity of HS signal		0							Positive polarity Vsync	
				1							Negative polarity Vsync	
		PIN_INV_HS Invert polarity of HS signal (or CSync if selected)	0								Positive polarity	
			1								Negative polarity	

Table 84: Register 0x7D to 0x85

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x7D	CP HVF CONTROL 2	**END_HS[7:0]** see END_HS[9:0] above	0	0	0	0	0	0	0	0		
0x7E	CP HVF CONTROL 3	**START_HS[7:0]** see START_HS[9:0] above	0	0	0	0	0	0	0	0		
0x7F	CP HVF CONTROL 4	**END_VS[3:0]** End VS signal 4-bit 2`s complement number controlling the end of VSync					0	0	0	0		e.g. 0x0E=VS ends 2 lines early, 0x01= VS ends 1 line late
		START_VS[3:0] Start VS signal 4-bit 2`s complement number controlling the start of VSync	0	0	0	0						e.g. 0x0F=VS starts 1 line early, 0x01= VS end 3 lines late
0x80	CP HVF CONTROL 5	**START_FO[3:0]** Start FIELD odd signal 4-bit 2`s complement number controlling the start of odd field output					0	0	0	0		e.g. 0x0F=FIELD starts 1 line early, 0x02= FIELD ends 2 lines late
		START_FE[3:0] Start FIELD even signal 4-bit 2`s complement number controlling the start of even field output	0	0	0	0						e.g. 0x0D=FIELD starts 3 lines early, 0x05= FIELD starts 5 lines later
0x81	Reserved	Reserved	1	1	x	x	0	0	0	0	set to default	
0x82	Reserved	Reserved	0	0	0	0	0	1	0	0	set to default	
0x83	CP MEASURE CONTROL 3	**ISD_THR[7:0]** ISD Threshold Value. 8-bit number that controls the slice level.	0	0	0	0	0	0	0	0		When set to 0h slice level will be calculated automatically
0x84	CP MEASURE CONTROL 4	**ISFD_AVG** ISD Averaging selection								0	Average over 128 lines	ISD[8:0] is averaged to generate IFSD[8:0]
										1	Average over 256 lines	
		Reserved					1	1	0			
		CP_GAIN_FILT[3:0]	0	0	0	0					No Filtering i.e. Coeffficient A = 1	Functional only when manual gain is enabled
			0	0	0	1					Coefficient A = 1/128 Lines	
			0	0	1	0					Coefficient A = 1/256 Lines	
			0	0	1	1					Coefficient A = 1/512 Lines	
			0	1	0	0					Coefficient A = 1/1024 Lines	
			0	1	0	1					Coefficient A = 1/2048 Lines	
			0	1	1	0					Coefficient A = 1/4096 Lines	
			0	1	1	1					Coefficient A = 1/8192 Lines	
			1	0	0	0					Coefficient A = 1/16K Lines	
			1	0	0	1					Coefficient A = 1/32K Lines	
			1	0	1	0					Coefficient A = 1/64K Lines	
			1	0	1	1					Coefficient A = 1/128K Lines	
			1	1	0	0					Reserved	
			~	~	~	~					Reserved	
			1	1	1	1					Reserved	
0x85	CP DETECTION CONTROL 1	**DS_OUT** digital sync output enable								0	output asynchronous VS / asynchronous HS	
										1	output synchronous VS / asynchronous CS	
		SSPD_CONT sync source and polarity detector continuous mode							0		one shot triggered by TRIG_SSPD	
									1		Detector in continous mode	
		TRIG_SSPD trigger sync source and polarity detector						0			0 to 1 transition will cause SSPD block to examine sync signals	Not self clearing needs to be reset by the user
		SYN_SRC[1:0] SSPD sync source selection				0	0				Autodetect mode for sync source	
						0	1				Manual, separate HS_IN & VS_IN	
						1	0				Manual, CS on HS_IN pin	
						1	1				Manual, sync on SOG/SOG	
		POL_HSCS manual overwrite for polarity of HS SSPD			0						HS_IN pin negative polarity (HS or CS)	For this bit to be active POL_MAN_EN=1
					1						HS_IN pin positive polarity (HS or CS)	
		POL_VS manual overwrite for polarity of VS SSPD		0							VS_IN pin negative polarity	
				1							VS_IN pin positive polarity	
		POL_MAN_EN manual	0								Use result from SSPD autodetection	
			1								Use POL_VS and POL_HS	

Table 85: Register 0x86 to 0x8A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x86	CP MISC CONTROL 1	Reserved								1	Set to default	
		STDI_CONT standard identification continous							0		one shot triggered by TRIG_STDI	
									1		Detector in continous mode	
		TRIG_STDI trigger standard identification						0			0 to 1 transition triggers SDI measurement. Bit is not self clearing	
								1				
		STDI_LINE_COUNT_MODE					0				Old STDI "Sync Count" mode	Recommended to set this bit to 1
							1				New STDI "Line Count" mode	
		CPOP_INV_Crb Swap the interleaving of Cr and Cb in the output data stream				0					Output Cr & Cb interleaved	As per standard
						1					invert the order of Cr & Cb o/p	CPOP_SEL[3:0] set to 4:2:2 ouput format.
		Reserved	0	0	x						set to default	
0x87	CP TLLC CONTROL 1	PLL_DIV_RATIO[11:0] 12-bit multiplying factor that can be used in the sampling PLL										
		PLL_DIV_RATIO[11:8] see PLL_DIV_RATIO[11:0] above					0	0	1	1		
		PLL_DLL_UPD_VS_EN				0					PLL Divide Ratio and DLL Phase update immediately	
						1					PLL Divide Ration and DLL Phase update with following Vsync	
		Reserved		1	1						set to default	
		PLL_DIV_MAN_EN pll divide ratio manual enable	0								Auto-from PRIM_MODE[1:0] & VID_STD[3:0]	
			1								Use PLL_DIV_RATIO[11:0] as the multiplying factor	
0x88	CP TLLC CONTROL 2	**PLL_DIV_RATIO[7:0]** see PLL_DIV_RATIO[11:0] above	0	1	0	1	1	0	1	0		
0x89	CP TLLC CONTROL 3	Reserved					1	0	0	0	Set to Default	
		SWAP_CR_CB_WB (SDP) allows the swapping of Cr and Cb data in the wide bus modes of OF_SEL[3:0]				0					Output Cr & Cb as per OF_SEL[3:0]	NOTE: This refers to SDP output formatting
						1					Swap Cr & Cb (OF_SEL[3:0]wide bus modes)	
		Reserved	0	0	0						set to default	
0x8A	CP TLLC CONTROL 4	Reserved				1	0	0	0	0	set to default	
		VCO_RANGE[1:0] manual PLL		0	0						VCO center freq. 21Mhz . Max	For these settings to be active VCO_RANGE_MAN bit must be set to 1
				0	1						VCO center freq. 42Mhz . Max	
				1	0						VCO center freq. 85Mhz . Max	
				1	1						VCO center freq. 170Mhz . Max	
		VCO_RANGE_MAN Enable	0								Automatic VCO Range selection	
			1								PLL range from VCO_RANGE[1:0]	

Table 86: Register 0x8F to 0x9D

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x8F	Free Run Line Length 1 Write Only register	**FR_LL[10:8]** see FR_LL[[7:0] for more details (CP only modes)						0	0	0	Sets expected number of 28.63636MHz clock cycles for one line of video been processed in CP mode	
		Reserved					0				Set to default	
		LLC_PAD_SEL [2:0] enables manual selection of clock for LLC1 Pin		0	0	0					Automatic	
				1	0	1					SDP LLC2 selected (LLC1 divided by 2; nominally 13.5MHz).	
				1	1	1					Output Clock at twice data rate for data processed through the CP core only	
		Reserved	0								Set to default	
0x90	VBI info	Reserved								x		
		Reserved							x			
		Reserved						x				
		CGMSD CGMS sequence detected					0				No CGMS sequence detected	Status Bit for CGMS data detected by CP processor
							1				CGMS sequence decoded	
		Reserved	x	x	x	x						
0x90	Free Run Line Length 2 Write Only Register	**FR_LL[7:0]** Free Run Line length Expected number of	0	0	0	0	0	0	0	0		
0x91	DPP_CP_64 Write Only register	Reserved			0	1	0	0	0	0		
		Interlaced		0							Process 1080p / 1250p (@ 25 / 30Hz)	
				1							Process 1080i / 1250i	
		Reserved	0									
0x96	CGMS1[7:0] CGMS data register. Read Only Register	**CGMS1[7:0]**	x	x	x	x	x	x	x	x		
0x97	CGMS2[7:0] CGMS data register. Read Only Register	**CGMS2[7:0]**	x	x	x	x	x	x	x	x		
0x98	CGMS3[7:0] CGMS data register. Read Only Register	**CGMS3[7:0]**	x	x	x	x	x	x	x	x	CGMS3[7:4] are undetermined	
0x99	CCAP1[7:0] Closed caption data register. Read Only Register	**CCAP1[7:0]**	x	x	x	x	x	x	x	x	For VBI system 2 I2C readback - See VBI Applications note.	
0x9A	CCAP2[7:0] Closed caption data register. Read Only Register	**CCAP2[7:0]**	x	x	x	x	x	x	x	x	For VBI system 2 I2C readback - See VBI Applications note.	
0x9B	Letterbox 1 Read Only Register	**LB_LCT[7:0]**	x	x	x	x	x	x	x	x	reports number of black lines detected at top of active video	This feature examines the active video at the start and at the end of each field. It enables format detection even if the video is not accompainied by a CGMS or WSS sequence.
0x9C	Letterbox 2 Read Only Register	**LB_LCM[7:0]**	x	x	x	x	x	x	x	x	reports number of black lines detected in bottom half of active video if subtitles detected	
0x9D	Letterbox 3 Read Only Register	**LB_LCB[7:0]**	x	x	x	x	x	x	x	x	reports number of black lines detected at bottom of active video	

Table 87: Register 0xA0 to 0xAC

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xA0	RB CP AGC1 Read Only Register	CP_AGC_GAIN[9:0] feedback value of the actual gain used on channel A										
		CP_AGC_GAIN[9:8]							x	x		
		Reserved	0	0	0	0	0	0				
0xA1	RB CP AGC2 Read Only Register	**CP_AGC_GAIN[7:0]**	x	x	x	x	x	x	x	x		
0xA2	Reserved	Reserved	x	x	x	x	x	x	x	x		
0xA3	RB measure 2 Read Only Register	ISD[8:0] Hlock measurement read back										
		IFSD[8:0] Average Hlock measurement read back										
		ISD[8]								x		
		IFSD[8]							x			
		CALIB[10:0] calibration measurement feedback (average level over the extent of the window)										
		CALIB[10:8]				x	x	x				
		Reserved	0	0	0							
0xA4	RB measure 3 Read Only Register	**ISD[7:0]** see register A3h.	x	x	x	x	x	x	x	x		
0xA5	RB measure 4 Read Only Register	**IFSD[7:0]** see register A3h.	x	x	x	x	x	x	x	x		
0xA6	Reserved	Reserved	x	x	x	x	x	x	x	x		
0xA7	RB CP Hsync Dept 1 Read Only Register	HSD_CHA[9:0] Hsync depth channel A read back										
		HSD_CHB[9:0] Hsync depth channel B read back										
		HSD_CHC[9:0] Hsync depth channel read back										
		HSD_CHA[9:8]							x	x		
		HSD_CHB[9:8]					x	x				
		HSD_CHC[9:8]			x	x						
		Reserved	0	0								
0xA8	RB CP Hsync Dept 2 Read Only Register	**HSD_CHA[7:0]**	x	x	x	x	x	x	x	x		
0xA9	RB CP Hsync Dept 3 Read Only Register	**HSD_CHB[7:0]**	x	x	x	x	x	x	x	x		
0xAA	RB CP Hsync Dept 4 Read Only Register	**HSD_CHC[7:0]**	x	x	x	x	x	x	x	x		
0xAB	RB CP Hsync Dept 5 Read Only Register	HSD_FB[11:0] Hsync dept channel A read back (after gain multiplier)										
		HSD_FB[11:8]					x	x	x	x	2's complement number	
		Reserved	0	0	0	0						
0xAC	RB CP Hsync Dept 6	**HSD_FB[7:0]**	x	x	x	x	x	x	x	x		

Table 88: Register 0xAD to 0xB5

Subaddress	Register	Bit Desciption	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xAD	RB CP Peak Video 1 Read Only Register	PKV_CHA[9:0] peak video value on channel A read back										
		PKV_CHB[9:0] peak video value on channel B read back										
		PKV_CHC[9:0] peak video value on channel C read back										
		PKV_CHA[9:8]							x	x		
		PKV_CHB[9:8]					x	x				
		PKV_CHC[9:8]			x	x						
		Reserved	0	0								
0xAE	RB CP Peak Video 2 Read Only Register	**PKV_CHA[7:0]**	x	x	x	x	x	x	x	x		
0xAF	RB CP Peak Video 3 Read Only Register	**PKV_CHB[7:0]**	x	x	x	x	x	x	x	x		
0xB0	RB CP Peak Video 4 Read Only Register	**PKV_CHC[7:0]**	x	x	x	x	x	x	x	x		
0xB1	RB Standard Ident 1 Read Only Register	BL[13:0] block length readback, number of 27Mhz cycles in a block of 8 lines of input video										
		BL[13:8]			x	x	x	x	x	x		
		STDI_INTLCD		0							Non-Interlaced standard detected	
				1							Interlaced I/P standard detected	
		STDI_DVALID standard identification data valid read back. Indicates that the measurements in the STDI block are finished	0								BL, SCVS and SCF not valid	
			1								Valid BL, SCVS and SCF parameters	
0xB2	RB Standard Ident 2 Write Only Register	Reserved							0	0	Set as default	See CGMSD Address 90h, and CGMS1/2/3 Address 96h, 97h, 98h
		CRC_ENABLE Enable CRC						0			Turn off CRC check.	
								1			CGMSD goes high with valid	
		Reserved	0	0	0	1	1				Set as default	
0xB2	RB Standard Ident 2 Read Only Register	**BL[7:0]**	x	x	x	x	x	x	x	x		
0xB3	DPP_CP_98 Write Only Register	**CP_F_RUN_TH[2:0]** CP Free Run Threshold.						1	0	0	Default threshold	
		Reserved	0	1	0	1	0					
0xB3	RB Standard Ident 3 Read Only Register	LCF[10:0] Number of lines in field. SCF[10:0] Number of lines between two Vsyncs										For SCF & SCVS readback, STDI_LINE_COUNT (bit 3, 0x86) = 0 For LCF & LCVS readback, STDI_LINE_COUNT (bit 3, 0x86) = 1
		LCVS[4:0] Number of lines in a Vsync period. SCVS[4:0] Number of sync type pulses in a Vsync period.										
		SCF \ LCF[10:8]						x	x	x		
		SCVS \ LCVS[4:0]	x	x	x	x	x					
0xB4	RB Standard Ident 4 Read Only Register	**SCF \ LCF[7:0]**	x	x	x	x	x	x	x	x		
0xB5	RB Standard Ident 5	**CUR_SYNC[1:0]** current sync source selection SSPD read back							0	0	Invalid	
									0	1	Separate HS and VS sync on pins	
									1	0	Externl CS sync on HS_IN pin	
									1	1	Embedded SOG/SOY	
		Reserved						x				
		CUR_POL_HS currently detected polarity of HS_IN SSPD (CP)					1				HS_IN pin -negative polarity signal	
							0				HS_IN pin -positive polarity signal	
		HS_ACT activity of HS_IN SSPD (CP)				1					No activity detected	
						0					HS_IN pin carries an active signal	
		CUR_POL_VS currently detected polarity of VS SSPD (CP)			1						VS_IN pin -negative polarity signal	
					0						VS_IN pin -positive polarity signal	
		VS_ACT activity of VS _IN SSPD (CP)		1							No activity detected	
				0							HS_IN pin carries an active signal	
		SSPD_DVALID Valid Read back values	1								SSPD results not valid for read back	
			0								SSPD results valid	

Table 89: Register 0xBF to 0xC4

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xBF	CP DEF COL 1	**CP_DEF_COL_FORCE** Force output of default colours								0	Do not force default colour output	
										1	Force default colour output	Overwrite video data
		CP_DEF_COL_AUTO Automatic output of default							0		Disable auto insertion of default	
									1		Output default colours	When sync is lost
		CP_DEF_COL_MAN_VAL Enable manual selection of default colours						0			Use default colour blue	
								1			Output user programmable value	CP_DEF_COL_CHA/B/C[7:0]
		Reserved	x	x	x	x	x					
0xC0	CP DEF COL 2	**DEF_COL_CHA[7:0]** Manual default colour channel A	x	x	x	x	x	x	x	x		
0xC1	CP DEF COL 3	**DEF_COL_CHB[7:0]** Manual default colour channel B	x	x	x	x	x	x	x	x		
0xC2	CP DEF COL 4	**DEF_COL_CHC[7:0]** Manual default colour channel C	x	x	x	x	x	x	x	x		
0xC3	ADC SWITCH 1	**ADC0_SW[3:0]** Manual muxing control for ADC0					0	0	0	0	No connection	SETADC_sw_man_en = 1
							0	0	0	1	Ain1	
							0	0	1	0	Ain2	
							0	0	1	1	No connection	
							0	1	0	0	Ain4	
							0	1	0	1	Ain5	
							0	1	1	0	Ain6	
							0	1	1	1	No connection	
							1	0	0	0	No connection	
							1	0	0	1	No connection	
							1	0	1	0	No connection	
							1	0	1	1	No connection	
							1	1	0	0	Ain3	
							1	1	0	1	No connection	
							1	1	1	0	No connection	
							1	1	1	1	No connection	
		ADC1_SW[3:0] Manual muxing control for ADC1	0	0	0	0					No connection	
			0	0	0	1					No connection	
			0	0	1	0					No connection	
			0	0	1	1					No connection	
			0	1	0	0					Ain4	
			0	1	0	1					Ain5	
			0	1	1	0					Ain6	
			0	1	1	1					No connection	
			1	0	0	0					No connection	
			1	0	0	1					No connection	
			1	0	1	0					No connection	
			1	0	1	1					No connection	
			1	1	0	0					Ain3	
			1	1	0	1					No connection	
			1	1	1	0					No connection	
			1	1	1	1					No connection	
0xC4	ADC SWITCH 2	**ADC2_SW[3:0]** Manual muxing control for ADC2					0	0	0	0	No connection	SETADC_sw_man_en = 1
							0	0	0	1	No connection	
							0	0	1	0	Ain2	
							0	0	1	1	No connection	
							0	1	0	0	Ain 4	
							0	1	0	1	Ain5	
							0	1	1	0	Ain6	
							0	1	1	1	No connection	
							1	0	0	0	No connection	
							1	0	0	1	No connection	
							1	0	1	0	No connection	
							1	0	1	1	No connection	
							1	1	0	0	No connection	
							1	1	0	1	No connection	
							1	1	1	0	No connection	
							1	1	1	1	No connection	
		Reserved			x	x						
		SOG_SEL Selects the routing of the analogue sync stripper		0							Sync stripper connected to SOY/SOG	
		ADC_SW_MAN _EN Enable manual setting of the input signal muxing	0								Disable	
			1								Enable	

Table 90: Register 0xC5 to 0xE4

Subaddres	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xC5	Clamp Averaging	Reserved			x	x	x	0	0	1	Set to Default	
		CP Clamp Average Factor	0	0							No Averaging	
			0	1							Averaging with A =1/8	
			1	0							Averaging with A =1/16	default
			1	1							Averaging with A =1/32	
0xC6 to 0xC8	Reserved	Reserved										
0xC9	DDR Mode	**DPP_CP_BYPASS**								0		Set to 0 for analogue processing
		DDS_DIN_CLK_EN							0		DLL input clock same as ADC clock	Set to 0 for analogue processing
		DDR_I2C_RC_FIRST						0			Red component out Last	12 bit DDR mode
								1			Red component out first	
		DDR_EN					0				DDR Mode Disabled	
							1				DDR Mode Enabled	
		Reserved	0	0	0	0					Set to Default	
0xCA	Field Length Count 1 Read Only Register	FCL[12:0] The number of 27MHz clock cycles between sucessive VSYNCS										
		FCL[12:8] See FCL[12:0] above				x	x	x	x	x		
		Reserved	x	x	x							
0xCB	Field Length Count 2 Read Only Register	**FCL[7:0]** See FCL[12:0] above	x	x	x	x	x	x	x	x		
0xCC to 0xDB	Reserved	Reserved										
0xDC	Letterbox Contorl 1	**LB_TH [4:0]** Set the threshold value which will detect a black				0	1	1	0	0	Default threshold for detection of black lines.	
		Reserved	1	0	1						Set as default	
0xDD	Letterbox Control 2	**LB_EL[3:0]** programme the end line of the activity window for LB detection (end of field).					1	1	0	0	LB detection ends with last line of active video on a field. 1100: 262/525	
		LB_SL[3:0] programme the start line of the activity window for LB detection (start of field).	0	1	0	0					Letterbox detection aligned with start of active video. 0100: 23/286 NTSC	
0xDE	ST Noise Readback 1 Read Only Register	ST_NOISE[10:0] Noise measurement.										
		ST_NOISE[10:8] See ST_NOISE[10:0] above						x	x	x		
		ST_NOISE_VLD					x				1 = ST[Noise[10:0] measurement is valid	
		Reserved	x	x	x	x						
0xDF	ST Noise Readback 2 Read Only Register	**ST_NOISE[7:0]** See ST_NOISE[10:0] above	x	x	x	x	x	x	x	x		
0xE0	Reserved	Reserved	0	0	0	1	0	1	0	0		
0xE1	SD Offset Cb	**SD_OFF_CB [7:0]** adjust hue by selecting offset for Cb channel	1	0	0	0	0	0	0	0		
0xE2	SD Offset Cr	**SD_OFF_CR [7:0]** adjust hue by selecting offset for Cr channel	1	0	0	0	0	0	0	0		
0xE3	SD Saturation Cb	**SD_SAT_CB [7:0]** adjust saturation of picture by affecting gain on Cb channel	1	0	0	0	0	0	0	0	Chroma gain =0dB	
0xE4	SD Saturation Cr	**SD_SAT_CR [7:0]** adjust saturation of picture by affecting gain on Cr channel	1	0	0	0	0	0	0	0	Chroma gain =0dB	

Table 91: Register 0xE5 to 0xEA

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xE5	NTSC V bit begin	**NVBEG[4:0]** how many lines after lcount rollover to set V high				0	0	1	0	1	NTSC Default (BT.656)	
		NVBEGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NVBEGDELE Delay V bit going high by one line relative to NVBEG (even field)		0							No delay	
				1							Additional delay by 1 line	
		NVBEGDELO Delay V bit going high by one line relative to NVBEG (odd field)	0								No delay	
			1								Additional delay by 1 line	
0xE6	NTSC V bit end	**NVEND[4:0]** how many lines after lcount rollover to set V low				0	0	1	0	0	NTSC Default (BT.656)	
		NVENDSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NVENDDELE Delay V bit going low by one line relative to NVEND (even field)		0							No delay	
				1							Additional delay by 1 line	
		NVENDDELO Delay V bit going low by one line relative to NVEND (odd field)	0								No delay	
			1								Additional delay by 1 line	
0xE7	NTSC F bit toggle	**NFTOG[4:0]** how many lines after lcount rollover to toggle F signal				0	0	0	1	1	NTSC Default (BT.656)	
		NFTOGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NFTOGDELE Delay F transition by one line relative to NFTOG (even field)		0							No delay	
				1							Additional delay by 1 line	
		NFTOGDELO Delay F transition by one line relative to NFTOG (odd field)	0								No delay	
			1								Additional delay by 1 line	
0xE8	PAL V bit begin	**PVBEG[4:0]** how many lines after lcount rollover to set V high										
						0	0	1	0	1	PAL Default (BT.656)	
		PVBEGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PVBEGDELE Delay V bit going high by one line relative to PVBEG (even field)		0							No delay	
				1							Additional delay by 1 line	
		PVBEGDELO Delay V bit going high by one line relative to PVBEG (odd field)	0								No delay	
			1								Additional delay by 1 line	
0xE9	PAL V bit end	**PVEND[4:0]** how many lines after lcount rollover to set V low				1	0	1	0	0	PAL Default (BT.656)	
		PVENDSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PVENDDELE Delay V bit going low by one line relative to PVEND (even field)		0							No delay	
				1							Additional delay by 1 line	
		PVENDDELO Delay V bit going low by one line relative to PVEND (odd field)	0								No delay	
			1								Additional delay by 1 line	
0xEA	PAL F bit toggle	**PFTOG[4:0]** how many lines after lcount rollover to toggle F signal				0	0	0	1	1	PAL Default (BT.656)	
		PFTOGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PFTOGDELE Delay F transition by one line relative to PFTOG (even field)		0							No delay	
				1							Additional delay by 1 line	
		PFTOGDELO Delay F transition by one line relative to PFTOG (odd field)	0								No delay	
			1								Additional delay by 1 line	

Table 92: Register 0xEB to 0xEC

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xEB	V Blank Control 1	**PVBIELCM[1:0]** PAL VBI Even Field Line Control							0	0	VBI ends 1 line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on Even field in **PAL**
									0	1	ITU-R BT.470 Compliant(Line 336)	
									1	0	VBI ends 1 line later (Line 337)	
									1	1	VBI ends 2 lines later (Line 338)	
		PVBIOLCM[1:0] PAL VBI Odd Field Line Control					0	0			VBI ends 1 line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on Odd field in **PAL**
							0	1			ITU-R BT.470 Compliant (Line23)	
							1	0			VBI ends 1 line later (Line 24)	
							1	1			VBI ends 2 lines later (Line 25)	
		NVBIELCM[1:0] NTSC VBI Even Field Line Control			0	0					VBI ends 1 line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on Even field in **NTSC.**
					0	1					ITU-R BT.470 Compliant (Line 283)	
					1	0					VBI ends 1 line later (Line 284)	
					1	1					VBI ends 2 lines later (Line 285)	
		NVBIOLCM[1:0] NTSC VBI Odd Field Line Control	0	0							VBI ends 1 line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on Odd field in **NTSC.**
			0	1							ITU-R BT.470 Compliant (Line21)	
			1	0							VBI ends 1 line later (Line 22)	
			1	1							VBI ends 2 lines later (Line 23)	
0xEC	V Blank Control 2	**PVBIECCM[1:0]** PAL VBI Even field Colour control							0	0	Colour output beginning line 335	Controls the position of first line which outputs colour after VBI on Even Field in **PAL**
									0	1	Colour output beginning line 336 ITU-R BT470 Compliant	
									1	0	Colour output beginning line 337	
									1	1	Colour output beginning line 338	
		PVBIOCCM[1:0] PAL VBI Odd field Colour control					0	0			Colour output beginning line 22	Controls the position of first line which outputs colour after VBI on Odd Field in **PAL**
							0	1			Colour output beginning line 23 ITU-R BT470 Compliant	
							1	0			Colour output beginning line 24	
							1	1			Colour output beginning line 25	
		NVBIECCM[1:0] NTSC VBI Even Field Colour Control			0	0					Colour output beginnng line 282	Controls the position of first line which outputs colour after VBI on Even Field in **NTSC**
					0	1					Colour output beginning line 283 ITU-R BT470 compliant	
					1	0					Colour output beginning line 284	
					1	1					Colour output beginning line 285	
		NVBIOCCM[1:0] NTSC VBI Odd Field Colour Control	0	0							Colour output beginnng line 20	Controls the position of first line which outputs colour after VBI on Odd Field in **NTSC**
			0	1							Colour output beginning line 21 ITU-R BT470 compliant	
			1	0							Colour output beginning line 22	
			1	1							Colour output beginning line 23	

Table 93: Register 0xED to 0xF1

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xED	FB_CONTROL 1 Write Only register	**FB_MODE[1:0]** PAL VBI Even field Colour control							0	0	Static Switch mode - Full RGB or Full CVBS data	
									0	1	Fixed Alpha Blending - See MAN_ALPHA_VAL[6:0]	
									1	0	Dynamic Switching (Fast Mux)	
									1	1	Dynamic Switching with edge enhancement	
		CVBS_RGB_SEL						0			CVBS Source	Selects either CVBS or RGB to be O/P
								1			RGB Source	
		FB_INV					0				FB pin active High	
							1				FB pin active Low	
		Reserved	0	0	0	1						
0xED	FB_STATUS Read Only register	Reserved					x	x	x	x		
		FB_STATUS[3:0] Provides information on the status of the FB pin										
		FB_STATUS[0]				x					FB_RISE, 1 = there has beeen a rising edge on FB pin since last I2C read	Self clearing bit
		FB_STATUS[1]			x						FB_FALL, 1 = there has been a falling edge on FB pin since last I2C read	Self clearing bit
		FB_STATUS[2]		x							FB_STAT, Instantaneous value of FB signal at time if I2C read	
		FB_STATUS[3]	x								FB_HIGH, Indicates that the FB signal gas gone high since the last read of this register	Self clearing bit
0xEE	FB_CONTROL 2	**MAN_ALPHA_VAL[6:0]** Determines in what proportion the video from the CVBS source and the RGB source are blended		0	0	0	0	0	0	0	0d = 100% CVBS signal 32d = 50% CVBS, 50% RGB 64d = 100% RGB	FB_MODE[1:0] = 01b (Fixed alpha blending selected)
		FB_CSC_MAN	0								Automatic configuration of the CSC for SCART support	CSC is used to convert RGB porion of SCART signal to YCrCb
			1								Enable manual programming of CSC	
0xEF	FB_CONTROL 3	**FB_EDGE_SHAPE[2:0]**						0	0	0	No Edge Shaping	Improves picture transition for high speed fast blank switching
								0	0	1	Level 1 Edge Shaping	
								0	1	0	Level 2 Edge Shaping	
								0	1	1	Level 3 Edge Shaping	
								1	0	0	Level 4 Edge Shaping	
		CNTR_ENABLE					0				Contrast Reduction mode disabled, FB signal is interpreted as a binary	
							1				Contrast Reduction mode enabled, FB signal is interpreted as a tri-level	
		FB_SP_ADJUST[3:0]	0	1	0	0					Adjusts FB timing in reference to the sampling clock	Each LSB corresponds to 1/8 of an ADC clock cycle
0xF0	FB_CONTROL 4	**FB_DELAY[3:0]**					0	1	0	0	Delay on FB signal in 27MHz clock cycles	
		Reserved	0	1	0	0						
0xF1	FB_CONTROL 5	**RGB_IP_SEL**								0	Reserved	
										1	SD RGB input for FB on AIN4, AIN5 and AIN6	
		Reserved							0		Set tozero	
		CNTR_MODE[1:0] Allows adjustment of contrast level in the contrast reduction box					0	0			25%	
							0	1			50%	
							1	0			75%	
							1	1			100%	
		FB_LEVEL[1:0] Controls Reference Level for Fast Blank Comparator			0	0					CR_ENABLE = 0, FB Threshold = 1.4V; CR_ENABLE = 1, FB Threshold = 1.6V	
					0	1					CR_ENABLE = 0, FB Threshold = 1.6V; CR_ENABLE = 1, FB Threshold = 1.8V	
					1	0					CR_ENABLE = 0, FB Threshold = 1.8V; CR_ENABLE = 1, FB Threshold = 2.0V	
					1	1					CR_ENABLE = 0, FB Threshold = 2.0V; CR_ENABLE = 1, FB Threshold = Not Used	
		CNTR_LEVEL[1:0] Controls Reference Level for Contrast Reduction Comparator	0	0							0.4V Contrast reduction level	CR_Enable = 1
			1	0							0.6V Contrast reduction level	
			1	0							0.8V Contrast reduction level	
			1	1							Not used	

Table 94: Register 0xF3 to 0xF8

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xF3	AFE_CONTROL 1	**AA_FILT_EN[0]**								0	Disables the internal anti-aliasing filter on channel 0	
										1	Enables the internal anti-aliasing filter on channel 0	
		AA_FILT_EN[1]							0		Disables the internal anti-aliasing filter on channel 1	
									1		Enables the internal anti-aliasing filter on channel 1	
		AA_FILT_EN[2]						0			Disables the internal anti-aliasing filter on channel 2	
								1			Enables the internal anti-aliasing filter on channel 2	
		AA_FILT_EN[3]					0				Disables the internal anti-aliasing filter on channel 3	
							1				Enables the internal anti-aliasing filter on channel 3	
		ADC3_SW[3:0] manual muxing	0	0	0	0					No connection	
			0	0	0	1					No connection	
			0	0	1	0					No connection	
			0	0	1	1					No connection	
			0	1	0	0					Ain4	
			0	1	0	1					No connection	
			0	1	1	0					No connection	
			0	1	1	1					No connection	
			1	0	0	0					No connection	
			1	0	0	1					Ain7	
			1	0	1	0					No connection	
			1	0	1	1					No connection	
			1	1	0	0					No connection	
			1	1	0	1					No connection	
			1	1	1	0					No connection	
			1	1	1	1					No connection	
0xF4	Drive Strength	**DR_STR_S[1:0]** Select the drive strength of the sync signals HS,VS and F, can be increased or decreased for EMC or cross-talk							0	0	low drive strength (1x)	
									0	1	medium low (2x)	
									1	0	medium high (3x)	
									1	1	high drive strength (4x)	
		DR_STR_C[1:0] Select the strength of the clock signal output driver, can be increased or decreased for EMC or cross-talk					0	0			low drive strength (1x)	
							0	1			medium low (2x)	
							1	0			medium high (3x)	
							1	1			high drive strength (4x)	
		DR_STR[1:0] Drive Strength of data output drivers. Can be increased or decreased for EMC or cross-talk reasons.			0	0					Low Drive 1X	
					0	1					Medium Low 2X	Recommended
					1	0					Medium High 3X	
					1	1					High Drive 4X	
		Reserved	x	x							Set to Default	
0xF5 to 0xF7	Reserved	Reserved										
0xF8	IF Filter	**IFFILTERSEL.0[2:0]** IF Filter Selection for PAL and NTSC						0	0	0	Bypass Mode, 0dB	
											2MHz **5MHz**	NTSC Filters
								0	0	1	-3dB +2dB	
								0	1	0	-6dB +3.5dB	
								0	1	1	-10dB +5dB	
								1	0	0	x	
											3MHz **6MHz**	PAL Filters
								1	0	1	-2dB +2dB	
								1	1	0	-5dB +3dB	
								1	1	1	-7dB +5dB	
		Reserved	0	0	0	0	0					

Table 95: Register 0xF9 to 0xFC

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0xF9	VS Mode Control	**EXTEND_VS_MAX_FREQ**								0	Limit Maximum Vsync frequency to 66.25Hz (475 lines/frame)	
										1	Limit Maximum Vsync frequency to 70.09Hz (449 lines/frame)	
		EXTEND_VS_MIN_FREQ							0		Limit Minimum Vsync frequency to 42.75Hz (731 lines/frame)	
									1		Limit Minimum Vsync frequency to 39.51Hz (791 lines/frame)	
		VS_COAST_MODE[1:0]					0	0			Auto Coast Mode	This value sets up the output coast frequency for the SDP
							0	1			50Hz Coast Mode	
							1	0			60Hz Coast Mode	
							1	1			Reserved	
		Reserved	0	0	0	0						
0xFA	Reserved	Reserved										
0xFB	Peaking Control	**PEAKING_GAIN[7:0]** Increases / decreses the gain for high frequency portions of the video signal	0	1	0	0	0	0	0	0		
0xFC	Coring Threshold 2	**DNR_TH2[7:0]**	0	0	0	0	0	1	0	0	specifies the max. edge that will be interpreted as noise and therefore blanked	

11.6 I^{2}C Interrupt System

The ADV7181C has a comprehensive interrupt register set. This map is located in the User Sub Map. Access to this map is described in Figure 77.

11.6.1 Interrupt Request Output Operation

When an interrupt event occurs, the interrupt pin $\overline{\text{INT}}$ goes low with a programmable duration given by INT_DUR_SEL[1:0]

Table 96: INT_DUR_SEL[1:0] *Address 0x40 [7:6]*

Interrupt Duration Select INT_DURSEL[1:0]	**Interrupt Active Duration**	**Note**
00	3 Xtal Periods	Default
01	15 Xtal Periods	
10	63 Xtal Periods	
11	Active until cleared	

Note: When the Active until cleared interrupt duration is selected and the event that caused the interrupt is no longer in force, the interrupt persists until it is masked or cleared.

Example: If the SDP core loses lock, an interrupt is generated and $\overline{\text{INT}}$ pin goes low. If the SDP core returns to the locked state, $\overline{\text{INT}}$ continues to drive low until the SD_LOCK bit is either masked or cleared.

11.6.2 Interrupt Drive Level

Table 97: INT_OP_SEL[1:0] *Address 0x40 [1:0]*

Interrupt Output Select INT_OP_SEL[1:0]	**$\overline{\text{INT}}$ Functionality**	**Note**
00	Open Drain	Default
01	Drive low when active	
10	Drive high when active	
11	Reserved	

The ADV7181C resets with Open Drain enabled and all interrupts masked off. Therefore $\overline{\text{INT}}$ will be in a high impedance state after reset.

01 or 10 has to be written to INT_OP_SEL[1:0] for a logic level to be driven out from the $\overline{\text{INT}}$ pin.

It is also possible to write to a register in the ADV7181C, which manually asserts the $\overline{\text{INT}}$ pin. This bit is MPU_STIM_INT.

11.6.3 Multiple Interrupt Events

If interrupt event 1 occurs and then interrupt event 2 occurs before the system controller has cleared or masked interrupt event 1, the ADV7181C does not generate a second interrupt signal. The system controller should check all unmasked interrupt status bits as more than one may be active.

11.6.4 Macrovision Interrupt Selection Bits

The user can select between Pseudo sync pulse and Color Stripe detection as shown in Table 98.

Table 98: MV_INT_SEL[1:0] *Address 0x40 [5:4]*

Macrovision Interrupt Select MV_INT_SEL[1:0]	**Macrovision Interrupt Event**	**Note**
00	Reserved	
01	Pseudo Sync Only	Default
10	Color Stripe Only	
11	Either Pseudo sync or Color Stripe	

Additional information relating to the interrupt system is detailed in Table 99, Table 100, Table 100, and Table 101.

11.7 User Sub Map (I^{2}C Interrupt and VDP Register Map)

Note: The following registers are located in the User Sub Map 1 (refer to Table 60)

Table 99: Register 0x40 to 0x43

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x40	Interrupt configuration 0	**INT_OP_SEL[1:0]**							0	0	Open Drain	
									0	1	Drive Low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		MPU_STIM_INT						0			Manual Interrupt Mode disabled	
								1			Manual Interrupt Mode enabled	
		Not used					x				Not used	
		MV_INT_SEL[1:0]			0	0					Reserved	
					0	1					Pseudo Sync Only	
					1	0					Color Stripe Only	
					1	1					Pseudo Sync or Colour Stripe	
		INT_DUR_SEL[1:0]	0	0							3 Xtal Periods	
			0	1							15 Xtal Periods	
			1	0							63 Xtal Periods	
			1	1							Active until cleared	
0x42	Interrupt Status 1	**SD_LOCK_Q**								0	No change	These Bits can be cleared or masked in Registers 43h and
										1	SD Input has caused the Decoder to go from an unlocked state to a locked state	
		SD UNLOCK_Q							0		No change	
									1		SD Input has caused the Decoder to go from a locked state to an unlocked state	
		CP_LOCK_Q						0			No change	
								1			CP Input has caused the Decoder to go from an unlocked state to a locked state	
		CP_UNLOCK_Q					0				No change	
							1				CP Input has caused the Decoder to go from a locked state to an unlocked state	
		STDI_DVALID_Q				0					No change	
						1					The STDI Valid has changed state.	
		SD_FR_CHNG_Q			0						No change	
					1						Denotes a change in the Free run status.	
		MV_PS_CS_Q		0							No change	
				1							Pseudo sync / Color striping detected. See Reg 40h MV_INT_SEL[1:0] for selection	
		Not used	x								Not used	
0x43	Interrupt Clear 1	**SD_LOCK_CLR**								0	Do not Clear	
										1	Clears SD_LOCK_Q Bit	
		SD UNLOCK_CLR							0		Do not Clear	
									1		Clears SD_UNLOCK_Q Bit	
		CP_LOCK_CLR						0			Do not Clear	
								1			Clears CP_LOCK_Q Bit	
		CP_UNLOCK_CLR					0				Do not Clear	
							1				Clears CP_UNLOCK_Q Bit	
		STDI_DVALID_CLR				0					Do not Clear	
						1					Clears STDI_DVALID_Q Bit	
		SD_FR_CHNG_CLR			0						Do not Clear	
					1						Clears SD_FR_CHNG_Q Bit	
		MV_PS_CS_CLR		0							Do not Clear	
				1							Clears MV_PS_CS_Q Bit	
		Not used	x								Not used	

Table 100: Register 0x44 to 0x47

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x44	Interrupt Mask 1	**SD_LOCK_MSKB**								0	Masks SD_LOCK_Q Bit	
										1	Unmasks SD_LOCK_Q Bit	
		SD UNLOCK_MSKB							0		Masks SD_UNLOCK_Q Bit	
									1		Unmasks SD_UNLOCK_Q Bit	
		CP_LOCK_MSKB						0			Masks CP_LOCK_Q Bit	
								1			Unmasks CP_LOCK_Q Bit	
		CP_UNLOCK_MSKB					0				Masks CP_UNLOCK_Q Bit	
							1				Unmasks CP_UNLOCK_Q Bit	
		STDI_DVALID_MSKB				0					Masks STDI_DVALID_Q Bit	
						1					Unmasks STDI_DVALID_Q Bit	
		SD_FR_CHNG_MSKB			0						Masks SD_FR_CHNG_Q Bit	
					1						Unmasks SD_FR_CHNG_Q Bit	
		MV_PS_CS_MSKB		0							Masks MV_PS_CS_Q Bit	
				1							Unmasks MV_PS_CS_Q Bit	
		Not used	x								Not used	
0x45	Raw Status 2	**CCAPD**								0	No CCAPD data detected	These bits are status bits only. They **cannot** be cleared or masked.
										1	CCAPD data detected	
		Reserved					x	x	x			
		EVEN_FIELD				0					Current SD field is not EVEN	
						1					Current SD field is EVEN	
		Reserved		x	x							
		MPU_STIM_INTRQ	0								MPU_STIM_INT = 0	
			1								MPU_STIM_INT = 1	
0x46	Interrupt status 2 Read Only register	**CCAPD_Q**								0	Closed Captioning not detected in the input video signal	These bits can be cleared or masked by Registers 47h and 48h respectively Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Close Captioning data detected in the video input signal	
		GEMD_Q							0		Gemstar Data not detected in the input video signal	
									1		Gemstar data detected in the input Video signal	
		CGMS_CHNGD_Q						0			No change detected in CGMS data in the input video signal	
								1			A change in CGMS data detected in the input video Signal	
		WSS_CHNGD_Q					0				No change in WSS data detected in the input video Signal	
							1				A change in WSS data detected in the input video Signal	
		SD_FIELD_CHNGD_Q				0					SD signal has not changed Field from ODD to EVEN or vice	
						1					SD signal has changed Field from ODD to EVEN or vice vearsa	
		Not used		x	x						Not used	
		MPU_STIM_INT_Q	0								Manual interrupt not Set	
			1								Manual interrupt Set	
0x47	Interrupt Clear 2	**CCAPD_CLR**								0	Do not clear	Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Clears CCAPD_Q Bit	
		GEMD_CLR							0		Do not clear	
									1		Clears GEMD_Q Bit	
		CGMS_CHNGD_CLR						0			Do not clear	
								1			Clears CGMS_CHNGD_Q Bit	
		WSS_CHNGD_CLR					0				Do not clear	
							1				Clears WSS_CHGND_Q Bit	
		SD_FIELD_CHNGD_CLR				0					Do not clear	
						1					Clears SD_FIELD_CHNGD_Q	
		Not used		x	x						Not used	
		MPU_STIM_INT_CLR	0								Do not clear	
			1								Clears MPU_STIM_INT_Q Bit	

Table 101: Register 0x48 to 0x4B

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Note
0x48	Interrupt Mask 2	**CCAPD_MSKB**								0	Masks CCAPD_Q Bit	Note that interrupt in register 0x46 for the CCAP, Gemstar, CGMS and WSS data is using the mode 1 VBI data slicer. (i.e. not VDP)
										1	Unmasks CCAPD_Q Bit	
		GEMD_MSKB							0		Masks GEMD_Q Bit	
									1		Unmasks GEMD_Q Bit	
		CGMS_CHNGD_MSKB						0			Masks CGMS_CHNGD_Q Bit	
								1			Unmasks CGMS_CHNGD_Q Bit	
		WSS_CHNGD_MSKB					0				Masks WSS_CHGND_Q Bit	
							1				Unmasks WSS_CHGND_Q Bit	
		SD_FIELD_CHNGD_MSKB				0					Masks SD_FIELD_CHNGD_Q	
						1					Unmasks SD_FIELD_CHNGD_Q	
		Not used		x	x						Not used	
		MPU_STIM_INT_MSKB	0								Masks MPU_STIM_INT_Q Bit	
			1								Unmasks MPU_STIM_INT_Q Bit	
0x49	Raw Status 3 Read Only register User Sub Map	**SD_OP_50Hz**								0	SD 60Hz signal detected at the Output	These bits **cannot** be cleared or masked. Register 4Ah is used for this purpose
										1	SD 50Hz signal detected at the Output	
		SD_V_LOCK							0		SD Vertical sync Lock not established	
									1		SD Vertical sync Lock established	
		SD_H_LOCK						0			SD Horizontal sync lock not established	
								1			SD Horizontal sync Lock established	
		Not used					x				Not used	
		SCM_LOCK Secam Lock				0					SECAM Lock not established	
						1					SECAM Lock established	
		Not used	x	x	x						Not used	
0x4A	Interrupt status 3 Read only register User Sub Map	**SD_OP_CHNGD_Q** SD 60/50Hz frame rate at output								0	No change in SD Signal standard detected	Can be used in blue screen mode. Tells the user what standard is being o/p These bits can be cleared and Masked by register 4Bh and 4Ch respectively
										1	A change of SD signal standard has been detected	
		SD_V_LOCK_CHNG_Q							0		SD Vertical sync lock not established	
									1		SD Vertical sync Lock established	
		SD_H_LOCK_CHNG_Q						0			SD Horizontal sync lock not established	
								1			SD Horizontal sync Lock established	
		SD_AD_CHNG_Q					0				No change in **AD_RESULT[2:0]** Bits in STATUS 1 register	
							1				**AD_RESULT[2:0]** Bits in STATUS 1 register has changed	
		SCM_LOCK_CHNG_Q				0					No change in SECAM lock status	
						1					SECAM Lock status has changed	
		PAL_SW_LK_CHNG_Q			0						No change in PAL Swinging Burst lock status	
					1						PAL Swinging Burst lock status has changed	
		Not used	x	x							Not used	
0x4B	Interrupt Clear 3 Write only register User Sub Map	**SD_OP_CHNG_CLR**								0	Do not Clear	
										1	Clear SD_OP_CHNG_Q Bit	
		SD_V_LOCK_CHNG_CLR							0		Do not Clear	
									1		Clear SD_V_LOCK_CHNG_Q	
		SD_H_LOCK_CHNG_CLR						0			Do not Clear	
								1			Clear SD_H_LOCK_Q Bit	
		SD_AD_CHNG_CLR					0				Do not Clear	
							1				Clear SD_AD_CHNG_Q Bit	
		SCM_LOCK_CHNG_CLR				0					Do not Clear	
						1					Clear SCM_LOCK_CHNG_Q	
		PAL_SW_LK_CHNG_CLR			0						Do not Clear	
					1						Clear PAL_SW_LK_CHNG_Q	
		Not used	x	x							Not used	

Table 102: Register 0x4C to 0x50

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x4C	Interrupt Mask 2 Read/Write register User Sub Map	**SD_OP_CHNGD_MSKB**								0	Mask SD_OP_CHNGD Bit	
										1	Unmask SD_OP_CHNGD Bit	
		SD_V_LOCK_MSKB							0		Mask V_LOCK Bit	
									1		Unmask V_LOCK Bit	
		SD_H_LOCK						0			Mask SD_H_LOCK Bit	
								1			Unmask SD_H_LOCK Bit	
		SD_AD_CHNGD_MSKB					0				Mask SD_AD_CHNGD Bit	
							1				Unmask SD_AD_CHNGD Bit	
		SCM_LOCK_CHNG_MSKB				0					Mask SCM_LOCK_CHNG	
						1					Unmask SCM_LOCK_CHNG	
		PAL_SW_LK_CHNG_MSKB			0						Mask PAL_SW_LK_CHNG bit	
					1						Unmask PAL_SW_LK_CHNG bit	
		Not used	x	x							Not used	
0x4E	Interrupt Status 4 Read-Only Register User Sub Map	**VDP_CCAPD_Q**								0	Closed Captioning not detected	These bits can be cleared and masked / unmasked by registers 0x4F and 0x50 respectively. Note that the interrupt signals in 0x4E are using the VDP VBI dataslicer
										1	Closed Captioning detected	
		Reserved							x		Not used	
		VDP_CGMS_WSS_CHNGD_Q Please see 0x9C bit 4 (User Sub Map) to determine if interrupt is issued for a change in detected data or for when data is detected regardless of content						0			CGMS / WSS data is not changed / not available	
								1			CGMS / WSS data is changed / available	
		Reserved					x				Not used	
		VDP_GS_VPS_PDC_UTC_CHNGD_Q Please see 0x9C bit 5 (User Sub Map) to determine if interrupt is issued for a change in detected data or for when data is detected regardless of content				0					GemStar / PDC / VPS / UTC data is not changed / not available	
						1					GemStar / PDC / VPS / UTC data is changed / available	
		Reserved			x						Not used	
		VDP_CCAPD_Q		0							VITC data is not available	
				1							VITC data is available	
		Reserved	x								Not used	
0x4F	Interrupt clear 4 Read only register User Sub Map	**VDP_CCAPD_CLR**								0	Do not Clear	
										1	Clears VDP_CCAPD_Q	
		Reserved							x		Not used	
		VDP_CGMS_WSS_CHNGD_CLR									Do not Clear	
								0			Clears VDP_CGMS_WSS_CHNGD_Q	
		Reserved						1			Not used	
		VDP_GS_VPS_PDC_UTC_CHNGD_CLR				0					Do not Clear	
						1					Clears VDP_GS_VPS_PDC_UTC_CHNGD_Q	
		Reserved			x						Not used	
		VDP_VITC_CLR		0							Do not Clear	
				1							Clears VDP_VITC_Q	
		Reserved	x								Not used	
0x50	Interrupt Mask 4 Write only register User Sub Map	**VDP_CCAPD_MSKB**								0	Masks VDP_CCAPD_Q	
										1	Unmasks VDP_CCAPD_Q	
		Reserved							0		Not used	
		VDP_CGMS_WSS_CHNGD_MSKB							1		Masks VDP_CGMS_WSS_CHNGD_Q	
								0			Unmasks VDP_CGMS_WSS_CHNGD_Q	
		Reserved						1			Not used	
		VDP_GS_VPS_PDC_UTC_CHNGD_MSKB					0				Masks VDP_GS_VPS_PDC_UTC_CHNGD_Q	
							1				Unmasks VDP_GS_VPS_PDC_UTC_CHNGD_Q	
		Reserved				0					Not used	
		VDP_VITC_MSKB				1					Masks VDP_VITC_Q	
					0						Unmasks VDP_VITC_Q	
		Reserved			1						Not used	

Table 103: Register 0x60 to 0x66

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x60	VDP_Config_1 Read/Write register User Sub Map	**VDP_TTXT_TYPE_MAN[1:0]**							0	0	PAL: TeleText-ITU-BT.656-625/50-A NTSC: Reserved	
									0	1	PAL: TeleText-ITU-BT.656-625/50-B(WST) NTSC: TeleText-ITU-BT.656-525/60-B	
									1	0	PAL: TeleText-ITU-BT.656-625/50-C NTSC: TeleText-ITU-BT.656-525/60-C OR EIA516 (NABTS)	
									1	1	PAL: TeleText-ITU-BT.656-625/50-D NTSC: TeleText-ITU-BT.656-525/60-D	
		VDP_TTXT_TYPE_MAN_ENABLE						0			User Programming of TeleText type disabled	
								1			User Programming of TeleText type enabled	
		Reserved	1	0	0	0	1					
0x61	VDP_Config_2 Read/Write register User Sub Map	Reserved					x	x	0	0		
		AUTO_DETECT_GS_TYPE				0					Disable Autodetection of GemStar Type	
						1					Enable Autodetection of GemStar Type	
		Reserved	0	0	0							
0x62	VDP_ADF_Config_1 Read/Write register User Sub Map	**ADF_DID[4:0]**				1	0	1	0	1	User Specified DID sent in the ancillary data stream with VDP decoded data	
		ADF_MODE[1:0]		0	0						Nibble Mode	
				0	1						Byte Mode, no code restrictions	
				1	0						Byte Mode, with 0x00 and 0xFF prevented	
				1	1						Reserved	
		ADF_ENABLE	0								Disable insertion of VBI decoded data into ancillary 656 stream	
			1								Enable insertion of VBI decoded data into ancillary 656 stream	
0x63	VDP_ADF_Config_2 Read/Write register User Sub Map	**ADF_SDID[5:0]**			1	0	1	0	1	0	User Specified SDID sent in the ancillary data stream with VDP decoded data	
		Reserved		x								
		DUPLICATE_ADF	0								Ancilliary data packet is spread across the Y & C data streams	If set to 1, all VBI_DATA_Px_Ny bits must be set as desired
			1								Ancilliary data packet duplicated on the Y & C data streams	
0x64	VDP_LINE_00E Read/Write register User Sub Map	**VBI_DATA_P318[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 318 NTSC - N/A	
		Reserved		0	0	0						
		MAN_LINE_PGM	0								Decode default standards on the lines indicated in table 32	
			1								Manually program the VBI standard to be decoded on each line. See table 33.	
0x65	VDP_LINE_00F Read/Write register User Sub Map	**VBI_DATA_P319_N286[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 319 NTSC - 286	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P6_N23[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 6 NTSC - 23	
0x66	VDP_LINE_010 Read/Write register User Sub Map	**VBI_DATA_P320_N287[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 320 NTSC - 287	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P7_N24[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 7 NTSC - 24	

Table 104: Register 0x67 to 0x6E

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x67	VDP_LINE_011 Read/Write register User Sub Map	**VBI_DATA_P321_N288[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 321 NTSC - 288	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P8_N25[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 8 NTSC - 25	
0x68	VDP_LINE_012 Read/Write register User Sub Map	**VBI_DATA_P322[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 322 NTSC - N/A	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P9[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 9 NTSC - N/A	
0x69	VDP_LINE_013 Read/Write register User Sub Map	**VBI_DATA_P323[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 323 NTSC - N/A	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P10[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 10 NTSC - N/A	
0x6A	VDP_LINE_014 Read/Write register User Sub Map	**VBI_DATA_P324_N272[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 324 NTSC - 272	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P11[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 11 NTSC - N/A	
0x6B	VDP_LINE_015 Read/Write register User Sub Map	**VBI_DATA_P325_N273[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 325 NTSC - 273	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P12_N10[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 12 NTSC - 10	
0x6C	VDP_LINE_016 Read/Write register User Sub Map	**VBI_DATA_P326_N274[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 326 NTSC - 274	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P13_N11[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 13 NTSC - 11	
0x6D	VDP_LINE_017 Read/Write register User Sub Map	**VBI_DATA_P327_N275[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 327 NTSC - 275	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P14_N12[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 14 NTSC - 12	
0x6E	VDP_LINE_018 Read/Write register User Sub Map	**VBI_DATA_P328_N276[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 328 NTSC - 276	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P15_N13[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 15 NTSC - 13	

Table 105: Register 0x6F to 0x76

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x6F	VDP_LINE_019 Read/Write register User Sub Map	**VBI_DATA_P329_N277[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 329 NTSC - 277	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P16_N14[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 16 NTSC - 14	
0x70	VDP_LINE_01A Read/Write register User Sub Map	**VBI_DATA_P330_N278[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 330 NTSC - 278	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P17_N15[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 17 NTSC - 15	
0x71	VDP_LINE_01B Read/Write register User Sub Map	**VBI_DATA_P331_N279[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 331 NTSC - 279	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P18_N16[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 18 NTSC - 16	
0x72	VDP_LINE_01C Read/Write register User Sub Map	**VBI_DATA_P332_N280[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 332 NTSC - 280	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P19_N17[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 19 NTSC - 17	
0x73	VDP_LINE_01D Read/Write register User Sub Map	**VBI_DATA_P333_N281[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 333 NTSC - 281	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P20_N18[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 20 NTSC - 18	
0x74	VDP_LINE_01E Read/Write register User Sub Map	**VBI_DATA_P334_N282[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 334 NTSC - 282	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P21_N19[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 21 NTSC - 19	
0x75	VDP_LINE_01F Read/Write register User Sub Map	**VBI_DATA_P335_N283[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 335 NTSC - 283	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P22_N20[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 22 NTSC - 20	
0x76	VDP_LINE_020 Read/Write register User Sub Map	**VBI_DATA_P336_N284[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 336 NTSC - 284	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P23_N21[3:0]	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 23 NTSC - 21	

Table 106: Register 0x77 to 0x79

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x77	VDP_LINE_021	**VBI_DATA_P337_N285[3:0]**					0	0	0	0	Sets VBI standard to be decoded from line: Pal - 337 NTSC - 285	MAN_LINE_PGM must be set to 1 for these bits to be effective
	Read/Write register User Sub Map	**VBI_DATA_P24_N22[3:0]**	0	0	0	0					Sets VBI standard to be decoded from line: Pal - 24 NTSC - 22	
0x78	VDP_STATUS	**CC_AVL**								0	Closed Captioning not detected	CC_CLEAR resets the CC_AVL bit
	Read only register									1	Closed Captioning detected	
	User Sub Map	**CC_EVEN_FIELD**							0		Closed Captioning decoded from Odd Field	
									1		Closed Captioning decoded from Even Field	
		CGMS_WSS_AVL						0			CGMS_WSS not detected	CGMS_WSS_CLEAR resets the CGMS_WSS_AVL bit
								1			CGMS_WSS detected	
		Reserved					0					
		GS_PDC_VPS_UTC_AVL				0					VPS not detected	GS_PDC_VPS_UTC_CLEAR resets the GS_PDC_VPS_UTC_AVL bit
						1					VPS detected	
		GS_DATA_TYPE			0						GemStar 1x detected	
					1						GemStar 2x detected	
		VITC_AVL		0							VITC not detected	VITC_CLEAR resets the VITC_AVL bit
				1							VITC detected	
		TTXT_AVL	0								TeleText not detected	
			1								TeleText detected	
0x78	VDP_CLEAR	**CC_CLEAR**								0	Do not re-initialise the CCAP registers	This is a self-clearing bit
	Write only register									1	Re-initialises the CCAP registers	
	User Sub Map	Reserved							0			
		CGMS_WSS_CLEAR						0			Do not re-initialise the CGMS/WSS registers	This is a self-clearing bit
								1			Re-initialises the CGMS/WSS read back registers	
		Reserved					0					
		GS_PDC_VPS_UTC_CLEAR				0					Do not re-initialise the GS/PDC/VPS/UTC registers	This is a self-clearing bit
						1					Re-initialises the GS/PDC/VPS/UTC read back registers	
		Reserved			0							
		VITC_CLEAR		0							Do not re-initialise the VITC registers	This is a self-clearing bit
				1							Re-initialises the VITC read back registers	
		Reserved	0									
0x79	VDP_CCAP_DATA_0 Read only register User Sub Map	**CCAP_BYTE_1[7:0]**	x	x	x	x	x	x	x	x	Decoded Byte 1 of CCAP	

Table 107: Register 0x7A to 0x8A

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x7A	VDP_CCAP_DATA_1 Read only register User Sub Map	**CCAP_BYTE_2[7:0]**	x	x	x	x	x	x	x	x	Decoded Byte 2 of CCAP	
0x7D	VDP_CGMS_WSS_DATA_0 Read only register User Sub Map	**CGMS_CRC[5:2]**					x	x	x	x	Decoded CRC sequence for CGMS	
		Reserved	0	0	0	0						
0x7E	VDP_CGMS_WSS_DATA_1 Read only register User Sub Map	**CGMS_WSS[13:8]**			x	x	x	x	x	x	Decoded CGMS/WSS data	
		CGMS_CRC[1:0]	x	x							Decoded CRC sequence for CGMS	
0x7F	VDP_CGMS_WSS_DATA_2 Read only register User Sub Map	**CGMS_WSS[7:0]**	x	x	x	x	x	x	x	x	Decoded CGMS/WSS data	
0x84	VDP_GS_VPS_PDC_UTC_0 Read only register User Sub Map	**GS_VPS_PDC_UTC_BYTE_0[7:0]**	x	x	x	x	x	x	x	x	Decoded GemStar / VPS / PDC / UTC data	
0x85	VDP_GS_VPS_PDC_UTC_1 Read only register User Sub Map	**GS_VPS_PDC_UTC_BYTE_1[7:0]**	x	x	x	x	x	x	x	x	Decoded GemStar / VPS / PDC / UTC data	
0x86	VDP_GS_VPS_PDC_UTC_2 Read only register User Sub Map	**GS_VPS_PDC_UTC_BYTE_2[7:0]**	x	x	x	x	x	x	x	x	Decoded GemStar / VPS / PDC / UTC data	
0x87	VDP_GS_VPS_PDC_UTC_3 Read only register User Sub Map	**GS_VPS_PDC_UTC_BYTE_3[7:0]**	x	x	x	x	x	x	x	x	Decoded GemStar / VPS / PDC / UTC data	
0x88	VDP_VPS_PDC_UTC_4 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_4[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x89	VDP_VPS_PDC_UTC_5 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_5[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x8A	VDP_VPS_PDC_UTC_6 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_6[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	

Table 108: Register 0x8B to 0x96

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x8B	VDP_VPS_PDC_UTC_7 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_7[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x8C	VDP_VPS_PDC_UTC_8 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_8[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x8D	VDP_VPS_PDC_UTC_9 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_9[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x8E	VDP_VPS_PDC_UTC_10 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_10[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x8F	VDP_VPS_PDC_UTC_11 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_11[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x90	VDP_VPS_PDC_UTC_12 Read only register User Sub Map	**VPS_PDC_UTC_BYTE_12[7:0]**	x	x	x	x	x	x	x	x	Decoded VPS / PDC / UTC data	
0x92	VDP_VITC_DATA_0 Read only register User Sub Map	**VITC_DATA_0[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x93	VDP_VITC_DATA_1 Read only register User Sub Map	**VITC_DATA_1[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x94	VDP_VITC_DATA_2 Read only register User Sub Map	**VITC_DATA_2[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x95	VDP_VITC_DATA_3 Read only register User Sub Map	**VITC_DATA_3[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x96	VDP_VITC_DATA_4 Read only register User Sub Map	**VITC_DATA_4[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	

Table 109: Register 0x97 to 0x9C

Subaddress	Register	Bit Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment	Note
0x97	VDP_VITC_DATA_5 Read only register User Sub Map	**VITC_DATA_5[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x98	VDP_VITC_DATA_6 Read only register User Sub Map	**VITC_DATA_6[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x99	VDP_VITC_DATA_7 Read only register User Sub Map	**VITC_DATA_7[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x9A	VDP_VITC_DATA_8 Read only register User Sub Map	**VITC_DATA_8[7:0]**	x	x	x	x	x	x	x	x	Decoded VITC data	
0x9B	VDP_VITC_CALC_CRC Read only register User Sub Map	**VITC_CRC[7:0]**	x	x	x	x	x	x	x	x	DataDecoded VITC CRC data	
0x9C	VDP_OUTPUT_SEL Read/Write Register User Sub Map	Reserved					0	0	0	0		
		WSS_CGMS_CB_CHANGE				0					Disable content based updation of CGMS & WSS data	When these bits are enabled, the corresponding "Available" bit will show the availability of data only when there has been any change in content
						1					Enable content based updation of CGMS & WSS data	
		GS_VPS_PDC_UTC_CB_CHANGE			0						Disable content based updation of GemStar, VPS, PDC & UTC data	
					1						Enable content based updation of GemStar, VPS, PDC & UTC data	
		I2C_GS_VPS_PDC_UTC[1:0]	0	0							Gemstar 1x / 2x	
			0	1							VPS	
			1	0							PDC	
			1	1							UTC	

Appendix A

PCB Layout Recommendations

The ADV7181C is a high-precision, high-speed mixed signal device. It is important to have a well laid-out PCB board, in order to achieve the maximum performance from the part. The following sections are a guide for designing a board using the ADV7181C.

Analogue Interface Inputs

It is extremely important to use the following layout techniques on the graphics inputs.

The trace length running into the graphics inputs should be minimized. This is accomplished by placing the ADV7181C as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they pick up more noise from the board and other external sources.

The 75 ohm termination resistors (refer to Figure 82) should be placed as close as possible to the ADV7181C chip. Any additional trace length between the termination resistors and the input of the ADV7181C increases the magnitude of reflections, which corrupts the graphics signal. 75 ohm matched impedance traces should be used. Trace impedances other than 75 ohms also increase the chance of reflections.

The ADV7181C has high input bandwidth. While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it also captures any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. The user should avoid running any digital traces near the analogue inputs.

Due to the high bandwidth of the ADV7181C, sometimes low-pass filtering the analogue inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75 ohm termination resistor is helpful in filtering out excess noise. Specifically, the part used was the # 2508051217Z0 from Fair-Rite, but each application may work best with a different bead value.

The non-graphics input should also receive care when being routed on the PCB. Again track lengths should be kept to a minimum and 75R traces impedances should be used where possible.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1uF and a 10nF capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. In addition, the user should avoid placing the capacitor on the opposite side of the PC board from the ADV7181C, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane => capacitor => power pin. The power connection should not be made between the capacitor and the power pin. Generally, the best approach is to place a via underneath the 100nF capacitor pads down to the power plane (refer to Figure 78).

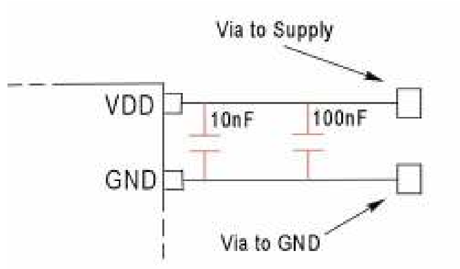


Figure 78: Recommended Power Supply Decoupling

It is particularly important to maintain low noise and good stability of PVDD (the clock generator supply). Abrupt changes in PVDD can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analogue circuitry groups (AVDD, DVDD, DVDDIO and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analogue supply regulator, which can in turn produce changes in the regulated analogue supply voltage. This can be mitigated by regulating the analogue supply, or at least PVDD, from a different, cleaner, power source, e.g. from a +12V supply.

It is also recommended to use a single ground plane for the entire board. This signal ground plane should have a spacing gap between the analogue and digital sections of the PCB (refer to Figure 79).

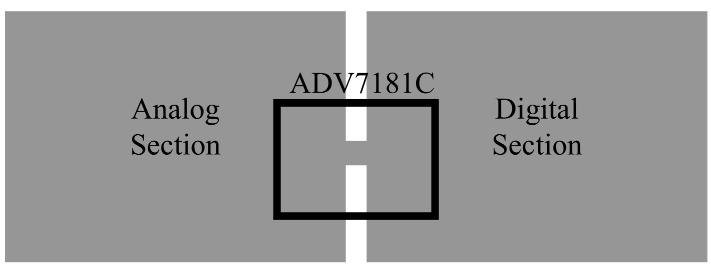


Figure 79: PCB Ground Layout

Experience has shown repeatedly that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to place, at least, a single ground plane under the ADV7181C. The location of the split should be under the ADV7181C. For this case it is even more important to place components wisely because the current loops will be much longer, (current takes the path of least resistance).

Example of a current loop:
Power plane => ADV7181C => digital output trace => digital data receiver => digital ground plane => analogue ground plane.

PLL

The PLL loop filter components should be placed close to the ELPF pin. Digital or other high frequency traces should not be placed near these components. The values suggested in the datasheet with 10% tolerances or less should be used.

Digital Outputs (Data and Clocks)

The trace length that the digital outputs have to drive should be minimized. Longer traces have higher capacitance, which requires more current that cause more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor of value between 50-200 ohms can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7181C. If series resistors are used, they should be placed as close as possible to the ADV7181C pins (although you should try not to add vias or extra length to the output trace in order to get the resistors closer).

If possible, you should limit the capacitance that each of the digital outputs drives to less than 15pF. This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside the ADV7181C, creating more digital noise on its power supplies.

Digital Inputs

The digital inputs on the ADV7181C were designed to work with 3.3V signals, and are not tolerant of 5.0V signals. Therefore, extra components are required if 5.0V logic signal are to be applied to the decoder. (Refer to the diode protection circuitry on HS_IN and VS_IN pins in Figure 82.)

Any noise that gets onto the HS_IN input trace will add jitter to the system. Therefore, the trace length should be minimized; and digital or other high frequency traces should not be run near it.

Xtal and Load Cap Value Selection

Figure 80 shows an example of a reference clock circuit for the ADV7181C. Special care must be taken when using a crystal circuit to generate the reference clock for the ADV7181C. Small variations in reference clock frequency can cause autodetection issues and impair the ADV7181C performance.

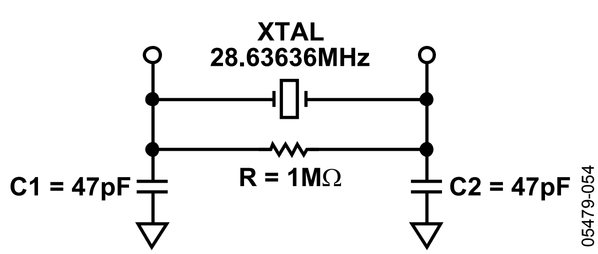


Figure 80: Crystal Circuit

The following guidelines should be used to ensure correct operation:

- Use the correct frequency crystal, which is 28.63636 MHz. Tolerance should be 50 ppm or better.
- Use a parallel-resonant crystal.
- Know the C_{load} for the crystal part selected. The values of the C1 and C2 capacitors must be calculated using this C_{load} value.

To find C1 and C2, use the following formula:

$$C = 2(C_{load} - C_{stray}) - C_{pg}$$

Where C_{stray} is usually 2 pF to 3 pF, depending on board traces, and C_{pg} (pin-to-ground capacitance) is 4 pF for the ADV7181C.

Example:
C_{load} = 30 pF. C1 = 50 pF, C2 = 50 pF (in this case 47 pF is the nearest “real-life” cap value to 50 pF)

Appendix B

Recommended External Loop Filter Components

Note that the external loop filter components for ELPF pins should be placed as close as possible to the respective pins. The recommended component values are specified in Figure 81.

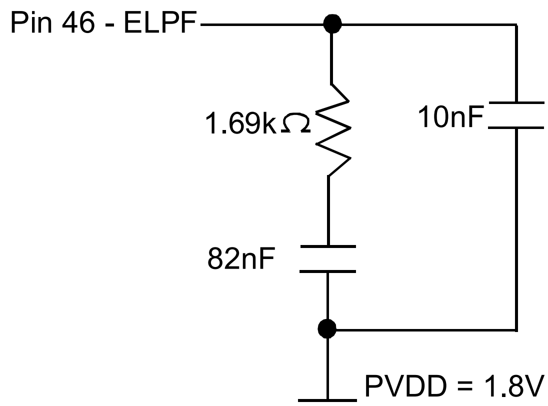


Figure 81: ELPF Components

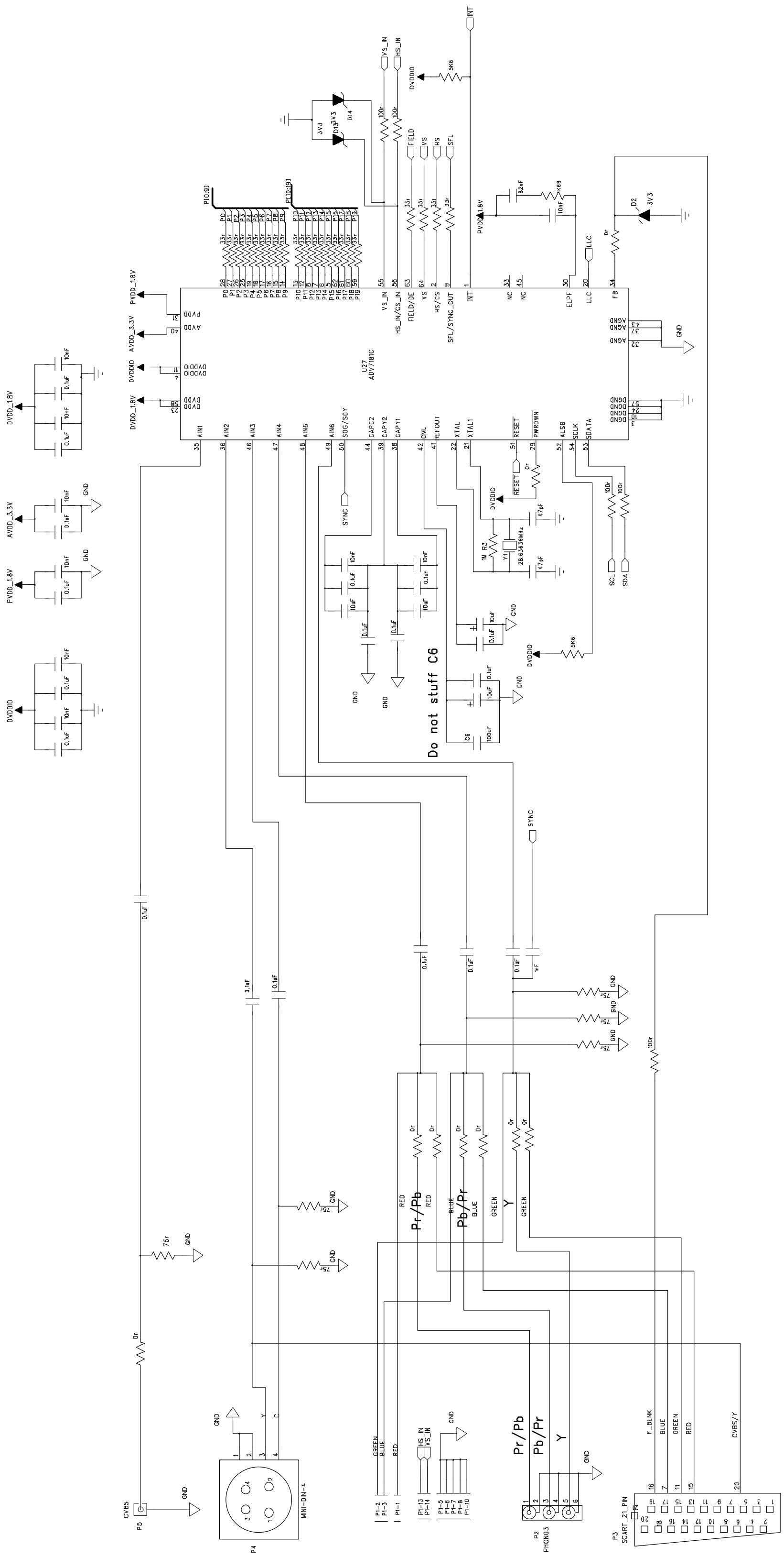


Figure 82: ADV7181C Typical Connection Diagram

Appendix C

Package Outline Drawings

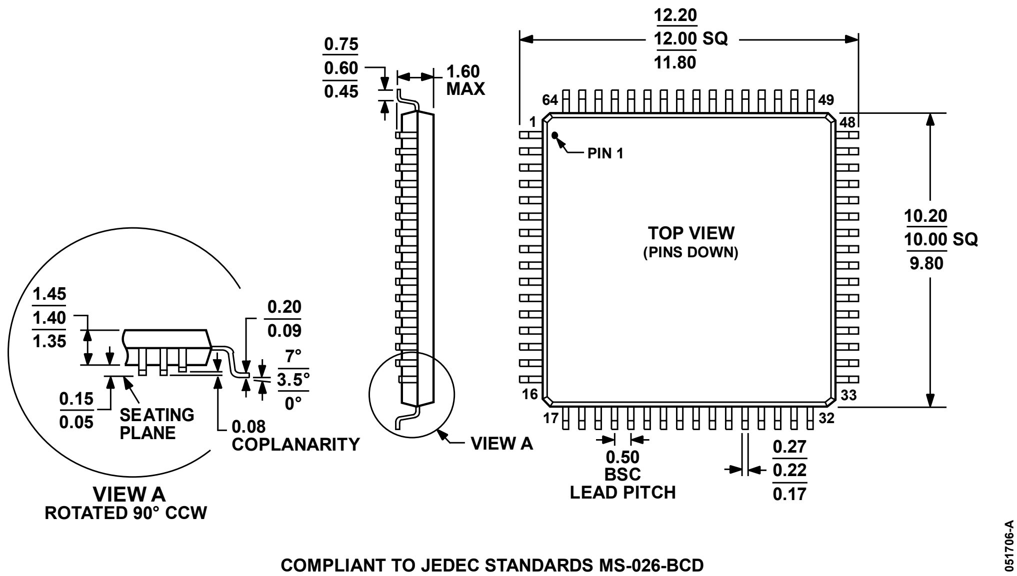


Figure 83: 64-Lead Low Profile Quad Flat Package (ST-64-2)

(Dimensions are shown in millimeters.)

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Document Revision History

Revision	Date	Changes
Rev.0	07/2008	Initial
Rev.A	04/2009	Updated typo entire document
Rev.B	05/2010	Decreased maximum supported graphics rate to XGA @ 70Hz
		DUT description in Acronyms and Abbreviations table (p2) modified
		Functional Block Diagram (p9) modified
		Updates to Pin Function Description table (p11)
		Updates to section 3.1.(Analogue Input Muxing)
		Updates to Table 8
		Updates to section 5.1.1 (Power-down)
		Updates to Table 10 (PLL Recommended Settings for GR Modes)
		Updates to section 7.4.2 (Latch Clock Setting)
		Updates to section 7.5 (Data Preprocessors)
		Updates to Figure 16 (CP AGC Automatic Enable)
		Updates to section 7.11 (Synchronization Source Polarity Detector)
		Updates to section 7.13.2 (HS Timing Controls (CP))
		Updates to section 7.13.3 (VS Timing Controls (CP))
		Updates to section 7.13.4 (FIELD Timing Controls (CP))
		Updates to section 7.14 (Standard Detection and Identification)
		Updates to section 8.18.6 (CGMS and WSS)
		Updated Register map
Rev.C	09/2010	Removed reference to Confidential