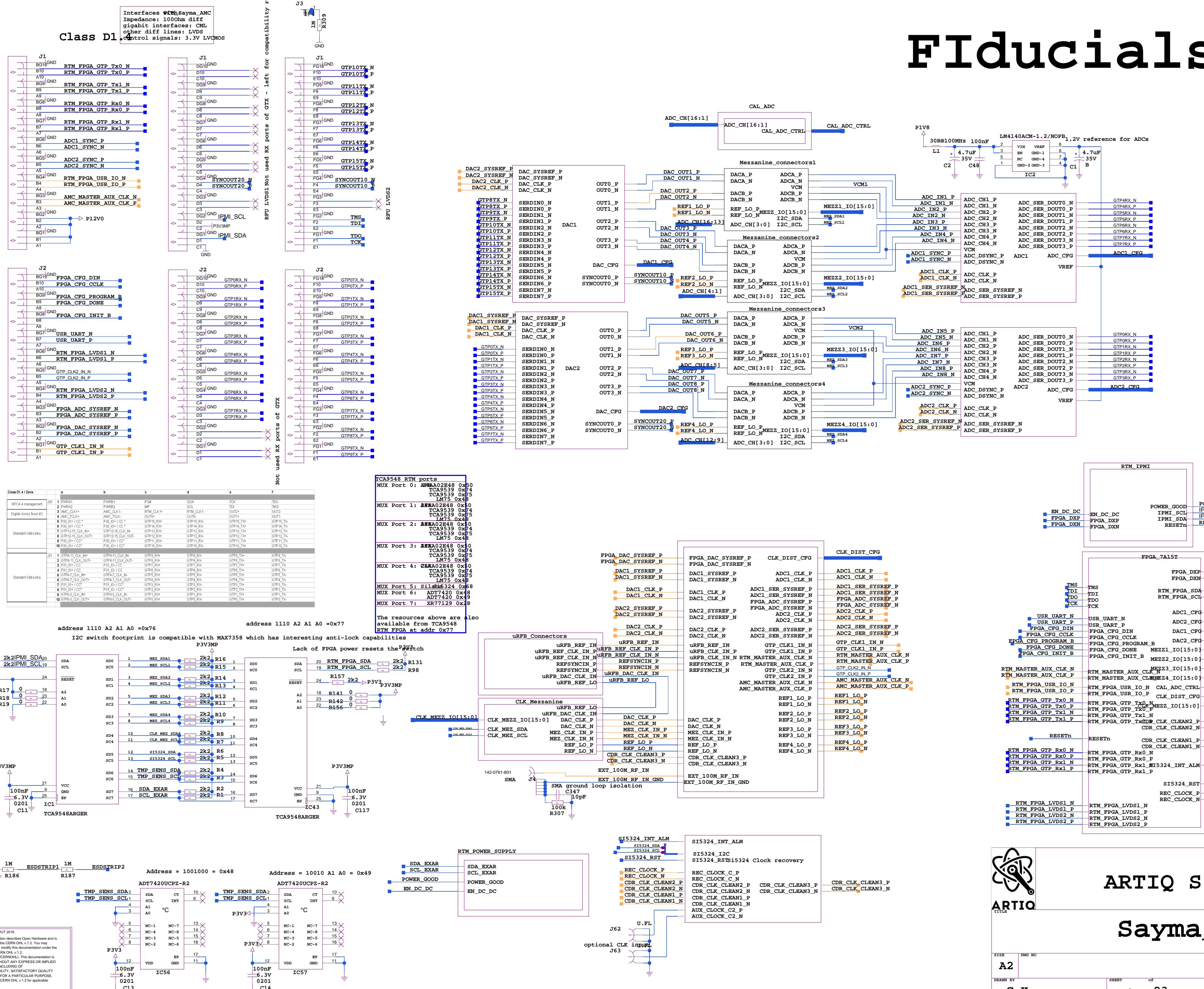
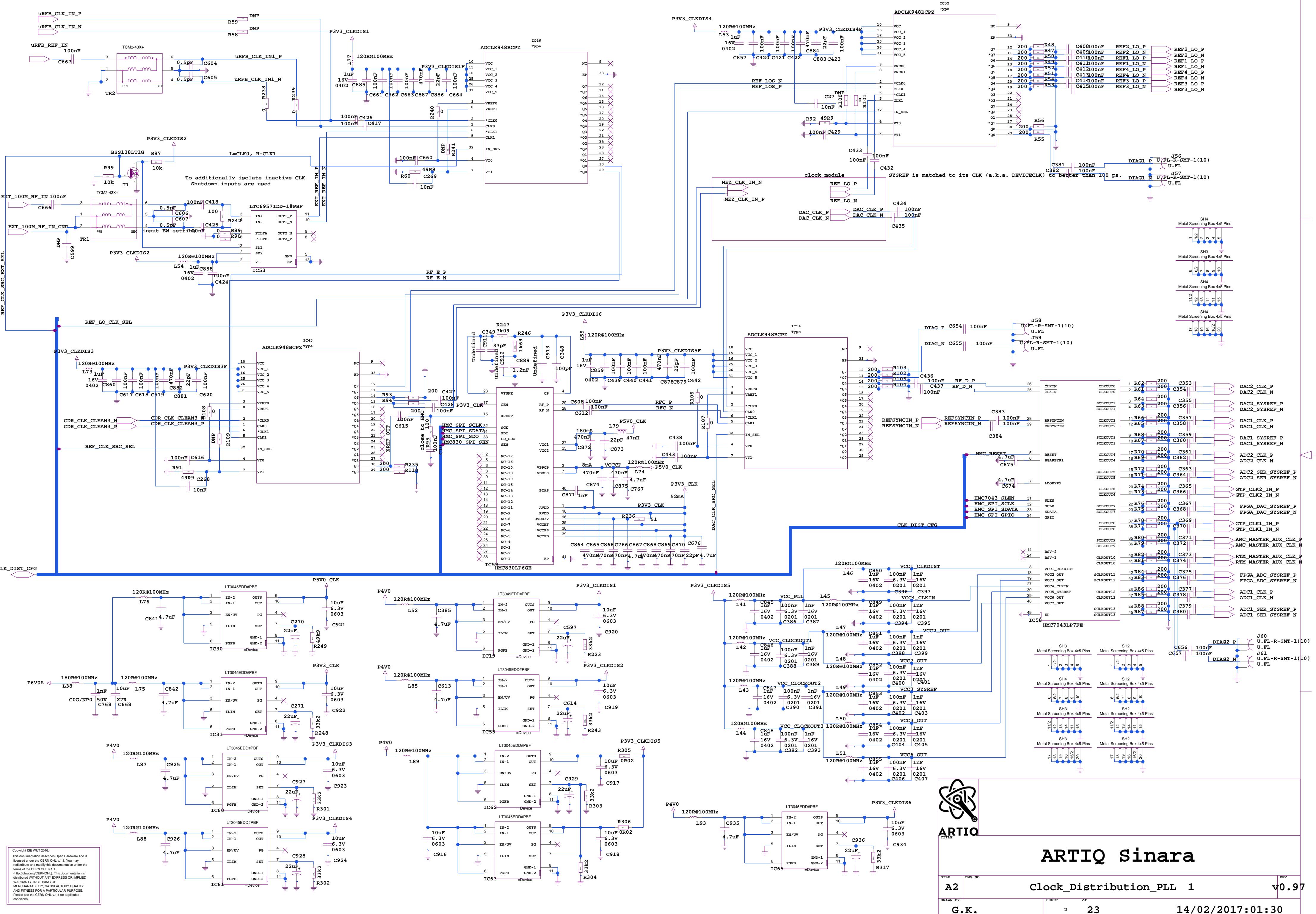
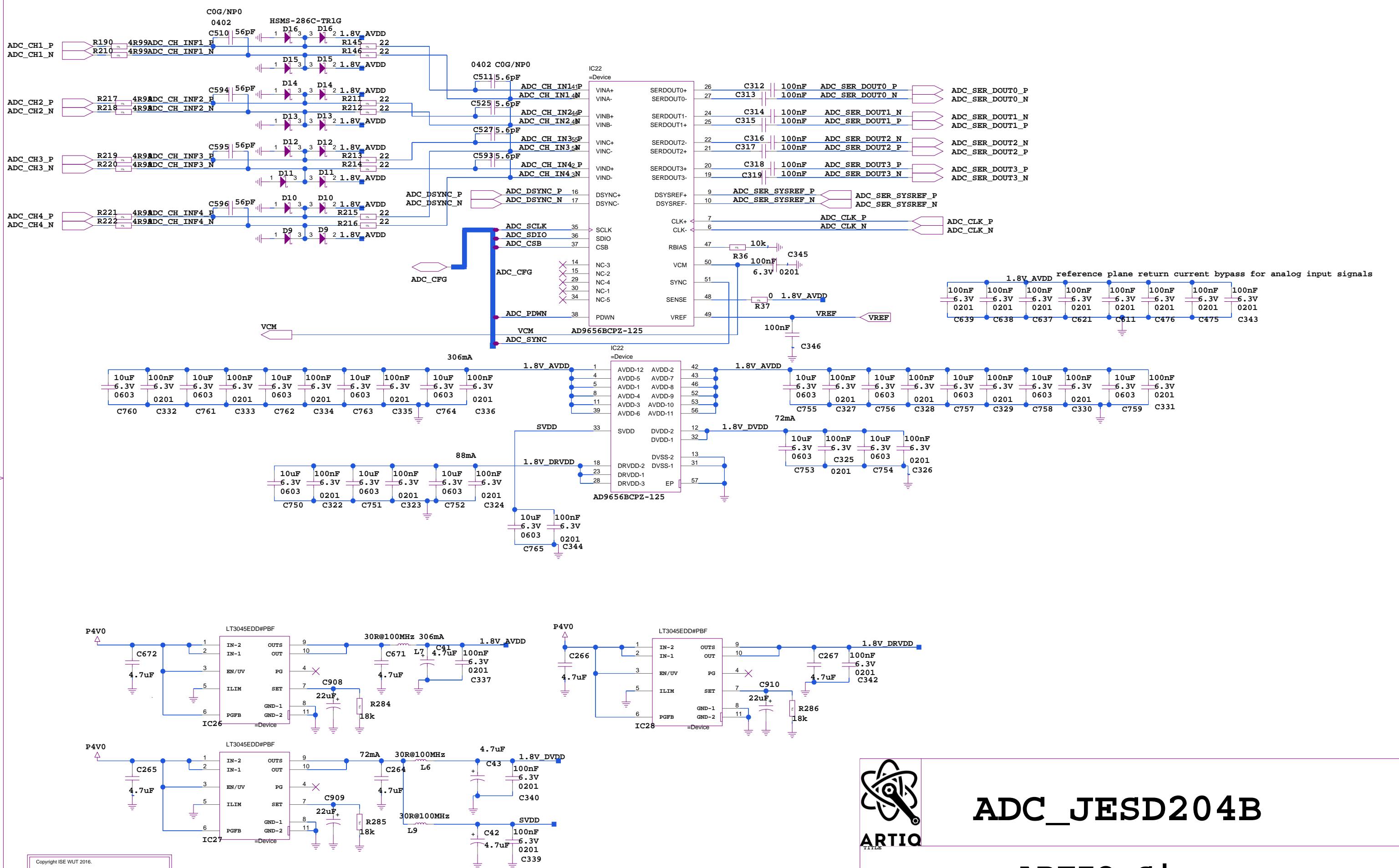


# FIducials miss:

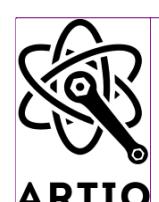






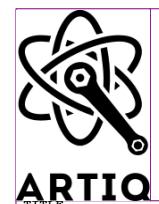
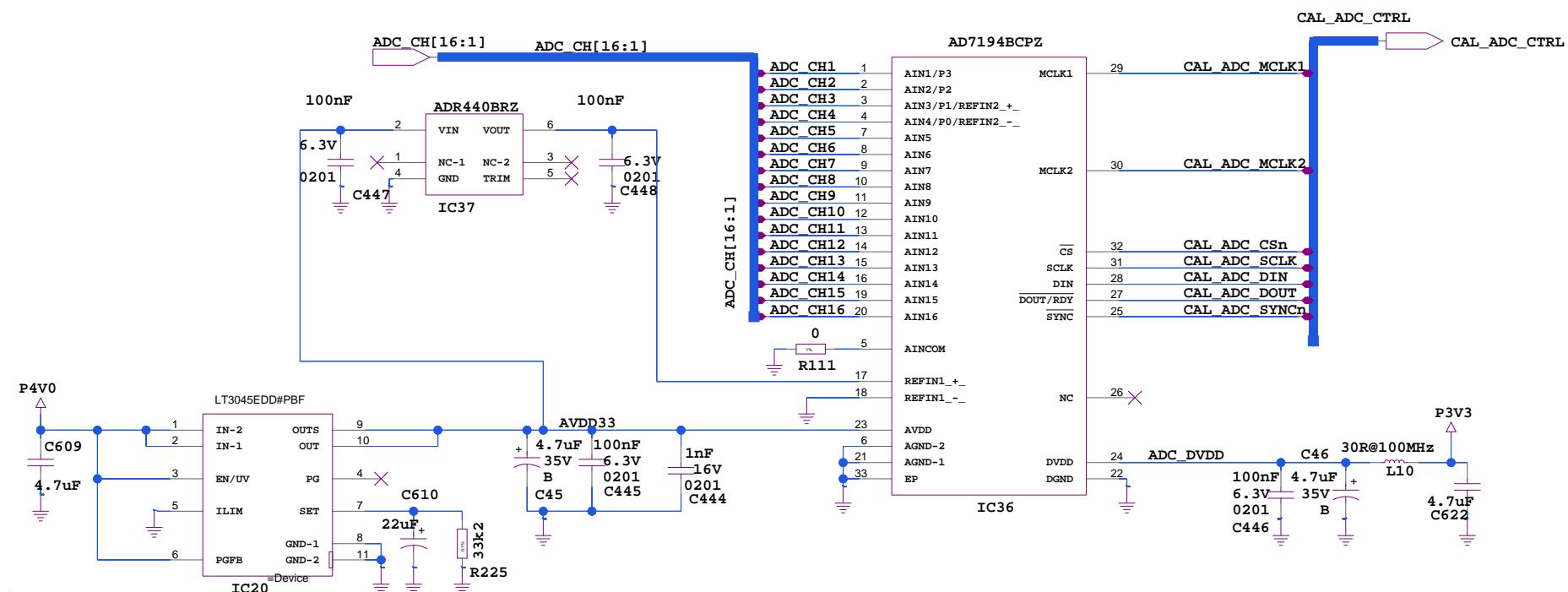


Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2 (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions.



# ADC\_JESD204B

## ARTIQ Sinara

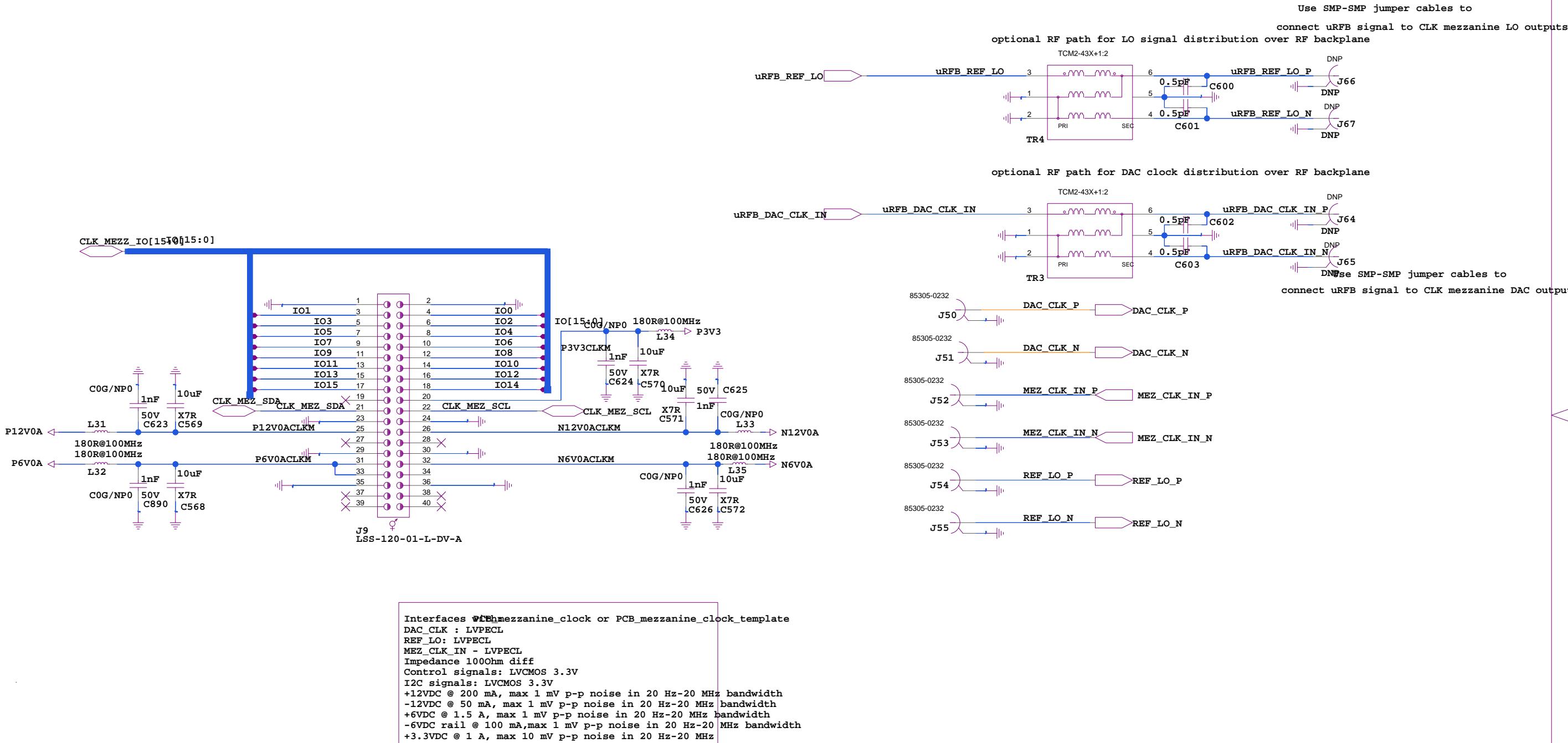


**ARTIQ Sinara**

# CAL\_ADC

Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.  
<http://cernohl.org> (or CERN OHL). This documentation is distributed "AS IS" WITHOUT EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable conditions.

SIZE DWG NO  
A3 1 REV v0.97  
DRAWN BY G.K. SHEET 5 of 23  
24/01/2017:23:14



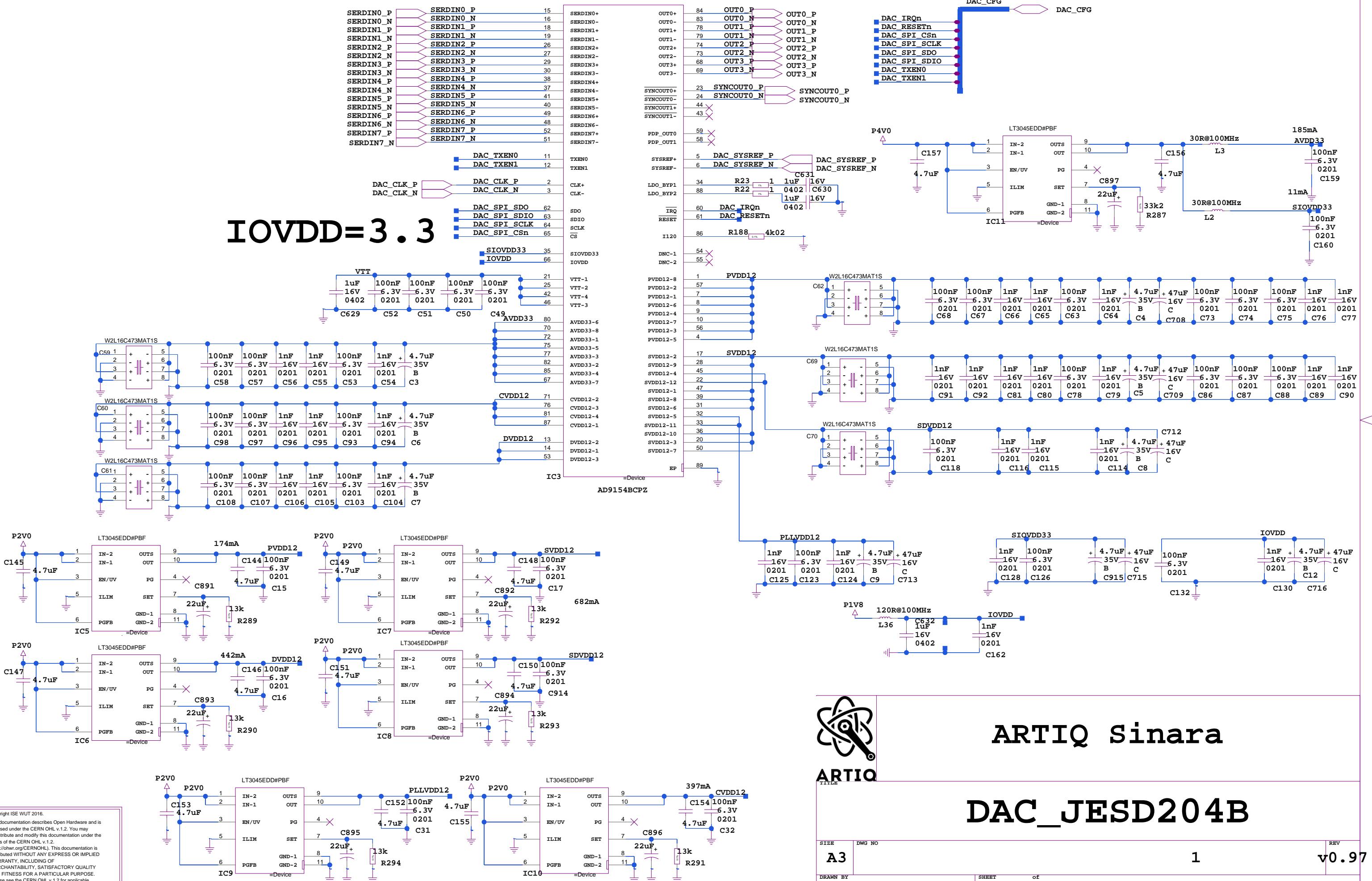
Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.  
(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable conditions.



**ARTIQ Sinara**

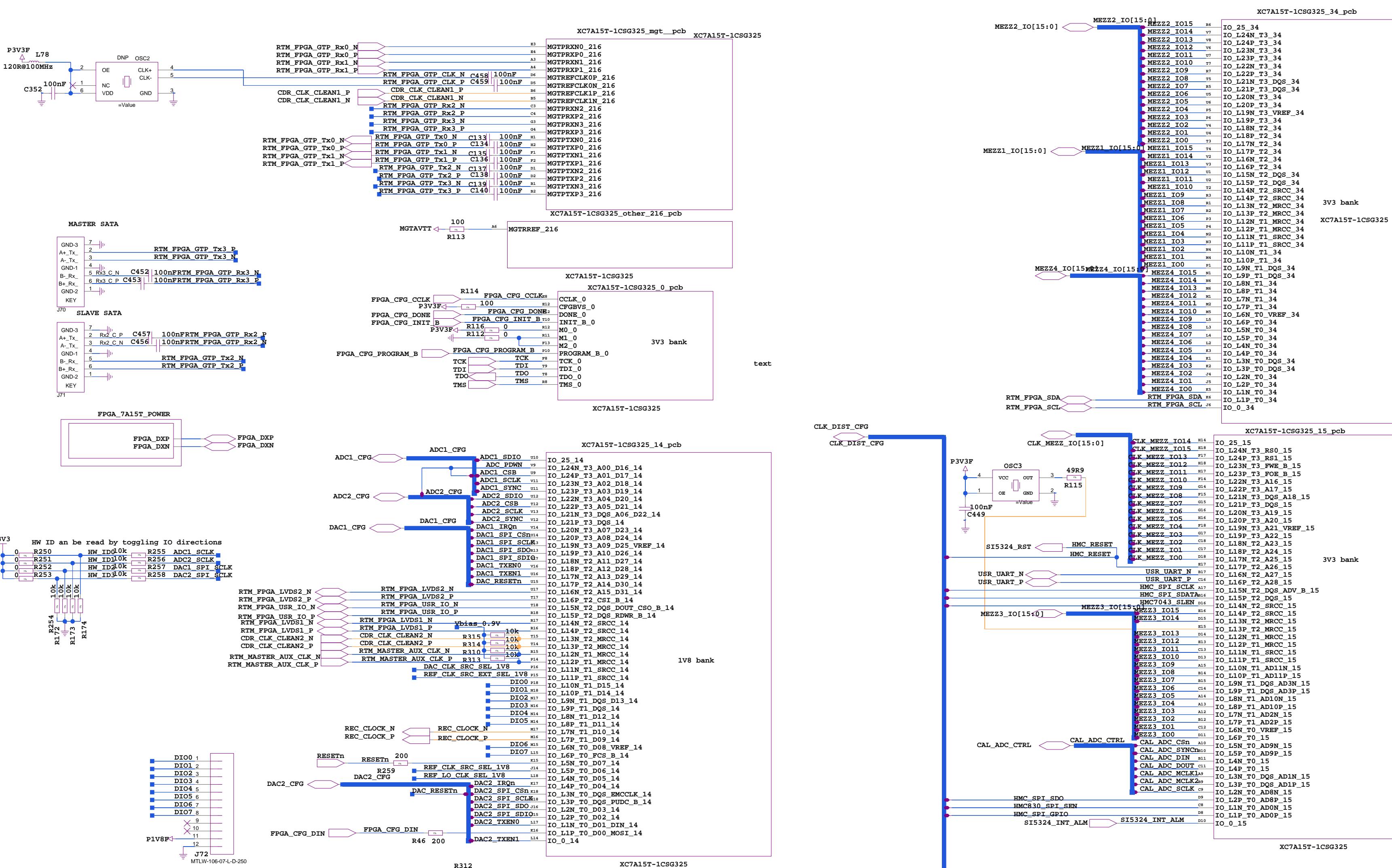
**CLK\_Mezzanine**

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY		1
G.K.		23
12/02/2017:15:32		



Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is  
licensed under the CERN OHL v.1.2. You may  
redistribute and modify this documentation under the  
terms of the CERN OHL v.1.2.  
<http://ohwr.org/CERNohl>. This documentation is  
distributed WITHOUT ANY EXPRESS OR IMPLIED  
WARRANTY, INCLUDING OF  
MERCHANTABILITY, SATISFACTORY QUALITY  
AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable  
conditions.

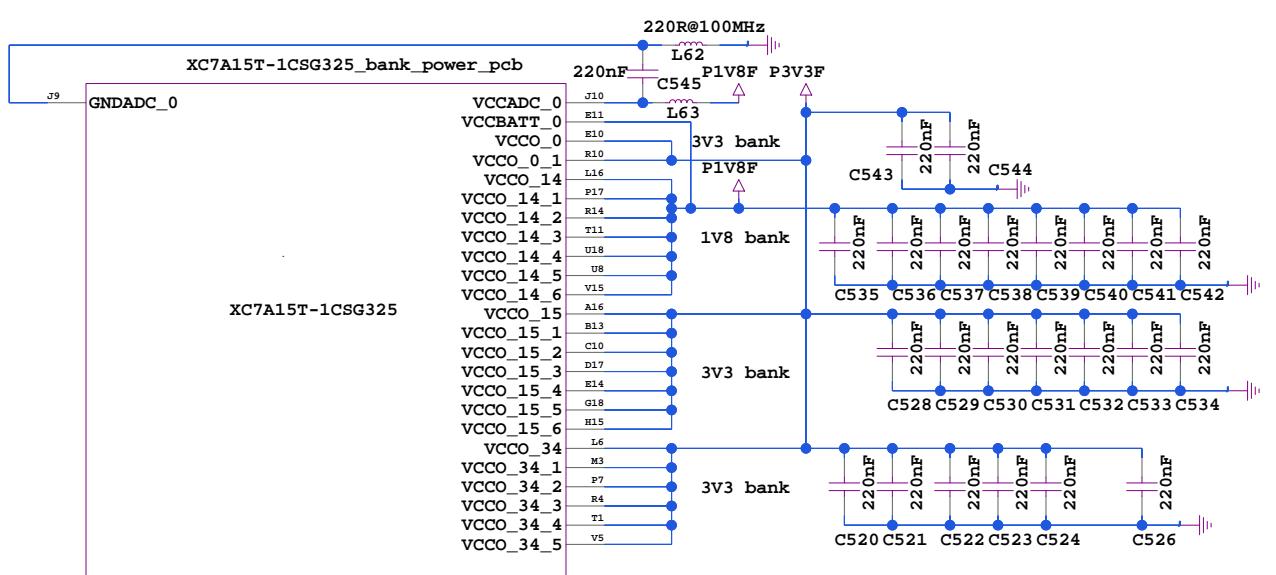
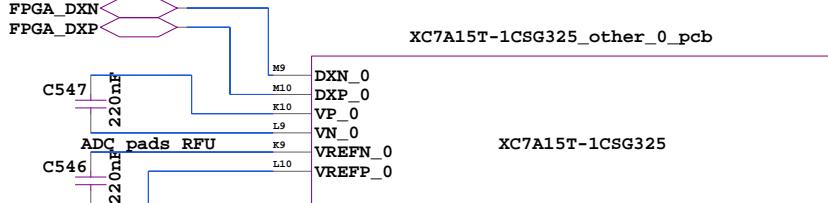




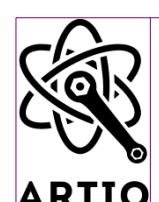
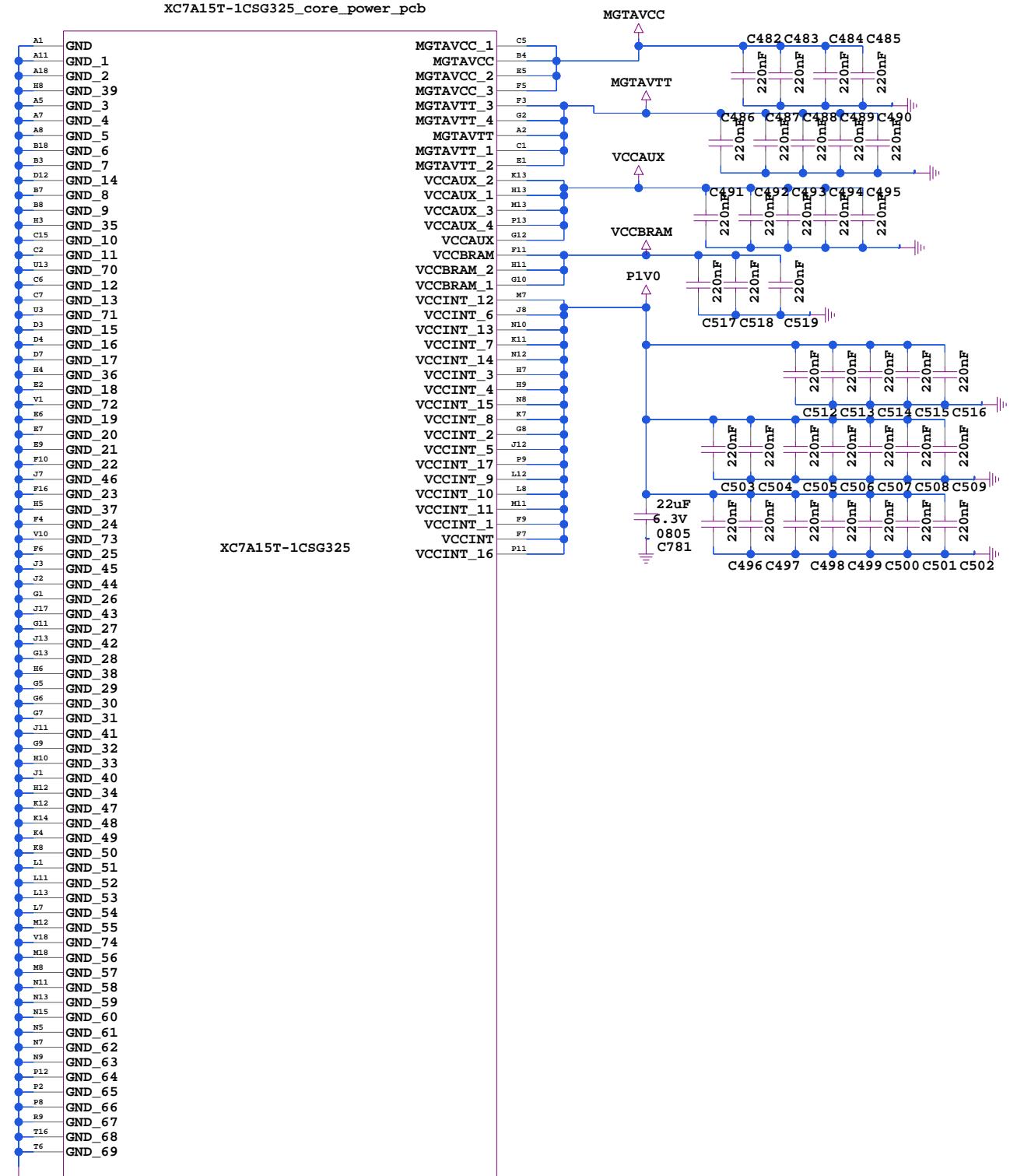
ARTIQ Sinara

FPGA 7A15T

Copyright ISE WUT 2016.  
This documentation defines Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and/or modify the documentation under the terms of the CERN OHL v.1.2  
(<http://ohwr.org/CERN-OHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions.



XC7A15T-1CSG325\_core\_power\_pcb



**ARTIQ Sinara**

# FPGA\_7A15T\_POWER

SIZE DWG NO

A3

DRAWN BY

G.K.

SHEET

of

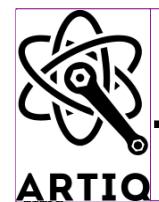
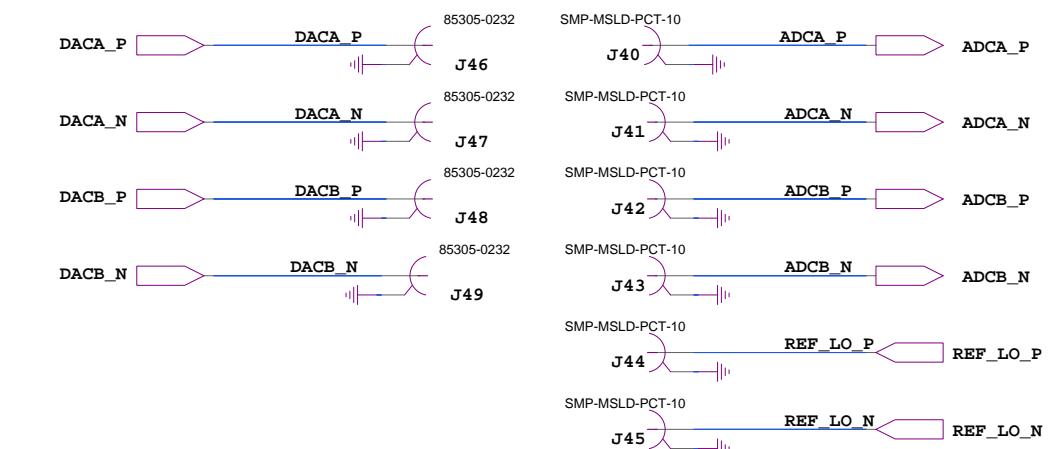
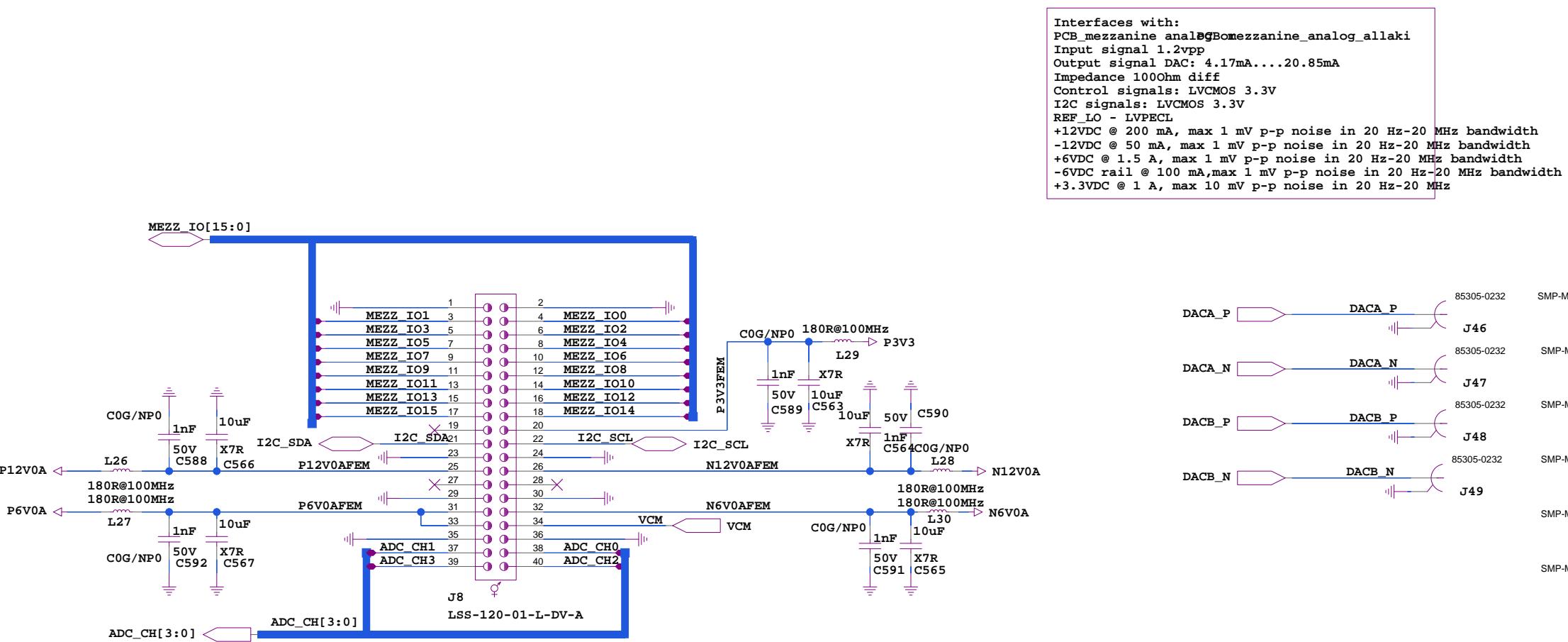
1

REV  
v0.97

10

23

24/01/2017:23:14



# ADC\_DAC\_AFE\_Mezzanine

ARTIQ

## ARTIQ Sinara

TITLE

REV

v0.97

SIZE DWG NO

A3

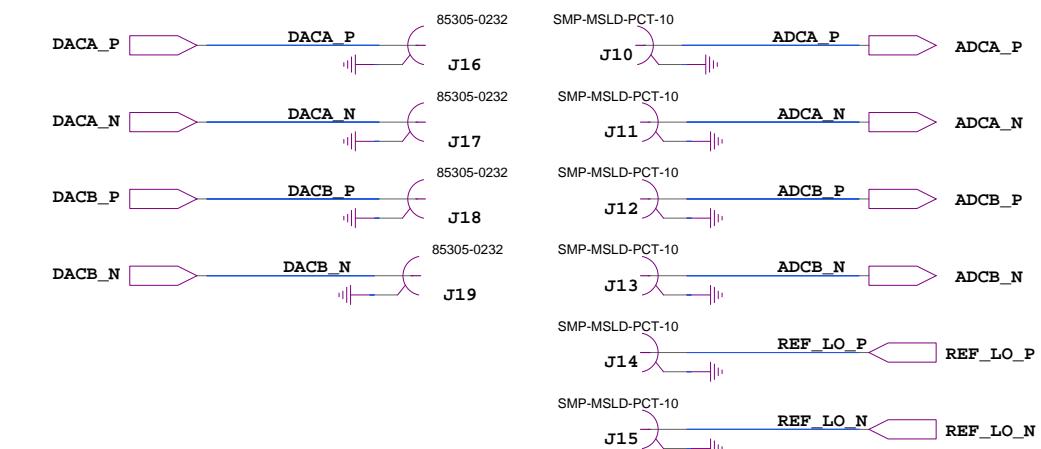
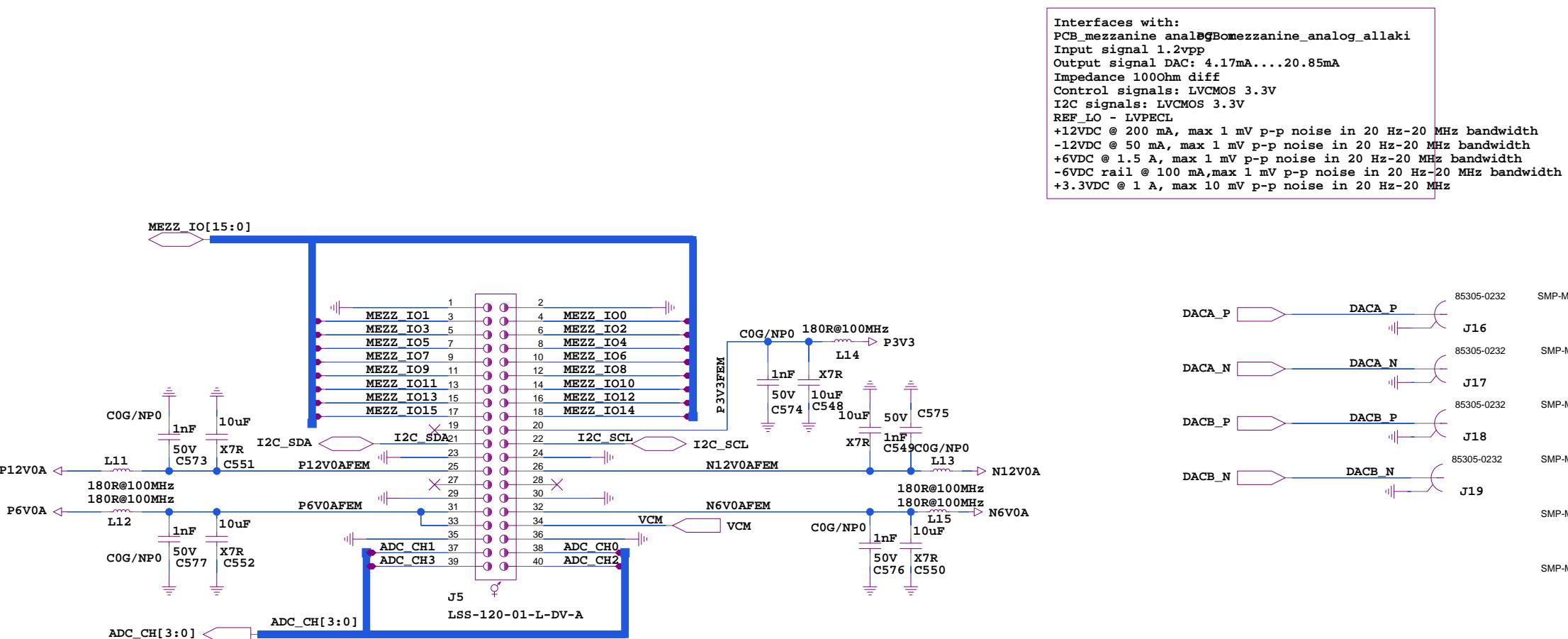
DRAWN BY

G.K.

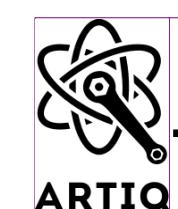
SHEET of

11 23

02/02/2017:23:29



Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.  
(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable conditions.

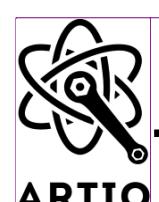
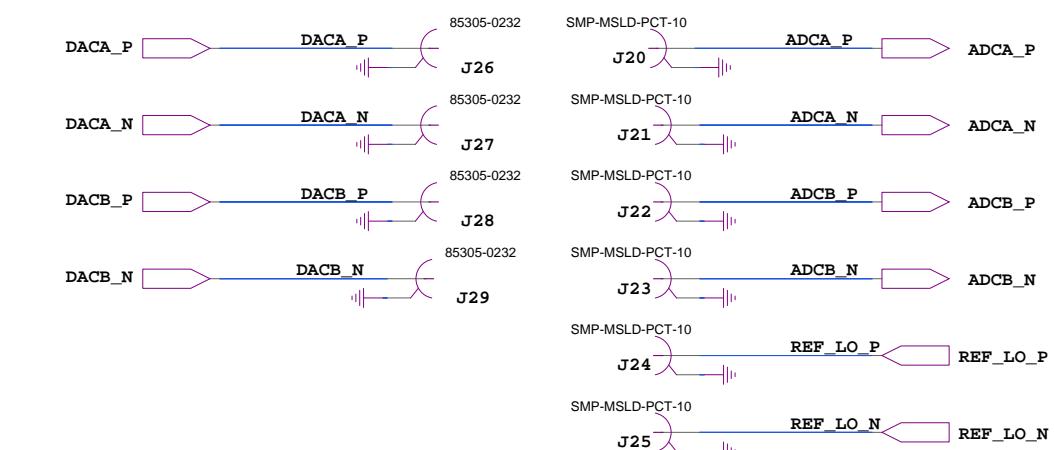
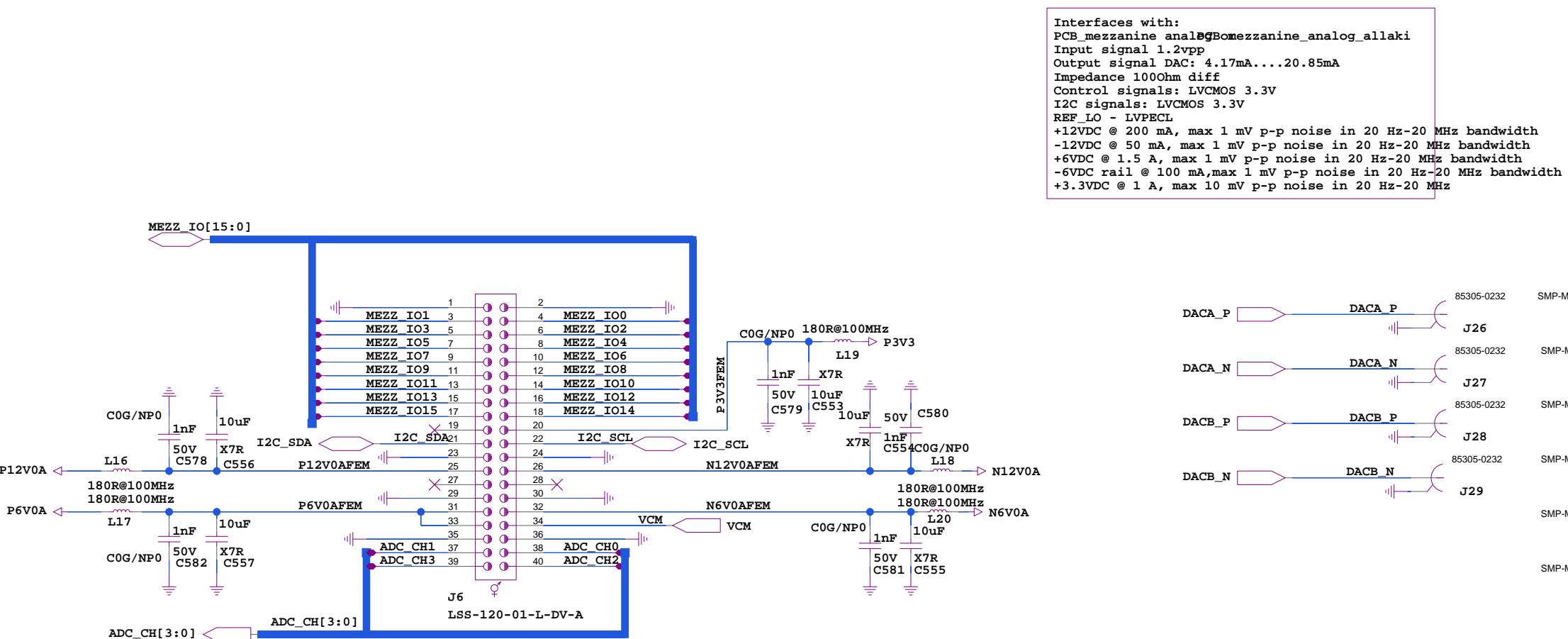


TITLE

# ADC\_DAC\_AFE\_Mezzanine

## ARTIQ Sinara

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY		1
G.K.		23
02/02/2017:23:29		



## ADC\_DAC\_AFE\_Mezzanine

TITLE

ARTIQ Sinara

SIZE DWG NO

A3

REV

v0.97

DRAWN BY

G.K.

SHEET

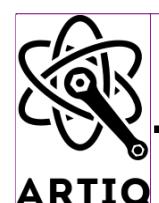
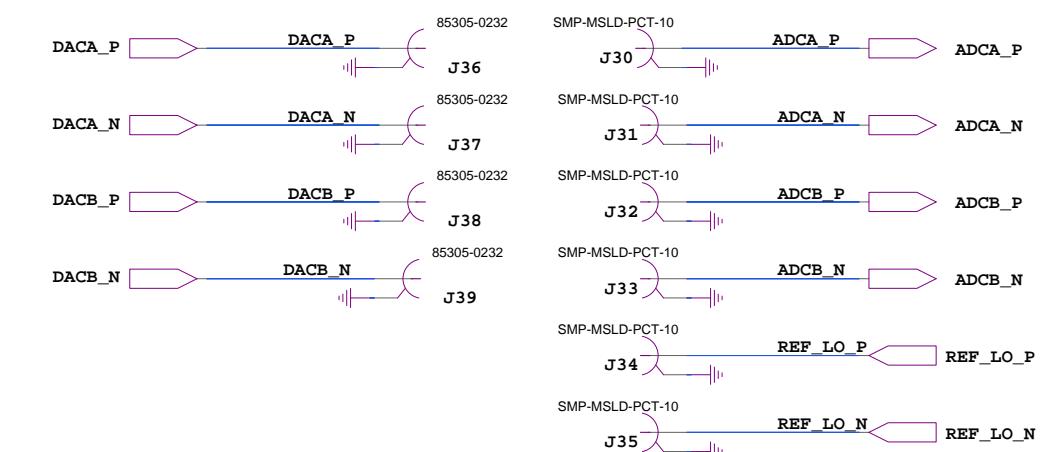
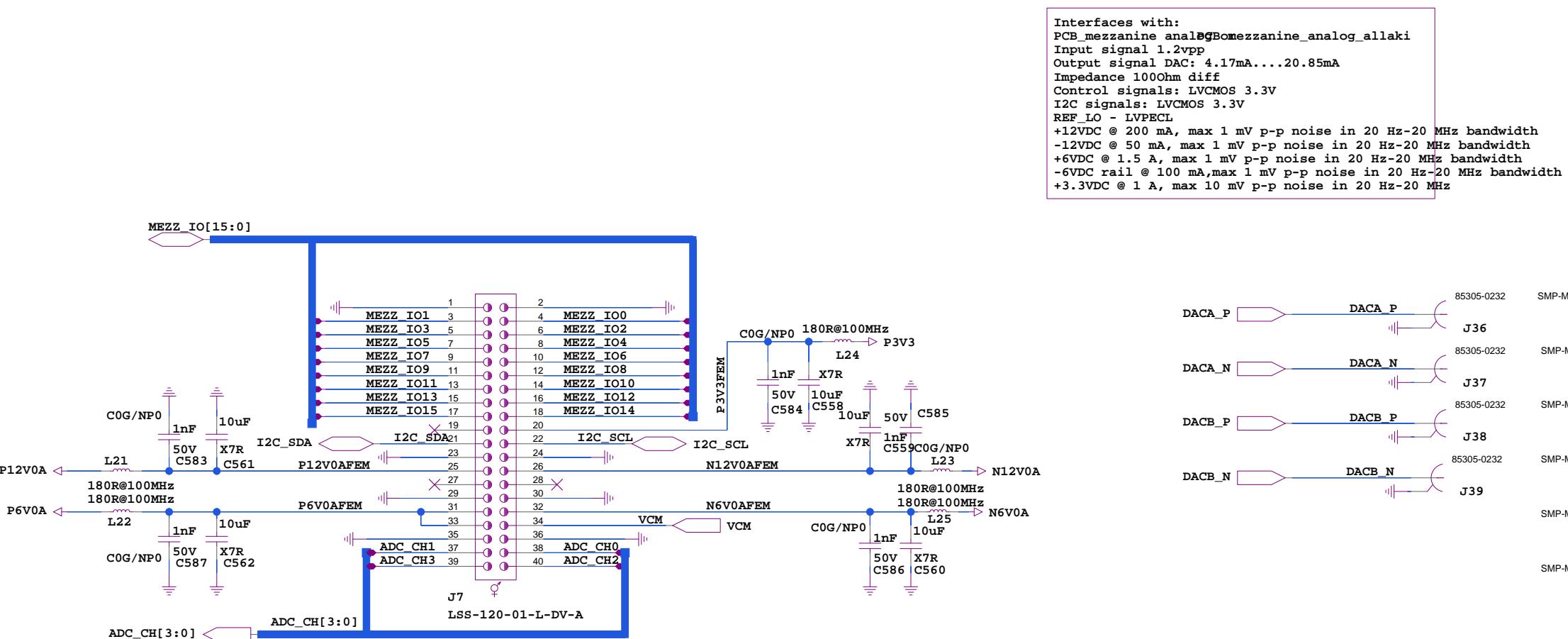
of

13

23

1

02/02/2017:23:29



# ADC\_DAC\_AFE\_Mezzanine

TITLE

## ARTIQ Sinara

SIZE DWG NO

A3

REV

v0.97

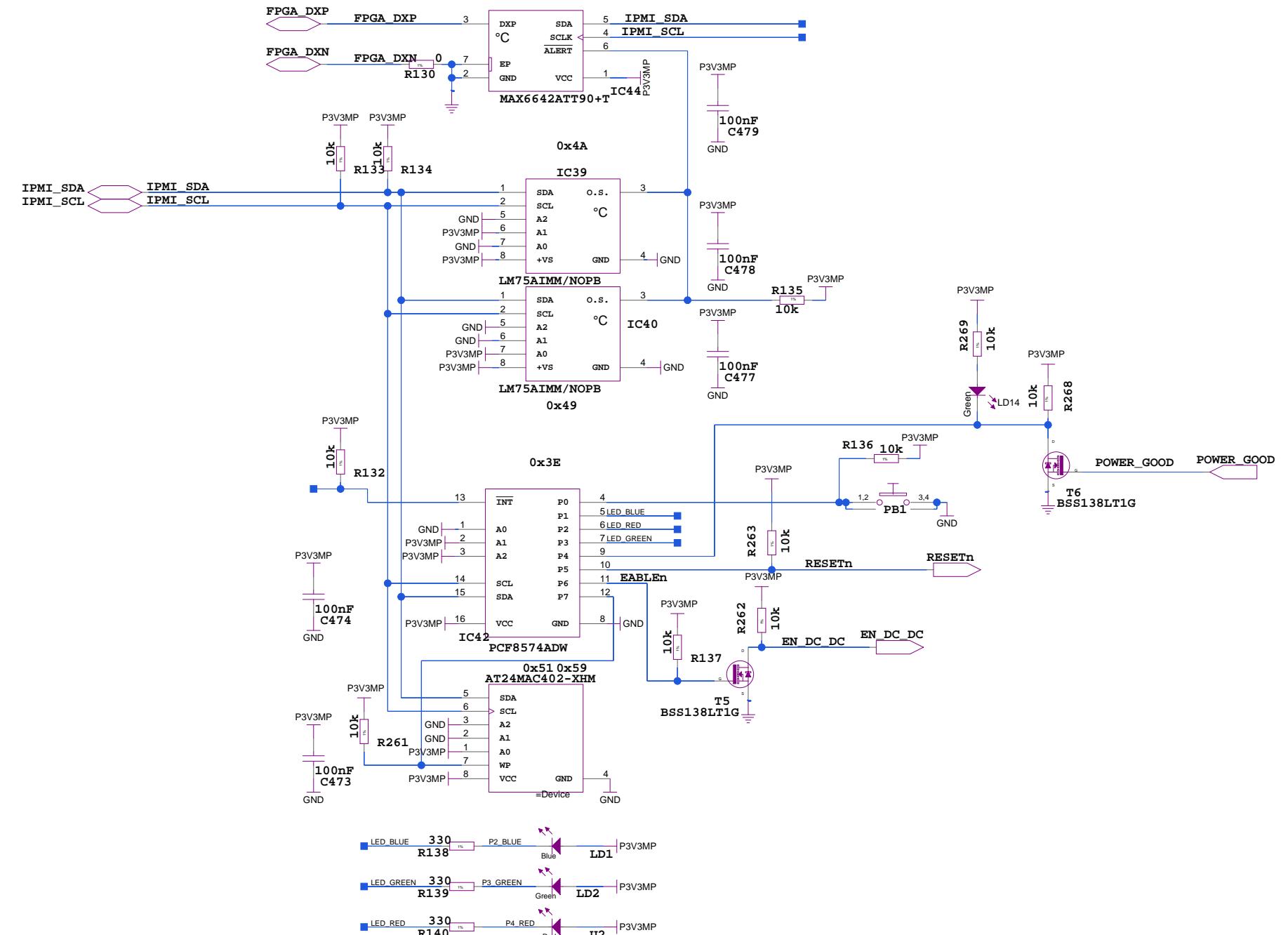
DRAWN BY

G.K.

SHEET of

14 23

1



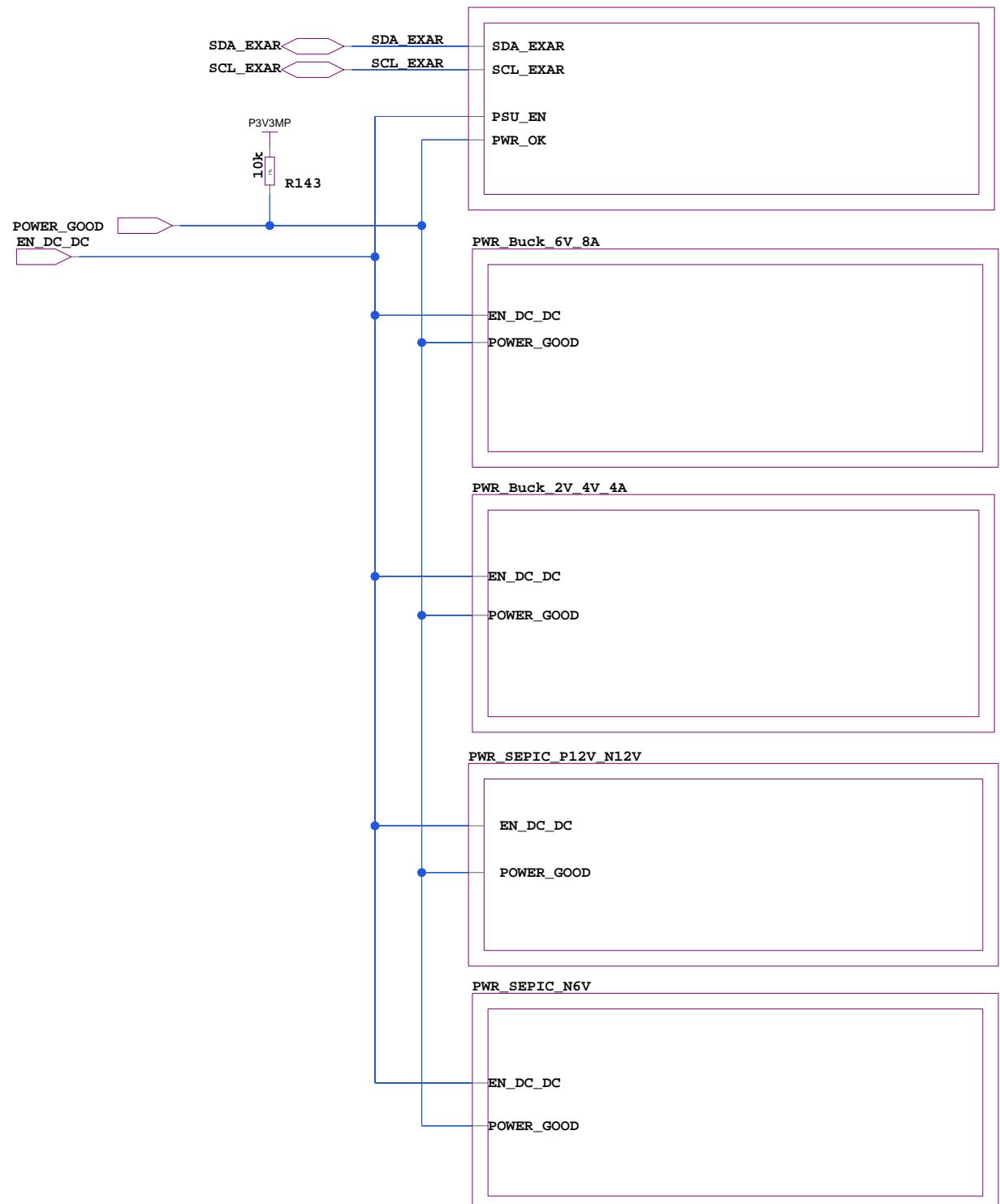
check addresses ARTIQ sinara



**RTM\_IPMI**

Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is  
licensed under the CERN OHL v.1.2. You may  
redistribute and modify this documentation under the  
terms of the CERN OHL v.1.2.  
(<http://ohwr.org/CERNOHL>). This documentation is  
distributed WITHOUT ANY EXPRESS OR IMPLIED  
WARRANTY, INCLUDING OF  
MERCHANTABILITY, SATISFACTORY QUALITY  
AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable  
conditions.

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY		
G.K.		1
SHEET		of
15		23
13/02/2017:18:44		

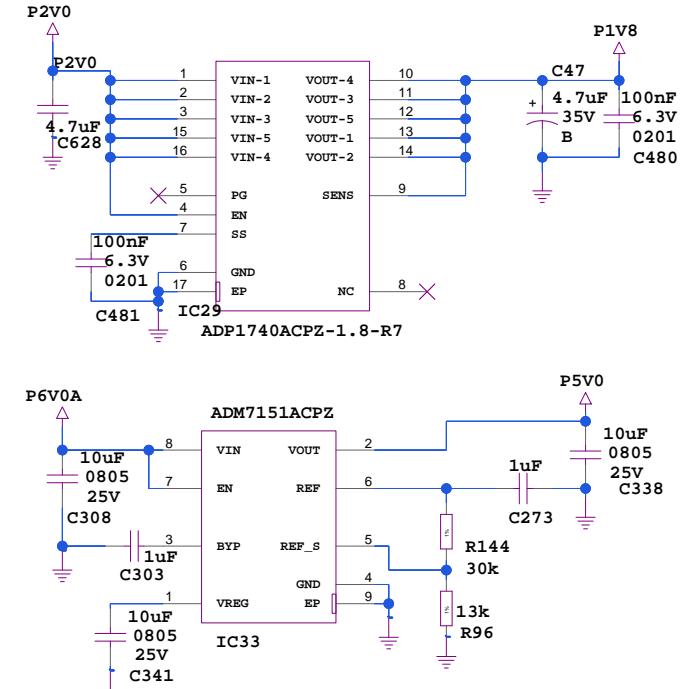


## RTM modules power requirements

+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth  
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth  
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth  
-6VDC rail @ 750 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth  
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

### RTM power requirement

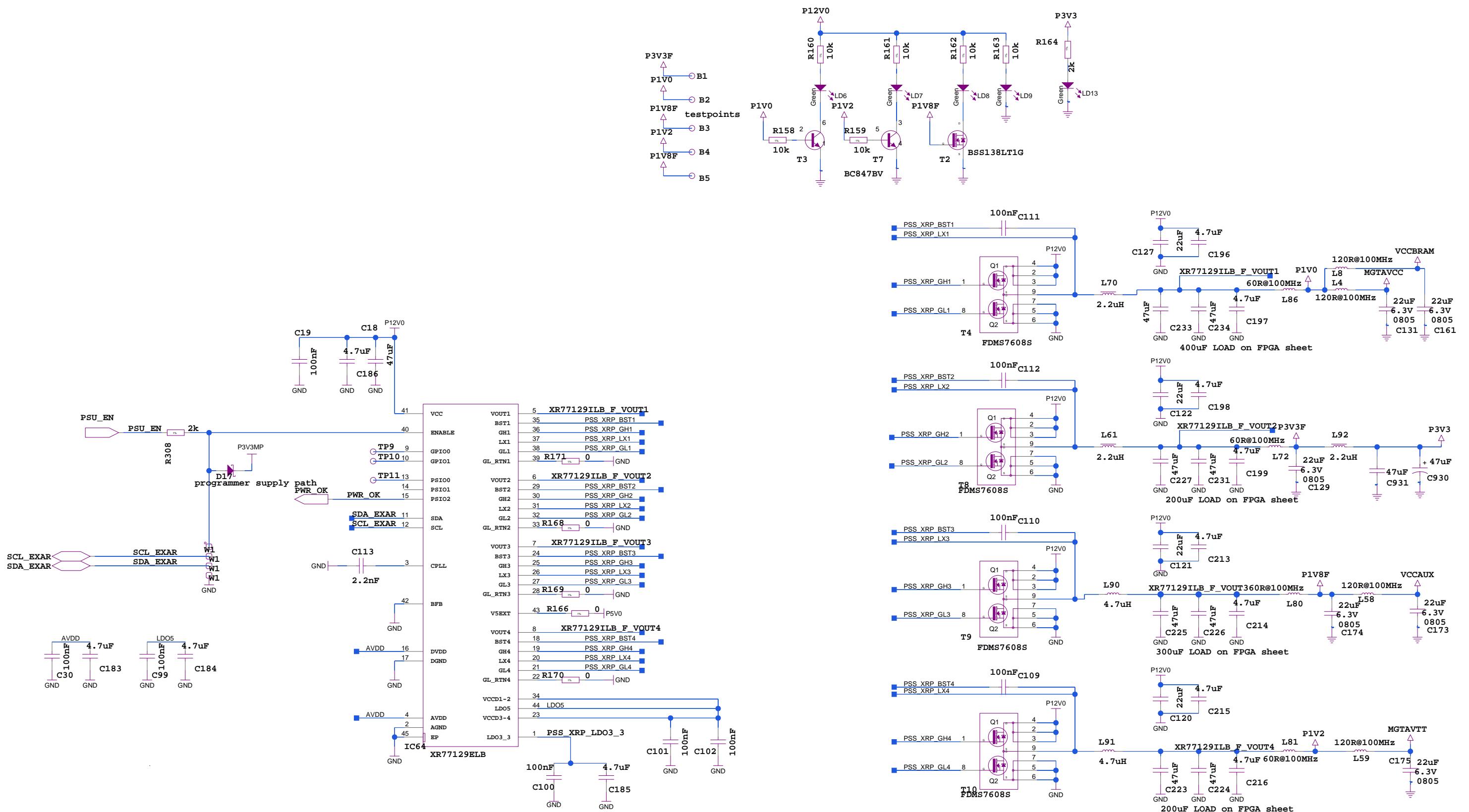
+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz  
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz



# ARTIQ Sinara

# **RTM\_POWER\_SUPPLY**

SIZE	DWG NO		REV
A3		1	v0.97
DRAWN BY	SHEET	OF	
G.K.	16	23	24/01/2017:23:14

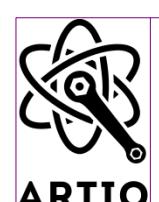
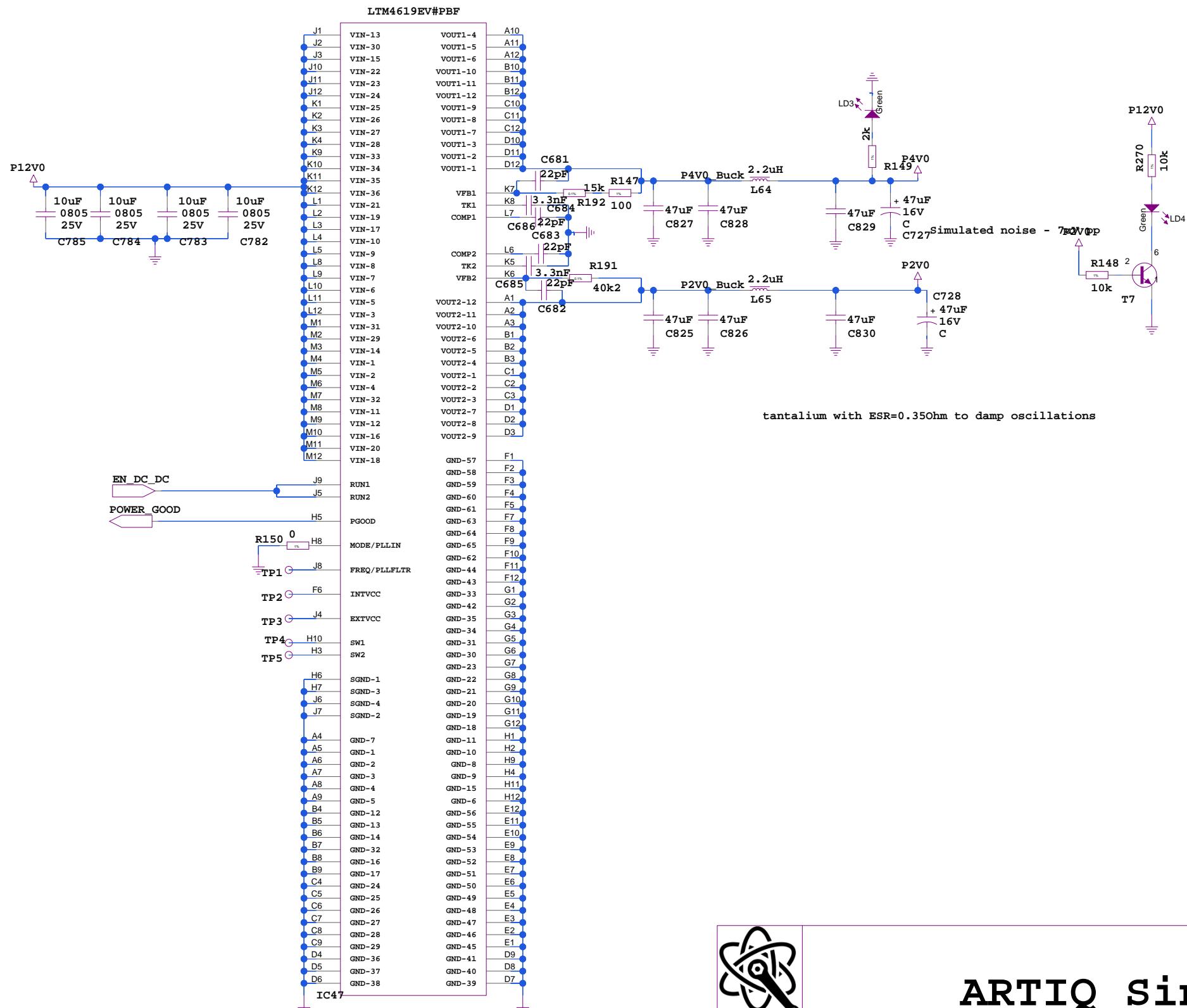


# ARTIQ Sinara

# PWR buck FPGA EXAR

Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is  
licensed under the CERN OHL v.1.2. You may  
redistribute and modify this documentation under the  
terms of the CERN OHL v.1.2.  
(<http://ohwr.org/CERNOHL>). This documentation is  
distributed WITHOUT ANY EXPRESS OR IMPLIED  
WARRANTY, INCLUDING OF  
MERCHANTABILITY, SATISFACTORY QUALITY  
AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable  
conditions.

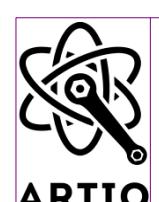
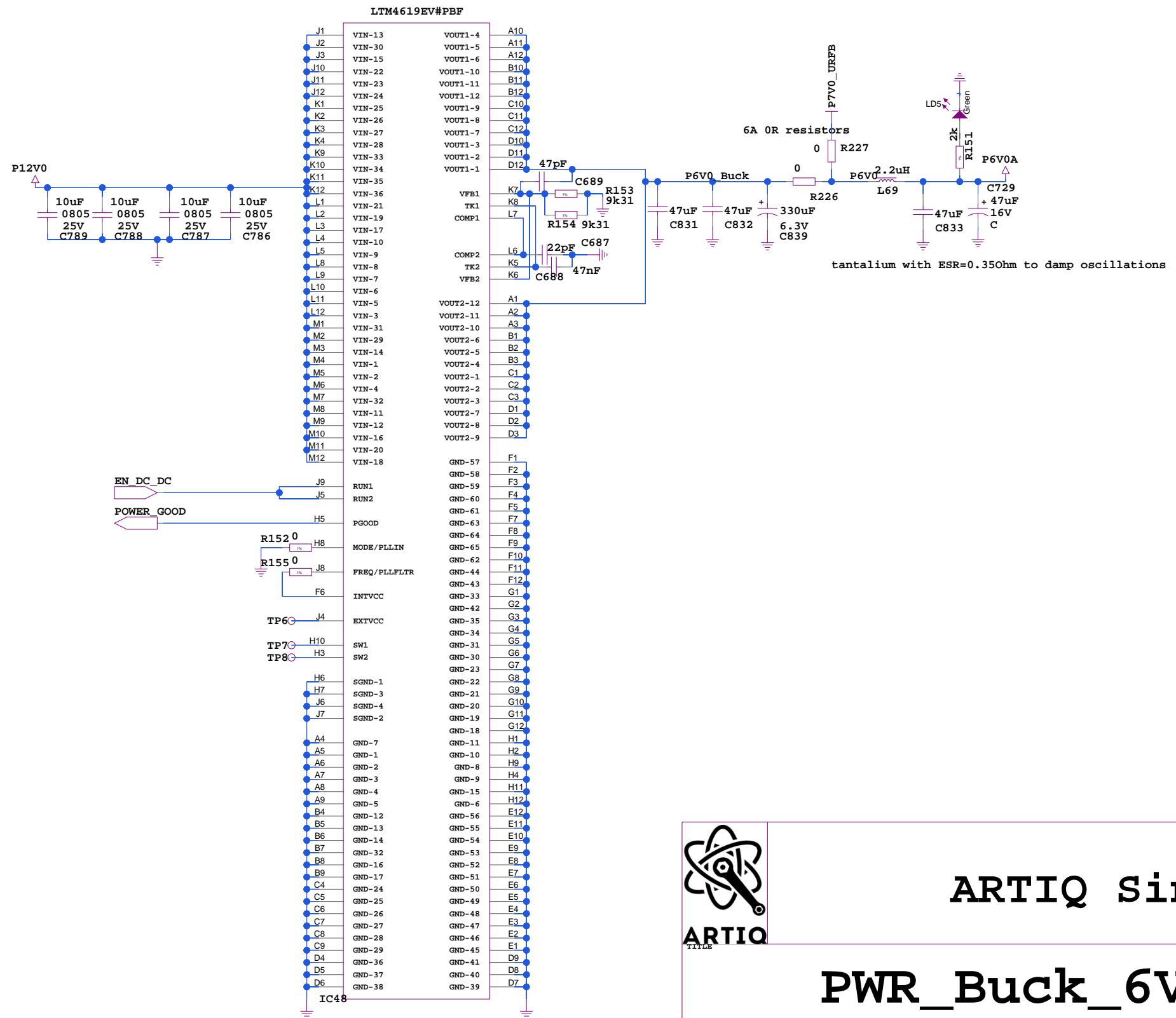
TITLE		<b>PWR_buck_FPGA_EXAR</b>		
SIZE	DWG NO			REV
<b>A3</b>		<b>1</b>		<b>v0.97</b>
DRAWN BY	SHEET	of		
<b>G.K.</b>	<b>17</b>	<b>23</b>	<b>13/02/2017:00:13</b>	



ARTIQ Sinara

PWR\_Buck\_2V\_4V\_4A

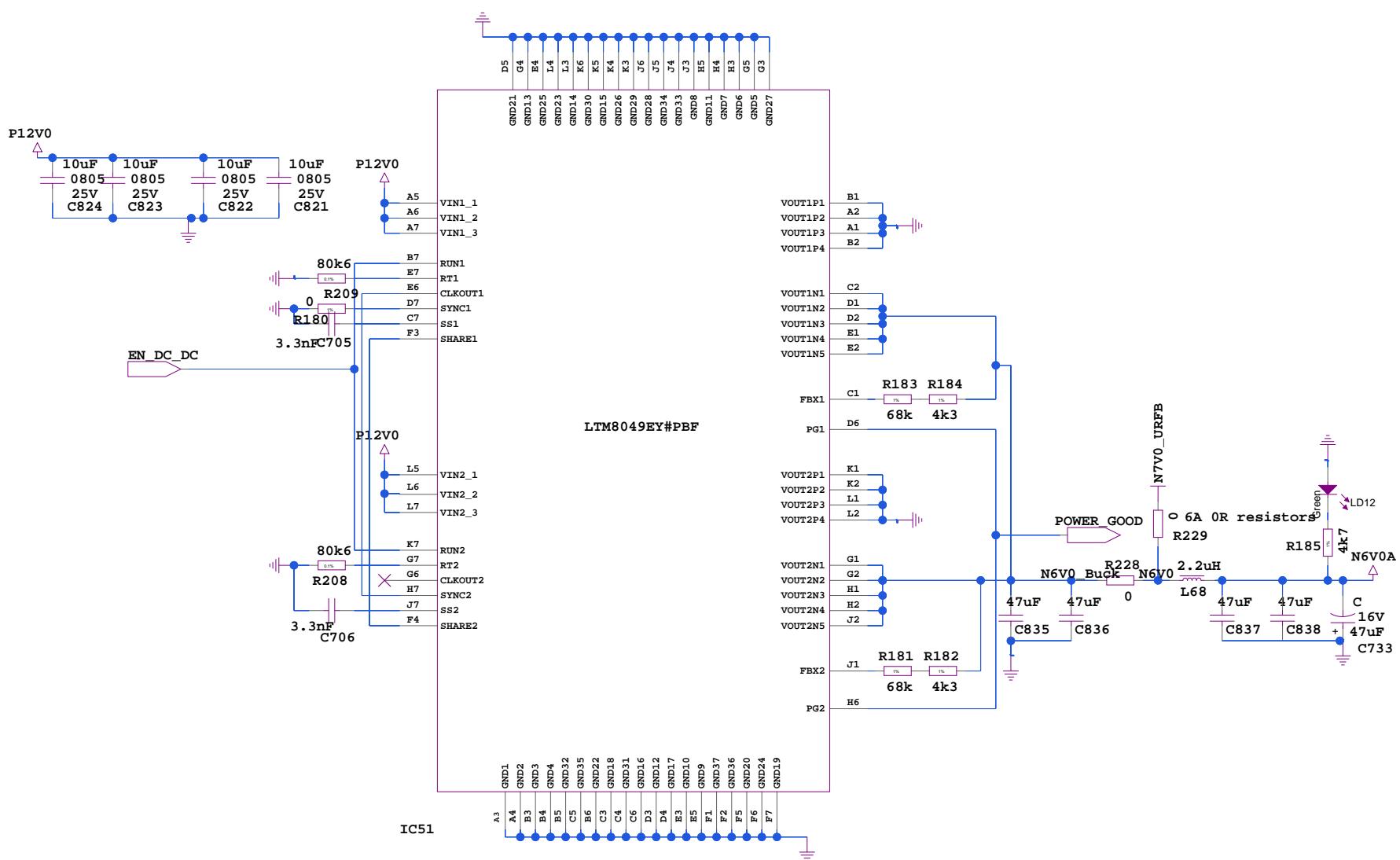
SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	18	23
24/01/2017:23:14		



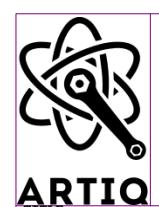
**ARTIQ Sinara**

**PWR\_Buck\_6V\_8A**

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET	of
G.K.	19	23



Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is  
licensed under the CERN OHL v.1.2. You may  
redistribute and modify this documentation under the  
terms of the CERN OHL v.1.2.  
(<http://ohwr.org/CERNOHL>). This documentation is  
distributed WITHOUT ANY EXPRESS OR IMPLIED  
WARRANTY, INCLUDING OF  
MERCHANTABILITY, SATISFACTORY QUALITY  
AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable  
conditions.



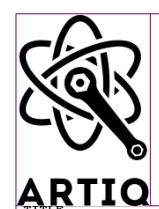
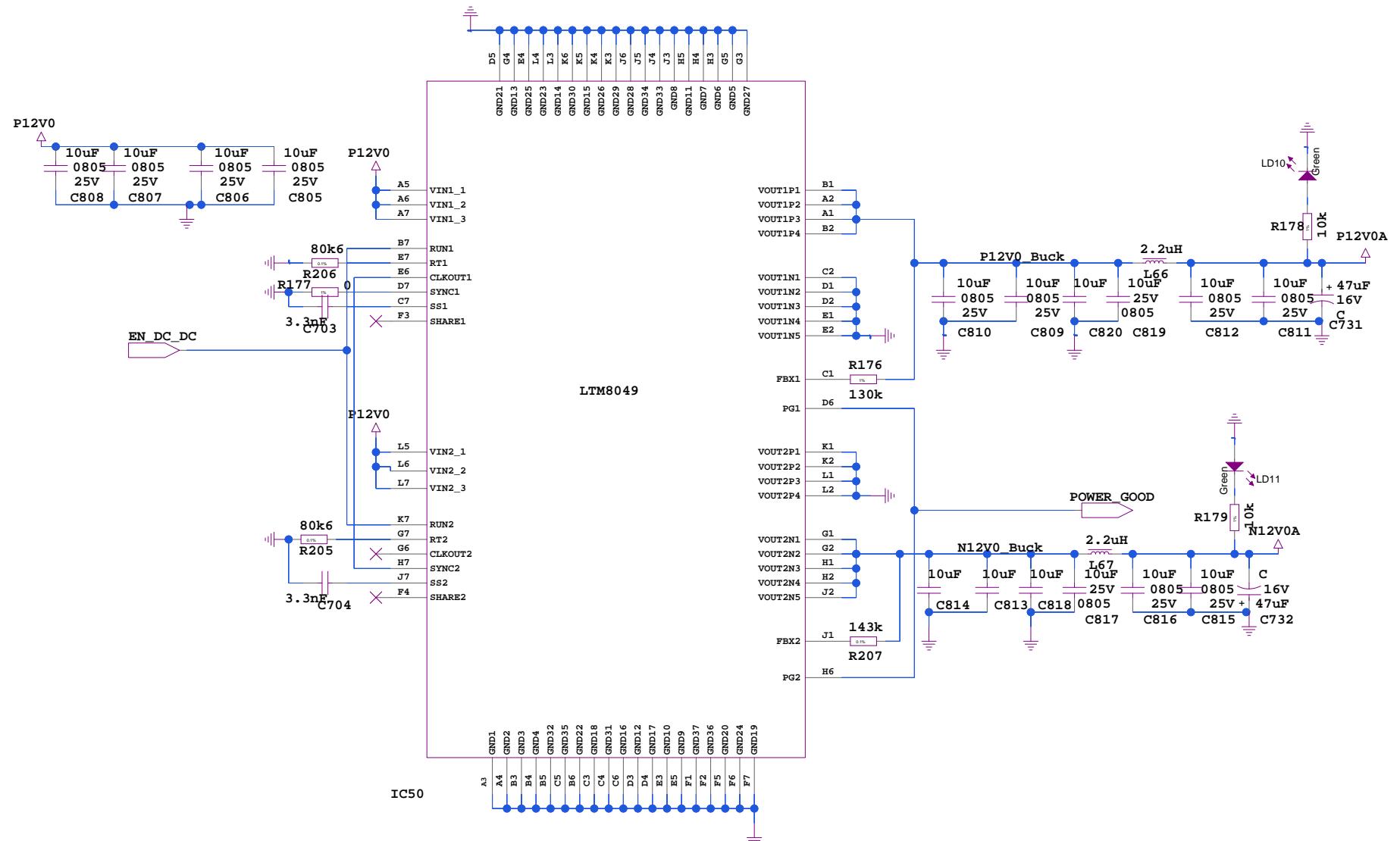
**ARTIQ Sinara**

**PWR\_SEPIC\_N6V**

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	20	23

1

24/01/2017:23:14

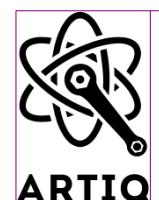
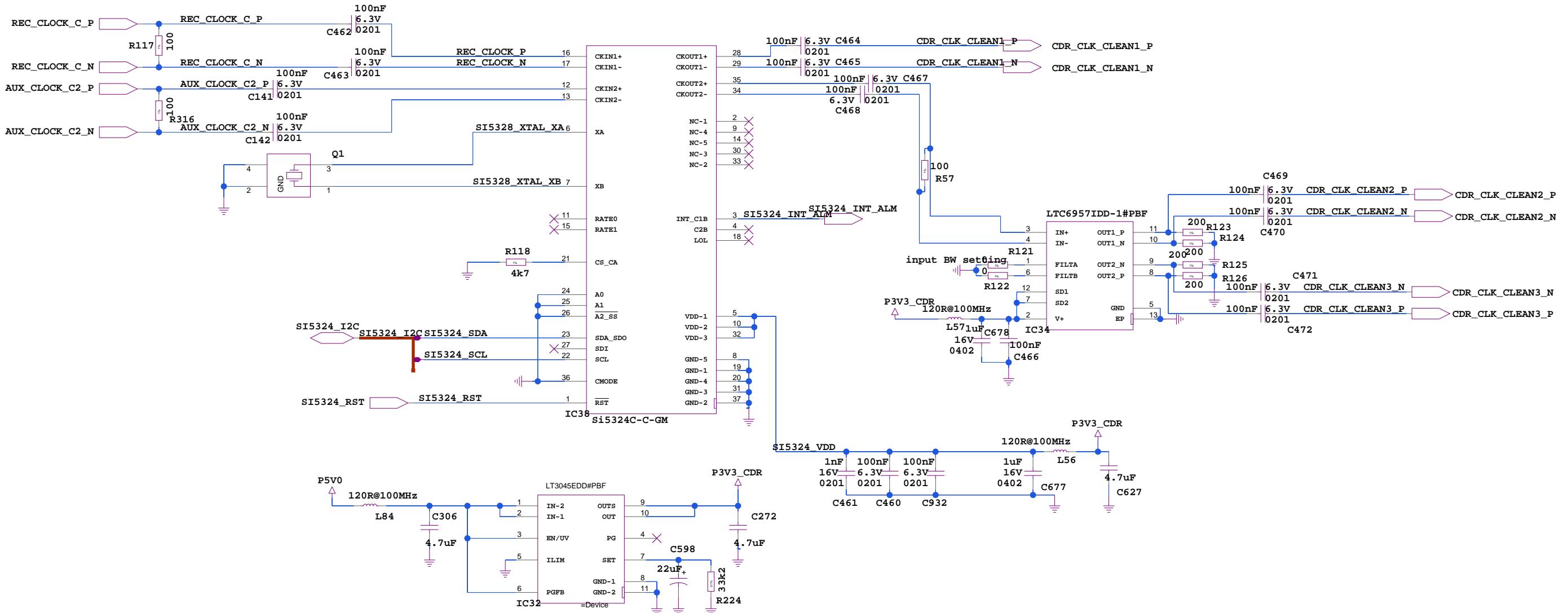


**ARTIQ Sinara**

## PWR\_SEPIC\_P12V\_N12V

SIZE	DWG NO	REV
A3		
DRAWN BY	SHEET of	
G.K.	21	23

Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.  
(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.  
Please see the CERN OHL v.1.2 for applicable conditions.

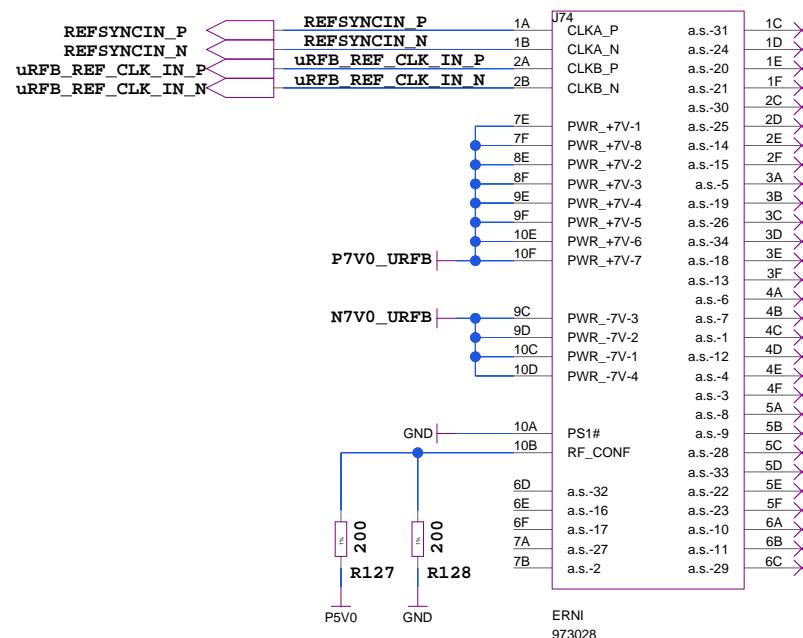


ARTIQ Sinara

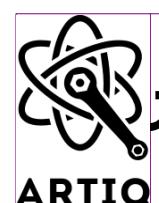
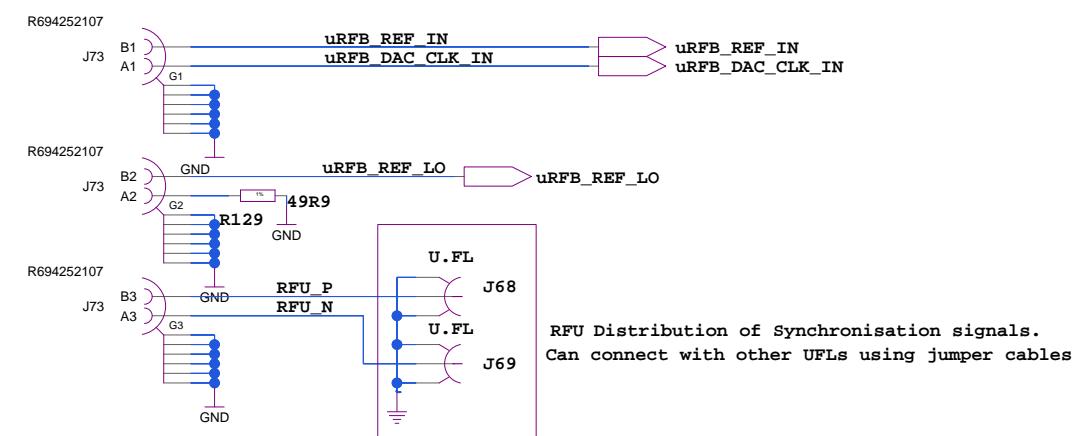
## SI5324\_CLK\_RECOVERY

Copyright ISE WUT 2016.  
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.  
https://cern.ch/CERNOHL This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions.

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	22	23



**Interfaces uRFB:**  
 uRFB\_REF\_IN : LVPECL  
 uRFB\_DAC\_CLK\_IN: LVPECL  
 uRFB\_REF\_LO - LVPECL  
 Impedance 50Ω SE, 100Ω diff  
 REFSYNCIN\_P/N : LVPECL  
 uRFB\_REF\_CLK\_IN\_P/N: LVPECL



## uRFB\_Connectors

ARTIQ

ARTIQ Sinara

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	23	23