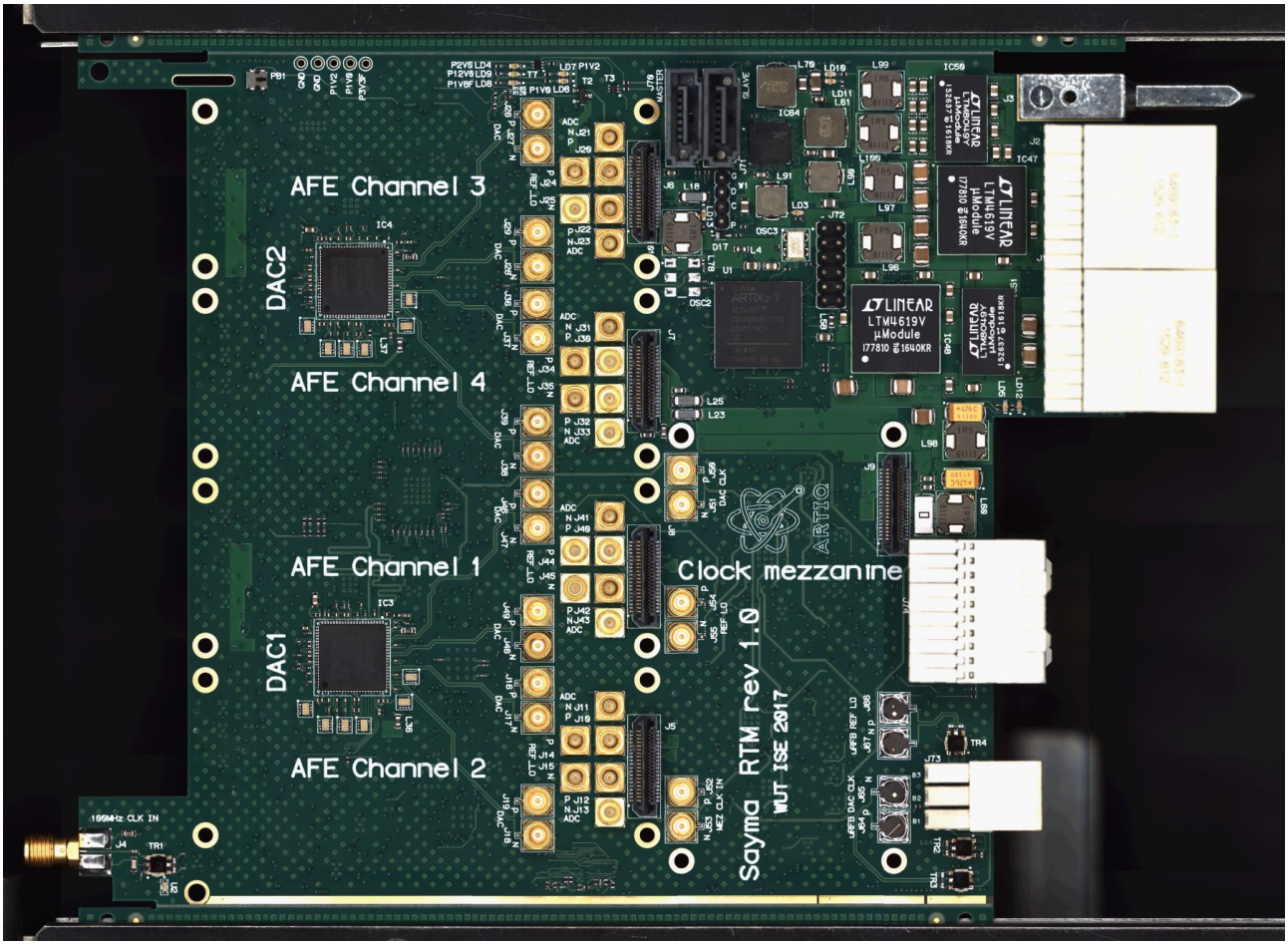
DRAFT

SAYMA RTM
specification



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Todo list

Contents

1 Project description **4**

2 Functional specifications **4**

3 Product view **5**

4 Routing **7**

5 Signal tables **9**

A Appendix **11**

1 Project description

The Sayma RTM module extends Sayma AMC board connectivity by DACs and ADCs modules.

2 Functional specifications

Programmable resources:

- Xilinx Artix-7 XC7A15T-1CSG325

Memory:

- EEPROM with MAC and unique ID

Connectivity:

- 4x mezzaninne connector LSS-120-01-L-DV-A
- 40x SMP connector for ADC/DAC
- Stand-alone 12V power connector
- RTM connector with 16 GTP pair routed to it.
- GTP on RTM connector connected to:
  - DAC x16 [Tx]
  - ADC x8 [Rx]
  - FPGA MGT 2x2 [Tx + Rx]
  - SATA x2
- uRFB connector

Supply:

- Monitoring of voltage and Power supply for FPGA and P3V3

Clocking:

- UFL CLK input
- SMA CLK output
- Si5324 Clock recovery

Other:

- Temperature, voltage and current monitoring for critical power buses

3 Product view

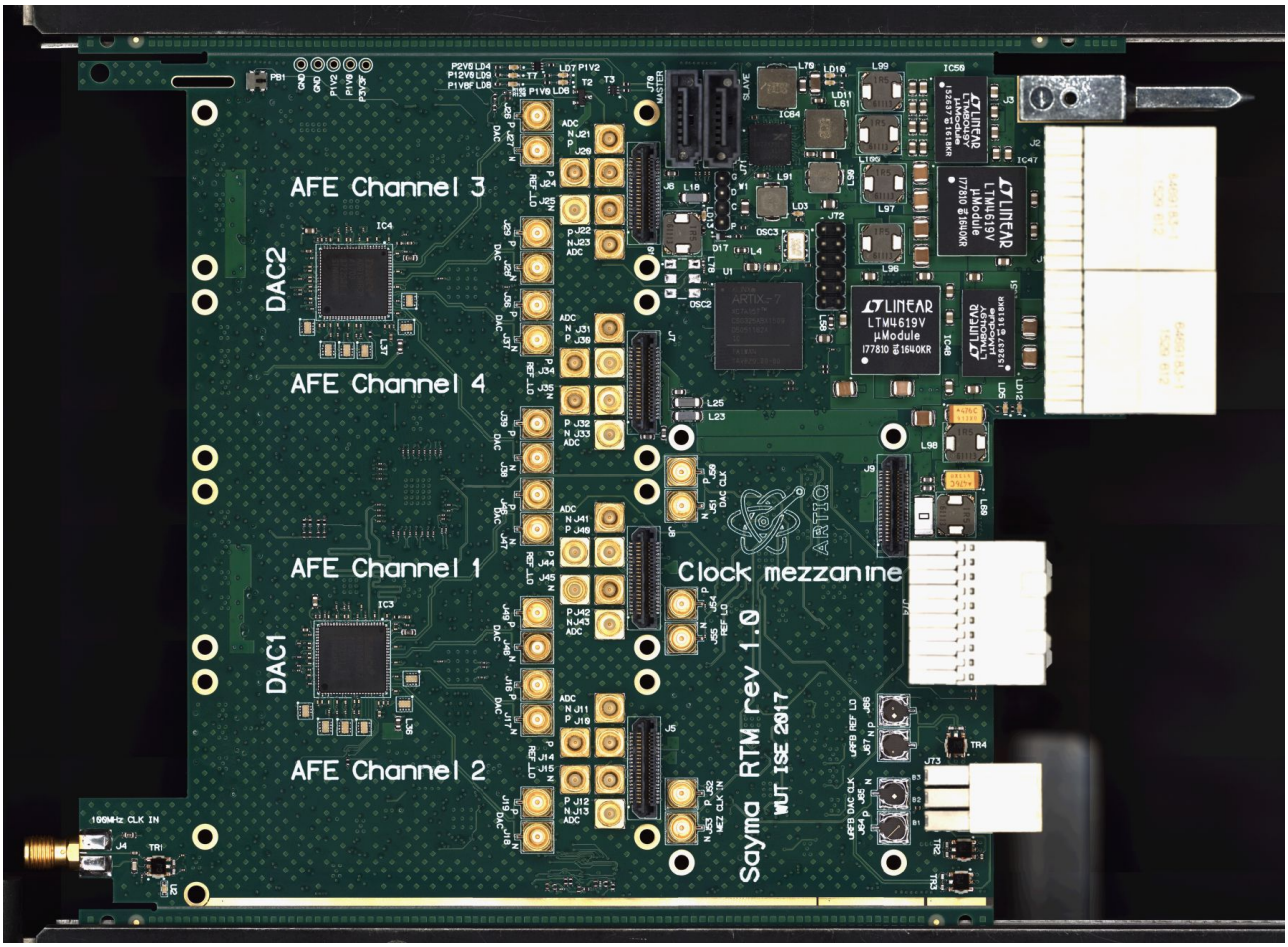

Figure 1: Top view

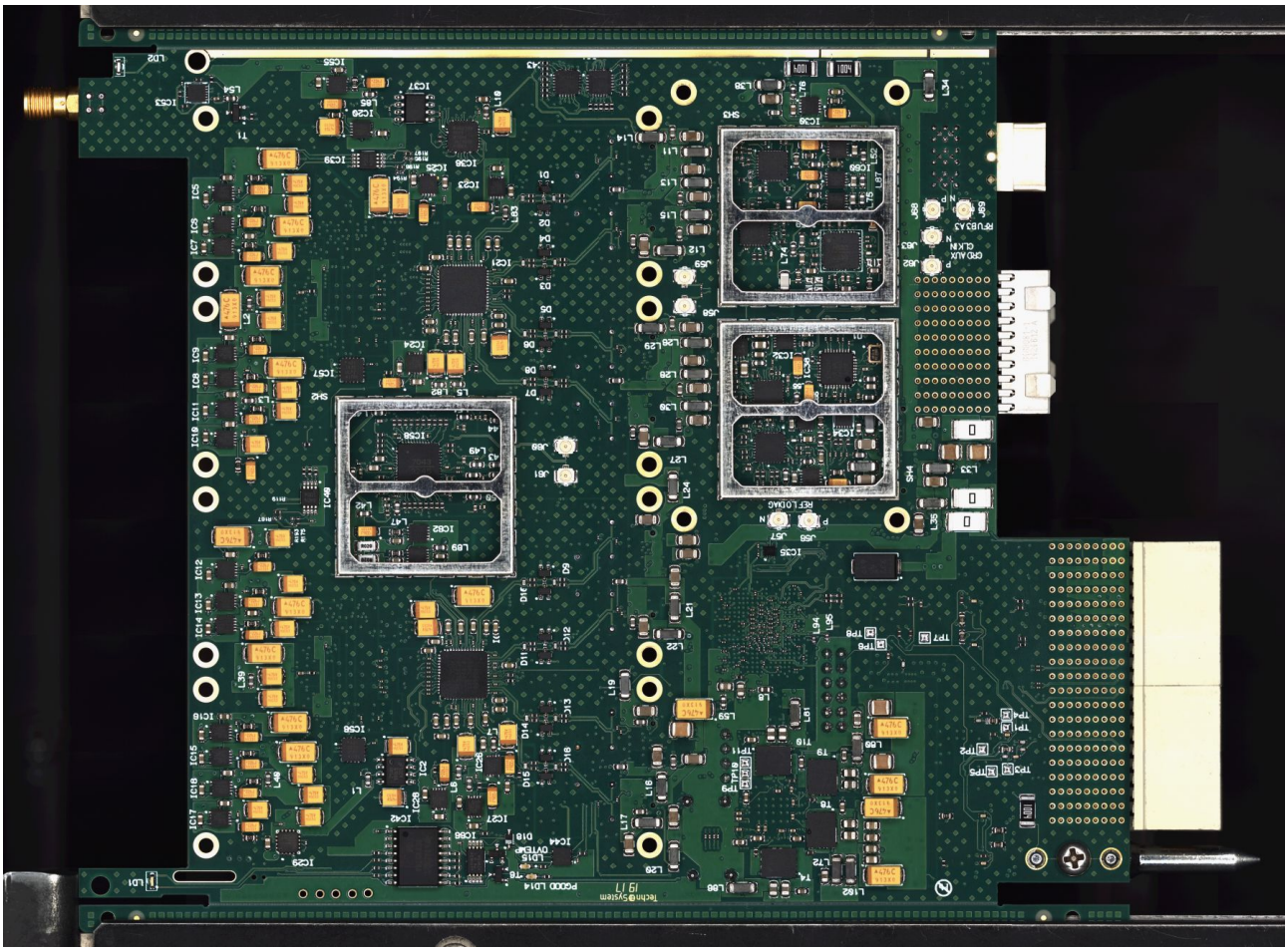

Figure 2: Bottom view

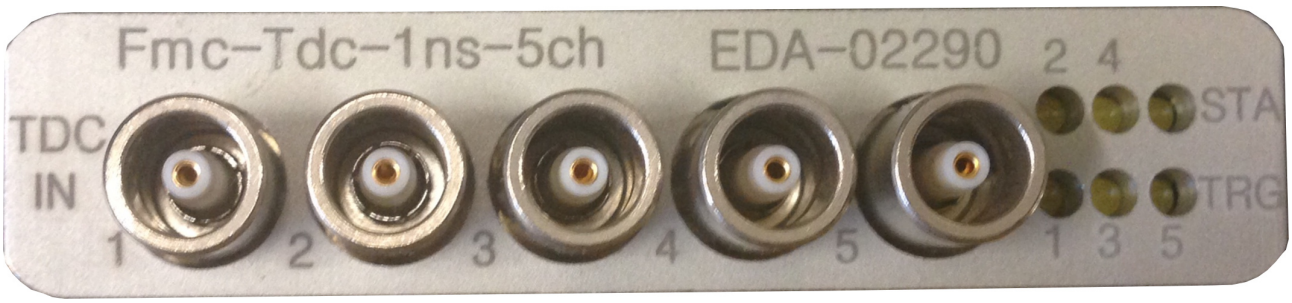

Figure 3: Front view

4 Routing

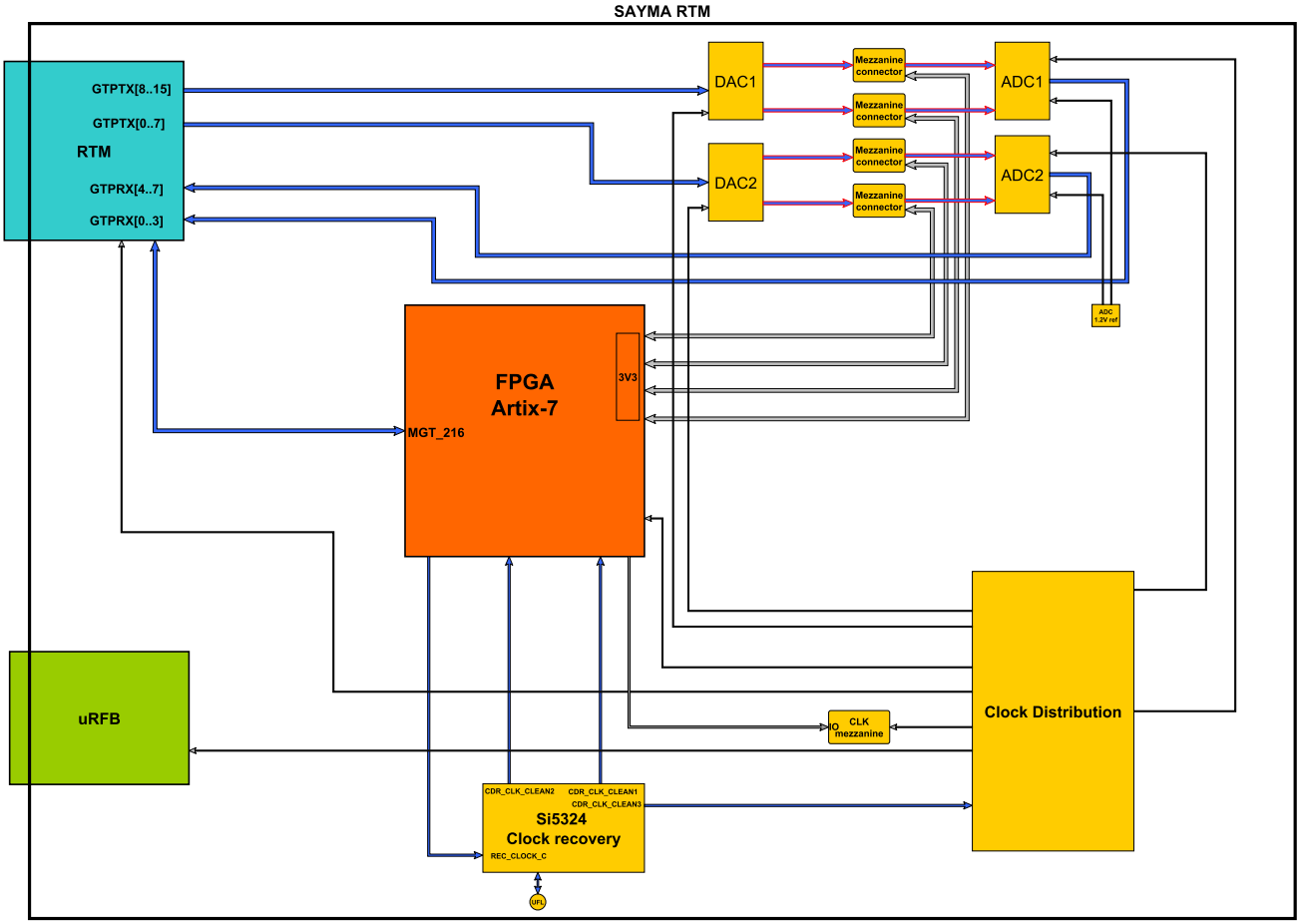

Figure 4: Block Scheme

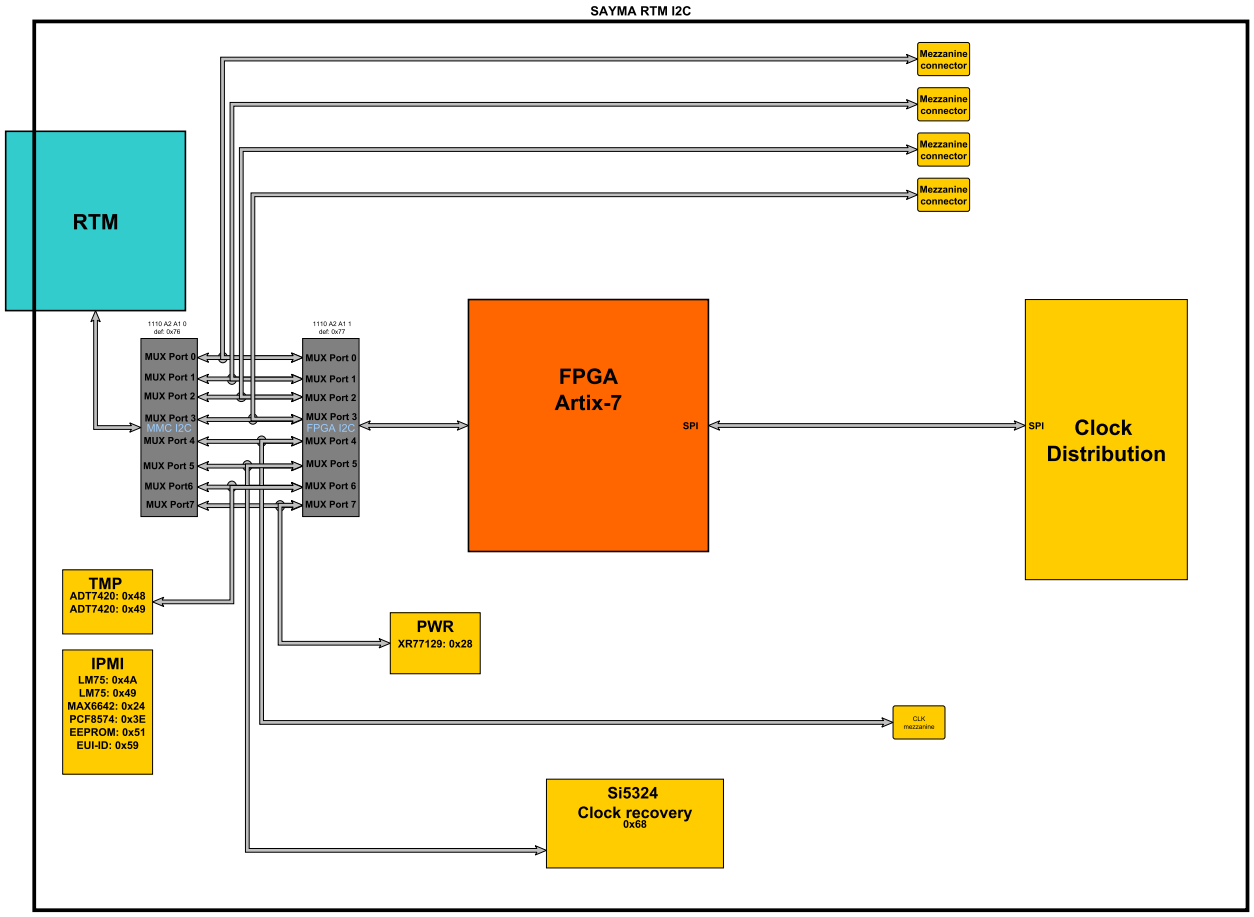

Figure 5: I2C

5 Signal tables

RTM		
E3	MGTPRXN0_216	RTM_FPGA_GTP_Rx0_N
E4	MGTPRXP0_216	RTM_FPGA_GTP_Rx0_P
H1	MGTPTXN0_216	RTM_FPGA_GTP_Tx0C_N
H2	MGTPTXP0_216	RTM_FPGA_GTP_Tx0C_P
A3	MGTPRXN1_216	RTM_FPGA_GTP_Rx1_N
A4	MGTPRXP1_216	RTM_FPGA_GTP_Rx1_P
F1	MGTPTXN1_216	RTM_FPGA_GTP_Tx1C_N
F2	MGTPTXP1_216	RTM_FPGA_GTP_Tx1C_P
C3	MGTPRXN2_216	RTM_FPGA_GTP_Rx2_N
C4	MGTPRXP2_216	RTM_FPGA_GTP_Rx2_P
D1	MGTPTXN2_216	RTM_FPGA_GTP_Tx2C_N
D2	MGTPTXP2_216	RTM_FPGA_GTP_Tx2C_P
G3	MGTPRXN3_216	RTM_FPGA_GTP_Rx3_N
G4	MGTPRXP3_216	RTM_FPGA_GTP_Rx3_P
B1	MGTPTXN3_216	RTM_FPGA_GTP_Tx3C_N
B2	MGTPTXP3_216	RTM_FPGA_GTP_Tx3C_P
D5	MGTREFCLK0N_216	RTM_FPGA_GTP_CLKC_P
D6	MGTREFCLK0P_216	RTM_FPGA_GTP_CLKC_N
J6	IO_0_34	RTM_FPGA_SCL
K6	IO_L1P_T0_34	RTM_FPGA_SDA
P14	IO_L12P_T1_MRCC_14	RTM_MASTER_AUX_CLK_P
R15	IO_L12N_T1_MRCC_14	RTM_MASTER_AUX_CLK_N
R16	IO_L14P_T2_SRCC_14	RTM_FPGA_LVDS1_P
R17	IO_L14N_T2_SRCC_14	RTM_FPGA_LVDS1_N
T17	IO_L16P_T2_CSI_B_14	RTM_FPGA_LVDS2_P
U17	IO_L16N_T2_A15_D31_14	RTM_FPGA_LVDS2_N
T18	IO_L15N_T2_DQS_DOUT_CSO_B_14	RTM_FPGA_USR_IO_N
P14	IO_L12P_T1_MRCC_14	RTM_MASTER_AUX_CLK_P
R15	IO_L12N_T1_MRCC_14	RTM_MASTER_AUX_CLK_N

Mezzanine1 IO		
P1	IO_L9N_T1_DQS_34	MEZZ1_IO0
M4	IO_L10P_T1_34	MEZZ1_IO1
N4	IO_L10N_T1_34	MEZZ1_IO2
N3	IO_L11P_T1_SRCC_34	MEZZ1_IO3
N2	IO_L11N_T1_SRCC_34	MEZZ1_IO4
P4	IO_L12P_T1_MRCC_34	MEZZ1_IO5
P3	IO_L12N_T1_MRCC_34	MEZZ1_IO6
R2	IO_L13P_T2_MRCC_34	MEZZ1_IO7
R1	IO_L13N_T2_MRCC_34	MEZZ1_IO8
R3	IO_L14P_T2_SRCC_34	MEZZ1_IO9
T2	IO_L14N_T2_SRCC_34	MEZZ1_IO10
U2	IO_L15P_T2_DQS_34	MEZZ1_IO11
U1	IO_L15N_T2_DQS_34	MEZZ1_IO12
V3	IO_L16P_T2_34	MEZZ1_IO13
V2	IO_L16N_T2_34	MEZZ1_IO14
T4	IO_L17P_T2_34	MEZZ1_IO15

Mezzanine2 IO		
T3	IO_L17N_T2_34	MEZZ2_IO0
U4	IO_L18P_T2_34	MEZZ2_IO1
V4	IO_L18N_T2_34	MEZZ2_IO2
P6	IO_L19P_T3_34	MEZZ2_IO3
P5	IO_L19N_T3_VREF_34	MEZZ2_IO4
U6	IO_L20P_T3_34	MEZZ2_IO5
U5	IO_L20N_T3_34	MEZZ2_IO6
R5	IO_L21P_T3_DQS_34	MEZZ2_IO7
T5	IO_L21N_T3_DQS_34	MEZZ2_IO8
R7	IO_L22P_T3_34	MEZZ2_IO9
T7	IO_L22N_T3_34	MEZZ2_IO10
U7	IO_L23P_T3_34	MEZZ2_IO11
V6	IO_L23N_T3_34	MEZZ2_IO12
V8	IO_L24P_T3_34	MEZZ2_IO13
V7	IO_L24N_T3_34	MEZZ2_IO14
R6	IO_25_34	MEZZ2_IO15

Mezzanine3 IO		
D11	IO_L6P_T0_15	MEZZ3_IO0
C12	IO_L6N_T0_VREF_15	MEZZ3_IO1
B12	IO_L7P_T1_AD2P_15	MEZZ3_IO2
A12	IO_L7N_T1_AD2N_15	MEZZ3_IO3
A13	IO_L8P_T1_AD10P_15	MEZZ3_IO4
A14	IO_L8N_T1_AD10N_15	MEZZ3_IO5
C14	IO_L9P_T1_DQS_AD3P_15	MEZZ3_IO6
B15	IO_L9N_T1_DQS_AD3N_15	MEZZ3_IO7
B14	IO_L10P_T1_AD11P_15	MEZZ3_IO8
A15	IO_L10N_T1_AD11N_15	MEZZ3_IO9
D13	IO_L11P_T1_SRCC_15	MEZZ3_IO10
C13	IO_L11N_T1_SRCC_15	MEZZ3_IO11
E13	IO_L12P_T1_MRCC_15	MEZZ3_IO12
D14	IO_L12N_T1_MRCC_15	MEZZ3_IO13
D15	IO_L13N_T2_MRCC_15	MEZZ3_IO14
E16	IO_L14P_T2_SRCC_15	MEZZ3_IO15

Mezzanine4 IO		
K5	IO_L1N_T0_34	MEZZ4_IO0
J5	IO_L2P_T0_34	MEZZ4_IO1
J4	IO_L2N_T0_34	MEZZ4_IO2
K2	IO_L3P_T0_DQS_34	MEZZ4_IO3
K1	IO_L3N_T0_DQS_34	MEZZ4_IO4
K3	IO_L4P_T0_34	MEZZ4_IO5
L2	IO_L4N_T0_34	MEZZ4_IO6
L4	IO_L5P_T0_34	MEZZ4_IO7
L3	IO_L5N_T0_34	MEZZ4_IO8
L5	IO_L6P_T0_34	MEZZ4_IO9
M5	IO_L6N_T0_VREF_34	MEZZ4_IO10
M2	IO_L7P_T1_34	MEZZ4_IO11

M1	IO_L7N_T1_34	MEZZ4_IO12
M6	IO_L8P_T1_34	MEZZ4_IO13
N6	IO_L8N_T1_34	MEZZ4_IO14
N1	IO_L9P_T1_DQS_34	MEZZ4_IO15

Mezzanine CLK IO		
D18	IO_L17N_T2_A25_15	CLK_MEZZ_IO0
C17	IO_L18P_T2_A24_15	CLK_MEZZ_IO1
C18	IO_L18N_T2_A23_15	CLK_MEZZ_IO2
G17	IO_L19P_T3_A22_15	CLK_MEZZ_IO3
F18	IO_L19N_T3_A21_VREF_15	CLK_MEZZ_IO4
H16	IO_L20P_T3_A20_15	CLK_MEZZ_IO5
G16	IO_L20N_T3_A19_15	CLK_MEZZ_IO6
G15	IO_L21P_T3_DQS_15	CLK_MEZZ_IO7
F15	IO_L21N_T3_DQS_A18_15	CLK_MEZZ_IO8
G14	IO_L22P_T3_A17_15	CLK_MEZZ_IO9
F14	IO_L22N_T3_A16_15	CLK_MEZZ_IO10
H17	IO_L23P_T3_FOE_B_15	CLK_MEZZ_IO11
H18	IO_L23N_T3_FWE_B_15	CLK_MEZZ_IO12
F17	IO_L24P_T3_RS1_15	CLK_MEZZ_IO13
H14	IO_25_15	CLK_MEZZ_IO14
	IO_L24N_T3_RS0_15	CLK_MEZZ_IO15

A Appendix

FPGA ball	FPGA signal	Signal on the board
A1	GND	GND
A2	MGTAVTT	MGTAVTT
A3	MGTPRXN1_216	RTM_FPGA_GTP_Rx1_N
A4	MGTPRXP1_216	RTM_FPGA_GTP_Rx1_P
A5	GND_3	GND
A6	MGTRREF_216	NC
A7	GND_4	GND
A8	GND_5	GND
A9	IO_L3N_T0_DQS_AD1N_15	CAL_ADC_MCLK1
A10	IO_L5N_T0_AD9N_15	CAL_ADC_CSn
A11	GND_1	GND
A12	IO_L7N_T1_AD2N_15	MEZZ3_IO3
A13	IO_L8P_T1_AD10P_15	MEZZ3_IO4
A14	IO_L8N_T1_AD10N_15	MEZZ3_IO5
A15	IO_L10N_T1_AD11N_15	MEZZ3_IO9
A16	VCCO_15	P3V3F
A17	IO_L15N_T2_DQS_ADV_B_15	HMC_SPI_SCLK
A18	GND_2	GND
B1	MGTPTXN3_216	RTM_FPGA_GTP_Tx3C_N
B2	MGTPTXP3_216	RTM_FPGA_GTP_Tx3C_P
B3	GND_7	GND
B4	MGTAVCC	MGTAVCC
B5	MGTREFCLK1N_216	CDR_CLK_CLEAN1_N
B6	MGTREFCLK1P_216	CDR_CLK_CLEAN1_P
B7	GND_8	GND
B8	GND_9	GND
B9	IO_L3P_T0_DQS_AD1P_15	CAL_ADC_MCLK2
B10	IO_L5P_T0_AD9P_15	CAL_ADC_SYNCn
B11	IO_L4N_T0_15	CAL_ADC_DIN
B12	IO_L7P_T1_AD2P_15	MEZZ3_IO2
B13	VCCO_15_1	P3V3F
B14	IO_L10P_T1_AD11P_15	MEZZ3_IO8
B15	IO_L9N_T1_DQS_AD3N_15	MEZZ3_IO7
B16	IO_L15P_T2_DQS_15	HMC_SPI_SDATA
B17	IO_L16N_T2_A27_15	USR_UART_N
B18	GND_6	GND
C1	MGTAVTT_1	MGTAVTT
C2	GND_11	GND
C3	MGTPRXN2_216	RTM_FPGA_GTP_Rx2_N
C4	MGTPRXP2_216	RTM_FPGA_GTP_Rx2_P
C5	MGTAVCC_1	MGTAVCC
C6	GND_12	GND
C7	GND_13	GND
C8	IO_L1N_T0_AD0N_15	HMC830_SPI_SEN
C9	IO_L2N_T0_AD8N_15	CAL_ADC_SCLK
C10	VCCO_15_2	P3V3F
C11	IO_L4P_T0_15	CAL_ADC_DOUT
C12	IO_L6N_T0_VREF_15	MEZZ3_IO1
C13	IO_L11N_T1_SRCC_15	MEZZ3_IO11
C14	IO_L9P_T1_DQS_AD3P_15	MEZZ3_IO6

C15	GND_10	GND
C16	IO_L16P_T2_A28_15	USR_UART_P
C17	IO_L18P_T2_A24_15	CLK_MEZZ_IO1
C18	IO_L18N_T2_A23_15	CLK_MEZZ_IO2
D1	MGTPTXN2_216	RTM_FPGA_GTP_Tx2C_N
D2	MGTPTXP2_216	RTM_FPGA_GTP_Tx2C_P
D3	GND_15	GND
D4	GND_16	GND
D5	MGTREFCLK0N_216	RTM_FPGA_GTP_CLKC_P
D6	MGTREFCLK0P_216	RTM_FPGA_GTP_CLKC_N
D7	GND_17	GND
D8	IO_L1P_T0_AD0P_15	HMC_SPI_GPIO
D9	IO_L2P_T0_AD8P_15	HMC_SPI_SDO
D10	IO_0_15	SI5324_INT_ALM
D11	IO_L6P_T0_15	MEZZ3_IO0
D12	GND_14	GND
D13	IO_L11P_T1_SRCC_15	MEZZ3_IO10
D14	IO_L12N_T1_MRCC_15	MEZZ3_IO13
D15	IO_L13N_T2_MRCC_15	MEZZ3_IO14
D16	IO_L14N_T2_SRCC_15	HMC7043_SLEN
D17	VCCO_15_3	P3V3F
D18	IO_L17N_T2_A25_15	CLK_MEZZ_IO0
E1	MGTAVTT_2	MGTAVTT
E2	GND_18	GND
E3	MGTPRXN0_216	RTM_FPGA_GTP_Rx0_N
E4	MGTPRXP0_216	RTM_FPGA_GTP_Rx0_P
E5	MGTAVCC_2	MGTAVCC
E6	GND_19	GND
E7	GND_20	GND
E8	CCLK_0	FPGA_CFG_CCLK
E9	GND_21	GND
E10	VCCO_0	P3V3F
E11	VCCBATT_0	P1V8F
E12	CFGBVS_0	NC
E13	IO_L12P_T1_MRCC_15	MEZZ3_IO12
E14	VCCO_15_4	P3V3F
E15	IO_L13P_T2_MRCC_15	NC
E16	IO_L14P_T2_SRCC_15	MEZZ3_IO15
E17	IO_L17P_T2_A26_15	SI5324_RST
E18	IO_L24N_T3_RS0_15	CLK_MEZZ_IO15
F1	MGTPTXN1_216	RTM_FPGA_GTP_Tx1C_N
F2	MGTPTXP1_216	RTM_FPGA_GTP_Tx1C_P
F3	MGTAVTT_3	MGTAVTT
F4	GND_24	GND
F5	MGTAVCC_3	MGTAVCC
F6	GND_25	GND
F7	VCCINT	P1V0
F8	TCK_0	TCK
F9	VCCINT_1	P1V0
F10	GND_22	GND
F11	VCCBRAM	VCCBRAM
F12	DONE_0	FPGA_CFG_DONE
F13	M2_0	NC

F14	IO_L22N_T3_A16_15	CLK_MEZZ_IO10
F15	IO_L21N_T3_DQS_A18_15	CLK_MEZZ_IO8
F16	GND_23	GND
F17	IO_L24P_T3_RS1_15	CLK_MEZZ_IO13
F18	IO_L19N_T3_A21_VREF_15	CLK_MEZZ_IO4
G1	GND_26	GND
G2	MGTAVTT_4	MGTAVTT
G3	MGTPRXN3_216	RTM_FPGA_GTP_Rx3_N
G4	MGTPRXP3_216	RTM_FPGA_GTP_Rx3_P
G5	GND_29	GND
G6	GND_30	GND
G7	GND_31	GND
G8	VCCINT_2	P1V0
G9	GND_32	GND
G10	VCCBRAM_1	VCCBRAM
G11	GND_27	GND
G12	VCCAUX	VCCAUX
G13	GND_28	GND
G14	IO_L22P_T3_A17_15	CLK_MEZZ_IO9
G15	IO_L21P_T3_DQS_15	CLK_MEZZ_IO7
G16	IO_L20N_T3_A19_15	CLK_MEZZ_IO6
G17	IO_L19P_T3_A22_15	CLK_MEZZ_IO3
G18	VCCO_15_5	P3V3F
H1	MGTPTXN0_216	RTM_FPGA_GTP_Tx0C_N
H2	MGTPTXP0_216	RTM_FPGA_GTP_Tx0C_P
H3	GND_35	GND
H4	GND_36	GND
H5	GND_37	GND
H6	GND_38	GND
H7	VCCINT_3	P1V0
H8	GND_39	GND
H9	VCCINT_4	P1V0
H10	GND_33	GND
H11	VCCBRAM_2	VCCBRAM
H12	GND_34	GND
H13	VCCAUX_1	VCCAUX
H14	IO_25_15	CLK_MEZZ_IO14
H15	VCCO_15_6	P3V3F
H16	IO_L20P_T3_A20_15	CLK_MEZZ_IO5
H17	IO_L23P_T3_FOE_B_15	CLK_MEZZ_IO11
H18	IO_L23N_T3_FWE_B_15	CLK_MEZZ_IO12
J1	GND_40	GND
J2	GND_44	GND
J3	GND_45	GND
J4	IO_L2N_T0_34	MEZZ4_IO2
J5	IO_L2P_T0_34	MEZZ4_IO1
J6	IO_0_34	RTM_FPGA_SCL
J7	GND_46	GND
J8	VCCINT_6	P1V0
J9	GNDADC_0	NC
J10	VCCADC_0	NC
J11	GND_41	GND
J12	VCCINT_5	P1V0

J13	GND_42	GND
J14	IO_L5P_T0_D06_14	REF_CLK_SRC_SEL_1V8
J15	IO_L2P_T0_D02_14	DAC2_SPI_SDIO
J16	IO_L2N_T0_D03_14	DAC2_SPI_SDO
J17	GND_43	GND
J18	IO_L3P_T0_DQS_PUDC_B_14	DAC2_SPI_SCLK
K1	IO_L3N_T0_DQS_34	MEZZ4_IO4
K2	IO_L3P_T0_DQS_34	MEZZ4_IO3
K3	IO_L4P_T0_34	MEZZ4_IO5
K4	GND_49	GND
K5	IO_L1N_T0_34	MEZZ4_IO0
K6	IO_L1P_T0_34	RTM_FPGA_SDA
K7	VCCINT_8	P1V0
K8	GND_50	GND
K9	VREFN_0	NC
K10	VP_0	NC
K11	VCCINT_7	P1V0
K12	GND_47	GND
K13	VCCAUX_2	VCCAUX
K14	GND_48	GND
K15	IO_L5N_T0_D07_14	NC
K16	IO_L1P_T0_D00_MOSI_14	NC
K17	IO_L4P_T0_D04_14	DAC2_IRQn
K18	IO_L3N_T0_DQS_EMCCLK_14	DAC2_SPI_CSn
L1	GND_51	GND
L2	IO_L4N_T0_34	MEZZ4_IO6
L3	IO_L5N_T0_34	MEZZ4_IO8
L4	IO_L5P_T0_34	MEZZ4_IO7
L5	IO_L6P_T0_34	MEZZ4_IO9
L6	VCCO_34	P3V3F
L7	GND_54	GND
L8	VCCINT_10	P1V0
L9	VN_0	NC
L10	VREFP_0	NC
L11	GND_52	GND
L12	VCCINT_9	P1V0
L13	GND_53	GND
L14	IO_0_14	DAC2_TXEN1
L15	IO_L6P_T0_FCS_B_14	DIO7
L16	VCCO_14	P1V8F
L17	IO_L1N_T0_D01_DIN_14	DAC2_TXEN0
L18	IO_L4N_T0_D05_14	REF_LO_CLK_SEL_1V8
M1	IO_L7N_T1_34	MEZZ4_IO12
M2	IO_L7P_T1_34	MEZZ4_IO11
M3	VCCO_34_1	P3V3F
M4	IO_L10P_T1_34	MEZZ1_IO1
M5	IO_L6N_T0_VREF_34	MEZZ4_IO10
M6	IO_L8P_T1_34	MEZZ4_IO13
M7	VCCINT_12	P1V0
M8	GND_57	GND
M9	DXN_0	FPGA_DXN
M10	DXP_0	FPGA_DXP
M11	VCCINT_11	P1V0

M12	GND_55	GND
M13	VCCAUX_3	VCCAUX
M14	IO_L8P_T1_D11_14	DIO5
M15	IO_L6N_T0_D08_VREF_14	DIO6
M16	IO_L7P_T1_D09_14	REC_CLOCK_P_1
M17	IO_L7N_T1_D10_14	REC_CLOCK_N_1
M18	GND_56	GND
N1	IO_L9P_T1_DQS_34	MEZZ4_IO15
N2	IO_L11N_T1_SRCC_34	MEZZ1_IO4
N3	IO_L11P_T1_SRCC_34	MEZZ1_IO3
N4	IO_L10N_T1_34	MEZZ1_IO2
N5	GND_61	GND
N6	IO_L8N_T1_34	MEZZ4_IO14
N7	GND_62	GND
N8	VCCINT_15	P1V0
N9	GND_63	GND
N10	VCCINT_13	P1V0
N11	GND_58	GND
N12	VCCINT_14	P1V0
N13	GND_59	GND
N14	IO_L8N_T1_D12_14	DIO4
N15	GND_60	GND
N16	IO_L9P_T1_DQS_14	DIO3
N17	IO_L9N_T1_DQS_D13_14	DIO2
N18	IO_L10P_T1_D14_14	DIO1
P1	IO_L9N_T1_DQS_34	MEZZ1_IO0
P2	GND_65	GND
P3	IO_L12N_T1_MRCC_34	MEZZ1_IO6
P4	IO_L12P_T1_MRCC_34	MEZZ1_IO5
P5	IO_L19N_T3_VREF_34	MEZZ2_IO4
P6	IO_L19P_T3_34	MEZZ2_IO3
P7	VCCO_34_2	P3V3F
P8	GND_66	GND
P9	VCCINT_17	P1V0
P10	PROGRAM_B_0	FPGA_CFG_PROGRAM_B
P11	VCCINT_16	P1V0
P12	GND_64	GND
P13	VCCAUX_4	VCCAUX
P14	IO_L12P_T1_MRCC_14	RTM_MASTER_AUX_CLK_P
P15	IO_L11P_T1_SRCC_14	REF_CLK_SRC_EXT_SEL_1V8
P16	IO_L11N_T1_SRCC_14	DAC_CLK_SRC_SEL_1V8
P17	VCCO_14_1	P1V8F
P18	IO_L10N_T1_D15_14	DIO0
R1	IO_L13N_T2_MRCC_34	MEZZ1_IO8
R2	IO_L13P_T2_MRCC_34	MEZZ1_IO7
R3	IO_L14P_T2_SRCC_34	MEZZ1_IO9
R4	VCCO_34_3	P3V3F
R5	IO_L21P_T3_DQS_34	MEZZ2_IO7
R6	IO_25_34	MEZZ2_IO15
R7	IO_L22P_T3_34	MEZZ2_IO9
R8	TMS_0	TMS
R9	GND_67	GND
R10	VCCO_0_1	P3V3F

R11	M1_0	NC
R12	M0_0	NC
R13	IO_L19P_T3_A10_D26_14	DAC1_SPI_SDO
R14	VCCO_14_2	P1V8F
R15	IO_L12N_T1_MRCC_14	RTM_MASTER_AUX_CLK_N
R16	IO_L14P_T2_SRCC_14	RTM_FPGA_LVDS1_P
R17	IO_L14N_T2_SRCC_14	RTM_FPGA_LVDS1_N
R18	IO_L15P_T2_DQS_RDWR_B_14	RTM_FPGA_USR_IO_P
T1	VCCO_34_4	P3V3F
T2	IO_L14N_T2_SRCC_34	MEZZ1_IO10
T3	IO_L17N_T2_34	MEZZ2_IO0
T4	IO_L17P_T2_34	MEZZ1_IO15
T5	IO_L21N_T3_DQS_34	MEZZ2_IO8
T6	GND_69	GND
T7	IO_L22N_T3_34	MEZZ2_IO10
T8	TDO_0	TDO
T9	TDI_0	TDI
T10	INIT_B_0	FPGA_CFG_INIT_B
T11	VCCO_14_3	P1V8F
T12	IO_L22P_T3_A05_D21_14	ADC2_CSB
T13	IO_L19N_T3_A09_D25_VREF_14	DAC1_SPI_SCLK
T14	IO_L13P_T2_MRCC_14	CDR_CLK_CLEAN2_P
T15	IO_L13N_T2_MRCC_14	CDR_CLK_CLEAN2_N
T16	GND_68	GND
T17	IO_L16P_T2_CSI_B_14	RTM_FPGA_LVDS2_P
T18	IO_L15N_T2_DQS_DOUT_CSO_B_14	RTM_FPGA_USR_IO_N
U1	IO_L15N_T2_DQS_34	MEZZ1_IO12
U2	IO_L15P_T2_DQS_34	MEZZ1_IO11
U3	GND_71	GND
U4	IO_L18P_T2_34	MEZZ2_IO1
U5	IO_L20N_T3_34	MEZZ2_IO6
U6	IO_L20P_T3_34	MEZZ2_IO5
U7	IO_L23P_T3_34	MEZZ2_IO11
U8	VCCO_14_5	P1V8F
U9	IO_L24P_T3_A01_D17_14	ADC1_CSB
U10	IO_25_14	ADC1_SDIO
U11	IO_L23P_T3_A03_D19_14	ADC1_SYNC
U12	IO_L22N_T3_A04_D20_14	ADC2_SDIO
U13	GND_70	GND
U14	IO_L20P_T3_A08_D24_14	DAC1_SPI_CSn
U15	IO_L17P_T2_A14_D30_14	DAC2_RESETn
U16	IO_L17N_T2_A13_D29_14	DAC1_TXEN1
U17	IO_L16N_T2_A15_D31_14	RTM_FPGA_LVDS2_N
U18	VCCO_14_4	P1V8F
V1	GND_72	GND
V2	IO_L16N_T2_34	MEZZ1_IO14
V3	IO_L16P_T2_34	MEZZ1_IO13
V4	IO_L18N_T2_34	MEZZ2_IO2
V5	VCCO_34_5	P3V3F
V6	IO_L23N_T3_34	MEZZ2_IO12
V7	IO_L24N_T3_34	MEZZ2_IO14
V8	IO_L24P_T3_34	MEZZ2_IO13
V9	IO_L24N_T3_A00_D16_14	ADC2_PDWN

V10	GND_73	GND
V11	IO_L23N_T3_A02_D18_14	ADC1_SCLK
V12	IO_L21P_T3_DQS_14	ADC2_SYNC
V13	IO_L21N_T3_DQS_A06_D22_14	ADC2_SCLK
V14	IO_L20N_T3_A07_D23_14	DAC1_IRQn
V15	VCCO_14_6	P1V8F
V16	IO_L18P_T2_A12_D28_14	DAC1_TXEN0
V17	IO_L18N_T2_A11_D27_14	DAC1_SPI_SDIO
V18	GND_74	GND