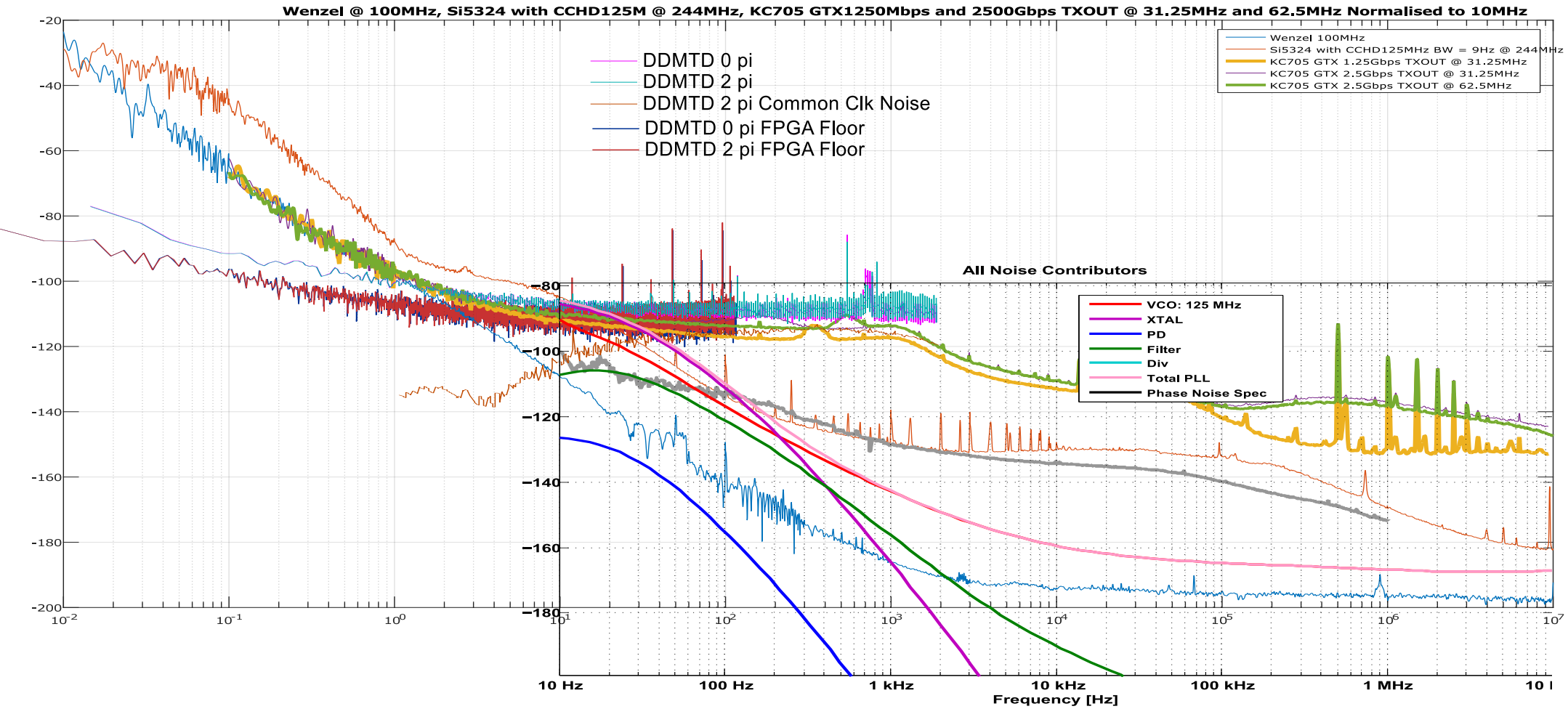
Wenzel @ 100MHz, Si5324 with CCHD125M @ 244MHz, KC705 GTX1250Mbps and 2500Gbps TXOUT @ 31.25MHz and 62.5MHz Normalised to 10MHz
DDMTD 0 pi
DDMTD 2 pi
DDMTD 2 pi Common Clk Noise
DDMTD 0 pi FPGA Floor
DDMTD 2 pi FPGA Floor
Wenzel 100MHz
Si5324 with CCHD125MHz BW = 9Hz @ 244MHz
KC705 GTX 1.25Gbps TXOUT @ 31.25MHz
KC705 GTX 2.5Gbps TXOUT @ 31.25MHz
KC705 GTX 2.5Gbps TXOUT @ 62.5MHz
All Noise Contributors
VCO: 125 MHz
XTAL
PD
Filter
Div
Total PLL
Phase Noise Spec
10 Hz
100 Hz
1 kHz
10 kHz
100 kHz
1 MHz
Frequency [Hz]