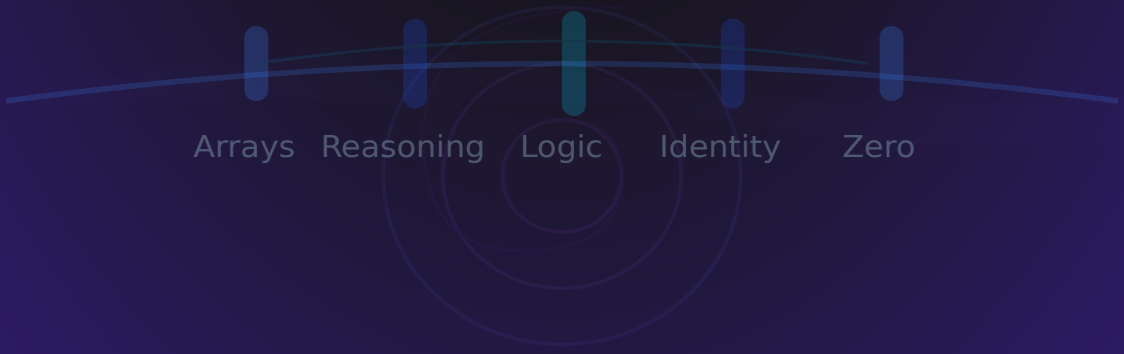
ARLIZ

A JOURNEY THROUGH ARRAYS



LIVING FIRST EDITION

ARLI

ARRAYS • REASONING • LOGIC • IDENTITY • ZERO

"From ancient counting stones to quantum algorithms—
every data structure tells the story of human ingenuity."

LIVING FIRST EDITION

Updated November 18, 2025

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A Living Architecture of Computing

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Repository: The complete source code (LaTeX, diagrams, examples) is available at: `https://github.com/m-mdy-m/Arliz`

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Contents

Preface

EVERY BOOK HAS ITS ORIGIN STORY, and this one is no exception. If I were to capture the essence of creating this book in a single word, that word would be **curiosity**—though *improvised* comes as a close second. What you hold in your hands (or view on your screen) is the result of years of persistent questioning, a journey that began with a simple yet profound realization: I didn't truly understand what an array was.

This might sound trivial to some. After all, arrays are fundamental to programming, covered in every computer science curriculum, explained in countless tutorials. Yet despite encountering terms like `array`, `stack`, `queue`, `linked list`, `hash table`, and `heap` repeatedly throughout my studies, I found myself increasingly frustrated by the superficial explanations typically offered. Most resources assumed you already knew what these structures fundamentally represented—their conceptual essence, their implementation mechanics, their performance characteristics.

But I wanted the *roots*. I needed to understand not just how to use an array, but what it truly meant at every level—from hardware representation to high-level abstractions. This led me to a decisive moment:

If I truly want to understand, I must build from the foundation.

And so began the journey that became Arliz.

The Name and Its Meaning

The name "Arliz" started as a somewhat arbitrary choice—I needed a title, and it sounded right. However, as the book evolved, I discovered a fitting expansion that captures its essence:

Arliz = Arrays, Reasoning, Logic, Identity, Zero

This backronym embodies the core pillars of our exploration:

- **Arrays:** The fundamental data structure we seek to understand from implementation to application

- **Reasoning:** The systematic thinking behind data organization and algorithmic design
- **Logic:** The formal principles that govern computation and data manipulation
- **Identity:** The concept of distinguishing, indexing, and assigning meaning to elements within structures
- **Zero:** The foundation from which all indexing, computation, and systematic organization originates

You may pronounce it "Ar-liz," "Array-Liz," or however feels natural to you. I personally say "ar-liz," but the pronunciation matters less than the journey it represents.

The Genesis of This Work

This book was not conceived in its current form. Originally, Arliz was intended to be a comprehensive seven-part exploration spanning:

1. Philosophical and Historical Foundations
2. Mathematical Fundamentals
3. Data Representation
4. Computer Architecture and Logic
5. Array Odyssey
6. Data Structures and Algorithms
7. Parallelism and Systems

As I delved deeper into writing the first two parts—covering the historical evolution of counting systems and the mathematical prerequisites for understanding data structures—I confronted an uncomfortable reality. These sections were becoming substantial works in their own right, yet they were foundational not only for arrays but for understanding algorithmic analysis and computational thinking more broadly.

Simultaneously, I realized that array analysis alone could not stand without a proper treatment of algorithmic complexity. Understanding why an array operation is $O(1)$ or $O(n)$ requires deep analytical foundations that extend far beyond arrays themselves.

This led to a critical decision: rather than compromise the depth of treatment by constraining everything within a single volume, I would separate the foundational material into dedicated works. Thus emerged:

- **Mathesis: The Mathematical Foundations of Computing** — A comprehensive treatment of the mathematical concepts underlying all of computer science, from ancient number systems through modern discrete mathematics and linear algebra
- **The Art of Algorithmic Analysis** — A rigorous exploration of analytical techniques for understanding computational complexity, from asymptotic notation through advanced amortized analysis and complexity theory

These books were not afterthoughts or supplements—they became the essential prerequisites that enable Arliz to focus purely on what it does best: a deep, implementation-focused exploration of arrays and their role in computing systems.

The current Arliz, therefore, begins where those foundations end. It assumes mathematical maturity at an intermediate level—comfort with discrete mathematics, basic linear algebra, and algorithmic analysis—and builds from there into the concrete realities of array implementation, optimization, and application.

What This Book Represents

Arliz is not a gentle introduction to programming, nor is it a purely theoretical treatment of data structures. Instead, it represents something more focused and, I believe, more valuable: a comprehensive technical exploration of the most fundamental data structure in computing, examined from every relevant angle.

This living work evolves continuously as I discover better explanations, uncover new implementation details, or recognize deeper connections between concepts. As long as I continue learning, Arliz will continue growing. Your engagement—through corrections, suggestions, and questions—makes you part of this evolution.

The structure reflects a deliberate progression through increasingly sophisticated understanding:

- **Data Representation** — How information is encoded in digital systems, from number systems to character encoding
- **Computer Architecture and Logic** — The hardware foundations that determine how arrays actually work
- **Array Odyssey** — Deep exploration of array implementation, behavior, and optimization
- **Data Structures and Algorithms** — How arrays enable other structures and algorithmic techniques
- **Parallelism and Systems** — Arrays in multi-threaded, distributed, and high-performance contexts

Prerequisites and Expectations

This book assumes you have completed (or are comfortable with) the material in:

- **Mathesis** — Mathematical foundations including discrete mathematics, linear algebra, and basic analysis
- **The Art of Algorithmic Analysis** — Asymptotic analysis, recurrence relations, and algorithmic complexity

Without these foundations, much of this book will be challenging. With them, it becomes a focused, deep dive into one of computing's most elegant and essential abstractions.

We will not shy away from technical complexity. Array implementation touches hardware architecture, memory hierarchies, compiler optimizations, and operating system interfaces. Understanding arrays properly means understanding these layers and their interactions.

That said, I have worked to avoid unnecessary mathematical abstraction. While mathematical rigor appears where needed—particularly when analyzing performance characteristics or proving correctness properties—the focus remains practical: how do arrays actually work, why do they behave as they do, and how can we use them effectively?

My Approach and Principles

Throughout the writing process, I have maintained three core principles:

1. **Implementation Focus:** Every abstract concept is grounded in concrete implementation. You will see how arrays are actually represented in memory, how compilers optimize array operations, and how hardware characteristics influence performance.
2. **Visual Understanding:** Complex concepts are accompanied by diagrams, memory layouts, and visual representations. Arrays are inherently spatial structures—understanding them requires seeing their organization.
3. **Practical Code:** Nearly every topic includes working implementations that can be studied, modified, and adapted. Theory without implementation is incomplete; implementation without theory is fragile.

An important disclosure: many of the implementations in this book are my own constructions, built from first principles to demonstrate concepts clearly. Some may

run slower than heavily optimized production libraries—others may reveal surprising efficiencies. The goal is understanding, not necessarily optimal performance in every case.

About the Author

I am **Mahdi**, though you may know me by my online alias: *Genix*. At the time of writing, I am a Computer Engineering student, but more fundamentally, I am someone driven by a relentless need to understand the systems I work with at their deepest levels.

My relationship with computers has been one of continuous investigation—never satisfied with surface-level explanations, always pushing toward the foundational principles that make everything work. This book represents that drive crystallized into a focused exploration of arrays.

How to Use This Book

Arliz is freely available and open source. You can access the complete PDF, LaTeX source code, and related materials at:

`https://github.com/m-mdy-m/Arliz`

Each chapter includes carefully designed exercises and implementation challenges. These are not optional—they are essential components of the learning process. True understanding of arrays comes only through implementing them yourself, seeing how they break under stress, and discovering their performance characteristics through measurement.

I encourage you to approach this book as a collaborative effort. If you discover errors, have implementation insights, or develop optimizations worth sharing, please contribute. This book improves through community engagement.

A Living Technical Document

Finally, I want to be transparent about what you are engaging with. This is not a finished, polished textbook in the traditional sense. It is an evolving technical exploration, growing and improving as understanding deepens and new implementation techniques emerge.

You may encounter sections that could be clearer, implementations that could be more efficient, or explanations that could be more rigorous. This is intentional—Arliz

represents learning in progress, understanding in development. It invites you to participate in this process of refinement rather than simply consume its content.

I hope this book serves you well—whether you are building your first serious data structures, optimizing performance-critical systems, or simply satisfying intellectual curiosity about how arrays actually work. And if you learn something valuable, discover an error, or develop an insight worth sharing, I hope you will contribute.

After all, this book grows with all of us.

Mahdi
2025

> *"The purpose of abstraction is not to be vague, but to create a new semantic level in which one can be absolutely precise."*
>
> — EDSGER W. DIJKSTRA

Acknowledgments

I would like to express my gratitude to everyone who supported me during the creation of this book. Special thanks to the open-source community for their invaluable resources and to all those who reviewed early drafts and provided feedback.

How to Read This Book

Understanding the Structure

Arliz is organized as a progressive deepening of understanding. Each part builds on previous material, developing increasingly sophisticated perspectives on arrays and their implementation. You cannot skip ahead without missing essential foundations.

The Five Parts

Part I: Data Representation
Begin here. Always. This part establishes how information is encoded in digital systems—the absolute foundation for understanding how array elements are stored and manipulated. Without this foundation, later material becomes incomprehensible.

Part II: Computer Architecture & Logic
Arrays live in hardware. This part examines that hardware: logic gates, memory systems, processor architecture, cache behavior. Understanding these realities is essential for writing efficient array code.

Part III: Array Odyssey
The core of the book. Here we explore arrays themselves: their mathematical properties, memory layouts, performance characteristics, optimization techniques. This is where everything converges.

Part IV: Data Structures & Algorithms
Arrays enable other structures. This part examines how stacks, queues, heaps, hash tables, and other structures build on array foundations. We also explore algorithmic techniques that leverage array properties.

Part V: Parallelism & Systems
Modern computing is parallel and distributed. This part examines arrays in multi-threaded, concurrent, and distributed contexts—showing how classical concepts extend to contemporary challenges.

Reading Strategies

Sequential Reading (Recommended)

For most readers, sequential reading provides the best experience. Start with Part I, work through each chapter carefully, complete the exercises, implement the examples, and progress to the next part only when you have mastered the current material.

This approach takes time—months, not weeks—but produces deep, lasting understanding. Concepts build systematically. Each part prepares you for the next. Skipping ahead creates gaps that will eventually force you to backtrack.

Selective Reading (For Experienced Readers)

If you have strong backgrounds in both computer architecture and mathematical analysis, you might consider selective reading:

- **Part I:** Review chapter summaries. If material seems familiar, proceed to Part II. If anything seems unclear, read the full chapters.
- **Part II:** Same approach—review summaries, read full chapters for unfamiliar material.
- **Part III:** Read completely. This is the core material that justifies the book's existence.
- **Parts IV-V:** Read sequentially for complete understanding, or select chapters based on your specific interests.

Be honest with yourself about your preparation. Overestimating your background leads to gaps that undermine later understanding.

Reference Use

Once you have read the book completely, it serves as a reference. The detailed table of contents, comprehensive index, and clear section organization enable targeted consultation when specific questions arise.

But initial reading should be sequential. Reference use only becomes effective after establishing comprehensive understanding.

Engaging with the Material

Work Every Example

Examples are not illustrations—they are essential learning tools. For each example:

1. Read the example carefully, ensuring you understand each step
2. Implement the example in your preferred programming language
3. Run the implementation and verify it produces expected results
4. Modify the example to test your understanding
5. Measure performance characteristics when relevant

Understanding comes through implementation, not merely reading.

Complete the Exercises

Exercises test and deepen understanding. They range from straightforward verification of concepts through challenging implementation problems to open-ended research questions.

- **Basic exercises:** Verify you understand fundamental concepts
- **Intermediate exercises:** Apply concepts to new situations
- **Advanced exercises:** Extend concepts in novel directions
- **Research problems (⋆):** Open questions requiring substantial investigation

Do not skip exercises. They are not optional—they are core components of the learning process.

Measure Performance

Array performance is empirical. Throughout the book, we make performance predictions based on theoretical analysis. Verify these predictions through measurement:

1. Implement the operation being analyzed
2. Measure its actual performance using timing tools
3. Compare measurements to theoretical predictions
4. Investigate and explain any discrepancies
5. Vary parameters to observe how behavior changes

This empirical engagement develops performance intuition that no amount of reading can provide.

Question Everything

Active questioning drives deeper understanding. As you read:

- Why does this operation have this cost?
- How would changing this parameter affect behavior?
- What hardware characteristics influence this performance?
- Could this technique be implemented differently?
- What are the trade-offs in this design decision?
- How does this concept connect to material in other chapters?

When you find yourself unable to answer such questions, that indicates areas requiring deeper study.

Prerequisites and Preparation

Essential Mathematical Background

You should be comfortable with:

- **Discrete Mathematics:** Sets, relations, functions, graph theory, combinatorics
- **Linear Algebra:** Vectors, matrices, linear transformations
- **Mathematical Analysis:** Asymptotic notation, series, limits
- **Probability:** Basic probability theory, random variables, expected values

If these topics seem unfamiliar, work through *Mathesis: The Mathematical Foundations of Computing* before continuing with *Arliz*.

Essential Algorithmic Background

You should understand:

- **Asymptotic Analysis:** Big-O, Big-Omega, Big-Theta notation
- **Recurrence Relations:** Solving recurrences, Master theorem
- **Algorithm Analysis:** Analyzing time and space complexity
- **Basic Data Structures:** Conceptual understanding of lists, trees, graphs

If this material seems unfamiliar, work through *The Art of Algorithmic Analysis* before continuing with *Arliz*.

Programming Proficiency

You should:

- Be proficient in at least one programming language (C, C++, Java, or Python recommended)
- Be comfortable reading code in multiple languages
- Understand basic computer architecture concepts (CPU, memory, registers)
- Have experience implementing and debugging non-trivial programs

This book is not for beginners. It assumes substantial programming experience.

Notation and Conventions

Mathematical Notation

We use standard mathematical notation throughout:

- $\mathcal{O}(f(n))$: Big-O notation for asymptotic upper bounds
- $\Omega(f(n))$: Big-Omega notation for asymptotic lower bounds
- $\Theta(f(n))$: Big-Theta notation for tight asymptotic bounds
- $[n]$: The set $\{1, 2, \ldots, n\}$
- $\log n$: Logarithm base 2 unless otherwise specified

Pseudocode Conventions

Pseudocode uses clear, imperative style:

- Array indexing starts at 0 unless explicitly stated otherwise
- $A[i]$ accesses element at index i of array A
- $\leftarrow$ denotes assignment
- Loops use clear indentation to show scope
- Comments appear in italic type

Implementation Examples

Code examples appear in monospace font with syntax highlighting:

- Primary examples use C for clarity and control

- Alternative implementations may appear in C++, Java, or Python
- Assembly code appears when discussing low-level implementation
- All code is complete and executable unless marked as pseudocode

Common Pitfalls to Avoid

Skipping Mathematical Development

Mathematical analysis is not optional decoration—it is essential substance. When a theorem appears, read its proof carefully. When an analysis uses mathematical techniques, work through the mathematics. This rigor distinguishes genuine understanding from surface familiarity.

Reading Without Implementing

Reading about arrays is not the same as implementing array operations. Reading about cache behavior is not the same as measuring cache performance. Reading about optimization techniques is not the same as applying those techniques to real code.

Implementation is not optional. Do the work.

Ignoring Hardware Realities

Arrays do not exist in abstract mathematical space—they exist in physical hardware with specific characteristics and constraints. Cache lines, memory alignment, TLB behavior, SIMD instructions—these realities determine actual performance. Understanding them is essential.

Settling for Vague Understanding

When you find yourself thinking "I sort of understand this," stop. That signals insufficient understanding. Go back. Read again. Implement examples. Work exercises. Achieve precise, confident understanding before proceeding.

Vague understanding compounds over chapters, eventually producing complete confusion.

When You Get Stuck

Getting stuck is normal—it signals you have encountered material requiring deeper engagement. When stuck:

1. Return to the previous chapter and verify you truly understood that material
2. Re-read the challenging section carefully, taking notes
3. Implement examples from the section
4. Work through exercises, even if they seem difficult
5. Consult the references cited in the chapter
6. Take a break and return with fresh perspective

Persistent difficulty despite these strategies may indicate insufficient prerequisites. Be honest with yourself—return to *Mathesis* or *The Art of Algorithmic Analysis* if necessary.

Using This Book as a Course Text

Undergraduate Course

For an undergraduate course on data structures or advanced programming:

- Parts I-III provide core material for a semester-long course
- Part IV material can be integrated as time permits
- Part V provides advanced material for motivated students
- Exercises provide abundant homework and project material

Graduate Course

For a graduate course on advanced data structures or performance optimization:

- Assume students have mastered prerequisites
- Part III provides core material
- Parts IV-V provide substantial advanced material
- Research problems ($\star$) provide thesis-level investigations

Final Advice

This book rewards patience, persistence, and active engagement. It punishes skimming, skipping, and passive reading.

Take your time. Work through examples. Implement techniques. Measure performance. Question constantly. When concepts seem difficult, that is normal—persist until understanding comes.

The journey requires sustained effort, but the destination—deep, rigorous understanding of the most fundamental data structure in computing—justifies every moment invested.

Welcome to *Arliz*. Begin when ready.

Introduction

ARRAYS ARE EVERYWHERE. Every image you view, every text you read, every game you play, every database query you execute—arrays underlie them all. Yet despite their ubiquity, arrays remain poorly understood by most programmers. They are treated as primitive constructs, learned hastily and used mechanically, their true nature obscured by layers of abstraction.

This book exists to remedy that situation.

What This Book Is

Arliz is a focused, technical exploration of the most fundamental data structure in computing: the array. Unlike comprehensive data structures textbooks that survey many structures superficially, we examine arrays with unprecedented depth—from their hardware representation in memory through their implementation in programming languages to their role in advanced algorithmic techniques.

This is not a book for casual reading. It demands engagement, rewards persistence, and assumes substantial mathematical and computational maturity. If you seek quick tutorials or surface-level explanations, you will find this book frustrating. If you seek deep, rigorous understanding of how arrays actually work and why they behave as they do, you have found the right resource.

The Architecture of This Work

The book progresses through five major parts, each building on the foundations established by its predecessors:

Part I: Data Representation
We begin with the fundamental question: how is information encoded in digital systems? From binary representation through character encoding, from integer formats to floating-point arithmetic, we establish the representational foundations that determine how array elements are actually stored and manipulated at the machine level.

Part II: Computer Architecture & Logic

Arrays do not exist in abstract space—they live in physical hardware with specific characteristics and constraints. We examine logic gates, processor architecture, memory hierarchies, and cache behavior. Understanding these hardware realities is essential for writing array code that performs well on real systems.

Part III: Array Odyssey

This is the heart of the book. We explore arrays from every angle: their mathematical properties, their implementation in memory, their performance characteristics, their optimization techniques. We examine one-dimensional arrays, multidimensional arrays, sparse arrays, and specialized array variants. We analyze cache behavior, memory alignment, and hardware-level optimization strategies.

Part IV: Data Structures & Algorithms

With arrays deeply understood, we examine how they enable other data structures. Stacks, queues, heaps, hash tables—all build on array foundations. We explore algorithmic techniques that leverage array properties, from sorting algorithms through dynamic programming.

Part V: Parallelism & Systems

Modern computing is parallel and distributed. We examine how arrays behave in multi-threaded environments, how they scale across distributed systems, and how they enable high-performance computing. This part connects classical array concepts to cutting-edge computational challenges.

What Makes This Different

Several characteristics distinguish this treatment:

Implementation Focus We do not merely describe abstract properties—we examine actual implementations. You will see precisely how arrays are represented in memory, how compilers optimize array operations, and how hardware characteristics influence performance.

Performance Analysis Every operation receives rigorous performance analysis. We measure cache behavior, count memory accesses, and analyze asymptotic complexity. Understanding why operations cost what they cost is central to using arrays effectively.

Mathematical Rigor Arrays are mathematical objects with well-defined properties. We develop this mathematics carefully, proving theorems about array behavior and analyzing operations with formal precision.

Hardware Awareness Arrays cannot be understood independently of the hardware that implements them. We examine how memory systems work, how caches behave, and how processors optimize array access patterns.

Prerequisites

This book assumes substantial preparation:

Mathematical Maturity: You should be comfortable with discrete mathematics, linear algebra, and basic mathematical analysis. Specifically, you should have completed (or be comfortable with) the material in *Mathesis: The Mathematical Foundations of Computing*.

Algorithmic Analysis: You should understand asymptotic notation, recurrence relations, and basic complexity analysis. The material in *The Art of Algorithmic Analysis* provides the necessary foundations.

Programming Experience: You should be proficient in at least one programming language and comfortable reading code in multiple languages. We use pseudocode, C, and occasionally other languages for examples.

Without these prerequisites, you will struggle with substantial portions of this book. With them, you are prepared for a deep, rewarding exploration of arrays.

How to Approach This Material

This book rewards active engagement:

Work Through Examples: Every example can be implemented and experimented with. Do so. Understanding comes through doing, not merely reading.

Measure Everything: Array performance is empirical. Write code, measure its behavior, and compare measurements to theoretical predictions. This develops intuition no amount of reading can provide.

Question Constantly: Why does this operation cost what it costs? How would changing this parameter affect performance? What hardware characteristics influence this behavior? Active questioning drives deeper understanding.

Implement Techniques: The optimization techniques we discuss should be implemented and tested. Theory becomes meaningful only when connected to practice.

The Living Nature of This Work

Like all my books, *Arliz* evolves continuously. As I discover better explanations, identify errors, recognize new connections, or encounter new implementation techniques, the book improves. Your engagement—through corrections, suggestions, implementations, and questions—contributes to this evolution.

Check the GitHub repository regularly for updates. The version you read today will be superseded by improved versions tomorrow. This is not a weakness but a strength—the book remains current, accurate, and relevant.

A Note on Difficulty

This book is challenging by design. Arrays may seem simple on the surface, but their full understanding requires grappling with hardware architecture, memory systems, compiler optimizations, and algorithmic analysis. Some sections will require sustained effort to master.

This difficulty is intentional. Genuine understanding is never cheap—it demands intellectual investment, persistent effort, and willingness to struggle with complex concepts. If you find sections difficult, that is normal. Persist. Work through examples. Implement the techniques. Understanding will come through sustained engagement.

What You Will Gain

By the end of this journey, you will possess:

- **Deep Implementation Understanding:** Precise knowledge of how arrays are represented, stored, and manipulated at every level from hardware through high-level languages
- **Performance Intuition:** Ability to predict array performance characteristics and optimize array-based code effectively
- **Algorithmic Capability:** Understanding of how arrays enable algorithmic techniques and data structure implementations
- **Hardware Awareness:** Knowledge of how memory hierarchies, caches, and processors influence array behavior
- **Design Insight:** Ability to choose appropriate array representations and implementations for specific problems

More fundamentally, you will have developed a way of thinking about data structures that transcends arrays themselves. The analytical techniques, performance

reasoning, and implementation understanding you develop here transfer to all subsequent work with computational systems.

Begin

Five parts await. Each deepens your understanding of arrays—from representation through implementation to application. Each builds essential capabilities for working effectively with the most fundamental data structure in computing.

Welcome to **Arliz**. Let us explore arrays with the depth and rigor they deserve.

"Simplicity is prerequisite for reliability."

— EDSGER W. DIJKSTRA

"The purpose of abstraction is not to be vague, but to create a new semantic level in which one can be absolutely precise."

— EDSGER W. DIJKSTRA

"Premature optimization is the root of all evil."

— DONALD E. KNUTH

Part I

Data Representation

Before we can understand how arrays store elements, we must first understand how computers represent information itself. Every piece of data—numbers, text, images, instructions—exists as patterns of bits. This part explores the foundational question: how do we encode meaning into binary?

> *"The choice of representation is often more important than the choice of algorithm."*
>
> — Donald E. Knuth

Chapter 1

The Philosophy of Representation

Why representation matters. Historical evolution from tally marks to bits. The abstraction hierarchy. Information theory fundamentals. Shannon's insight.

Chapter 2

Physical Representation: Voltage to Bits

How transistors encode binary states, voltage levels, noise margins, signal integrity, why binary won over ternary.

Chapter 3

Binary Representation and Boolean Algebra

Two-state logic, Boolean operations, truth tables, De Morgan's laws, bit as fundamental unit.

Chapter 4

Number Systems and Bases

Positional notation, decimal, binary, octal, hexadecimal. Base conversion algorithms. Historical development. Why different bases matter for different purposes.

Chapter 5

Integer Representation: Unsigned

Binary positional notation, range limitations, conversion algorithms, hexadecimal convenience.

Chapter 6

Signed Integer Representation

Sign-magnitude, one's complement, two's complement (why it won), arithmetic operations, overflow detection.

Chapter 7

Integer Overflow and Wraparound Behavior

Undefined behavior, modular arithmetic, detecting overflow, saturating arithmetic, language-specific behaviors.

Chapter 8

Fixed-Point Representation

Q-format notation, scaling factors, precision-range tradeoffs, embedded systems applications, fixed-point arithmetic.

Chapter 9

Floating-Point Representation: IEEE 754

Sign, exponent, mantissa encoding, normalized and denormalized numbers, single vs. double precision.

Chapter 10

Special Floating-Point Values

Infinity (positive and negative), NaN (quiet and signaling), signed zero, subnormal numbers.

Chapter 11

Floating-Point Arithmetic Operations

Addition, multiplication, division, rounding modes (round to nearest, toward zero, toward ±), fused multiply-add.

Chapter 12

Floating-Point Error Analysis

Precision loss, catastrophic cancellation, machine epsilon, relative error, Kahan summation algorithm.

Chapter 13

Decimal Floating-Point Representation

IEEE 754-2008 decimal formats, financial computing requirements, densely packed decimal.

Chapter 14

Extended Precision and Arbitrary Precision

80-bit extended precision, quadruple precision (128-bit), arbitrary precision libraries (GMP, MPFR).

Chapter 15

Character Encoding: ASCII and Extensions

7-bit ASCII, extended ASCII variants, code pages, limitations for internationalization.

Chapter 16

Unicode: Universal Character Encoding

Code points, planes, combining characters, grapheme clusters, normalization forms (NFC, NFD, NFKC, NFKD).

Chapter 17

Unicode Transformation Formats

UTF-8 (variable length, backward compatible), UTF-16 (surrogate pairs), UTF-32 (fixed length), BOM issues.

Chapter 18

Text Processing Complexities

Grapheme vs. code point counting, case folding, locale-dependent operations, text segmentation.

Chapter 19

Endianness: Byte Ordering

Big-endian vs. little-endian, historical reasons, network byte order, bi-endian systems, byte swapping.

Chapter 20

Cross-Platform Data Exchange

Serialization formats, portable binary formats, protocol design considerations.

Chapter 21

Bitwise Operations Fundamentals

AND, OR, XOR, NOT operations, truth tables, bit manipulation primitives.

Chapter 22

Bit Shifting and Rotation

Logical shift, arithmetic shift, rotate left/right, applications to multiplication/division by powers of 2.

Chapter 23

Bit Manipulation Techniques

Setting/clearing/toggling bits, bit masks, extracting bit fields, counting set bits (population count).

Chapter 24

Bit Packing and Flags

Packing multiple boolean flags, bitfields in structs, union tricks, bit arrays.

Chapter 25

Advanced Bit Hacking

Finding rightmost set bit, isolating bit patterns, bit reversal, Gray code conversion.

Chapter 26

Data Alignment Fundamentals

Natural alignment, alignment requirements by type, misalignment penalties.

Chapter 27

Structure Padding and Layout

Compiler padding rules, struct member ordering, packing pragmas, cache line awareness.

Chapter 28

Alignment Optimization Techniques

Manual padding, alignment attributes, reordering for cache efficiency.

Chapter 29

Color Representation Models

RGB, RGBA, HSV, HSL, CMYK, YUV, color spaces, gamma correction.

Chapter 30

Pixel Formats and Bit Depth

1-bit, 8-bit indexed, 16-bit (RGB565), 24-bit, 32-bit (with alpha), HDR formats.

Chapter 31

Image Compression Fundamentals

Lossless (PNG, GIF) vs. lossy (JPEG), compression ratios, quality tradeoffs.

Chapter 32

Video Encoding Principles

Frame types (I, P, B), motion compensation, codecs (H.264, H.265, VP9, AV1).

Chapter 33

Audio Representation: Sampling Theory

Nyquist theorem, sample rate, bit depth, quantization noise, aliasing.

Chapter 34

Audio Encoding Formats

PCM (uncompressed), FLAC (lossless), MP3, AAC, Opus (lossy), perceptual coding.

Chapter 35

Signal Processing Representations

Time domain, frequency domain, spectrograms, wavelet transforms.

Chapter 36

Pointer Representation

How pointers are stored in memory, pointer size (32-bit vs. 64-bit), pointer tagging.

Chapter 37

Pointer Arithmetic and Address Calculation

Array element addressing, struct member offsets, pointer subtraction.

Chapter 38

Special Pointer Values

Null pointers, wild pointers, dangling pointers, pointer alignment requirements.

Chapter 39

Error Detection Codes

Parity bits (even/odd), checksums, CRC algorithms, hash-based integrity.

Chapter 40

Error Correction Codes

Hamming codes, Reed-Solomon codes, LDPC codes, convolutional codes.

Chapter 41

Cyclic Redundancy Checks (CRC)

CRC polynomials, CRC-8, CRC-16, CRC-32 standards, efficient implementation using tables, applications in data integrity.

Chapter 42

Data Serialization Fundamentals

Converting in-memory structures to byte streams, portability issues.

Chapter 43

Binary Serialization Formats

Protocol Buffers, FlatBuffers, Cap'n Proto, MessagePack, CBOR.

Chapter 44

Text Serialization Formats

JSON, XML, YAML, TOML, human-readable vs. machine-efficient tradeoffs.

Chapter 45

Custom Binary Protocols

Designing efficient binary formats, alignment considerations, versioning.

Chapter 46

Data Compression Theory

Information theory basics, entropy, lossless vs. lossy bounds.

Chapter 47

Dictionary-Based Compression

LZ77, LZ78, LZW, Lempel-Ziv family, dictionary construction.

Chapter 48

Entropy Coding

Huffman coding, arithmetic coding, asymmetric numeral systems (ANS).

Chapter 49

Modern Compression Algorithms

zlib, gzip, bzip2, LZMA, Zstandard, Brotli, compression levels.

Chapter 50

Specialized Compression

Run-length encoding, delta encoding, columnar compression, domain-specific methods.

Part II

Computer Architecture & Logic

ARRAYS EXIST *in physical hardware. To understand array performance, we must understand the machines that execute our code—from transistors to complete systems. This part builds a complete picture of computational machinery.*

What Makes This Different:

- ***Silicon to Software:*** *Complete vertical integration*
- ***Modern Architecture:*** *Multi-core, SIMD, heterogeneous systems*
- ***Performance Foundations:*** *Why code runs fast or slow*
- ***Hardware-Software Contract:*** *What each layer assumes*

> *"The purpose of computing is insight, not numbers."*
>
> — RICHARD HAMMING

Chapter 51

Semiconductor Physics Foundations

Silicon properties, doping (n-type, p-type), P-N junctions, depletion regions, how semiconductors enable switching.

Chapter 52

MOSFET Transistors

Gate, source, drain, channel, threshold voltage, NMOS and PMOS, how transistors act as switches.

Chapter 53

CMOS Logic Fundamentals

Complementary MOS, pull-up and pull-down networks, static power vs. dynamic power, why CMOS won.

Chapter 54

Logic Gate Implementation

CMOS implementation of NOT, NAND, NOR gates, gate delay, rise/fall time, fan-out limitations.

Chapter 55

Logic Gate Families

AND, OR, XOR, XNOR from NAND/NOR, transmission gates, tri-state buffers.

Chapter 56

Combinational Circuit Design

Truth tables to logic expressions, Karnaugh maps, minimization, multi-level logic.

Chapter 57

Arithmetic Circuits: Adders

Half adder, full adder, ripple-carry adder, carry-lookahead adder, carry-select adder.

Chapter 58

Arithmetic Circuits: Multipliers and Dividers

Array multiplier, Booth multiplier, Wallace tree, division algorithms, restoring vs. non-restoring.

Chapter 59

Multiplexers and Demultiplexers

2:1 mux, 4:1 mux, tree structures, using muxes for logic implementation.

Chapter 60

Encoders and Decoders

Binary encoding, priority encoding, 7-segment decoder, address decoding.

Chapter 61

Arithmetic Logic Circuits

Half adder, full adder, ripple-carry adder, carry-lookahead adder, carry-save adder, subtraction using two's complement, magnitude comparators.

Chapter 62

Advanced Arithmetic Units

Multipliers (array multiplier, Booth's algorithm, Wallace tree), dividers, floating-point units (FPUs), fused multiply-add (FMA).

Chapter 63

Sequential Logic Fundamentals

Difference between combinational and sequential logic, feedback, state, clock signals, synchronous versus asynchronous design.

Chapter 64

Comparators and Magnitude Detection

Equality comparator, magnitude comparator, signed vs. unsigned comparison.

Chapter 65

Sequential Logic Fundamentals

Need for memory elements, clock signals, synchronous vs. asynchronous design.

Chapter 66

Latches: SR, D Latches

Set-reset latch, gated D latch, transparent latch, latch vs. flip-flop distinction.

Chapter 67

Flip-Flops: D, JK, T Flip-Flops

Edge-triggered flip-flops, master-slave configuration, setup and hold time, clock-to-Q delay.

Chapter 68

Registers and Register Files

Parallel-load register, shift registers (SISO, SIPO, PISO, PIPO), register banks for CPU.

Chapter 69

Counters and Timers

Ripple counter, synchronous counter, up/down counter, modulo-N counter, timer circuits.

Chapter 70

Finite State Machines

Moore vs. Mealy machines, state diagrams, state table, state minimization, FSM implementation.

Chapter 71

Memory Cell Design: SRAM

6-transistor SRAM cell, read and write operations, stability analysis, SRAM array organization.

Chapter 72

Memory Cell Design: DRAM

1-transistor 1-capacitor cell, charge storage, sense amplifiers, refresh requirement.

Chapter 73

Memory Array Organization

Row and column decoding, wordline and bitline, memory cell array structure, address multiplexing.

Chapter 74

DRAM Operation and Timing

Row activation, column access, precharge, timing parameters (tRCD, tRP, tRAS, CAS latency).

Chapter 75

DRAM Generations

SDR SDRAM, DDR, DDR2, DDR3, DDR4, DDR5, bandwidth evolution, power efficiency.

Chapter 76

Advanced DRAM Features

Burst mode, bank interleaving, dual-channel, command queuing, on-die termination.

Chapter 77

Non-Volatile Memory Technologies

Flash memory (NAND, NOR), program/erase cycles, wear leveling, EEPROM, ROM variants.

Chapter 78

Flash Memory Operations

Programming (writing), erasing, read operations, wear leveling, write amplification, garbage collection, over-provisioning.

Chapter 79

Emerging Memory Technologies

Phase-change memory (PCM), resistive RAM (ReRAM), magnetoresistive RAM (MRAM), 3D XPoint.

Chapter 80

Memory Hierarchy Fundamentals

Pyramid structure, latency-capacity tradeoffs, why hierarchies exist, locality principles.

Chapter 81

Cache Memory Fundamentals

Temporal locality, spatial locality, cache line (block), tag-data organization.

Chapter 82

Cache Mapping Strategies

Direct-mapped cache, fully-associative cache, set-associative cache (2-way, 4-way, 8-way, N-way).

Chapter 83

Cache Replacement Policies

LRU (least recently used), LFU, FIFO, random, pseudo-LRU, practical implementations.

Chapter 84

Cache Write Policies

Write-through, write-back, write-allocate, no-write-allocate, dirty bits.

Chapter 85

Multi-Level Cache Hierarchies

L1 instruction and data caches, unified L2 cache, L3 shared cache, inclusive vs. exclusive caches.

Chapter 86

Victim Caches and Advanced Structures

Victim cache for conflict misses, stream buffers for prefetching, trace caches.

Chapter 87

Cache Coherence Problem

Shared memory multiprocessors, cache inconsistency, coherence vs. consistency.

Chapter 88

Cache Coherence Protocols: MESI

Modified, Exclusive, Shared, Invalid states, state transitions, bus snooping.

Chapter 89

Cache Coherence Protocols: MOESI and Beyond

Owned state, directory-based coherence, scalability issues.

Chapter 90

Cache Performance Analysis

Hit rate, miss rate, average memory access time (AMAT), miss penalty, classifying misses (compulsory, capacity, conflict).

Chapter 91

Cache Optimization Techniques

Blocking/tiling, array padding, loop interchange, prefetching, cache-aware algorithms.

Chapter 92

Instruction Set Architecture (ISA)

RISC versus CISC philosophy, instruction encoding and formats, addressing modes, register architecture, condition codes.

Chapter 93

x86 Architecture

x86 instruction encoding, variable-length instructions, complex addressing modes, backward compatibility, x86-64 extensions.

Chapter 94

ARM Architecture

Load-store architecture, fixed-length instructions (ARM mode), Thumb instruction set, NEON SIMD, ARM versus x86 comparison.

Chapter 95

RISC-V Architecture

Open ISA, modular extensions, base integer instruction set, standard extensions (M, A, F, D, C), design philosophy.

Chapter 96

Pipelining Fundamentals

Instruction pipeline stages (IF, ID, EX, MEM, WB), throughput improvement, latency, ideal CPI, pipeline diagrams.

Chapter 97

Pipeline Hazards

Structural hazards, data hazards (RAW, WAR, WAW), control hazards, stalls and bubbles, hazard detection and resolution.

Chapter 98

Data Forwarding and Bypassing

Forwarding paths, bypassing results from later stages, forwarding logic, load-use hazard, limitations of forwarding.

Chapter 99

Branch Handling in Pipelines

Branch penalty, delayed branches, branch prediction necessity, flushing pipeline on misprediction, branch delay slots.

Chapter 100

Branch Prediction Techniques

Static prediction (always taken, always not-taken, backward taken forward not-taken), dynamic prediction, branch history.

Chapter 101

Advanced Branch Prediction

Two-bit saturating counters, branch history table (BHT), branch target buffer (BTB), two-level adaptive predictors, tournament predictors.

Chapter 102

Return Address Stack

Function call prediction, hardware return address stack, depth and accuracy, correlation with call-return patterns.

Chapter 103

Superscalar Architecture

Multiple issue, instruction-level parallelism (ILP), dispatch width, execution units, dependency checking, instruction window.

Chapter 104

Out-of-Order Execution

Tomasulo's algorithm, reservation stations, register renaming, reorder buffer (ROB), commit stage, speculative execution.

Chapter 105

Register Renaming

Eliminating false dependencies (WAR, WAW), physical versus architectural registers, register alias table (RAT), freelist management.

Chapter 106

Speculative Execution

Branch speculation, memory speculation, exceptions in speculative execution, precise interrupts, ROB and commit.

Chapter 107

Speculative Execution Vulnerabilities

Spectre attacks (branch target injection, bounds check bypass), Meltdown (rogue data cache load), side-channel exploitation, mitigations.

Chapter 108

Memory Hierarchy Principles

Principle of locality (temporal and spatial), access time gaps, capacity and cost tradeoffs, memory wall problem.

Chapter 109

Virtual Memory Fundamentals

Virtual address space, physical address space, address translation, memory protection.

Chapter 110

Page Tables and Address Translation

Page table entry structure, multi-level page tables, page table walk.

Chapter 111

Translation Lookahead Buffer (TLB)

TLB structure, TLB hit/miss, TLB reach, large pages (huge pages, superpages).

Chapter 112

Page Replacement Algorithms

Optimal (Belady), FIFO, LRU, clock (second chance), working set model.

Chapter 113

Demand Paging and Page Faults

Page fault handling, major vs. minor faults, swap space, thrashing.

Chapter 114

Memory Management Unit (MMU)

Hardware implementation, page table base register, protection bits, privilege levels.

Chapter 115

Memory Protection and Isolation

Process isolation, kernel vs. user space, protection rings, segmentation.

Chapter 116

CPU Microarchitecture Overview

Instruction fetch, decode, execute, memory, writeback, datapath and control path.

Chapter 117

Instruction Set Architecture Principles

Instruction formats, operand addressing, register vs. memory operands, RISC philosophy.

Chapter 118

CISC vs. RISC

Complex instruction set (x86), reduced instruction set (ARM, RISC-V), microcode, instruction encoding density.

Chapter 119

Register Architecture

General-purpose registers, special-purpose registers (PC, SP, flags), register windows, register renaming.

Chapter 120

Addressing Modes

Immediate, register direct, memory direct, register indirect, indexed, PC-relative, stack addressing.

Chapter 121

Instruction Encoding

Fixed-length vs. variable-length, opcode, operands, prefix bytes (x86), instruction alignment.

Chapter 122

Pipelining Fundamentals

Instruction pipeline stages, throughput vs. latency, ideal speedup, pipeline registers.

Chapter 123

Pipeline Hazards

Structural hazards, data hazards (RAW, WAR, WAW), control hazards (branches).

Chapter 124

Data Forwarding and Bypassing

Forwarding paths, resolving data hazards, bypass network.

Chapter 125

Pipeline Stalls and Bubbles

When forwarding isn't enough, NOP insertion, performance impact.

Chapter 126

Branch Prediction Fundamentals

Static prediction, dynamic prediction, branch history, importance for performance.

Chapter 127

Branch Prediction: Simple Schemes

1-bit predictor, 2-bit saturating counter, bimodal predictor.

Chapter 128

Branch Prediction: Advanced Schemes

Two-level adaptive predictors, local vs. global history, correlating predictors.

Chapter 129

Branch Target Buffer and Return Stack

BTB for target prediction, return address stack (RAS) for function returns, indirect branch prediction.

Chapter 130

Speculative Execution

Executing before knowing if needed, branch prediction enabling speculation, squashing mispredicted paths.

Chapter 131

Out-of-Order Execution

Instruction reordering, Tomasulo's algorithm, reservation stations, reorder buffer.

Chapter 132

Register Renaming

Eliminating false dependencies (WAR, WAW), physical vs. architectural registers, register allocation table.

Chapter 133

Instruction Scheduling

Issue width, instruction window, dependency checking, wake-up and select logic.

Chapter 134

Superscalar Execution

Multiple issue, dispatch width, execution units, commit width, IPC (instructions per cycle).

Chapter 135

Very Long Instruction Word (VLIW)

Static scheduling by compiler, explicit parallelism, no dependency checking hardware, Itanium example.

Chapter 136

Simultaneous Multithreading (SMT)

Hyper-threading, thread-level parallelism, sharing execution resources, Intel and AMD implementations.

Chapter 137

Memory Ordering and Consistency

Load/store reordering, memory fences, barriers, acquire-release semantics.

Chapter 138

Consistency Models

Sequential consistency, total store order (TSO), weak ordering, relaxed models.

Chapter 139

Input/Output Systems

I/O devices and controllers, I/O address space (port-mapped versus memory-mapped I/O), programmed I/O, interrupt-driven I/O.

Chapter 140

Interrupt Handling

Interrupt request (IRQ), interrupt vector table, interrupt service routine (ISR), interrupt priority, nested interrupts, interrupt latency.

Chapter 141

Direct Memory Access (DMA)

DMA controller, bus mastering, DMA transfer modes (burst, cycle stealing), scatter-gather DMA, reducing CPU overhead.

Chapter 142

I/O Buses and Interconnects

System bus, front-side bus, peripheral buses, PCIe (lanes, endpoints, root complex), bus arbitration, bandwidth and latency.

Chapter 143

Storage Controllers and Interfaces

SATA, SAS, NVMe, NVMe over Fabrics, command queuing, storage protocol stack, queue depth and parallelism.

Chapter 144

Multi-Core Processors

Chip multiprocessors (CMP), symmetric multiprocessing (SMP), shared L2/L3 caches, on-chip interconnect (ring, mesh, crossbar).

Chapter 145

NUMA Architecture

Non-uniform memory access, memory affinity, local versus remote memory, NUMA domains, NUMA-aware programming.

Chapter 146

SIMD and Vector Processing

Single instruction multiple data, vector registers, lane-based execution, packed operations.

Chapter 147

x86 SIMD Extensions

MMX, SSE, SSE2-SSE4, AVX, AVX2, AVX-512, register width evolution.

Chapter 148

ARM NEON and SVE

NEON instruction set, Scalable Vector Extension, predication, variable vector length.

Chapter 149

GPU Architecture Overview

Massively parallel architecture, streaming multiprocessors, SIMT execution model.

Chapter 150

GPU Execution Model

Threads, warps/wavefronts, thread blocks, grid, kernel launch, occupancy.

Chapter 151

GPU Memory Hierarchy

Global memory, shared memory, registers, constant memory, texture memory, L1/L2 caches.

Chapter 152

GPU Programming Models

CUDA, OpenCL, compute shaders, host-device interaction, kernel code.

Chapter 153

Input/Output Architecture

I/O devices, device controllers, I/O buses, programmed I/O vs. interrupt-driven I/O.

Chapter 154

Interrupt Mechanism

Interrupt vector table, interrupt service routines, interrupt priority, nested interrupts.

Chapter 155

Interrupt Handling Details

Context saving/restoration, interrupt latency, interrupt masking, edge vs. level triggered.

Chapter 156

Exception Handling

Faults, traps, aborts, exception vectors, privilege level transitions.

Chapter 157

Direct Memory Access (DMA)

DMA controllers, bus mastering, scatter-gather DMA, DMA descriptors, reducing CPU overhead.

Chapter 158

I/O Memory Management Unit (IOMMU)

Device address translation, DMA protection, virtualization support, IOMMU page tables.

Chapter 159

Bus Architecture and Protocols

System bus, memory bus, I/O bus, bus arbitration, split transactions.

Chapter 160

Interconnect Fabrics

Point-to-point links, crossbar switches, mesh networks, ring interconnects.

Chapter 161

PCIe Architecture

Lanes, link width, generations (1.0-6.0), packets and transactions, TLP/DLLP/Physical layers.

Chapter 162

Cache-Coherent Interconnects

Intel QPI/UPI, AMD Infinity Fabric, coherence traffic, non-uniform cache access (NUCA).

Chapter 163

Network-on-Chip (NoC)

On-chip routing, wormhole routing, virtual channels, deadlock avoidance.

Chapter 164

Power Management Mechanisms

Dynamic voltage and frequency scaling (DVFS), clock gating, power gating, C-states, P-states.

Chapter 165

Thermal Design and Throttling

Thermal design power (TDP), temperature monitoring, thermal throttling, cooling solutions.

Chapter 166

Hardware Performance Counters

Performance monitoring units (PMU), counting events (cycles, instructions, cache misses, branch mispredictions).

Chapter 167

Profiling with Hardware Counters

Perf tools, VTune, hardware event sampling, attributing performance to code.

Chapter 168

Hardware Security Features

Secure boot, trusted execution environments (SGX, TrustZone), memory encryption (SEV, TME).

Chapter 169

Spectre and Meltdown

Speculative execution vulnerabilities, side-channel attacks, mitigations (KPTI, retpoline, microcode updates).

Chapter 170

Memory Safety Mechanisms

Bounds checking (Intel MPX), pointer authentication (ARM PAC), tagged memory, stack canaries.

Chapter 171

Hardware Debugging Infrastructure

JTAG, boundary scan, trace debugging, watchpoints, breakpoints.

Chapter 172

Design for Testability

Scan chains, built-in self-test (BIST), fault injection, manufacturing test.

Chapter 173

Hardware Description Languages

Verilog and SystemVerilog, VHDL, behavioral vs. structural modeling, simulation vs. synthesis.

Chapter 174

Digital Design Flow

RTL design, logic synthesis, place and route, timing closure, physical design.

Chapter 175

FPGA Architecture

Look-up tables (LUTs), configurable logic blocks (CLBs), programmable interconnect, block RAM, DSP slices.

Chapter 176

ASIC vs. FPGA Tradeoffs

Performance, power, cost, flexibility, development time, reconfigurability.

Part III

Array Odyssey

AT LAST we arrive at arrays themselves—the most fundamental data structure in computing. This part explores arrays from every conceivable angle: theory, implementation, optimization, and application.

What Makes This Different:

- ***Complete Coverage:*** *Every variant, every technique*
- ***Hardware Awareness:*** *Cache effects, alignment, prefetching*
- ***Rigorous Analysis:*** *Mathematical foundations and performance*
- ***Practical Optimization:*** *Making arrays fast in real systems*

> *"Simplicity is prerequisite for reliability."*
>
> — EDSGER W. DIJKSTRA

Chapter 177

Mathematical Foundations of Arrays

Formal definition, array as function from index set to value set, properties, mathematical operations.

Chapter 178

Array as Abstract Data Type

Interface specification, invariants, preconditions, postconditions, ADT vs. implementation.

Chapter 179

One-Dimensional Array: Memory Layout

Contiguous allocation, base address, element offset calculation, memory alignment.

Chapter 180

Address Calculation and Pointer Arithmetic

Computing element addresses, stride, pointer arithmetic rules, bounds.

Chapter 181

Zero-Based vs. One-Based Indexing

Historical reasons, language conventions, conversion, pros and cons.

Chapter 182

Array Bounds and Boundary Conditions

Index range, out-of-bounds access, undefined behavior, bounds checking strategies.

Chapter 183

Array Allocation: Stack vs. Heap

Automatic (stack) allocation, dynamic (heap) allocation, lifetime management, size limitations.

Chapter 184

Static Array Declaration

Compile-time size, storage duration, initialization, usage patterns.

Chapter 185

Dynamic Memory Allocation for Arrays

malloc/calloc/realloc, new/delete, memory leaks, fragmentation.

Chapter 186

Array Deallocation and Resource Management

Proper cleanup, RAII pattern, smart pointers, memory ownership.

Chapter 187

Array Initialization Techniques

Zero-initialization, value initialization, aggregate initialization, designated initializers.

Chapter 188

Array Initialization Performance

memset internals, compiler optimizations, initialization costs, lazy initialization.

Chapter 189

Array Copying Fundamentals

Shallow vs. deep copy, copy semantics, assignment operators.

Chapter 190

Memory Transfer Operations

memcpy, memmove, bulk copy performance, vectorized copying.

Chapter 191

Array Access Patterns and Performance

Sequential access, random access, strided access, impact on cache and prefetching.

Chapter 192

Cache Line Utilization

Cache line size (64 bytes typical), spatial locality, utilizing full cache lines.

Chapter 193

Prefetching for Array Access

Hardware prefetching, software prefetching, prefetch instructions, prefetch distance.

Chapter 194

Array Traversal Optimization

Loop order, blocking/tiling, minimizing cache misses, memory access patterns.

Chapter 195

Dynamic Arrays: Implementation

Capacity vs. size, growth strategy, amortized analysis, C++ std::vector internals.

Chapter 196

Dynamic Array Growth Strategies

Doubling, multiplicative (2, golden ratio), additive growth, tradeoff analysis.

Chapter 197

Dynamic Array Amortized Analysis

Proving O(1) amortized append, potential method, aggregate analysis.

Chapter 198

Dynamic Array Reallocation

In-place vs. move to new location, realloc behavior, minimizing copying.

Chapter 199

Dynamic Array Shrinking

Shrink-to-fit, hysteresis, when to shrink, avoiding oscillation.

Chapter 200

Multidimensional Array Fundamentals

Dimensions, shape, indexing multiple dimensions, row-major vs. column-major.

Chapter 201

Row-Major Order (C Convention)

Layout in memory, linearization formula, cache implications.

Chapter 202

Column-Major Order (Fortran Convention)

Layout differences, when it matters, interfacing with Fortran libraries (BLAS, LAPACK).

Chapter 203

Multidimensional Array Address Calculation

Linear index from multiple indices, stride computation, optimization.

Chapter 204

Multidimensional Array Traversal

Loop nesting order, cache-friendly traversal, impact of memory layout.

Chapter 205

Array of Arrays vs. True Multidimensional

Pointer indirection, flexibility, memory overhead, cache implications.

Chapter 206

Jagged Arrays

Non-rectangular arrays, array of arrays for irregular sizes, applications.

Chapter 207

Dope Vectors and Array Descriptors

Metadata representation, bounds information, enabling flexible array operations.

Chapter 208

Sparse Array Fundamentals

When most elements are zero (or default), compression ratio, sparsity pattern.

Chapter 209

Sparse Array: Coordinate List (COO)

List of (row, col, value) tuples, easy construction, inefficient access.

Chapter 210

Sparse Array: Compressed Sparse Row (CSR)

Row pointers, column indices, values, efficient row operations.

Chapter 211

Sparse Array: Compressed Sparse Column (CSC)

Column-oriented version of CSR, efficient column operations.

Chapter 212

Sparse Array: Dictionary of Keys (DOK)

Hash table representation, flexible construction, conversion to other formats.

Chapter 213

Sparse Array: List of Lists (LIL)

List per row, incremental construction, conversion to CSR.

Chapter 214

Sparse Matrix Operations

Sparse matrix-vector multiply, sparse-sparse operations, fill-in problem.

Chapter 215

Bit Arrays: Representation

Packing bits into words, storage efficiency, applications (sets, flags).

Chapter 216

Bit Array: Indexing and Access

Computing word and bit offset, extracting bits, setting bits.

Chapter 217

Bit Array Operations

Bitwise operations on arrays, parallel operations, applications.

Chapter 218

Bitmap Indexes

Using bitmaps for indexing, rank and select operations, succinct data structures preview.

Chapter 219

Circular Arrays and Ring Buffers

Wrap-around indexing, modulo arithmetic, avoiding data movement, queue implementation.

Chapter 220

Circular Array: Head and Tail Management

Tracking fill level, full vs. empty distinction, producer-consumer patterns.

Chapter 221

Array Searching: Linear Search

Sequential scan, early termination, best/worst/average case, sentinel technique.

Chapter 222

Array Searching: Binary Search

Prerequisites (sorted array), algorithm, invariants, complexity analysis.

Chapter 223

Binary Search: Implementation Variants

Iterative vs. recursive, overflow-safe midpoint, lower$_b$*oundvs.upper*$_b$*ound*.

Chapter 224

Binary Search: Applications

Finding insertion point, counting occurrences, rotated arrays.

Chapter 225

Interpolation Search

Estimating position, prerequisites (uniform distribution), O(log log n) average case.

Chapter 226

Exponential Search

Unbounded search, doubling range, combination with binary search.

Chapter 227

Ternary Search

Dividing into three parts, unimodal functions, finding extrema.

Chapter 228

Jump Search

Block jumping, optimal jump size (n), combination with linear search, cache-friendly properties.

Chapter 229

Fibonacci Search

Division using Fibonacci numbers, single comparison per step, applications.

Chapter 230

Sorting Fundamentals

Comparison-based lower bound ((n log n)), stability, adaptivity, in-place vs. out-of-place.

Chapter 231

Bubble Sort

Adjacent swaps, optimization (early termination), adaptive behavior, teaching value.

Chapter 232

Selection Sort

Finding minimum, swap to position, in-place but not stable, $O(n^2)$ always.

Chapter 233

Insertion Sort

Inserting into sorted prefix, adaptive (O(n) on nearly sorted), online algorithm.

Chapter 234

Shell Sort

Gap sequences, h-sorting, diminishing increments, performance depends on gap sequence.

Chapter 235

Merge Sort Fundamentals

Divide and conquer, merge procedure, guaranteed O(n log n), stability.

Chapter 236

Merge Sort: Implementation Variants

Top-down recursive, bottom-up iterative, in-place merging attempts, natural merge sort.

Chapter 237

Merge Sort: Optimization Techniques

Switching to insertion sort for small subarrays, eliminating copy to auxiliary array.

Chapter 238

External Merge Sort

Sorting data larger than memory, multi-way merge, minimizing I/O, B-tree connection.

Chapter 239

Quick Sort Fundamentals

Partitioning, divide and conquer, average O(n log n), worst $O(n^2)$.

Chapter 240

Quick Sort: Pivot Selection Strategies

First element, random element, median-of-three, median-of-medians, ninther.

Chapter 241

Quick Sort: Partitioning Schemes

Lomuto partition, Hoare partition, three-way partition (Dutch National Flag).

Chapter 242

Quick Sort: Optimizations

Tail recursion elimination, switching to insertion sort, handling duplicates.

Chapter 243

Randomized Quick Sort

Random pivot selection, probabilistic analysis, expected O(n log n).

Chapter 244

Introsort

Hybrid algorithm, depth limiting, switching to heapsort, C++ std::sort implementation.

Chapter 245

Heap Sort Fundamentals

Building heap, extract-max repeatedly, in-place, not stable, guaranteed O(n log n).

Chapter 246

Binary Heap: Array Representation

Complete binary tree in array, parent/child index formulas, level-order storage.

Chapter 247

Heapify Operations

Sift-up (bubble-up), sift-down (percolate-down), building heap in O(n).

Chapter 248

Heap Sort: Optimization

Bottom-up heap construction, cache optimization, comparison count.

Chapter 249

Counting Sort

Integer sorting, counting occurrences, cumulative sum, linear time O(n+k).

Chapter 250

Radix Sort Fundamentals

Digit-by-digit sorting, LSD vs. MSD, stable sub-sorting required.

Chapter 251

Radix Sort: Implementations

Base/radix selection, counting sort as sub-routine, in-place variants.

Chapter 252

Bucket Sort

Distributing into buckets, uniform distribution assumption, O(n) average case.

Chapter 253

Timsort

Python's sorting algorithm, galloping mode, merge runs, adaptive merging.

Chapter 254

pdqsort (Pattern-Defeating Quicksort)

Rust's sort, detecting bad patterns, fallback strategies, block partitioning.

Chapter 255

Sorting Networks

Comparator networks, Batcher's sort, bitonic sort, parallel sorting.

Chapter 256

Parallel Sorting Algorithms

Parallel merge sort, parallel quicksort, sample sort, GPU sorting.

Chapter 257

Array Rotation: Reversal Algorithm

Reverse portions, three reversals, in-place, O(n) time, elegant proof.

Chapter 258

Array Rotation: Juggling Algorithm

GCD-based, moving elements in cycles, in-place, optimal moves.

Chapter 259

Array Rotation: Block Swap Algorithm

Recursive block swapping, handling unequal blocks, in-place rotation.

Chapter 260

Array Reversal In-Place

Two-pointer technique, swapping elements, O(n) time, O(1) space.

Chapter 261

Array Permutation: Application

Applying permutation in-place, cycle decomposition, O(n) time.

Chapter 262

Array Permutation: Generation

Generating all permutations, lexicographic order, Heap's algorithm, iterative methods.

Chapter 263

Array Shuffling

Fisher-Yates shuffle, uniform random permutation, in-place, bias-free.

Chapter 264

Array Partitioning Algorithms

Two-way partition (quicksort), three-way partition (Dutch flag), k-way partition.

Chapter 265

Stable Partitioning

Maintaining relative order, applications, implementation strategies.

Chapter 266

Quickselect Algorithm

Finding k-th smallest element, partition-based selection, average O(n).

Chapter 267

Median of Medians

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Chapter 268

Two-Pointer Technique: Basics

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Chapter 269

Two-Pointer: Sliding Window Fixed Size

Window size k, maintaining window state, deque for min/max in window.

Chapter 270

Two-Pointer: Sliding Window Variable Size

Expanding and contracting, maintaining invariants, applications (substring problems).

Chapter 271

Three-Pointer and Multiple-Pointer Techniques

Dutch National Flag, merging sorted arrays, complex partitioning.

Chapter 272

Prefix Sum: Construction

Cumulative sum array, O(n) construction, range sum query in O(1).

Chapter 273

Prefix Sum: Applications

Range queries, subarray sum, equilibrium index, difference arrays.

Chapter 274

Two-Dimensional Prefix Sum

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Chapter 275

Difference Arrays

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Chapter 276

Kadane's Algorithm

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Chapter 277

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Subarray Problems

Subarray vs. subsequence, contiguous vs. non-contiguous, counting subarrays.

Chapter 279

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Three-way partitioning, single pass, constant space, applications to quicksort.

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Array Intersection

Finding common elements, sorted arrays (two-pointer), unsorted (hash set).

Chapter 281

Array Union and Set Operations

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Chapter 282

Merging Sorted Arrays

Two-way merge, k-way merge (heap-based), in-place merging.

Chapter 283

Array Compaction

Removing elements while maintaining order, in-place, stable compaction.

Chapter 284

Array Gap Removal

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Chapter 285

Array Element Frequency

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Majority Element Algorithm

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Array Rearrangement Problems

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Array Memory Alignment: SIMD

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Overhead analysis, optimization opportunities, eliminating redundant checks.

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Bounds Checking: Language Support

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Non-owning references, NumPy slicing, stride manipulation, views vs. copies.

Chapter 297

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Strided Array Access

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Chapter 299

Array Subviews and Windows

Creating windows without copying, sliding windows, overlapping windows.

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Array Broadcasting

Implicit dimension expansion, NumPy broadcasting rules, shape compatibility.

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Broadcasting: Implementation

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Chapter 302

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Chapter 303

Parallel Reduction Patterns

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Chapter 304

Array Scan Operations

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Parallel Scan Algorithms

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Chapter 306

Scan Applications

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Chapter 308

Array Scatter Operations

Indexed writes, scatter to array using index array, conflict handling.

Chapter 309

Gather-Scatter in SIMD

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Chapter 310

Array Comprehensions

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Array Generators and Iterators

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Chapter 312

Array Reshaping

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Array Transposition

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Chapter 314

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Joining arrays along axis, horizontal stack (column-wise), vertical stack (row-wise).

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Array Splitting

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Border padding (image processing), alignment padding, ghost cells (stencil computations).

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Special array structures, efficient storage, fast multiplication (FFT).

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Diagonal storage format, bandwidth, tridiagonal systems, efficient solvers.

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Array Vectorization Fundamentals

Writing vector-friendly code, enabling autovectorization, compiler hints.

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Loop Vectorization

Data dependencies, trip count, alignment, remainder loops.

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Array Versioning and Copy-on-Write

Persistent arrays, sharing data between versions, efficient versioning.

Chapter 326

Immutable Arrays

Functional programming, structural sharing, immutability benefits.

Chapter 327

Array Performance Profiling

Measuring access patterns, cache simulation tools, hardware counters.

Chapter 328

Roofline Model for Arrays

Arithmetic intensity, bandwidth bounds, computational bounds, optimization guidance.

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Array Benchmarking Methodology

Microbenchmarks, cache warming, timing techniques, statistical significance.

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Data Structures & Algorithms

Part V

Parallelism & Systems

Part VI

Synthesis & Frontiers

Glossary

Reflections at the End

As you turn the final pages of *Arliz*, I invite you to pause—just for a moment—and look back. Think about the path you've taken through these chapters. Let yourself ask:

> "Wait… what just happened? What did I actually learn?"

I won't pretend to answer that for you. The truth is—**only you can**. Maybe it was a lot. Maybe it wasn't what you expected. But if you're here, reading this, something must have kept you going. That means something.
This book didn't start with a grand plan. It started with a simple itch: **What even is an array, really?** What began as a curiosity about a "data structure" became something much stranger and—hopefully—much richer. We wandered through history, philosophy, mathematics, logic gates, and machine internals. We stared at ancient stones and modern memory layouts and tried to see the invisible threads connecting them.
If that sounds like a weird journey, well—yeah. It was.

This is Not the End

Arliz isn't a closed book. It's a snapshot. A frame in motion. And maybe your understanding is the same. You'll return to these ideas later, years from now, and see new angles. You'll say, "Oh. That's what it meant." That's good. That's growth.
Everything you've read here is connected to something bigger—algorithms, networks, languages, systems, even the people who built them. There's no finish line. And that's beautiful.

From Me to You

If this book gave you something—an idea, a shift in thinking, a pause to wonder—then it has done its job. If it made you feel like maybe programming isn't just code and rules, but a window into something deeper—then that means everything to me.

Thank you for being here.
Thank you for not skipping the hard parts.
Thank you for choosing to think.

One More Thing

You're not alone in this.
The Arliz project lives on GitHub, and the conversations around it will (hopefully) continue. If you spot mistakes, have better explanations, or just want to say hi—come by. Teach me something. Teach someone else. That's the best way to say thanks.
Knowledge grows in community.
So share. Build. Break. Rebuild.
Ask better questions.
And always, always—stay curious.

Final Words

Arrays were just the excuse.
Thinking was the goal.
And if you've started to think more clearly, more deeply, or more historically about what you're doing when you write code—then this wasn't just a technical book.
It was a human one.
Welcome to the quiet, lifelong joy of understanding.

This completes the first living edition of Arliz.

Thank you for joining this journey from zero to arrays, from ancient counting to modern computation.

The exploration continues...

Author's Notes and Reflections

On Naming Conventions and Creative Processes

I should confess something about my naming process: I tend to pick names first and find meaningful justifications later. Very scientific, I know! The name "Arliz" started as a random choice that simply felt right phonetically. Only after committing to it did I discover the backronym that now defines its meaning. This probably says something about my creative process—intuition first, rationalization second.

This approach extends beyond naming. Many aspects of this book emerged organically from curiosity rather than systematic planning. What began as personal notes to understand arrays evolved into a comprehensive exploration of computational thinking itself.

On Perfectionism and Living Documents

You should know that many of the algorithms presented in this book are my own implementations, built from first principles rather than copied from optimized sources. This means you might encounter code that runs slower than industry standards—or occasionally faster, when serendipity strikes.

Some might view this as a weakness, but I consider it a feature. The goal isn't to provide the most optimized implementations but to demonstrate the thinking process that leads to understanding. When you can reconstruct a solution from fundamental principles, you've achieved something more valuable than memorizing an optimal algorithm.

On Academic Formality and Personal Voice

You might notice that this book alternates between formal academic language and more conversational tones. This is intentional. While I respect the precision that formal writing provides, I also believe that learning happens best in an atmosphere of intellectual friendship rather than academic intimidation.

When I suggest you could "use this book as a makeshift heating device" if you find the approach ridiculous, I'm not being flippant—I'm acknowledging that not every approach works for every learner. Intellectual honesty includes admitting when your methods might not suit your audience.

On Scope and Ambition

The scope of this book—from ancient counting to modern distributed systems—might seem overly ambitious. Some might argue that such breadth necessarily sacrifices depth. I disagree, but I understand the concern.

My experience suggests that understanding connections between disparate fields often provides insights that narrow specialization misses. When you see arrays as part of humanity's broader intellectual project, you understand them differently than when you see them as isolated programming constructs.

That said, if you find the historical sections tedious or irrelevant, you have my permission to skip ahead. The book is designed to be valuable even when read non-sequentially.

On Errors and Imperfection

I mentioned that you'll find errors in this book. This isn't false modesty—it's realistic acknowledgment. Complex explanations, mathematical derivations, and code implementations inevitably contain mistakes, especially in a work that grows and evolves over time.

Rather than viewing this as a flaw, I encourage you to see it as an opportunity for engagement. When you find an error, you're not just identifying a problem—you're participating in the process of building better understanding. The best learning often

happens when we encounter and resolve contradictions.

On Time Investment and Expectations

When I suggest this book requires months rather than weekends to master, I'm not trying to inflate its importance. Complex concepts genuinely require time to internalize. Mathematical intuition develops gradually, through repeated exposure and active practice.

If you're looking for quick solutions to immediate programming problems, this book will frustrate you. If you're interested in developing the kind of deep understanding that serves you throughout your career, the time investment will prove worthwhile.

On Community and Collaboration

This book exists because of community—the open-source community that provides tools and resources, the academic community that develops and refines concepts, and the programming community that applies these ideas in practice.

Your engagement with this material makes you part of that community. Whether you find errors, suggest improvements, or simply work through the exercises thoughtfully, you're contributing to the collective understanding that makes books like this possible.

Final Reflection

Writing this book has been an exercise in understanding my own learning process. I've discovered that I learn best by building connections between disparate ideas, by understanding historical context, and by implementing concepts from scratch rather than accepting them as given.

Your learning process might be entirely different. Use what serves you from this book, adapt what needs adaptation, and don't hesitate to supplement with other resources when my explanations fall short.

The goal isn't for you to learn exactly as I did, but for you to develop your own path to deep understanding.

These notes reflect thoughts and observations that didn't fit elsewhere but seemed worth preserving. They represent the informal side of a formal exploration—the human element in what might otherwise seem like purely technical content.