basic heuristics. The experimental results show that the new heuristic can lead to significant performance gain for a variety of scenarios.

Keywords: Task scheduling, Grid computing, Min-Min, Max-Min

(Code: 2725)

Title: Model Driven Safety Testing: Evolutionary Approach

Afshin Amighi, Mohammad Reza Akhavan

Abstract: The aim of this paper is to present a method for detecting safety conditions violations using Genetic Algorithms based on UML2.0 diagrams in Software design phase. Finding any data that violate a system's safety conditions in software design phase is significant point of our method. Therefore, having an automatic safety test based on our rule, will decrease the cost of changes due to safety critical systems validation. Safety critical Systems validation is the main application of this method.

Keywords: Validation, UML, Genetic Algorithms, Safety Testing, Safety Critical Systems

(Code: 2873)

Title: Staffing Software Maintenance Projects with Multiple Service Levels in SLA

Mahdi Ghorbalipoor Drav, Mohammad Reza Meybodi

Abstract: Today outsourcing a software system's maintenance is common in software industry. Software maintenance organizations need to estimate the size of software maintenance team, in order to make decisions about acceptance or rejection of a project. In this paper we present a method to estimate the optimal staffing needed for a project that has multiple service levels with different priority and response time. The priority and response time determined with a SLA. We use results of queuing theory to model the maintenance environment with non-preemptive priority M/M/c queue. We also show that response time of an arbitrary request can not be less than a specified time

Keywords: Outsourcing, Software Maintenance, Non-preemptive Priority M/M/c Queue.

COMP11
Computer Architecture 1

(Code: 1522)

Title: A High Speed Low Power Signed Digit Adder

Ghassem Jaberipur, Saeid Gorgin

Abstract: Signed digit (SD) number systems provide the possibility of constant-time addition, where inter-digit carry propagation is eliminated. Such carry-free addition is primarily a three-step process. The special case of maximally redundant SD number systems leads to more efficient carry-free addition. This has been previously achieved based on speculation of transfer values and use of three parallel adders. We propose an alternative nonspeculative addition scheme that computes the transfer values through a fast combinational logic. The proposed carry-free addition scheme is shown to improve performance in terms of speed, power and area. The simulation and synthesis of three previous works and this work, based on 0.13 μm CMOS technology, confirms the latter claim.

Keywords: Computer arithmetic, Carry-free addition, Signed-digit number system, Low power design, Maximal redundancy.

(Code: 1868)

Title: High Speed Pattern Recognition with Reconfigurable Neural Network Multi Expert System

Mahmood Fazlali, Ali Zakerolhoseini, Majid Mohamadi, Foad Lotfifar

Abstract: There are many algorithms presented in image processing. Multi expert system is a method that increases recognition rate by employing some concurrent algorithms. In this paper, a character recognition method based on the multi expert system is presented. Due to the hidden learning power in neural networks, experts are implemented using the neural networks. Due to the high complexity of these experts and thus low execution time, hardware implementation is used. The system is implemented on FPGA and for its flexibility in learning. The results have shown decrease in execution time and at the same time increase in the recognition rate with proposed reconfigurable neural network.

Keywords: Reconfigurable Computing, Multi Expert System, Character Recognition, FPGA

(Code: 2275)

Title: An Adaptive Architecture for the Bit-Serial Multiplication in the Galois Fields GF(2m)

Morteza Nikooghadam, Ehsan Malekian, Ali Zakerolhosseini

Abstract: In this paper, an efficient architecture for the implementation of polynomial basis multipliers over GF(2m) is presented. The proposed architecture provides an efficient execution of the Least Significant Bit (LSB)-first, bit-serial multiplication for different operand lengths. The selection of (LSB)-first over the (MSB)-first, is its implementation suitability with reduced delay time. The main features of the proposed architecture are its hardware simplicity which results in small area implementation, flexible Galois field sizes, and improvement of maximum clock frequency with lessen critical path delay.