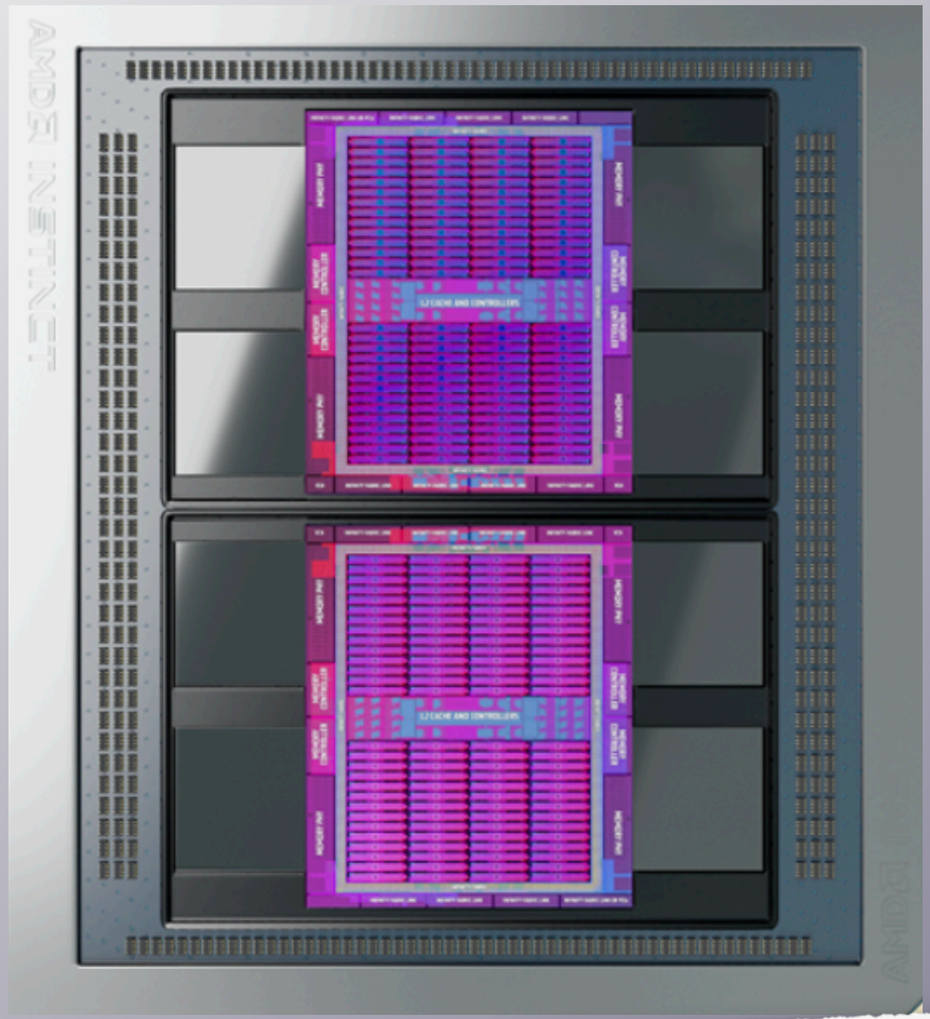
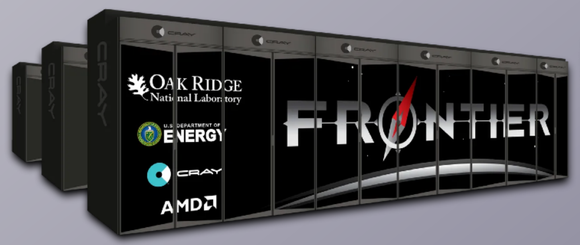
>2.3B Transistors

58B transistors on TN6



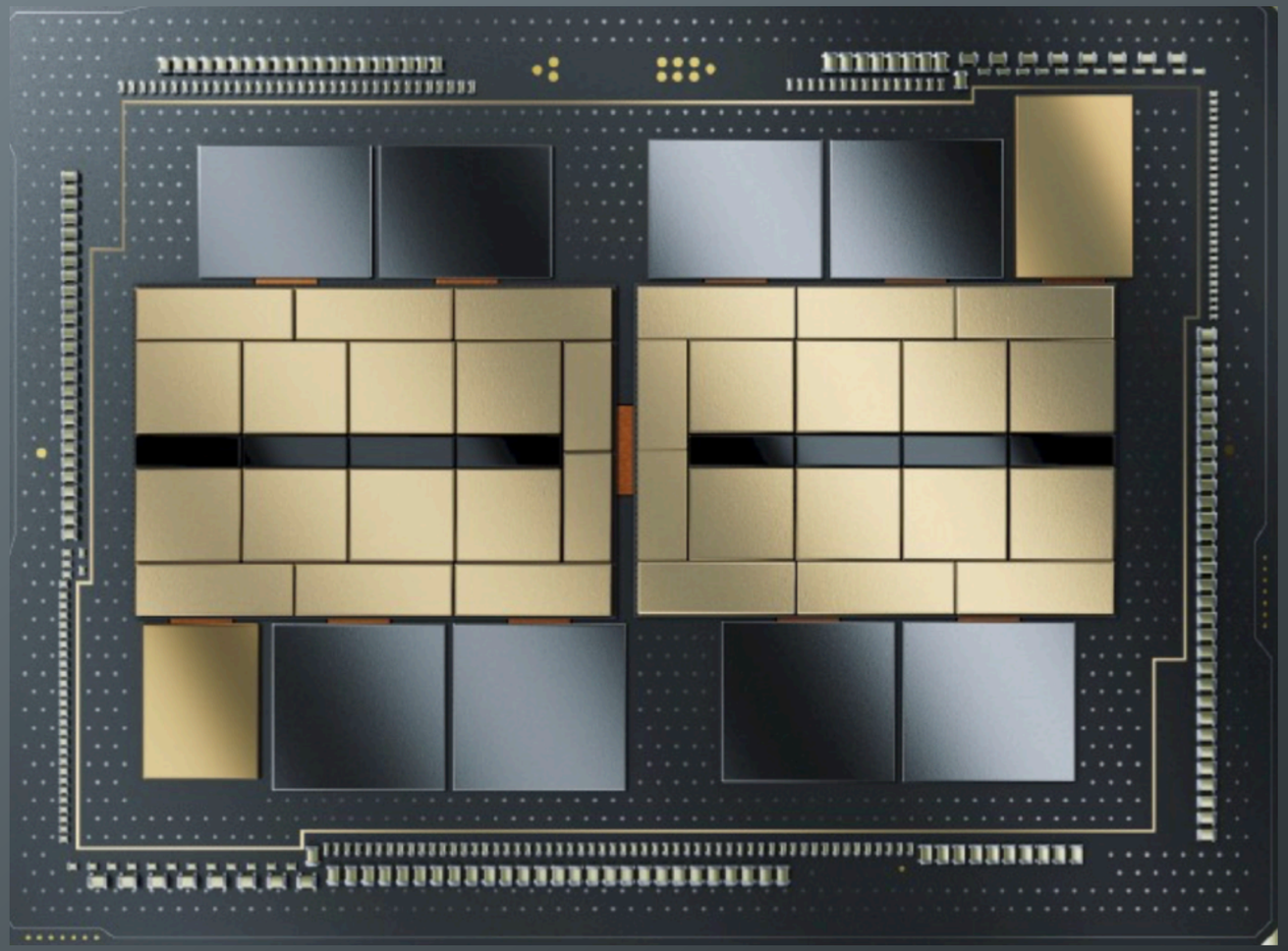


Frontier ≈ 4×10^4

MI-250X (AMD)

>6B Transistors

>100B transistors on TN5, (IN7, IN10)



Aurora ≈ 6×10^4

Xe (PVC) (Intel)

Aurora[1]

Leadership Computing Facility
Exascale Supercomputer

PEAK PERFORMANCE
≧ 2 Exaflops DP

Intel GPU
Ponte Vecchio

Intel Xeon PROCESSOR
Sapphire Rapids + HBM

PLATFORM
HPE Cray-Ex

Compute Node
2 SPR+HBM processor;
6 PVC; Unified
Memory Architecture;
8 fabric endpoints;

GPU Architecture
Xe arch-based “Ponte Vecchio” GPU
Tile-based chiplets
HBM stack
Foveros 3D integration

System Interconnect
HPE Slingshot 11; Dragonfly topology with adaptive routing

Network Switch
25.6 Tb/s per switch, from 64–200 Gb/s ports (25 GB/s per direction)

Node Performance
>130 TF

System Size
>9,000 nodes

Aggregate System Memory
>10 PB aggregate System Memory

High-Performance Storage
220 PB @ EC16+2, ≧**25 TB/s**
DAOS

Programming Models
oneAPI, MPI, OpenMP, C/C++, Fortran, SYCL/DPC++
Python-based environments
ML + Deep learning frameworks

1: *The Computer That WIll Change Everything*