System Controller Firmware Porting Guide

NXP

Fri Jun 19 2020 19:05:21

Chapter 1

Overview

The System Controller (SC) provides an abstraction to many of the underlying features of the hardware. This function runs on a Cortex-M processor which executes SC firmware (FW). This overview describes the features of the SCFW and the APIs exposed to other software components.

Features include:

- System Initialization and Boot
- System Controller Communication
- Power Management
- Resource Management
- Pad Configuration
- Timers
- Interrupts
- Security
- Miscellaneous

Due to this abstraction, some HW described in the SoC RM that is used by the SCFW is not directly accessible to other cores. This includes:

- All resources in the SCU subsystem (SCU M4, SCU LPUART, SCU LPI2C, etc.).
- All resource accessed via MSI links from the SCU subsystem (inc. pads, DSC, XRDC2, eCSR)
- OCRAM controller, CAAM MP, eDMA MP & LPCG
- DB STC & LPCG, IMG GPR
- GIC/IRQSTR LPCG, IRQSTR.SCU and IRQSTR.CTI
- Some features of SNVS such as the RTC, button, and LPGPR1
- Any other resources reserved by the port of the SCFW to the board

Note also the SECO uses some resources like CAAM JR0-1, SNVS LPGPR0, etc.

1.1 System Initialization and Boot

The SC firmware runs on the SCU immediately after the SCU Read-only-memory (ROM) finishes loading code/data images from the first container. It is responsible for initializing many aspects of the system. This includes additional power and clock configuration and resource isolation hardware configuration. By default, the SC firmware configures the primary boot core to own most of the resources and launches the boot core. Additional configuration can be done by boot code.

1.2 System Controller Communication

Other software components in the system communicate to the SC via an exposed API library. This library is implemented to make Remote Procedure Calls (RPC) via an underlying Inter-Processor Communication (IPC) mechanism. The IPC is facilitated by a hardware-based mailbox system.

Software components (Linux, QNX, FreeRTOS, KSDK) delivered for i.MX8 already include ports of the client API. Other 3rd parties will need to first port the API to their environment before the API can be used. The porting kit release includes archives of the client API for existing SW. These can be used as reference for porting the client API. All that needs to be implemented is the IPC layer which will utilize messaging units (MU) to communicate with the SCFW.

1.3 System Controller Services

The SCFW provides API access to all the system controller functionality exported to other software systems. This includes:

1.3.1 Power Management Service

All aspects of power management including power control, bias control, clock control, reset control, and wake-up event monitoring are grouped within the SC Power Management service.

- **Power Control** - The SC firmware is responsible for centralized management of power controls and external power management devices. It manages the power state and voltage of power domains as well as bias control. It also resets peripherals as required due to power state transitions. This is all done via the API by communicating power state needs for individual resources.
- **Clock Control** - The SC firmware is responsible for centralized management of clock controls. This includes clock sources such as oscillators and PLLs as well as clock dividers, muxes, and gates. This is all done via the API by communicating clocking needs for individual resources.
- **Reset Control** - The SC firmware is responsible for reset control. This includes booting/rebooting a partition, obtaining reset reasons, and starting/stopping of CPUs.

Before any hardware in the SoC can be used, SW must first power up the resource and enable any clocks that it requires, otherwise access will generate a bus error. More detail can be found in the Power Management section. The Power Management (PM) API is documented here.

1.3.2 Resource Management Service

SC firmware is responsible for managing ownership and access permissions to system resources. The features of the resource management service supported by SC firmware include:

- Management of system resources such as SoC peripherals, memory regions, and pads
- Allows resources to be partitioned into different ownership groupings that are associated with different execution environments including multiple operating systems executing on different cores, TrustZone, and hypervisor
- Associates ownership with requests from messaging units within a resource partition
- Allows memory to be divided into memory regions that are then managed like other resources
- Allows owners to configure access permissions to resources
- Configures hardware components to provide hardware enforced isolation
- Configures hardware components to directly control secure/nonsecure attribute driven on bus fabric
- Provides ownership and access permission information to other system controller functions (e.g. pad ownership information to the pad muxing functions)

Protection of resources is provided in two ways. First, the SCFW itself checks resource access rights when API calls are made that affect a specific resource. Depending on the API call, this may require that the caller be the owner, parent of the owner, or an ancestor of the owner. Second, any hardware available to enforce access controls is configured based on the RM state. This includes the configuration of IP such as XRDC2, XRDC, or RDC, as well as management pages of IP like CAAM.

Partitions own resources, pads, and memory regions. This includes owning MU resources to communicate with the S↩ CFW. API calls to the SCFW lookup the owner of the MU the call comes in on, and that is treated as the calling partition. Different API calls then enforce operations based on the relationship of the calling partition to the partition being acted on. This association does not directly determine who can access the programming model of a resource IP. This is solely determine by the access rights defined (per partition) for the resource. Note partitions do not have owners (they are the owners), but they do have parent/child relationships. The creator of a partition is the parent unless that parent calls the API to change the parent. If no parent is desired, then the parent should be set to 0 (the SCFW itself). Being the patent provides some rights with respect to API calling (but not peripheral access).

More detail can be found in the Resource Management section. The Resource Management (RM) API is documented here.

1.3.3 Pad Configuration Service

Pad configuration is managed by SC firmware. The pad configuration features supported by the SC firmware include:

- Configuring the mux, input/output connection, and low-power isolation mode.
- Configuring the technology-specific pad setting such as drive strength, pullup/pulldown, etc.
- Configuring compensation for pad groups with dual voltage capability.

The Pad (PAD) API is documented here.

1.3.4 Timer Service

Many timer oriented services are grouped within the SC Timer service. This includes watchdogs, RTC, and system counter.

- **Watchdog** - The SC firmware provides "virtual" watchdogs for all execution environments. Features include update of the watchdog timeout, start/stop of the watchdog, refresh of the watchdog, return of the watchdog status such as maximum watchdog timeout that can be set, watchdog timeout interval, and watchdog timeout interval remaining.
- **Real-Time-Clock** - The SC firmware is responsible for providing access to the RTC. Features include setting the time, getting the time, and setting alarms.
- **System Counter** - The SC firmware is responsible for providing access to the SYSCTR. Features include setting an absolute alarm or a relative, periodic alarm. Reading is done directly via local hardware interfaces available for each CPU.

The Timer API is documented here.

1.3.5 Interrupt Service

The System Controller needs a method to inform users about asynchronous notification events. This is done via the Interrupt service. The service provides APIs to enable/disable interrupts to the user and to read the status of pending interrupts. Reading the status automatically clears any pending state. The Interrupt (IRQ) API is documented here.

1.3.6 Security Service

The SC firmware provides access to many security functions including:

- Image Authentication
- Generating, exporting, and loading key blobs
- Fuse programming
- Lifecycle management
- Attestation

The Security (SECO) API is documented here.

See the SECO API Reference Guide for more info.

1.3.7 Miscellaneous Service

On previous i.MX devices, miscellaneous features were controlled using IOMUX GPR registers with signals connected to configurable hardware. This functionality is being replaced with DSC GPR signals. SC firmware is responsible for programming the GPR signals to configure these subsystem features. The SC firmware also responsible for monitoring various temperature, voltage, and clock sensors.

- **Controls** - The SC firmware provides access to miscellaneous controls. Features include software request to set (write) miscellaneous controls and software request to get (read) miscellaneous controls.
- **DMA** - The SC firmware provides access to DMA channel grouping and priority functions.
- **Temp** - The SC firmware provides access to temperature sensors.

The Miscellaneous (MISC) API is documented here.

Chapter 2

Disclaimer

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.↩ com/SalesTermsandConditions. While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREE↩ NCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE P↩ LUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C 5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobile↩ GT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. Arm, AMBA, Arm Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and ?Vision are registered trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. Arm7, Arm9, Arm11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, Mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

Chapter 3

Porting Guide

The System Controller (SC) provides an abstraction to many of the underlying features of the hardware. This function runs on a Cortex-M processor which executes SC firmware (SCFW). The SCFW is responsible for some aspects of system boot, power/clock management, and resource management. As a result, the SCFW implementation is specific to the board. Board specific implementation includes mandatory PMIC support and optional DDR configuration. It also includes optional resource partition configuration.

The board support is contained in a board module consisting of a board.c implementation file and the board.h interface file. The board.c file has to be ported to any new board.

Functionality in the board module includes:

- **Initialization** - used to initialize board data structures and sometimes HW.
- **Configuration** - used to configure the SCFW, including which resources it keeps.
- **DDR Configuration** - used to configure DDR; This function is called indirectly by the ROM with all true parameters.
- **Resource Config** - used to optionally defined and configure resource partitions required before starting other CPUs
- **PMIC Support** - initialization, power supply control, temp sensor configuration and reporting, etc.
- **Board Reset** - generate board reset; usually standard but could require something unique on some boards
- **Board Control** - interface that can be exposed to SCFW clients handing things like PMIC temp sensor access and user-controlled voltages

The board.h interface is documented in the Board Interface Module section.

3.1 Release

The SCFW is released for porting as a collection of object files, header files, make files, build scripts, and source code for the board module. Using this package, one can port board.c for a new board, compile it, and link with the delivered object files to create an SCFW binary.

SCFW is released and tested as part of other SW releases such as Linux and QNX OS releases. As a result, the SCFW port to a board must be based on the version of SCFW supplied with an OS release. SCFW object/porting packages should be supplied with OS releases.

The porting kit contains separate tar files for each SoC/version combination. These can be combined using the following command:

```
find scfw_export_mx8*.gz -exec tar --strip-components 1 --one-top-level=scfw_export_mx8 -xzvf {} \;
```

Note porting kits are self-extracting archives and should be executed on a Linux system. They can also be opened with utilities like 7-zip.

3.2 Build Environment

SCFW builds are compiled with a cross compiler and will only run on i.MX8 hardware. The SC firmware is a 32-bit program compiled using the GNU C compiler (gcc), debugged using the GNU debugger (gdb/ddd), and documented using doxygen. As a result, a GNU-compliant build environment is required. Linux must be used to compile target builds as that requires a cross compiler.

3.3 Tool Chain

This SW package builds on a Linux host machine. The toolchain for compiling should be obtained from the ARM download site. The version used is the GNU Arm Embedded Toolchain: 8-2018-q4-major December 20, 2018. Download the toolchain source and follow ARM's instructions for compiling on the host Linux machine.

Install the cross-compile toolchain on the Linux host. The TOOLS environment variable then needs to be set to the directory containing the compiler directory. For example, if using the GCC 4.9 cross-compile tools chain and installing to /home/example/gcc-arm-none-eabi-8-2018-q4-major then TOOLS would be set to /home/example. Building also requires srec_cat which is usually found in the Linux srecord package. Optionally the cppcheck package is also useful.

If using bash, then set the TOOLS environment variable as follows:

```
export TOOLS=<your path to dir holding the toolchain>
```

This can be added to .bash_profile.user or .bash_profile depending on the environment.

If using tcsh, then set the TOOLS environment variable as follows:

```
setenv TOOLS <your path to dir holding the toolchain>
```

This can be added to .tcshrc.user or .tcshrc depending on the environment.

3.4 Compiling the Code

The SC firmware can be fully compiled using the Makefile. The command format is:

Usage: make TARGET OPTIONS

SCFW targets are based on the die, not the part number. Some parts are phantoms of other die (for example QP is a phantom of QM) created by fusing options. Phantoms are supported at run-time by the SCFW reading the fuses and adapting. Note some parts are available as both a die and phantom (early samples).

There are three primary die targets:

- **qm** : i.MX8QM die
- **qx** : i.MX8QX die
- **dxl** : i.MX8DXL die

These generate the image (scfw_tcm.bin) in their respective build directory.

There are several options that can be specified on the make command line:

Option	Action
V=0	quite output (default)
V=1	verbose output
D=0	configure for no debug
D=1	configure for debug (default)
DL=<level>	configure debug level (0-5)
M=0	no debug monitor (default)
M=1	include debug monitor
B=<board>	configure board (default=val)
U=<uart>	configure debug UART (default=0)
DDR_CON=<file>	specify DDR config file w/o extension
R=<srev>	silicon revision
T=<test>	run tests rather than boot next core

Note the debug level will only affect the code being compiled. It will not affect the code delivered in binary (i.e. object) form.

3.4.1 i.MX8QM (QP, some DM) Die Build

The i.MX8QM die targets are as follows:

Target	Action
qm	build for i.MX8QM die, output in build_mx8qm
clean-qm	remove all build files for the i.MX8QM die build

3.4.2 i.MX8QX (QXP, DX, DXP) Die Build

The i.MX8QX die targets are as follows:

Target	Action
qx	build for i.MX8QX die, output in build_mx8qx
clean-qx	remove all build files for the i.MX8QX die build

3.4.3 i.MX8DXL Die Build

The i.MX8DXL die targets are as follows:

Target	Action
dxl	build for i.MX8DXL die, output in build_mx8dxl
clean-dxl	remove all build files for the i.MX8DXL die build

3.4.4 Generic Targets

The Makefile supports some generic targets:

Target	Action
help	display help test
clean	delete all build directories

3.5 Production

When the SCFW is compiled for release into production devices, it is critical that this is done without debug (default is debug enabled, D=1) and without the debug monitor (default is no monitor, M=0). For example:

```
make qm R=B0 D=0 M=0
```

Turning off debug will eliminate the linking of the standard C library.

3.6 Porting

Porting starts with creating a copy of a NXP-supplied board port such as that for the MEK board (e.g. mx8qx_mek). These are found in the platform/board directory. Note the validation board ports dynamically detect the PMIC which affects boot time. Production ports should not do this.

- Create a copy and name it soc_board where soc is the name of the Soc and board is the name of the board
- The Makefile should be modified to compile all the board module files. Usually this is just board.c but it could also include other source files in the board directory such as DDR configuration code, etc.

- The board.bom file should be modified to include drivers required by the board file that are not part of the standard build. This is usually just PMIC drivers. LPI2C, GPIO, etc. drivers are built in already.
- Modify board.c to provide support for the new board.
- Build the SCFW as described in the next section (e.g. make qm B=newboard).

The resulting binary can be found in the output directory (e.g. build_mx8qx) as scfw_tcm.bin.

Note the board.c file can call any of the internal functions within the SCFW including driver functions and SCFW API functions. When calling SCFW API functions, use the internal version (those without the sc_ prefix). For example, call pm_get_clock_rate() instead of sc_pm_get_clock_rate(). The internal functions don't take an IPC channel as the first parameter and instead take a calling partition number. Use SC_PT for calls intended to come from the SCU and the partition number for calls intended to come from other partitions. The API description for the latter is included here for reference.

The SCFW is built on top of the MCUXpresso SDK. The CMSIS, C startup, and many of the drivers come from the KSDK. KSDK drivers include RGPIO, LPI2C, LPIT, LPUART, MU, and WDOG32. The RGPIO an LPI2C can be used in the board.c port to interface with the SCU RGPIO and SCU LPI2C.

3.7 Porting Notes

Below are some suggestions for board porting:

- Don't modify the section marked DO NOT CHANGE.
- Do not probe for a PMIC like the NXP validation board reference does (this consumes boot time).
- Don't communicate to the PMIC until absolutely necessary (I2C is slow).
- board_parameter() can be called at any time. If a return value is based on run-time detection (for example reading a GPIO) great care must be take to insure the return value is correct and that infrastructure is powered to allow this. This can be impossible if the API is not yet initialized. As a result, GPIO used for this should be connected to the SCU GPIO (not LSIO GPIO).
- Using the rom_caller variable in your DDR config file to avoid running from ROM is faster and easier to debug but it is too late when booting the AP cluster from DDR.
- board_ddr_config() might be called from the ROM (rom_caller = SC_TRUE). In this case, the SCFW startup has not yet run and it is not valid to call most SCFW function calls. **DSC_AIRegisterWrite() and SYSCTR_Time↩ Delay() are the only two functions that have are safe to call.** Most of the time this code is generated using the RPA tool and the generated code should not be modified.
- If M4 boot time is important and if the M4 code doesn't use DDR then don't configure DDR early. Wait until after the M4 has started. An 'early' parameter is passed to board_init_ddr() to indicate which phase the call is occurring in.
- Configure any supplies always needed in board_init(). Keep in mind this is still pretty late in the boot process (only after the SCFW is loaded and run). Any supplies needed to load the SCFW from the boot device must be configured using the OTP in the PMIC.
- board_set_power_mode() and board_set_voltage() are where mapping of SoC power inputs to PMIC supplies should be done. These functions may be called as a result of a client calling sc_pm_set_resource_power_mode() on a SoC resource or when changing the frequency for some resources that then need a different voltage.

- There are eight resources defined for board-level components (board resources). These are SC_R_BOARD_R0 through SC_R_BOARD_R7.
- board_trans_resource_power() is where mapping of board resource power inputs to PMIC supplies should be done. This function is called as a result of a client calling sc_pm_set_resource_power_mode() on a board resource.
- board_set_control() should be used if SCFW clients need to be able to set the voltage for PMIC supplies to board resources. The control would be SC_C_VOLTAGE. This function is called as a result of a client calling sc_misc_set_control().
- If power supplies are shared, usage counters will need to be used to keep track of how many domains or resources are using a supply and only change its state when the counter transitions from 0 to 1 or 1 to 0.
- Drivers are provided for the NXP PF100 and PF8100/8200 PMICs. If a new PMIC needs to be supported then the code should just be part of the board code base (not a new driver).
- If PF8100/PF8200 CRC operation is needed PMIC_CRC should be defined globally. Preferably in board.h
- board_parameter() is used to return various board design option info. For example, is the PCIe driven from an internal or external clock.
- board_rsrc_avail() returns SC_TRUE if a resource exists. The default is to return that all exist. Some boards will remove power for some resource (DRC 1, or ADC). This function then has to tell the SCFW that is the case else the SCFW will attempt to access, hang, and the SCFW WDOG reset the system. This is also the case for some i.MX8 packages.
- Isolate HW for booting cores by defining resource partitions in board_system_config(). Note these partitions should then be specified in the boot container using the mkimage -p option.
- The SCU and various other SS have temp sensors. They are all programmed to have a panic alarm temp. This is normally 127C junction temp but may vary by SoC (see AI_TEMP_PANIC in soc.h). This value cannot be changed as part of porting. If the SCU sensor panics then the system will reset. If the other sensors panic then board_panic() will be called and normally this is implemented to initiate a system reset.

3.8 Boot Flow

The i.MX8 boot architecture is described in a document by that name. By the time the SCFW runs, most of the initial images have been loaded (SCFW, SECO FW, AP IPL, M4 images, etc.). Loading of AP images is done later when the AP cores are started and run the ROM and/or AP IPL. All the loading is done by the SCU ROM and once it is done it jumps to the SCFW which has no ability to load anything further. The ROM does not start any of the CPUs. The SCFW does this only after it configures the isolation HW and is ready to field API requests from new running cores. The SCFW is also responsible for configuring the DRC if not already done by the SCU ROM via DCD. So, the basic boot flow of the SCFW is to configure the isolation HW, power up various parts of the SoC, configure the DDR, and start CPUs as requested by the ROM. It then enters a WFI loop executing API requests.

There are two primary boot modes supported by the SCFW: standard and early. In standard, no CPU is started until all the other steps are completed. At the end, all CPUs are started in the order they are requested by the ROM (which is based on the order they occur in the boot image). In early, some of the CPUs are started early before DDR is configured and before later CPUs are powered up or started. This mode is used to minimize the time from POR to M4 execution for some specific fast-boot use-cases. In this mode, early CPUs report they are done using sc_misc_boot_done().

The boot mode is configured using one of the flags in the boot container. Bit 22 of the flags (SC_BD_FLAGS_EARL↩ Y_CPU_START) must be set for early boot mode. This is done when the image is created using mkimage. The -flags argument passes a flag as a hex value. See Boot Flags for more info.

The boot flow diagrams below show the flow, including call-outs to the porting layer (board.c). Typical boot times are listed. These are measured values on existing i.MX8 reference boards. These times can change significantly as a result of board design, PMIC configuration, DDR configuration, and implementation of the porting layer. Compile is with DL=0 option to minimize debug output. The DRC is configured by the SCFW rather than by the ROM via DCD. The system config is an example that configures for all M4's to run in an isolated partition.

3.8.1 Standard Boot

The standard SCFW boot flow is show in the diagram below:

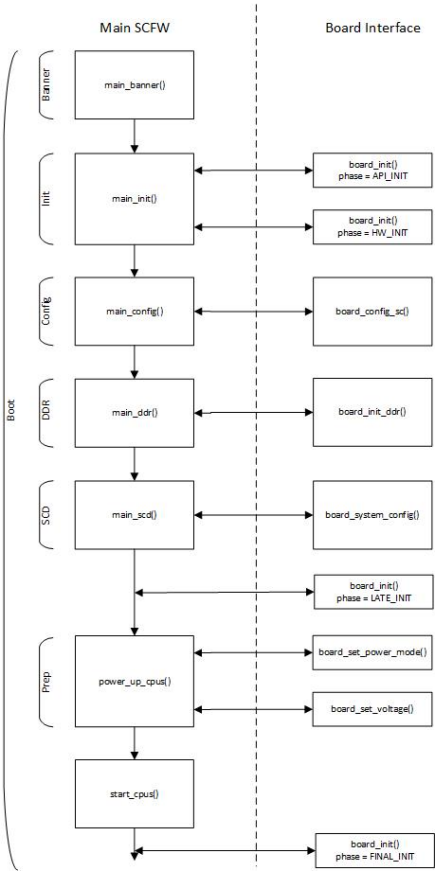

Figure 3.1 Standard SCFW Boot Flow

Details on the board.h interface are documented in the Board Interface Module section.

The typical boot times (measured on NXP reference boards) are as follows:

Phase	i.MX8QM B0 Time (ms)	i.MX8QX B0 Time (ms)	i.MX8QX C0 Time (ms)
Banner	0.1	0.1	0.1
Init	1.0	1.2	1.2
Config	4.6	4.2	3.1

Phase	i.MX8QM B0 Time (ms)	i.MX8QX B0 Time (ms)	i.MX8QX C0 Time (ms)
DDR	9.6	9.0	9.1
SConfig	7.6	3.3	3.1
Prep	5.8	4.7	3.9
Boot	31.8	25.6	22.1

The Boot time represents the time at which all the CPUs requested to be started by the ROM will be started (relative to the time SCFW runs).

3.8.2 Early Boot

The early SCFW boot flow is show in the diagram below:

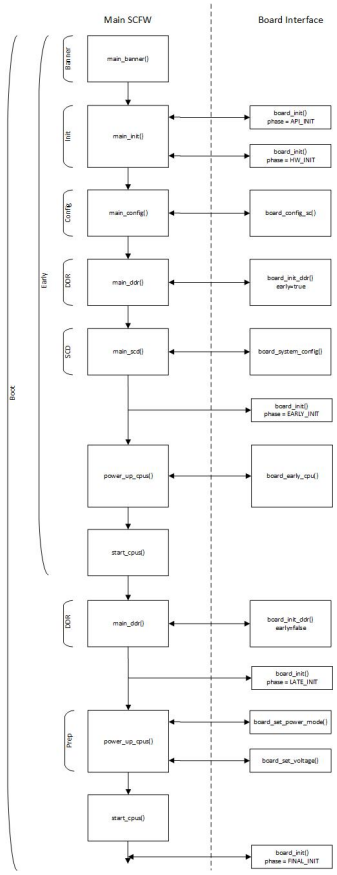

Figure 3.2 Early SCFW Boot Flow

Details on the board.h interface are documented in the Board Interface Module section.

The typical boot times (measured on NXP reference boards) are as follows:

Phase	i.MX8QM B0 Time (ms)	i.MX8QX B0 Time (ms)	i.MX8QX C0 Time (ms)
Banner	0.1	0.1	0.1
Init	1.0	1.2	1.2
Config	4.6	4.2	3.1
DDR	9.6	9.0	9.1
SConfig	7.6	3.3	3.1
Prep	5.2	4.7	3.9
Early	14.5	9.4	7.7
Boot	31.9	25.7	22.2

The Early time represents the relative time at which the early cores will be started. The Boot time represents the relative time at which the remaining CPUs requested to be started by the ROM will be started (usually the AP core). Early cores are usually M4 cores and determined by calling board_early_cpu().

Note that starting cores early is not sufficient to guarantee they can run to the point of handling critical tasks. SCFW API calls could block if the SCFW is configuring DDR, powering up other subsystems, or starting other CPUs. As a result, when in the early boot mode, the SCFW will wait for all cores started early to make an API call to inform the SCFW that they are past the critical boot stage and okay with SCFW API delays. The API call is sc_misc_boot_done(). While waiting on these calls, the SCFW is not proceeding to boot the non-early cores so this feature, while accelerating the boot of early cores, comes as the expense of boot time for non-early cores (usually the AP cores).

Note that the time reported for SConfig is dependent on customer-specific content added into the board_system_config() function. The SConfig times reported above include resource partitioning for the MEK hardware selected by setting the SC_BD_FLAGS_ALT_CONFIG flag in the image container.

Note that the DDR times reported above are specific to initializing and training the LPDDR4 memory included on the MEK hardware.

PMIC fuses are normally set to insure all power supplies are enabled and the voltage is correct for starting subsystems required for initial boot. This includes supplies for all early CPUs. The overhead for communicating to the PMIC (usually via I2C) is too high in a critical boot time case. Dynamic PMIC programming should be restricted to the power up of non-early subsystems and CPUs (typically AP cores, GPU, etc.).

3.9 SNVS and SECO

On all current i.MX8, the SNVS is contained in the SECO module. As a result, only SECO can directly access the SNVS. SECO FW exposes some functionality (functionality it doesn't use for itself, e.g. LPGPR0) to the SCU via an MU. This functionality is documented in the SECO API Reference Guide. This includes the following SECO messages:

- AHAB_WRITE_SNVS_PARAM_REQ
- AHAB_READ_SNSVS_PARAM_REQ
- AHAB_MANAGE_SNVS_REQ

Internal to the SCFW, these are exposed by the SCFW SECO Driver as:

- SECO_WriteSNVS() - do not call from board.c
- SECO_ReadSNVS() - do not call from board.c

- SECO_ManageSNVS()

While technically, these can be called in board.c code, it is advised not to use the first two. The SECO_ManageSNVS() function can be used to implement tamper detect, persistent storage, etc. Many aspects of the SNVS are used by SECO and not available for use (e.g. LPGPR0) and this function will not allow access to those registers/fields. Note also the main part of the SCFW uses some functionality (e.g. LPGPR1) and these are not available for use in board.c. This usage could change with updated SCFW releases.

Some aspects of the SNVS are then abstracted via the SCFW SNVS Driver. This does not abstract all the SNVS functionality. It only provides an API for the functions needed to implement the SCFW itself. Note that this includes management of the RTC (done internally in the SCFW) as well as the button, power off, etc.

Functions that can be called from board.c include:

- SNVS_PowerOff()
- SNVS_ConfigButton()
- SNVS_ButtonTime()
- SNVS_GetButtonStatus()
- SNVS_ClearButtonIRQ()
- SNVS_GetState()
- SNVS_ReadGP()
- SNVS_WriteGP() - idx = 2 or 3 only.

The SCFW SECO and Timer Service APIs make available some aspects of the SNVS to clients. This includes sc_↩ seco_tamper() to configure tamper.

The sc_seco_tamper() function is implemented using SECO_ManageSNVS(). It limits the register ID range to 0x40-0x4C, 0xA0-0xEC, and 0xF8. It also only allows access to the caller that owns SC_R_TAMPER. By default this is the booting core. board_config_sc() can be used to keep with the SCFW if that will manage tamper.

The SNVS API structure is show in the diagram below:

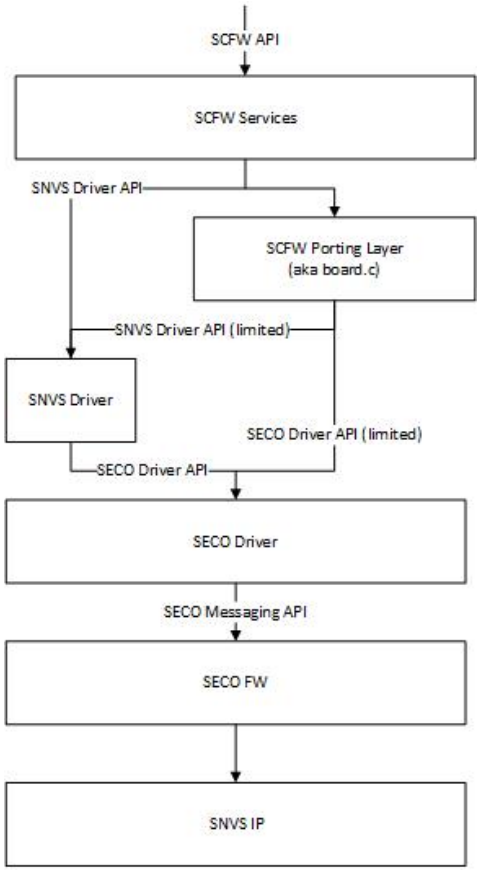

Figure 3.3 SNVS Access APIs

3.10 Power Management IC

Note that the porting layer (board.c) abstracts all access to the PMIC. There is no access to the PMIC that does not go through this file. This allows board ports to adapt to any PMIC, even a discrete PMIC (or no PMIC). Supply voltages for SoC boot must be on by default out of reset. The SCFW contains MCU SDK drivers for LPI2C, LPUART, etc. and these can be used to communicate to a custom PMIC.

The i.MX8 SoC also has some HW control signals that must be supported on the board. The PMIC-specific I/O includes:

- SCU_PMIC_ON_REQ - Driven by SNVS-LP to request system power on/off
- SCU_PMIC_STANDBY - Driven the by SCU LPC as the last stage of KS1 entry and the first stage of KS1 exit
- SCU_WDOG_OUT - Driven by the SCU to reflect warm reset events. External power supply logic should return cold boot condition.
- PMIC_INT_B - Driven by PMIC for events corresponding to power/temperature triggers

3.11 Testing

When bringing up a new board, SCFW tests should be run before attempting to boot Linux. The tests are primarily used internally to NXP and not documented in detail beyond this section. In general, any hangs when running the tests indicate lack of power from the PMIC, incorrect board configuration, or improper DDR configuration. Tests are compiled in using the T=<test> option.

Test	Description
a5x	Tests Cortex-A subsystem(s) power up and access
all	Runs all automatic test
audio	Tests audio subsystem power up and access
cci	Tests CCI subsystem power up and access
conn	Tests connectivity subsystem power up and access
db	Tests DB subsystem power up and access
dblogic	Tests DBLOGIC subsystem power up and access
dc	Tests display subsystem(s) power up and access
ddr	Basic DDR test
dma	Tests DMA subsystem power up and access
drc	Tests that the DRC(s) can be powered, configured, and DDR accessed
dsc	Test that all subsystems can be powered and each DSC accessed
gpu	Tests GPU subsystem(s) power up and access
hsio	Tests HSIO subsystem power up and access
img	Tests imaging subsystem power up and access
lsio	Tests LSIO subsystem power up and access
m4	Tests M4 subsystem(s) power up and access
pm	Tests power management service
pmic	Tests PMIC temp sensor(s)
rm	Tests resource management service
temp	Tests all SoC temp sensors
timer	Tests timer service
vpu	Tests VPU subsystem power up and access

The first test that should be run on a new board is the dsc test. This will determine if all resources (not removed via board_rsrc_avail()) can be powered and accessed. The drc, and ddr tests should then be run to insure the DDR passes basic test. In the end, all tests should be run without hangs. Then the DDR stress test application should be run. Then OS booting can be tested.

All tests can be run as a single test if the T=all option is used. In this case, the tests are stored in an overlay image called scfw_tests.bin. This needs to be loaded into OCRAM (0x100000). This can be done using the flash_scfw_test target for mkimage.

3.12 Board IOCTL

The sc_misc_board_ioctl() function is passed almost directly to the board_ioctl() function. This can be used to implement customer-specific functionality. Three parameters are passed and returned by pointer and an error code is returned.

This call has no resource associated and therefore no security. The MU the API call came from is passed in and the partition number that owns that MU is also passed in. These can be used to implement some kind of security.

The board_tick() function can be used to do periodic things like implement a HW monitor or custom watchdog, etc. There are two user defined IRQs (SC_IRQ_USR1/2) back to the SCFW API clients that can be triggered using ss_irq_trigger().

3.13 Debug

3.13.1 Logging

The SCFW can log to a UART. The board.c file determines which UART will be used. Ideally, this should be the SCU UART as use of any other UART will impact power as additional subsystems have to be powered up for the SCU to access other UARTs. Default baud rate is 115,200bps.

By default, the SCFW has debug enabled (D=1), with a debug level of 2 (DL=2). The default debug categories can be found in the debug.h file. The object files in the porting package are compiled with the default debug.h settings but with DL=0. The compile of the board port files can be controlled by modifying debug.h or overriding the debug level (DL option). This will only affect compilation so only the files being compiled (usually board.c) and not the files delivered as object files.

Debugging board port files should be done using the BOARD category which is enabled by default. Use the board_print() macro. The format of this macro is the same as standard printf() but with a debug level parameter as the first argument. Output will occur if the dl argument is less than or equal to the debug level. The debug level can be set at compile via the debug.h or the DL=<debug level>="">> make option.

board_print(dl, format string, optional args ...);

Output will occur if dl <= DEBUG_LEVEL.

Production SCFW should always be compiled with DL=0 to avoid extending boot time.

3.13.2 Debug Monitor

A debug monitor can be compiled into the SCFW using the M=1 make option. This can be used to R/W memory or registers, R/W power state, and dump some resource manager state. See Debug Monitor for more info.

Production SCFW should never have the monitor enabled (M=0, the default)!

3.13.3 JTAG

A JTAG debugger can also be used to debug the SCFW. Source-level debug is only available for the board port source files. Symbols are available in the object files as they are compiled with the -g -Os options. Note symbols should be stripped from final object files for production SCFW.

3.13.4 SC WDOG

The system controller includes watchdog hardware (WDOG) to protect the system by inducing a warm reset if the SCFW is unable to periodically service the WDOG timer. By default this is enabled by the SCFW at boot with a timeout of one second. Note this is not related at all to the SW watchdogs provided as an SCFW service to SCFW clients.

The system controller can reflect warm reset events including WDOG timeout events externally using the SCU_WDOG_OUT signal. Refer to the Reset - Board Design section for more information regarding interaction of SCU_WDOG_OUT and the external PMIC.

During development, it may be advantageous to inhibit the generation of internal/external SC WDOG events. Modifications to the board_init function allow users to control the SC WDOG configuration. It is recommended to add this SC WDOG configuration to the BOOT_PHASE_HW_INIT phase of board_init to make the settings active early during the boot of SCFW.

NOTE: Disabling the SC WDOG or inhibiting the assertion of SC_WDOG_OUT effectively removes the protection against harm to the system that can be caused as a result of SCFW hangs. Please use with caution and only during development.

Code added to board_init BOOT_PHASE_HW_INIT	Description
/∗ Disable System Controller WDOG ∗/ WDOG32_Unlock(WDOG_SC); WDOG32_SetTimeoutValue(WDOG_SC, 0xFFFF); WDOG32_Disable(WDOG_SC);	This sequence disables the SC WDOG. SCFW hangs **will not** result in a warm reset. SCFW hangs **will not** be reflected via SCU_WDOG_OUT. This configuration is useful if you want to attach a hardware debugger after the hang has occurred and inspect the SCU state.
For die targets with a dedicated SCU_WDOG_OUT pad: /∗ Disable SCU_WDOG_OUT by switching pad to unused mux mode ∗/ PAD_SetMux(IOMUXD__SCU_WDOG_OUT, 4U, SC↩ _PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF); **For die targets with SCU_WDOG_OUT multiplexed on JTAG_TRST_B:** /∗ Disable SCU_WDOG_OUT by switching pad to unused mux mode ∗/ PAD_SetMux(IOMUXD__JTAG_TRST_B, 4U, SC_P↩ AD_CONFIG_NORMAL, SC_PAD_ISO_OFF);	This sequence keeps the SC WDOG enabled but inhibits the assertion of SCU_WDOG_OUT. SCFW hangs **will** result in a warm reset. SCFW hangs **will not** be reflected via SCU_WDOG_OUT. Note that this configuration may not be needed if the PMIC is configured to keep the SC supplies powered after the assertion of SCU_WDOG_OUT. Refer to the Reset - Board Design section for more information. This configuration is useful if you want to see the SC core registers captured after hang has occurred, including the PC. This information will be reported by the SCFW after a warm reset sequence that follows a WDOG timeout. An example of this report is shown below: Reset reason = WDOG Previous SCFW boot incurred WDOG reset Exception stack frame: R0 = 0x20010F64 R1 = 0x00000000 R2 = 0x00000000 R3 = 0x200169D0 R12 = 0x00000001 LR = 0x1FFF98A7 PC = 0x1FFF98A6 PSR = 0x21000000

Chapter 4

Reference Boards

The SCFW has to be ported to the target board. This is because the SCFW has to be able to control board-level functions like PMIC, resets, DDR, and error handling. NXP provides reference ports to enable SCFW testing and to provide an initial starting point for customer ports.

NXP delivers two kinds of reference board ports:

- **VAL** - internal validation boards; modular with pluggable PMIC and base boards
- **MEK** - reference boards available to customers; pluggable base board

4.1 Image Compile

When compiling the SCFW, several options select which board and board configuration to use.

The build target and the B= option selects the board port. The arguments are used to generate the directory that will be used in the build. The directory is mx8[target]_[B]. When porting the SCFW to a new board, start by copying a reference port to a new directory and use the B= option to select during the build.

The DDR_CON= option is used to generate the file name for the DDR configure data (DCD) file. The name is dcd/[DDR_CON].cfg. This file should be generated using the RPA tool.

4.2 Board Initialization

Board initialization takes place in board_init(). Board initialization is divided into phases. There are seven phases to board initialization. The first phase is system init (*phase* = BOOT_PHASE_SYS_INIT). This happens before any HW access is possible. The second phase is the API phase (*phase* = BOOT_PHASE_API_INIT) and initializes all of the board interface data structures. The third phase (*phase* = BOOT_PHASE_HW_INIT) is the HW phase and this initializes the board hardware. The fourth phase (*phase* = BOOT_PHASE_EARLY_INIT) is just before starting early CPU. The fifth phase (*phase* = BOOT_PHASE_LATE_INIT) is just before starting the remaining CPUs. The sixth phase (*phase* = BOOT_PHASE_FINAL_INIT) is the final boot phase and is used to wrap up any needed init. A test phase (*phase* = BOOT_PHASE_TEST_INIT) is called only when an SCFW image is built with unit tests and is called just before any tests are run. They are shown in the boot flow diagrams.

Typical initialization in each phase for NXP ports:

- **BOOT_PHASE_API_INIT** - init any global variables in board.c.

- **BOOT_PHASE_HW_INIT** - configure GPIO and/or pads required to drive board-level resets from the SCU RG↩ PIO.
- **BOOT_PHASE_EARLY_INIT** - configure GPIO and/or pads required to drive board-level resets from the LSIO GPIO. This is because bus interconnects need to be powered.
- **BOOT_PHASE_FINAL_INIT**- force PMIC init, configure the ON/OFF button
- **BOOT_PHASE_TEST_INIT** - configure resources needed for unit tests to run

4.3 Debug Output

The SCFW can log data to a debug UART. It also has a debug monitor that can be exposed via the debug UART. The debug interface can also be exposed via the JTAG interface. To facilitate this, NXP reference ports make use of a build option (U=n) specified on the make line to select the debug interface. Customer boards don't need to UART selection as an option but it is highly recommended they make available the SCU UART for use during SCFW and OS porting debug.

The UART parameter is an integer. Its value is board dependent as the value is used in board.c.

For NXP MEK boards:

U	UART Config
0	No debug UART (default)
1	M4 UART
2	SCU UART
3	JTAG terminal

SCU UART is only available on later MEK board versions. SCU UART switch on the board must be ON. Turning on disconnects a couple of signals to the baseboard.

On the DXL MEK, option 1 is not used. Option 2 does not involve a switch on the board. It does however remove the M4 UART option for M4 code.

For NXP VAL boards:

U	UART Config
0	SCU UART (default)
1	JTAG terminal

This implementation affects the following board.c defines:

- **DEBUG_TERM_EMUL** - use JTAG
- **ALT_DEBUG_UART** - use the M4 UART (MEK only)
- **ALT_DEBUG_SCU_UART** - use the SCU UART (MEK only)

These defines in turn affect the following functions:

- board_get_debug_uart() - returns the debug UART instance
- board_config_debug_uart() - powers up the UART, configures the UART, indicates UART is ready
- board_disable_debug_uart() - powers off UART, indicate not ready
- board_config_sc() - keep the UART resource and pads

Note the debug UART board rate defaults to 115200 for the real board and 4000000 for emulation.

4.4 System Configuration

Much of a board port is configuration of the SCFW and hardware. This includes configuration of board parameters, pads used by the SCFW, resource partitioning, and resource availability.

4.4.1 Board Parameters

The board_parameter() function returns various parameters that affect the SCFW behavior. NXP ports return values for the following:

- **BOARD_PARM_PCIE_PLL** - configure the PCIe PLL location
- **BOARD_PARM_KS1_RESUME_USEC** - DDR config value (see DDR section below)
- **BOARD_PARM_KS1_RETENTION** - DDR config value (see DDR section below)
- **BOARD_PARM_KS1_ONOFF_WAKE** - DDR config value (see DDR section below)
- **BOARD_PARM_DC0_PLL0_SSC** - DC0 PLL0 spread spectrum config
- **BOARD_PARM_DC0_PLL1_SSC** - DC0 PLL1 spread spectrum config
- **BOARD_PARM_DC1_PLL0_SSC** - DC1 PLL0 spread spectrum config
- **BOARD_PARM_DC1_PLL1_SSC** - DC1 PLL1 spread spectrum config

A complete list of the possible parameters is listed in the docs for board_parm_t in board.h.

Spread spectrum parameters can return BOARD_PARM_RTN_NOT_USED to disable spread spectrum or BOARD_PARM_SSC_N_nnn to specify the spread percentage.

4.4.2 Pad Configuration

The board port is responsible for configuring pads used by the board port itself. This includes pads for any PMIC I2C, GPIO control, pads for the debug UART, etc.

- board_init() - configure pads required for GPIO driven board resets
- board_config_debug_uart() - configure pads for the debug UART

In NXP ports, pads for I2C to the PMIC are configured when the PMIC is initialized. This is done as late as possible (as a result of a need to communicate to the PMIC).

4.4.3 Resource Availability

The board_rsrc_avail() function is used to tell the SCFW that a resource normally available on the SoC die is not. This causes the SCFW to not access the peripheral and also result in the SCFW reporting to API clients that the resource is not available. Note a resource may be unavailable because it isn't connected on the board or because it isn't connected inside of the SoC package (the SCFW is unaware of the package). The SCFW automatically handles resources disabled via fuse.

For most NXP ports, the only resource reported as unavailable is the second DDR controller if the DDR configuration from the RPA tool indicates the second controller isn't used.

4.4.4 Resource Configuration

Resource configuration consists of allocating resources to various partitions. At boot, there are typically three partitions by default: SCU, SECO, and boot.

4.4.5 SCU Resources

The SCFW keeps resources it needs to operate. In board_config_sc(), additional resources that the SCFW needs to keep as a result of their use in board.c, need to be assigned to the SCU partition. This is typically UART, GPIO, and PMIC I2C. Both the IP and the pads used by the IP need to be assigned to the SCU partition. NXP ports do this based on the board design and the debug UART configuration.

4.4.6 Boot Resource Partitioning

By default, there is only one boot partition. It contains all the resources not used by the SCU or SECO. This includes all the CPUs. These can be started but will have no protection from each other. This configuration isn't practical for production devices and normally needs to be modified to partition the resources before starting the CPUs. If only one CPU is started by the ROM, then this partitioning can be done later in the boot by the started CPU. If multiple CPUs are started by the ROM, then this needs to be done in the SCFW first in board_system_config().

For NXP implementations, there is a need for two configurations decided at run-time. One where all the resources remain in the boot partition (used for individual OS testing) and one where the resources are partitioned like a production system (used for multi-OS testing). To facilitate doing this without rebuilding the SCFW, the SC_BD_FLAGS_ALT_CONFIG flag in the boot container is used.

In all cases, the memory size is adjusted by using rm_memreg_frag() and rm_memreg_free() to carve out the unused memory and remove it from the memory region list. This is the only task done in board_system_config() when the SC_BD_FLAGS_ALT_CONFIG flag is not set.

When the SC_BD_FLAGS_ALT_CONFIG is set, partitions are created for each M4 and for unused resources. The specific mix of peripherals, memory, and pads is a function of the test environment needs for NXP multi-OS testing. An M4 partition typically includes the M4 CPU, the other resources in the M4 subsystem, the M4 TCM, a chunk of DDR, a region of FlexSPI, and some MUs for communication.

4.4.7 Early CPUs

The NXP board ports return the M4 CPUs as early CPUs from board_early_cpu(). This means if the container is built with the SC_BD_FLAGS_EARLY_CPU_START flag set then the M4 CPUs will be started before the AP CPUs. The M4 CPUs must indicate they are done booting by calling sc_misc_boot_done() before the SCU watchdog expires.

4.5 DDR Configuration

When the system boots, it can initialize DDR in one of two ways. The ROM can do this by calling into the SCFW. If it doesn't, then the SCFW will do this.

4.5.1 DDR Init by ROM

When the boot container is created using mkimage, if "-dcd skip" is not specified, then the ROM will initialize DDR. This is required if the ROM needs to load any images into DDR. It does this by calling main_dcd() once the SCFW is loaded into TCM. This function has a known entry point the ROM can find. This function calls board_ddr_config() with SC_TRUE, BOARD_DDR_COLD_INIT. Note this is called before the SCFW is initialized so this function cannot safely call other SCFW functions outside of board.c or access global variables.

4.5.2 DDR Init by SCFW

SCFW will always call to initialize DDR. It does this two times, once before the early CPU start phase and once before the late CPU start phase. This is done by calling board_init_ddr() with early and ddr_initialized parameters. The early parameter will be SC_TRUE when called during the early phase. The ddr_initialized parameter will be SC_TRUE if the DDR was configured by the ROM.

The board_init_ddr() function usually does the following:

1. allocate global storage needed for DDR maintenance routines like retention or DQS2DQ training
2. return if the phase (early parameter) is not when it is desired to initialize DDR
3. if ROM did not init (ddr_initialized parameter), then init DDR by calling board_ddr_config() with SC_FALSE, BO↩ ARD_DDR_COLD_INIT
4. call ddrc_lpddr4_derate_init() to configure derate training
5. call soc_ddr_config_retention() to configure retention
6. call soc_ddr_dqs2dq_config() to configure DQS2DQ training
7. optionally call soc_ddr_dqs2dq_init() to configure manual periodic DQS2DQ training
8. call board_ddr_derate_periodic_enable() to enable derate training

Most of the above is enabled or disabled using defines declared in the DCD file.

4.5.3 DDR Configuration

The main function used to configure DDR is board_ddr_config(). This is called by ROM and the SCFW for various configuration actions. It has two parameters: rom_caller and action. The rom_caller parameter will be SC_TRUE when called by the ROM and SC_FALSE when called from board_init_ddr(). The action parameter will be one of the following (see board_ddr_action_t):

- **BOARD_DDR_COLD_INIT** - init DDR from POR (code from DCD)
- **BOARD_DDR_PERIODIC** - run periodic training by calling:
  - soc_ddr_dqs2dq_periodic()

- **BOARD_DDR_SR_DRC_ON_ENTER** - enter self-refresh (leave DRC on) by calling:
  - board_ddr_derate_periodic_enable() with SC_FALSE
  - board_ddr_periodic_enable() with SC_FALSE
  - soc_self_refresh_power_down_clk_disable_entry()
- **BOARD_DDR_SR_DRC_ON_EXIT** - exit self-refresh (DRC was on) by calling:
  - soc_refresh_power_down_clk_disable_exit()
  - ddrc_lpddr4_derate_init()
  - board_ddr_derate_periodic_enable() with SC_TRUE
  - soc_ddr_dqs2dq_periodic()
  - board_ddr_periodic_enable() with SC_TRUE
- **BOARD_DDR_SR_DRC_OFF_ENTER** - enter self-refresh (turn off DRC) by calling:
  - board_ddr_derate_periodic_enable() with SC_FALSE
  - board_ddr_periodic_enable() with SC_FALSE
  - soc_ddr_enter_retention()
- **BOARD_DDR_SR_DRC_OFF_EXIT** - exit self-refresh (DRC was off) by calling:
  - soc_ddr_exit_retention()
  - ddrc_lpddr4_derate_init()
  - board_ddr_derate_periodic_enable() with SC_TRUE
  - soc_ddr_dqs2dq_init()
  - board_ddr_periodic_enable() with SC_TRUE
- **BOARD_DDR_PERIODIC_HALT** - halt periodic training by calling:
  - board_ddr_derate_periodic_enable() with SC_FALSE
  - board_ddr_periodic_enable() with SC_FALSE
- **BOARD_DDR_PERIODIC_RESTART** - restart periodic training
  - ddrc_lpddr4_derate_init();
  - board_ddr_derate_periodic_enable() with SC_TRUE
  - soc_ddr_dqs2dq_periodic()
  - board_ddr_periodic_enable() with SC_TRUE
- **BOARD_DDR_DERATE_PERIODIC** - run periodic derate
  - ddrc_lpddr4_derate_periodic()
  - board_ddr_derate_periodic_enable() with SC_FALSE

Most of the above is enabled or disabled using defines declared in the DCD file.

4.5.4 RPA Tool

The DCD configuration file is generated using the RPA tool. This is a spreadsheet that contains DDR configuration parameters and outputs data the is copied into the ∗.cfg file. The configuration file to converted by the SCFW build tools into a header file. This header is included in the board.c file twice, once at the top to declare defines and once in the board_ddr_config() function to define the DDR configuration implementation.

4.6 Power Management

The PMIC is managed by the SCFW on a private I2C bus. The recommended PMIC is the PF8100/PF8200. PMIC drivers are located under drivers/pmic. Current drivers used a common I2C layer for communication in drivers/pmic/fsl_pmic.c. The individual device drivers make use of these functions to format and send individual I2C messages.

For boards where multiple PMICs are used and are defined at runtime(**VAL**) a function table is used at board/pmic.c Depending on what PMIC is detected the PF8100 or PF100 functions will be called. For boards that only have a predefined PMIC(**MEK**) the direct driver functions should be called instead.

Board power management is split into required power rails such as {AP cores, GPU} and peripherals power rails. Required power rails are managed through board_set_power_mode() and board_set_voltage(). Peripheral power rails are managed via the board_trans_resource_power().

General power modes for the entire system are managed via board_power() and board_lpm(). board_power() is called to power off the system completely while board_lpm() is called to enter and exit low power for the system.

Supplies required for boot will change per SoC and should be checked on the datasheet.

- pmic_init() - Calling this takes place very late in the boot process because of boot time considerations. In cases where there is critical adjustments to be done before M4 or AP boot this should be moved up. In this function the PMIC detection and any configuration changes for the OTP are done.

  One example of this can be found in the QM DDR4 validation port. In this case the DDR rail voltage must be changed to support the DDR4 memory before DDR initialization can take place. For this case the ROM skips the DDR Initialization and defers it until SCFW. SCFW then changes the PMIC voltage and configures DDR before kicking off the AP core.

  In production SCFW ports pmic_init() should be deferred to as late as possible to optimize boot time.

- board_set_power_mode() - This function sets the power mode of the required rails based on the assigned regulators under pmic_get_info(). This mapping should be updated according to board design.

- board_set_voltage() - In conjunction with board_set_power_mode() sets the voltage for required rails. This function also gets the mappings from pmic_get_info(). Depending on the mapped regulators the valid voltages could change thus the return must be checked.

- board_trans_resource_power() - This function implements any power changes for the 8 board resources. If the resource has a different voltage in LP or STBY modes this should be implemented here as well.

- board_lpm() - Function to make any voltage or power state changes for transitioning to low power modes.

- board_power() - Function called to turn system off completely.

- PMIC_IRQHandler() - Should be implemented to handle any enabled interrupts of the PMIC. In the provided NXP ports this function only handles the temperature interrupts from the PMIC. This can be extended to handle any interrupts such as OV/UV detection or PMIC WDOG.

4.6.1 PMIC Temperature Sensors

The PMIC temp sensors are controlled via the board_set_control() and board_get_control() functions. The SC_C_TEMP control allows reading of the temp and SC_C_TEMP_HI allows for R/W of the alarm value (by default set to max). The SC_C_TEMP_LOW control is not supported. The NXP PMICs cannot return the actual temperature. They only indicate if the temperature is above various fixed temp points with pretty large gaps between them. The PMIC interrupt handler PMIC_IRQHandler() notifies SCFW clients of an alarm event.

4.7 Reset and Fault Handling

The NXP implementations of board.c handle reset and faults as follows:

- board_reset() - all type/reasons initiate a system reset via NVIC_SystemReset()
- board_cpu_reset() - M4 lockups/memory errors result in calling board_fault(), all others result wdog action for the partition owning the CPU
- board_reboot_part() - no action override
- board_reboot_part_cont() - no action override
- board_reboot_timeout() - force board reboot on partition reboot timeout
- board_panic() - generate board reset by calling board_reset()
- board_fault() - for debug images disable watchdog and halt, for non-debug images call board_reset()
- board_security_violation() - no action

Note many of these actions may not be appropriate for a production image.

4.8 Button Handling

The button is configured in the BOOT_PHASE_FINAL_INIT phase of board_init(). It is configured for a rising edge interrupt. Debounce and power off times are left as default. The interrupt handler SNVS_Button_IRQHandler() just clears the interrupt and notifies SCFW clients.

Chapter 5

Usage

5.1 SCFW API

Calling the functions in the SCFW requires a client API which utilizes an RPC/IPC layer to communicate to the SC↩ FW binary running on the SCU. Application environments (Linux, QNX, FreeRTOS, KSDK) delivered for i.MX8 already include ports of the client API. Other 3rd parties will need to first port the API to their environment before the API can be used. The porting kit release includes archives of the client API for existing SW. These can be used as reference for porting the client API. All that needs to be implemented is the IPC layer which will utilize messaging units (MU) to communicate with the SCFW.

The SCFW API is documented in the individual API sections. There are examples in the Details section for each service.

- Resource Management
- Power Management
- Pad Configuration
- Timers
- Interrupts
- Miscellaneous

5.2 Loading

The SCFW is loaded by including the binary (scfw_tcm.bin) in the boot container.

5.3 Boot Flags

The image container holding the SCFW should also have the boot flags configured. This is a set of flags (32-bits) specified with the -flags option to mkimage.

These are defined as:

Flag	Bit	Meaning
SC_BD_FLAGS_NOT_SECURE	16	Initial boot partition is not secure
SC_BD_FLAGS_NOT_ISOLATED	17	Initial boot partition is not isolated
SC_BD_FLAGS_RESTRICTED	18	Initial boot partition is restricted
SC_BD_FLAGS_GRANT	19	Initial boot partition grants access to the SCFW
SC_BD_FLAGS_NOT_COHERENT	20	Initial boot partition is not coherent
SC_BD_FLAGS_ALT_CONFIG	21	Alternate SCFW config (passed to board.c)
SC_BD_FLAGS_EARLY_CPU_START	22	Start some CPUs early
SC_BD_FLAGS_DDRTEST	23	Config for DDR stress test
SC_BD_FLAGS_NO_AP	24	Don't boot AP even if requested by ROM

See the sc_rm_partition_alloc() function for more info. Note some of the flags are inverted before calling this function! This results in a default (all 0) which is appropriate for normal OS execution. That is a partition which is secure, isolated, not restricted, not grant, coherent, no early start, and no DDR test.

5.4 CPU Start Address

The execution address passed in the boot container is used by the SCFW to start the CPU. This is done by calling sc_pm_boot() or sc_pm_cpu_start(), depending on the partition info specified in the container. This address is restricted by the hardware implementation.

5.4.1 Cortex-A Start Address

These cores are restricted to the following. Note the allowed address is CPU dependent.

Address	CPU
0x00000000	Any
0x00000040	1
0x00000080	2
0x000000C0	3
0x00000100	0
0x00000140	1
0x00000180	2
0x000001C0	3
0x00010000	1
0x00020000	2
0x00030000	3
0x80000000	Any
0x80000040	1
0x80000080	2
0x800000C0	3
0x80000100	0
0x80000140	1
0x80000180	2
0x800001C0	3
0x80010000	1
0x80020000	2
0x80030000	3

Some devices alias OCRAM to ROM. On these, if an OCRAM address is specified the SCFW will modify it to a ROM address. This will allow the code to be fetched from the OCRAM. Be warned the PC will be in the ROM address space.

5.4.2 Cortex-M Start Address

The hardware has no mechanism to set the boot address. These cores will always start at the beginning of TCM. The SCFW will take any other address specified and write a jump instruction to the beginning of TCM.

5.5 Cortex-M4 DDR Aliasing

Devices without a SMMU include a basic translation block that can be leveraged to alias DDR memory onto the Cortex-M4 code bus. This aliasing allows performance improvements when Cortex-M4 code is located in DDR memory. The Cortex-M4 image can active aliasing during execution by updating the MCM Process ID register (MCM_PID). The DDR region will be aliased to the FlexSPI0 memory-mapped (XIP) space.

The following mappings are supported:

MCM_PID	DDR Region	Size	Alias
0x7E	0x88000000 - 0x8FFFFFFF	128MB	0x08000000 - 0x0FFFFFFF
0x7F	0x90000000 - 0x97FFFFFF	128MB	0x10000000 - 0x17FFFFFF
Other	N/A	N/A	No Alias

Aliasing must be activated while executing from a non-aliased region. The recommended flow to boot the Cortex-M4 into an aliased DDR region is as follows:

- Link the image for the aliased region
- Reset vector must point to unaliased DDR start address
- Specify the load address to be unaliased DDR region in the boot container
- After Cortex-M4 execution begins from unaliased DDR, jump to the aliased region

Notes:

- Enabling aliasing via the MCM_PID will result in loss of access to the corresponding FlexSPI address space.
- Use caution when using the Cortex-M4 code and system bus caches while aliasing is active to avoid coherency issues.

Chapter 6

Resource Management

SCFW is responsible for managing ownership and access permissions to system resources. The resource management functions of the SCFW are used to divide up the System on a Chip (SoC) resources and to control master transaction attributes and peripheral access permissions. The features supported by the SCFW are:

- Management of system resources such as SoC peripherals, memory regions and pads.
- Allows resources to be partitioned into different ownership groupings that are associated with different execution environments.
- Allows owners to configure access permissions to resources.
- Provides hardware enforced isolation.

See the Overview. The Resource Management (RM) API is documented here.

6.1 Partitions

One of the primary concepts of resource management in the SCFW is resource partitions (aka partitions). These are used to define a 'logical SoC' made up of resources, pads, and memory regions.

Partitions have the following characteristics. All partitions:

- can be created and destroyed, at boot and dynamically during run-time,
- have a hierarchical relationship, every partition has a parent,
- own resources (master and peripheral), pads, and memory regions,
- are restricted, by default, to only accessing the resources they own,
- can be booted, rebooted, and powered down,
- have a power state; can transition to other power states,
- have a watchdog timer, RTC alarm, and system counter alarm.

Partitions are created by calling the SCFW to allocate them. Resources, pads, memory regions, etc. are then assigned or moved to the new partition thus defining the 'logical SoC'. The SCFW uses an assignment scheme for resource management rather than an allocation scheme. This is similar to virtualization and VMs.

At boot all resources belong to one partition. The SCFW creates some partitions in the board porting layer and then others are created dynamically by the running CPUs. Partitions should be created in the SCFW for any CPU that will be started by the SCFW due to parameters passed from the ROM and defined in the boot image containers.

Partitions can be created in several ways. They can be created by default by the SCFW using parameters passed from the ROM (determined by parameters in the boot container), they can be created in the board_system_config() function of the board porting layer of the SCFW, or be created dynamically by calling sc_rm_partition_alloc().

Partitions have several attributes that are defined when they are created:

- **Secure** - by default, master would generate secure transactions and resources would require secure access. Only a secure partition can create another secure partition. Used primarily for TrustZone.
- **Isolated** - use XRDC2 to isolate. Should be true for all partitions except when a secure partition creates a non-secure partitions running on the same CPU as a secure partition. This parameter just results in the partition having the same DID as the parent.
- **Restricted** - true if the partition cannot create partitions.
- **Grant** - true if all resources in this partition should always remain accessible to the parent. Only used when creating a partition with no CPUs. Useful to just isolate the access of a bus master like a DMA channel to a subset of memory.
- **Coherent** - true if this partition will contain both AP clusters running in an SMP configuration.

The boot partition parameters come from the container. See the Boot Flags section.

In addition, partitions can be made confidential using the sc_rm_set_confidential() function. A confidential partition cannot not have any resource or memory assigned to it anymore. Useful for some security related use-cases.

The parent/child relationship directly affects partition reboot. When a partition is rebooted, its child partitions are automatically deleted and all resources returned to the parent. This allows the parent to rerun and again recreate the child partition like it did when it ran the first time. For more information on resets and partition reboot, see the Reset section of the Porting Guide.

6.2 Resources

Resources represent the IP blocks in the SoC. They can be masters (i.e. generate bus transactions), peripherals (i.e. have a programming model), or both. Resources always have an owning (only one) partition. Access control of resources consists of two primary mechanisms:

- **API Access** - the SCFW API functions use info like the calling partition and resource parameter to decide if actions can be take on a resource. The ownership of the resource and hierarchical relationship of the owning partition and the calling partition are used to decide if operations are authorized. These access rights vary by function and are described in the function documentation.

- **Hardware Protection** - the SCFW programs the underlying protection hardware (XRDC2 in the case of i.MX8) to control which masters can access which peripherals. Access permissions are maintained for each resource and can be set by the owner for each accessing partition. By default, only masters in a partition can only access peripherals in the same partition.

Resources can be assigned or moved by the owner to another partition. Master resources can have security, privilege, SMMU bypass, and streamID (SID) set. Peripheral resources can have access permissions set. The security state of masters can only be set if the partition owning the master is secure. Master resources generate a domain ID (DID) on the bus identifying what partition they belong to. All master resources in a partition generate the same ID so they all have the same access rights (CPUs and all other bus masters). For example, a DC assigned to a partition can only access memory accessible to that partition. The partition needs to either own the memory or the memory needs to have access rights granted to that partition using sc_rm_set_memreg_permissions(). If this needs to be a subset of memory then a new memory region should be created using one of the split or frag functions.

Note that not all resources have independent access controls. This is a function of the hardware design. Some peripherals share access control programming. This is often the case for display and camera interfaces. The entire interface (interface IP, PWM, I2C, LPCG, etc.) are in a single 64K page and have a single access control slot.

While Cortex-A cores part of a cluster can be assigned to different partitions, this is not guaranteed to always identify bus transactions as belonging to a core. Due to variations in microarchitecture of different Cortex-A cores, they have varying abilities to identify traffic as belonging to a specific core. This ability depends on transaction type (strongly ordered, device, exclusive, normal, etc.) as well as L1/L2 cache usage. Because cores can define these transaction properties themselves, isolation between CPUs in a cluster can never be considered secure. Because of this, i.MX8 processors do not have a product requirement to support this capability and the ability to isolate cores is not tested. CPUs in a cluster should always be in the same partition as the cluster.

6.3 Pads

Pads represent the individual pads of the SoC. They are owned by partitions. They have no direct access, so access control is similar to the SCFW API access control of resources.

6.4 Memory Regions

Memory regions represent blocks of memory with a start and end address. Once defined, they have ownership and access controls similar to resources. They support both kinds of access protections. The memory region owner can:

- assign/move to another partition
- can create a new memory region within the bounds of an existing owned region
- can split a region
- can configure access permissions

The SCFW implementation supports a maximum of 64 memory regions. Beyond this, the HW implementation further restricts the number of regions and this restriction varies depending on what HW checker is used for each memory and how many regions that specific checker supports. For example, most i.MX8 SoC have a limit of 16 regions for the DDR address range. Of these 16, one is used by the SCFW to define a I/O space pass through so the effective limit for SCFW API use is 15 unique DDR regions. Also, the SCFW will optimize usage of the HW regions. For example, if two regions are coincident, it will only use one HW region to enforce the access policy. These totals are for the entire system.

6.5 SCFW API

CPUs in partitions make SCFW API calls via a remote procedure call (RPC) mechanism. The RPC mechanism serializes the call and sends it over an inter-processor communication (IPC) mechanism implemented via message units (MU). Message units are resources and since all resources are owned by a partition, the SCFW can identify the owner and hence determine the calling partition. The calling partition is often used to determine if an operation is allowed or not.

The SCFW has the following services that operate on partitions and resources:

- **Resource Management (RM)** - used to manage partitions, resources, pads, memory regions
- **Power Management (PM)** - used to boot, reboot, and change power state of partitions and resources
- **Timer** - used to configure and use partitions-specific watchdogs and alarms
- **Interrupt (IRQ)** - used to manage interrupts sent to partitions via their MUs

The other services (pad, miscellaneous, and security) do not operate on partitions or resources. The Resource Management (RM) API is documented here.

Note there are eight MUs (five in LSIO, one in each M4, and one in the SCU itself) that are used to communicate to the SCFW). This is because one end of each of these is accessible only via a private bus used by the SCU.

- SC_R_MU_0A-4A (A side used by CPUs, B-side used by SCU)
- SC_R_M4_0_MU_1A (A side used by CPU, B-side used by SCU)
- SC_R_M4_1_MU_1A (A side used by CPU, B-side used by SCU)
- SC_R_SC_MU_1A in the SCU (both sides used by SCU for loopback testing)

The SCFW does not dictate which CPU uses each of these. Access is controlled by the standard SCFW RM partitioning. SCFW has to power at least one up for each CPU and these are specified in the boot container. The default in mkimage is the M4 MU for each M4 and MU_0A for the AP.

Beyond this, all usage is determined by the board.c port and the AP/M4 SW. Access to MUs is controlled by the SCFW RM partitioning which is configured in board.c and at run-time by the SW themselves. Typical usage is MU_0A is kept and used by the AP secure code and MU_1A is used by the AP non-secure code. Using AP clusters to run separate OSes or using a hypervisor would require additional usage of these MUs.

6.6 Hardware Resource/Memory Isolation

The i.MX8 SoC contains a mix of Cortex-A and Cortex-M CPUs which frequently operate in an asymmetric mode with different software environments executing on them (OSes, RTOSes, etc.). To keep these SW environments from unintentionally interfering with each other, i.MX8 contains HW mechanisms to enforce isolation. These mechanisms operate in a manner similar to ARM's TrustZone in that transactions from masters are annotated with user-side band information to indicate their domain and the access controls allow/disallow access to peripherals/memory based on this information.

The HW that does this is the XRDC2 (aka XRDC). The XRDC consists of a manager (per subsystem), MDAC, PAC, MSC, and MRC components. The MDAC is used to annotate the transactions and the PAC, MSC, and MRC are used to control access. See the figure below for the basic XRDC integration architecture. In i.MX8, the XRDC replaces the RDC and TrustZone components (CSU, TZASC, etc.) found in previous i.MX processors.

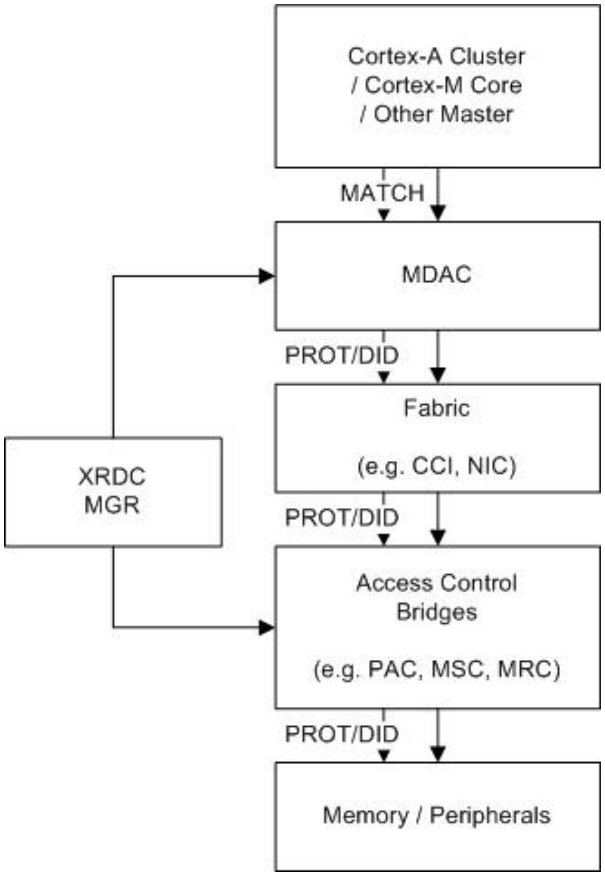

Figure 6.1 XRDC Interaction for Bus Transactions

There are five XRDC components:

- **Manager (MGR)** - provides the programming interface for the entire XRDC
- **Master Domain Assignment Controller (MDAC)** - identifies transaction sources/types and appends information such as domain ID (DID), streamID (SID), etc.
- **Peripheral Access Controller (PAC)** - accepts/rejects transactions based on transaction attributes and programmed permissions; supports up to 128 different peripherals (IPS or APB based); based on module enables and/or select signals so has no concept of addressing
- **Memory Space Controller (MSC)** - accepts/rejects transactions based on transaction attributes and programmed permissions; supports a single memory space; has no concept of addressing
- **Memory Region Controller (MRC)** - accepts/rejects transactions based on transaction attributes and programmed permissions; supports multiple memory spaces by allowing the overall space to be divided into regions (with programmable start/end addresses)

The SCFW configures the XRDC2 components based on partition, resource, and memory region configuration. For more information on the XRDC capabilities, refer to the XRDC2 section of the RM.

6.7 Example

The following shows the partition creation for an example system. Initially, the SCFW creates three partitions. The SCFW and SECO partitions are secure and isolated. The boot partition parameters depend on the boot flags from the boot image container. These would also normally be secure and isolated. The boot partition contains all the memory and almost all the resources. Only the minimal resources required for the SCFW and SECO to function are owned by those partitions.

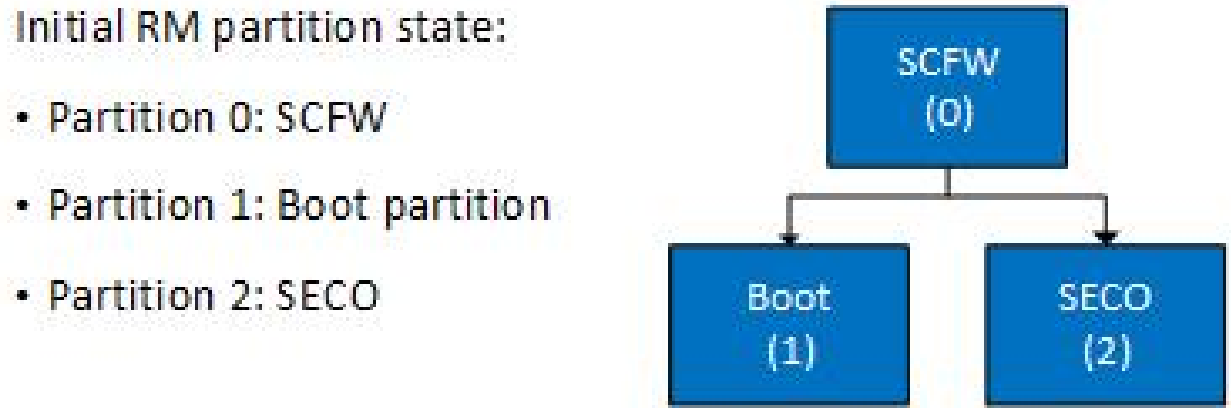

Figure 6.2 Initial Partition Configuration

Before starting the CPUs, the SCFW calls board_system_config(). This is where the partitions are created for CPUs started by the SCFW. These partitions usually have code loaded by the ROM and execution automatically started by the SCFW. Partitions can also be created for CPUs that aren't started immediately by the SCFW. Code can be loaded for these partitions by the ROM at boot by defining them as data images with mkimage. Code could also be loaded by the parent so long as it has access rights to the memory. The parent can then boot such a partition later by calling sc_pm_boot(). An M4 partition would normally be non-secure.

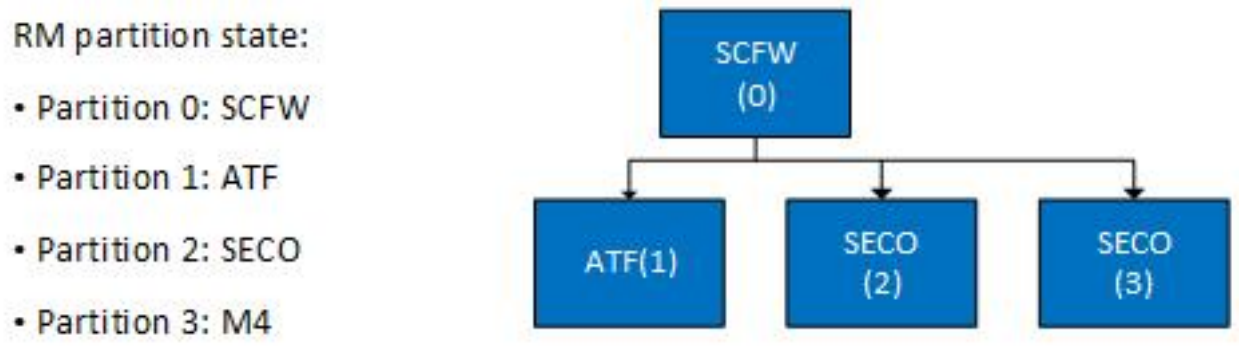

Figure 6.3 Board Partition Configuration

The boot partition can also be considered the ATF partition because that is the first thing run on the AP core. ATF creates a partition for Linux to use. This partition would typically be non-secure and not isolated. The Cortex-A CPUs, MU0A, the SC_R_SYSTEM resource, and a little bit of memory are kept by the ATF partition. All other resources are assigned to the Linux partition.

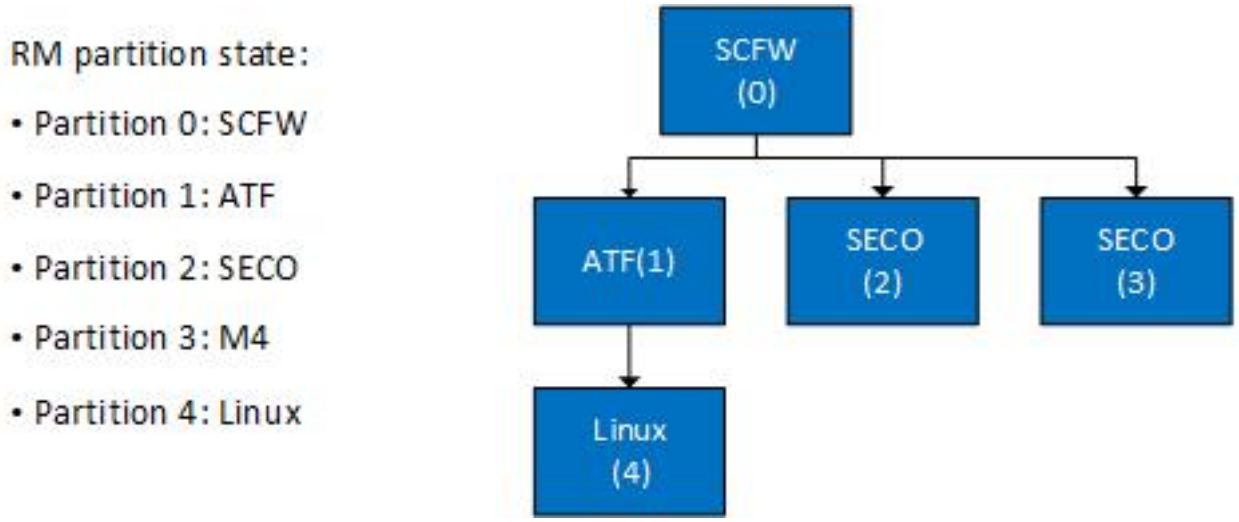

Figure 6.4 Final Partition Configuration

ATF starts Linux. Linux could dynamically create an additional partition for the other M4 to handle something like sensor fusion or a media processing engine.

Chapter 7

Power Management

SCFW is responsible for managing the power state of the SoC. This includes static and dynamic power management, clock management, and reset control. The features supported by the SCFW are:

- Changing the power state of the system, partitions, and resources.
- Configuring clocks and PLLs.
- Configuring and responding to wake-up sources.
- Reset control including booting/rebooting a partition, obtaining reset reasons, and starting/stopping of CPUs.

See the Overview. The Power Management (PM) API is documented here.

7.1 Wake from Low Power

7.1.1 Wake Event Sources

The SoC RM provides some background on the wakeup capability of the IRQSTEER and GIC modules. The wakeup outputs of the IRQSTEER and GIC are connected to IRQ lines of the SCU and fielded by SCFW to wake up the respective CPU for wake event processing. The SCFW Interrupt Service can also generate wakeup events that do not require the GIC or IRQSTEER to remain active. Each of these wake events sources are described in the sections below. Note the tradeoff between flexibility of the wakeup method and power consumption that must considered during system design.

7.1.2 GIC Wake Events

The GIC module provides a facility to transition each redistributor interface into a sleep state with wakeup capability. AP software uses the GICR_WAKER register to quiesce the respective redistributor interface. Prior to executing WFI, AP software notifies SCFW of the request to enter a deeper low-power mode using sc_pm_req_cpu_low_power_mode(). Note that the GIC must be powered and clocked to generate a wake event. The following table shows the GIC wakeup options available:

sc_pm_req_cpu_low_power_↩ mode wake_src parameter	Wakeup Description	Notes
SC_PM_SRC_GIC	GIC wakeup will cause SCFW to wake the respective CPU	GIC resource must remain powered and clocked (power mode >= LP). System power consumption will be higher to keep respective subsystem with GIC powered and clocked. K↩ S1 power mode is inhibited with this wake method.
SC_PM_WAKE_SRC_IRQSTEE↩ R_GIC	Refer to IRQSTEER wake events in the next section	

7.1.3 IRQSTEER Wake Events

One of the IRQSTEER module instances (SC_R_IRQSTR_SCU2) is reserved for AP wake events. The IRQST↩ EER does not require clocks to generate a wakeup event and therefore offers lower power consumption than GIC wakeup methods. Prior to executing WFI, AP software notifies SCFW of the request to enter a deeper low-power mode using sc_pm_req_cpu_low_power_mode(). Note that the IRQSTEER must be powered to generate a wake event. The following table shows the IRQSTEER wakeup options available:

sc_pm_req_cpu_low_power_↩ mode wake_src parameter	Wakeup Description	Notes
SC_PM_WAKE_SRC_IRQSTEE↩ R_GIC	2-stage wakeup with first stage being IRQSTEER and second stage being GIC	GIC and IRQSTEER resources must remain powered (power mode >= STBY). AP software must "replicate" the desired wake sources from the GIC to the IRQSTEER. System power consumption will be higher to keep respective subsystem with G↩ IC and IRQSTEER powered. K↩ S1 power mode is inhibited with this wake method.
SC_PM_WAKE_SRC_IRQSTEER	IRQSTEER wakeup will cause SC↩ FW to wake the "primary" CPU	IRQSTEER resource must remain powered (power mode >= STBY). System power consumption will be higher to keep respective subsystem with IRQSTEER powered. K↩ S1 power mode is inhibited with this wake method. Primary CPU designated using sc_pm_set_cpu↩ _resume.

7.1.4 SCU Wake Events

SCU wake events allow the entire system to be placed into retention/powered down. These wake sources are enabled using the SCFW IRQ service API (sc_irq_enable). Prior to executing WFI, AP software notifies SCFW of the request to enter a deeper low-power mode using sc_pm_req_cpu_low_power_mode(). The following table shows the SCU wakeup options available:

sc_pm_req_cpu_low_power_↩ mode wake_src parameter	Wakeup Description	Notes
SC_PM_WAKE_SRC_SCU	SCU wake event will wake the "primary" CPU	GIC and IRQSTEER resources can be powered down. KS1 power mode is possible with this wake method.

A summary of SCU wake events supported by SCFW:

- RTC
- ON_OFF button
- Pad event
- System Counter

7.1.5 Pad Wake Events

The pad modules provide a programmable wakeup capability. Software must enable and configure the respective pad to generate a wakeup using the SCFW IRQ Service API. The following is an example of the calls required to enable and service a pad wake events for the UART RX signal (note that SCFW API return error checking removed for simplicity).

```
/* Register for PAD wakeup */
sc_irq_enable(ipc, MU_RSRC, SC_IRQ_GROUP_WAKE, SC_IRQ_PAD, SC_TRUE);
/* Enable UART_RX pad wakeup */
sc_pad_set_wakeup(ipc, UART_RX_PAD, SC_PAD_WAKEUP_LOW_LVL);
/* Enter low-power mode and wait for wakeup... */
/* Query SCU wakeup event status */
uint32_t status;
sc_irq_status(ipc, MU_RSRC, SC_IRQ_GROUP_WAKE, &status);
/* Check for pad wakeup */
if (status & SC_IRQ_PAD)
{
    /* Check for UART_RX pad wakeup */
    /* Note:  SCFW updates pending pad wakeup config to SC_PAD_WAKEUP_OFF */
    sc_pad_wakeup_t uart_wakeup;
    sc_pad_get_wakeup(ipc, UART_RX_PAD, &uart_wakeup);
    if (uart_wakeup == SC_PAD_WAKEUP_OFF)
    {
        /* UART_RX pad generated wake event */
    }
    else
    {
        /* Else some other pad caused the wake event */
        /* Disable the UART_RX pad wakeup */
        sc_pad_set_wakeup(ipc, UART_RX_PAD, SC_PAD_WAKEUP_OFF);
    }
}
```

7.2 System Power Off

The system can be powered off by calling sc_pm_set_sys_power_mode() with mode = SC_PM_PW_MODE_OFF. This calls board_power() in board.c to allow for port specific control of the PMIC. Note only a caller with access to the SC_R_SYSTEM resource can call this function.

7.3 Reset Control

For more info on resets, see the Reset section. This includes booting and rebooting partitions, rebooting the system, starting/stopping CPUs, and watchdog usage.

Chapter 8

Reset

In a traditional application processor with a single SMP domain running a single software system, the reset types are normally limited to resetting the CPU, resetting the SoC, or resetting the entire system (i.e. board). There can be many sources of reset such as a SW request, watchdog expiration, fault, etc.

In most cases, resetting the CPU or SoC have limited value. When most software systems start they assume all the peripherals will be found to be in a reset state. For this reason, systems typically reset the entire board, or at least the entire part of a board used by a specific SoC (the SoC and all of its external peripherals, memory, etc.).

In an SoC like i.MX8, there are many CPUs and those CPUs are mostly running different software systems. These software systems are making use of different IP in the SoC. These resources are divided into "logical" systems (resource partitions) that ideally would have independent reset. In i.MX8, the definition of these resource partitions is configured at run-time. Resets in the SoC are mostly organized by power domain and so IP cannot be individually reset. As a result, if two resources are used by two different partitions and one of those partitions is rebooted, the peripheral cannot be reset. The common bus fabric, DDR controller, PMIC, padring, etc. also cannot be reset without affecting the other system. So reset of a resource partition in i.MX8 will result in a reset of the CPUs in that partitions and some of the IP. Which IP depends on how things are partitioned and how those things are organized into power domains within the SoC. The SCFW will reset everything it can without adversely affecting the other running partitions.

8.1 Board Design

For reset to work properly, the board design has to be correct. This involves the connection of the PMIC to i.MX8 and the PMIC fuse programming. The SCU_WDOG_OUT signal (aka JTAG_TRST_B) must be connected to the watchdog input of the PMIC (e.g. WDI). This is required so that the PMIC will reset the voltages back to the level and on/off state found at initial POR. The PMIC fuses must be programmed so that assertion of the watchdog signal will return the voltages to default but it must not allow the boot voltages (VDD_MAIN, SNVS, SCU_1P8) to go to 0 volts first. The POR (aka MCU_RESET) must also not get asserted. This is sometimes called a "soft" reset. Do not use the PMIC "hard" reset option. If this is not done correctly the reset reason may be lost. To try to support the reset reason better, the reason and the partition that caused the reset is also stored in the SNVS persistent storage. This requires that the SNVS supply not go to 0v when the board is reset.

It is also important to correctly make use of GPIO, I2C, SPI, etc. These must not have functionality required for multiple partitions shared on the same IP. Also, resets to external devices need to be correctly grouped to allow a rebooted partition to safely assert reset to its board-level devices.

If any GPIO (e.g. board version) is used to make dynamic decisions in board.c, the GPIO should be SCU GPIO. This allows the GPIO to be accessed early in the boot. Many functions in board.c are called very early in the boot cycle, even before infrastructure is powered up enough to access LSIO GPIO. For example board_parameter() can be called this early. board_ddr_config() may be called from the ROM.

8.2 CPU Reset

A CPU can be reset with sc_pm_cpu_reset(). Note this just resets the CPU. None of the peripherals or bus fabric used by the CPU is reset. State configured in the SCFW is not reset. Code is not reloaded. The SW running on the core has to understand and deal with this (most cannot). Note this can also leave the IPC protocol over an MU to the SCU in an confused state. For M4 cores, CPU reset can leave fabric and the cache controller in an unknown state so should not be used. There is no clean way to reset just the M4 core.

On M4 cores, calling NVIC_SystemReset() results in an interrupt to the SCU. This results in a call to board_cpu_reset(). This function should be implemented to handle the reset in the desired way. See the comments in the reference implementations of board.c.

8.3 Partition Reset

A partition reset can be initiated by sc_pm_reboot(), sc_pm_reboot_partition() or via a SW watchdog.

This kind of reset has limitations. IP on a common reset signal cannot be reset if the reset also applies to resources owned by other partitions. For example, if a CAN controller is owned by one partition and a DMA channel is owned by another partition, neither will be reset when resetting one partition because it would result in a peripheral in another partition getting inadvertently reset. For this reason, resource partitioning must be very carefully planned to allow most resources to get reset (this is not always possible). IP and settings in the always on (AON) power domain are also not reset. This includes things settings configured with sc_misc_set_control(). For all resources and settings not reset, the SW has to handle the situation where IP has not been reset, either with drivers that understand this or with early boot code that configures all peripherals back to a reset state. The second option is preferred as it will stop bus masters before continuing a boot. In addition, shared bus fabric is not reset and code is not reloaded.

It requires the following:

- creation of partitions representing various logical systems
- start of the partitions via sc_pm_boot()

8.3.1 Partition Creation

To reset only a partition, obviously that partition has to exist. By default, most of the resources are in one boot partition. Only those required for the SCFW or SECO are in other partitions. Creation of partitions is done via the SCFW Resource Management Service. This should be done by the SW that will start the partition. The SCFW RM documentation contains examples (see details) for this.

For SW systems started at boot (by the SCFW at the request of the boot ROM), partitions should be created in the SCFW board port (board.c). This is covered in detail in the Porting Guide. There is an example of this in the SCFW ports to all NXP boards.

Note that if the M4 uses DDR then that and the common bus fabric to get to DDR will not be reset.

8.3.2 Partition Boot

For a watchdog to understand how to reboot a partition, it must know which CPU to start (there can be multiple CPUs in a partition), which MU needs to be powered on for SCFW communication, and what address to start the CPU at. This info is provided in the sc_pm_boot() call.

This call can be made directly by boot SW that creates and starts a partition. It is also made when a partition is created and started by the SCFW as a result of info passed from the boot ROM. This info comes from the boot container. When creating a boot image, mkimage can take a partition argument (-p) along with the CPU and MU for an image added to a container. When this is done, sc_pm_boot() is called internally for that image. See the mkimage flash_regression_↩ linux_m4 target as an example.

Note a callout is made to board_reboot_part() in board.c to allow the SCFW board port to override the reboot, modify the parameters, log, or do a board reset. Implementations could count reboots within a period of time to determine a partition reboot is not sufficient and then do a board reset. This function could also reset IP or external HW if required. A 32-bit reboot mask is returned from this function which indicates which partitions should be given the opportunity to delay the reboot until some action is taken. This action could be to clean up some MU IPC protocol or even to power off resources in shared power domains so that when the reset is continued the peripheral reset can occur.

A callout is made to board_reboot_part_cont() when the partition's resources have been powered off but before they are powered back on and the primary CPU started. This can be used to log something, modify a boot parameter, or complete an action started in board_reboot_part().

8.3.3 mkimage

By default, the SCFW creates the following partitions:

- 0 - SCFW
- 1 - boot
- 2 - SECO

Additional partitions can be created in board.c or even at run-time.

By default, mkimage will specify AP images as partition 1 (boot) and M4 images as partition 0. This is the case even if the container only has an M4 image! A 0 partition in the container will tell the SCFW to start the core but it is not correctly associated with the boot partition. This means it cannot be rebooted via SW or wdog. This configuration should not be used.

The mkimage -p option can be used to set the partition number. All M4 images should have a -p option specified.

Additional partitions may be created by board.c. In addition, ATF will create another partition for the non-secure OS. This is usually 3 if board.c does not create any new partitions. ATF moves all resources it does not require to the OS non-secure partition.

Note a partition cannot have two primary images (images with partition != 0). This will result in the SCFW displaying a "multiple primary"" error message. A partition cannot contain a secondary image (partition == 0) and no primary image. This is result in a "missing primary" error message.

8.4 Board Reset

A board reset can be accomplished by calling sc_pm_reset(). For security, only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can call this function, otherwise SC_ERR_NOACCESS will be returned. This resets everything and results in a full reboot (code reloaded, etc.). This kind of reset can also be initiated by a watchdog.

8.5 Watchdog Reset

There are two kinds of watchdogs in the system: software (aka virtual) watchdogs and hardware watchdogs.

The SCFW implements a software watchdog for each partition. This can be used by any core including AP or M4. The action taken is set using the sc_timer_set_wdog_action().

- SC_TIMER_WDOG_ACTION_PARTITION - resets the associated partition (default)
- SC_TIMER_WDOG_ACTION_WARM - calls board_reset() with type = SC_PM_RESET_TYPE_COLD
- SC_TIMER_WDOG_ACTION_COLD - calls board_reset() with type = SC_PM_RESET_TYPE_WARM
- SC_TIMER_WDOG_ACTION_BOARD - calls board_reset() with type = SC_PM_RESET_TYPE_BOARD
- SC_TIMER_WDOG_ACTION_IRQ - sends interrupt to the partition and parent partition

For security, only the owner of SC_R_SYSTEM or a partition with access permissions to SC_R_SYSTEM can change the action via sc_timer_set_wdog_action(). See the Timer Service for more info on using the SCFW provided watchdogs.

The SC_TIMER_WDOG_ACTION_BOARD action will result in the SoC asserting the WDOG_OUT signal when it triggers. How that is treated by the PMIC is up to the PMIC fusing. The fusing for the NXP MEK is to bounce all the supplies and do a hard reset.

Virtual watchdogs are disabled by default. They can be enabled by the client or, if desired at boot, enabled in board_system_config() after creating the M4 partition. Use the version of the watchdog functions without the sc_ to call locally. The caller_pt parameter would be the partition in question for most calls. For timer_set_wdog_action(), caller_pt needs to be the partition that owns SC_R_SYSTEM. For example, to configure the M4 watchdog to be on and locked by default on the QXP MEK, add the following to board_system_config():

```
timer_set_wdog_timeout(pt_m4_0, 5000U);
timer_set_wdog_action(pt_boot, pt_m4_0, SC_TIMER_WDOG_ACTION_BOARD);
timer_start_wdog(pt_m4_0, SC_TRUE);
```

Hardware watchdogs are available on the SCU and the M4 cores. The SCU watchdog monitors the health of the SCU running SCFW and will reset the board if the SCFW fails so service the watchdog.

The M4 HW watchdog will initiate the action as specified by sc_timer_set_wdog_action() for the partition that owns the M4 core.

Many PMICs also have a watchdog. This would usually be serviced from the board timer function, board_tick(). This adds insurance the SCFW is alive and well. Then all the clients use the SCFW software watchdogs. To instead service from a client, add that ability through the board IOCTL function, board_ioctl(). Note the PMIC watchdog is mostly superfluous as the SCU HW watchdog, which is already used by the SCFW, will drive a signal out to the PMIC if it triggers resulting in a PMIC reboot. So this is effectively the same but without all the extra wasteful I2C communication. I2C communication is slow and using it frequently will adversely affect the SCFW performance, which in turn will affect the performance of all clients calling it.

8.5.1 Typical Usage

The intended watchdog architecture on i.MX8 is:

- The SCU has a hardware watchdog. The SCFW uses this to insure the availability of the SCFW.
- The SCFW provides a watchdog service to its clients via the SCFW timer API. This includes the ability to decide for each client what the watchdog action should be (reboot the system, reboot a partition, only an interrupt). Partitions with access rights to SC_R_SYSTEM can configure this action for all partitions. It also includes the ability to notify partitions when a watchdog has triggered.
- SCFW clients (such as ATF or M4 cores) use the SCFW wdog service via the SCFW API to insure their operation. ATF provides a watchdog API to its clients (OS or hypervisor).
- OSes uses the ATF or hypervisor watchdog API to insure its availability.

Note the SCU watchdog is enabled by default. To disable during debug, see the SC WDOG section.

8.6 Reset Reason

An SCFW client can call sc_pm_reset_reason() to get the reason for their last reset. It will only return the actual SoC reset reason if no other reset has occurred for the calling partition (in which case it will return the reason for the partition reset).

A reset reason is reported in the SCU and (2x) M4 ASMC. These reasons will be lost if the power to the SCU and/or M4 cores is lost as part of the reset. If the reason is known to the SCU before the reset, it will also store the reason and the partition causing the reset in the SNVS persistent storage (requires SNVS voltage not be lost). The partition causing the reset can be obtained using sc_pm_get_reset_part() function. The SCU can do this for all resets (partition and board) except for board resets triggered by the SCU HW (SCU watchdog, SCU lockup, SCU ECC error) and similar from SECO. All resets initiated by the AP or M4 result in interrupts to the SCU allowing it to record this reset info.

Another mechanism to communicate a reset reason is the messaging unit (MU). When the SCFW reboots a partition it will first set bit 18 (IR1) in the control register (CR) of the MU (SCU-side) used by that partition to communicate with the SCFW. This will generate general interrupt 1. This can be read/cleared on the client side in the status register (SR) as GIP1. This will also generate an interrupt if unmasked via GIE1 in the client-side MU CR.

Note depending on the connection of the WDOG_OUT signal and the OTP programming of the PMIC, some resets may trigger a system POR and the original reason or the SNVS stored reason may be lost. See the Board Design section.

8.7 Notification

The SCFW can generate interrupts to notify an impending partition reboot and notify the completion of the reboot. There is an IRQ group for these two conditions with one interrupt per partition. See Interrupts for more info.

- SC_IRQ_GROUP_REBOOT - IRQ to notify a reboot is about to start, occurs after the CPUs in the partition have been stopped but before anything else is reset
- SC_IRQ_GROUP_REBOOTED - IRQ to notify a reboot is done, occurs just before the primary CPU in the partition is started

The above are IRQ groups. Each bit position represents the interrupt associated with that partition number (e.g. bit 3 will be generated when partition 3 is rebooted).

If board_reboot_part() in the board.c porting code returns a mask indicating a partition can delay the reboot, then reboot IRQ must be used. The ISR should do any desired action, and indicate done by calling sc_pm_reboot_continue(). Only after all the partitions that can delay the reboot call this function will the reboot take place. This mechanism can be used to clean up an MU IPC protocol or even to power off resources in shared power domains so that when the reboot is continued the peripheral reset can occur.

A timeout for the reboot delay can be defined using the BOARD_PARM_REBOOT_TIME parameter returned by board_parameter(). If the timeout occurs, the action to be taken can be defined using board_reboot_timeout(). This incudes do nothing, force the reboot, or generate a board fault which calls board_fault() and can be implemented to reset the board.

8.8 AP Reset Scenarios

In a typical system, the M4 is in a separate partition with higher priority than the AP. There are various ways to detect and handle an AP CPU hang.

- Take no corrective action if the AP hangs. Configure the AP watchdog to just send an interrupt to the M4 so it is aware. M4 watchdog would be configured to reboot the board. See sc_timer_set_wdog_action().
- Implement a heartbeat between the M4 and AP. M4 will reboot the AP when it does not hear from the AP (immediately or schedule when most appropriate). The M4 is then aware if the AP is continuously rebooting. Can also use the heartbeat protocol to know if the AP successfully rebooted. If either of these then reboot the board by calling sc_pm_reset().
- Implement heartbeat by using the AP watchdog. Configure it to generate and interrupt to the M4 rather than a reboot. Then treat as above.
- Configure AP to reboot. M4 can use the reboot notification IRQ to determine AP is continuously rebooting and decide if/when to do a board reset.
- Implement board_reboot_part() to detect if the AP is continuously rebooting and take corrective action.

The above provide flexibility on if/when/kind of corrective action. Can be implemented across more than two partitions. Can also be implement with AP higher priority than M4.

8.9 Examples

There are several common use-cases which vary depending on which CPU boots which partition and what can reboot the partition. On SoC with multiple M4, these use- cases can be combined.

Note only the owner of SC_R_SYSTEM or a partition with access permissions to SC_R_SYSTEM can do things like power off the board, reset the board, and set the RTC. By default this is owned by the boot partition unless assigned to another partition.

8.9.1 AP Independent from M4

This is a common automotive use-case. The boot sequence is as follows:

- SCU ROM loads SECO FW and SCFW

- SCU ROM loads M4 and AP code (either could be a pre-loader/SPL)
- SCFW is run
- SCFW configures the partitions in board_system_config()
- SCFW starts the M4 followed by the AP

So long as the resources are partitioned correctly, both partitions can be rebooted without affecting the other. This can be done via watchdog expiration. It cannot be done via SCFW API call. Normally SC_R_SYSTEM would be assigned to the M4 and the AP would not have write permissions.

8.9.2 M4 Boots AP

This is a common automotive use-case (Android Auto). The boot sequence is as follows:

- SCU ROM loads SECO FW and SCFW
- SCU ROM loads M4 and AP code (either could be a pre-loader/SPL, AP image loaded as data only)
- SCFW is run
- SCFW starts the M4
- M4 code creates a new partition for the AP
- M4 boots the AP via sc_pm_boot()

In this case the M4 is the parent of the AP. If the resources are partitioned correctly, the AP can reboot without affecting the M4 and the partition of the AP remains unchanged so no action is required by the M4. This can be done via watchdog or the M4 can do by calling sc_pm_reboot_partition(). The M4 can be rebooted via watchdog but it will also cause the AP CPUs to stop and the AP partition to be freed. This allows the M4 to recreate the AP partition and restart the AP just like it did on the initial boot. Normally SC_R_SYSTEM would be assigned to the M4 and the AP would not have write permissions.

8.9.3 AP Boots M4

This is a common use-case when an M4 is used as a helper core. The boot sequence is as follows:

- SCU ROM loads SECO FW and SCFW
- SCU ROM loads AP code (could be a pre-loader/SPL)
- SCFW is run
- SCFW starts the AP
- AP code loads the M4 code
- AP code creates a new partition for the M4
- AP boots the M4 via sc_pm_boot()

In this case the AP is the parent of the M4. If the resources are partitioned correctly, the M4 can reboot without affecting the AP and the partition of the M4 remains unchanged so no action is required by the AP. This can be done via watchdog or the AP can do by calling sc_pm_reboot_partition(). The AP can be rebooted via watchdog but it will also cause the M4 CPU to stop and the M4 partition to be freed. This allows the AP to recreate the M4 partition and restart the M4 just like it did on the initial boot. Normally SC_R_SYSTEM would be assigned to the AP and the M4 would not have write permissions.

Chapter 9

Debug Monitor

If the SCFW is compiled using the M=1 option (default is M=0) then it will include a debug monitor. The debug monitor allows command-line interaction via the SCU UART. Inclusion of the debug monitor affects SCFW timing and therefore should never be deployed in a product!

Note the terminal needs to be in a mode that sends CR or LF for a new line (not CR+LF).

The following commands are supported:

Command	Description
exit	exit the debug monitor
quit	exit the debug monitor
reset [mode]	request reset with mode (default = board)
reboot partition [type]	request partition reboot with type (default = cold)
md.b address [count]	display count bytes at address
md.w address [count]	display count words at address
md[.l] address [count]	display count long-words at address
mm.b address value	modify byte at address
mm.w address value	modify word at address
mm[.l] address value	modify long-word at address
ai.r ss sel addr	read analog interface (AI) register
ai.w ss sel addr data	write analog interface (AI) register
fuse.r word	read OTP fuse word
fuse.w word value	write value to OTP fuse word
dump rm	dump all the resource manager (RM) info
dump rm part [part]	dump all partition info for part (default = all)
dump rm rsrc [part]	dump all resource info for part (default = all)
dump rm mem [part]	dump all memory info for part (default = all)
dump rm pad [part]	dump all pad info for part (default = all)
power.r [resource]	read/get power mode of resource (default = all)
power.w resource mode	write/set power mode of resource to mode (off, stby, lp, on)
info	display SCFW/SoC info like unique ID, etc.
seco lifecycle change	send SECO lifecycle update command (change) to SECO

Command	Description
seco info	display SECO info like FW version, lifecycle, etc.
seco debug	dump SECO debug log
seco events	dump SECO event log
seco commit	commit SRK and/or SECO FW version update
v2x info	display V2X info like FW version, etc.
pmic.r i2c_id reg	read pmic register i.e. pmic.r 0x8 0x1
pmic.w i2c_id reg val	write pmic register i.e pmic.w 0x8 0x60 0x0F
pmic.l i2c_id	list pmic info (rail voltages, etc) i.e. pmic.l 0x9

Resource and subsystem (ss) arguments are specified by name. All numeric arguments are decimal unless prefixed with 0x (for hex) or 0 (for octal).

Additional commands are available when the debug monitor is built from full source (available to NXP internal developers only). See the Debug Monitor section.

Chapter 10

RPC Protocol

Clients of the SCFW make function calls using a Remote Procedure Call (RPC) mechanism. This is constructed on top of an Inter-Processor Communication (IPC) layer. The RPC mechanism is independent of the IPC mechanism. All that is required is that the IPC mechanism can send and receive messages consisting of a series of 32-bit words. Message lengths can vary between different APIs but are fixed for a specific API.

The RPC protocol is documented here for reference ONLY. It is expected clients will make use of the exported API. Using the protocol directly is not supported and makes it impossible to provide customer support.

10.1 Remote Procedure Call

The RPC implementation is all generated via script. Interface Description Language (IDL) lines exist in the API header files to describe the calling conventions of each API call. This supports integer and unsigned values of 8-, 16-, 32-, and 64-bit sizes. Special provisions are also provided for boolean types and error returns. Float is not supported.

The RPC mechanism is synchronous. Almost all API calls construct a series of 32-bit words to form a request, send the request, receive a response, deconstruct the response (also a series of 32-bit words), and return to the caller. The corresponding function on the SCFW side (server side) is not called until a complete valid request is received.

Messages consist of a header followed by a variable number of parameter words. Parameter words are packed starting with the largest parameters. Parameters passed by pointer may exist in the send request and the response depending on how they are defined in the IDL (in, out, both). Empty slots are undefined and may not be 0.

The header is a single 32-bit word consisting of four bytes:

- **version** - the protocol version
- **size** - size of the message in words including the header
- **svc** - service index
- **func** - function index within the service

Note for return messages, svc=1U. Also, to minimize the number of words in the return value, func is replaced by the return value if it is an 8-bit type.

10.2 Inter-Processor Communication

The primary IPC mechanism implemented by the SCFW is via Message Unit (MU) IP (up to eight of them).

The MU has four TX and four RX registers, each capable of generating an interrupt. The SCFW IPC uses all four to create a single channel in both directions.

All message start with the first MU TX register. Words are written in order into successive registers and wrap back to the first if the message is greater than four words. Transmission blocks if the next TX register is not empty. The response is handled the same way. It always starts with the first RX register and wraps if the message is longer than four words. Transmission blocks if the next RX register is empty. On the SCFW-side, this is all interrupt driven. The message is buffered (per MU) and the API call into the SCFW only occurs when a complete valid request is received.

RPC messages can take many mS to complete. The API is fully synchronous and a timeout period should not be used as it would confuse the IPC state machine in the SCFW.

There is also an IPC mechanism implemented via UART as part of the SCFW debug monitor. This can be used to write test code that runs on a host connected via the SCU UART.

10.3 Interrupts

10.3.1 SCFW to Client Interrupts

The client-side IPC driver usually makes use of the MU TX/RX interrupts to transfer data. In addition, the SCFW makes use of the MU general-purpose interrupts to inform the client of various events that need attention. These four interrupts are defined in the rpc.h file delivered as part of the API export package:

Interrupt	MU GIRx	Use
SC_RPC_MU_GIR_SVC	0	Interrupt Service Request
SC_RPC_MU_GIR_WAKE	1	Cortex-M Wake
SC_RPC_MU_GIR_BOOT	2	Cold Boot Flag
SC_RPC_MU_GIR_DBG	3	Cortex-M Debug Wake

10.3.1.1 Interrupt Service Request

This interrupt is generated when the SCFW needs servicing. This behavior is managed using the Interrupt Service API. Interrupts are collected into groups, each containing up to 32 interrupts. The groups and interrupts are listed in the api.h file for the interrupt service.
The client should call sc_irq_enable() to enable an interrupt. When the interrupt is serviced, the client should call sc_irq_status() for each group to determine the needed actions and figure out what component (i.e. OS driver) call-backs should be called. Calling sc_irq_status() also clears the pending status of the interrupt. As a result, the SCFW Interrupt Service acts as an interrupt collector/dispatcher mechanism.

10.3.1.2 Cortex-M Wake

This MU general-purpose IRQ is used to force a wakeup event prior to stopping a Cortex-M CPU in order to maintain coherency between the AWIC and core sleep state. Cortex-M SW should always enable.

10.3.1.3 Cold Boot Flag

This interrupt is not used as an interrupt. It is used as a clearable flag that indicates the client is booting after a cold reset. Because the SoC has multiple CPUs that could be sharing memory, a cold reset of a single CPU may not be able to actually reset the memory that CPU is using. This flag informs clients they should clear any state maintained in memory.

10.3.1.4 Cortex-M Debug Wake

This MU general-purpose IRQ is used to force a wakeup event prior to attaching debug to a Cortex-M CPU. This wake event will be sent when the respective CoreSight GPR (Granular Power Requestor) is set by the debugger to notify SCFW that power/clocks should be restored to Cortex-M core debug registers. Cortex-M SW should always enable.

10.3.2 Client to SCFW Interrupts

Interrupt	MU GIRx	Use
SC_RPC_MU_GIR_RST	0	RPC/IPC Reset Request

10.3.2.1 RPC/IPC Reset Request

This MU general-purpose IRQ is used to request the SCFW to reset the RPC/IPC interface. This request can be used to recover the RPC/IPC interface if a client driver/task is terminated/restarted in the middle of RPC/IPC communication. The RPC/IPC reset sequence should be executed as follows:

1. Driver or task performing RPC/IPC communication is stopped
2. Client requests RPC reset by writing to the SC_RPC_MU_GIR_RST bit of the MU.CR register
3. Client polls MU.CR register until SC_RPC_MU_GIR_RST bit is cleared to indicate SCFW has completed the RPC/IPC reset
4. Client side of MU module should be reconfigured for RPC/IPC communication
5. RPC/IPC communication can proceed normally

10.4 Flags/Status

10.4.1 SCFW to Client Flags/Status

SCFW makes use of the MU general-purpose flags to provide the client status and information. Currently these flags are only used to convey the instance (Core ID) of Cortex-M4 subsystems.

MU Fx	Use
0-2	Conveys subsystem instance (only Cortex-M4 subsystems)

10.5 Porting

The SCFW porting kit contains ports of the SCFW client API for ATF, FreeRTOS, Linux, QNX, and u-boot. All implement the same API and protocol. The variations involve license, directory structure, file names, and include paths.

```
scfw_export_atf.tar.gz
scfw_export_freertos.tar.gz
scfw_export_linux.tar.gz
scfw_export_qnx.tar.gz
scfw_export_uboot.tar.gz
scfw_export_headers.tar.gz
```

Integrating the API involves implementing the IPC layer. This primarily involves implementing:

```
void sc_call_rpc(sc_ipc_t ipc, sc_rpc_msg_t *msg, sc_bool_t no_resp)
```

This function should send the message pointed to by msg via an MU (identified by ipc), word by word. If no_resp is SC_FALSE then it should wait on a response and return it in the same structure pointed to by msg. sc_call_rpc() must be atomic and often requires a semaphore to insure this is the case. The size of the message is in the message itself. The IPC implementation can be interrupt or poll driven, directly to the MU or via an MU driver.

The IPC layer typically implements functions like:

```
sc_err_t sc_ipc_open(sc_ipc_t *ipc, sc_ipc_id_t id)
void sc_ipc_close(sc_ipc_t ipc)
void sc_ipc_read(sc_ipc_t ipc, void *data)
void sc_ipc_write(sc_ipc_t ipc, const void *data)
```

but that is up to the implementer. All that the SCFW API requires is that sc_call_rpc() be implemented.

10.6 API Message Formats

Below is a list of all API calls and their message formats to send a request and receive a response. A select few API calls do not return a response (self reset and reboot functions).

Messages are expected to be in little-endian format. The description accounts for this in the location of the parameter but within a parameter bytes may be in a reverse order depending on how the protocol is examined.

10.6.1 sc_pm_set_sys_power_mode()

Send

w[0]	func=19U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mode

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.2 sc_pm_set_partition_power_mode()

Send

w[0]	func=1U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	mode	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.3 sc_pm_get_sys_power_mode()

Send

w[0]	func=2U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mode

10.6.4 sc_pm_partition_wake()

Send

w[0]	func=28U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.5 sc_pm_set_resource_power_mode()

Send

w[0]	func=3U	svc=2U	size=2U	ver=1U
w[1]	undefined	mode	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.6 sc_pm_set_resource_power_mode_all()

Send

w[0]	func=22U	svc=2U	size=2U	ver=1U
w[1]	mode	pt	exclude	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.7 sc_pm_get_resource_power_mode()

Send

w[0]	func=4U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mode

10.6.8 sc_pm_req_low_power_mode()

Send

w[0]	func=16U	svc=2U	size=2U	ver=1U
w[1]	undefined	mode	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.9 sc_pm_req_cpu_low_power_mode()

Send

w[0]	func=20U	svc=2U	size=2U	ver=1U
w[1]	wake_src	mode	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.10 sc_pm_set_cpu_resume_addr()

Send

w[0]	func=17U	svc=2U	size=4U	ver=1U
w[1]	address (MSW)			
w[2]	address (LSW)			
w[3]	undefined	undefined	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.11 sc_pm_set_cpu_resume()

Send

w[0]	func=21U	svc=2U	size=4U	ver=1U
w[1]	address (MSW)			
w[2]	address (LSW)			
w[3]	undefined	isPrimary	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.12 sc_pm_req_sys_if_power_mode()

Send

w[0]	func=18U	svc=2U	size=3U	ver=1U
w[1]	hpm	sys_if	resource	
w[2]	undefined	undefined	undefined	lpm

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.13 sc_pm_set_clock_rate()

Send

w[0]	func=5U	svc=2U	size=3U	ver=1U

```
| w[1] |                                  rate                                  |
-------------------------------------------------------------------------------
| w[2] |    undefined     |       clk        |              resource             |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=2U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |                                  rate                                  |
-------------------------------------------------------------------------------
```

10.6.14 sc_pm_get_clock_rate()

```
Send
-------------------------------------------------------------------------------
| w[0] |     func=6U      |      svc=2U      |     size=2U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |    undefined     |       clk        |              resource             |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=2U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |                                  rate                                  |
-------------------------------------------------------------------------------
```

10.6.15 sc_pm_clock_enable()

```
Send
-------------------------------------------------------------------------------
| w[0] |     func=7U      |      svc=2U      |     size=3U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |      enable      |       clk        |              resource             |
-------------------------------------------------------------------------------
| w[2] |    undefined     |    undefined     |    undefined     |      autog       |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------
```

10.6.16 sc_pm_set_clock_parent()

```
Send
-------------------------------------------------------------------------------
| w[0] |     func=14U     |      svc=2U      |     size=2U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |      parent      |       clk        |              resource             |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------
```

10.6.17 sc_pm_get_clock_parent()

Send

w[0]	func=15U	svc=2U	size=2U	ver=1U
w[1]	undefined	clk	resource	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	parent

10.6.18 sc_pm_reset()

Send

w[0]	func=13U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	type

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.19 sc_pm_reset_reason()

Send

w[0]	func=10U	svc=2U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	reason

10.6.20 sc_pm_get_reset_part()

Send

w[0]	func=26U	svc=2U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

10.6.21 sc_pm_boot()

Send

w[0]	func=8U	svc=2U	size=5U	ver=1U
w[1]	boot_addr (MSW)			
w[2]	boot_addr (LSW)			
w[3]	resource_mu		resource_cpu	
w[4]	undefined	pt	resource_dev	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.22 sc_pm_set_boot_parm()

Send

w[0]	func=27U	svc=2U	size=5U	ver=1U
w[1]	boot_addr (MSW)			
w[2]	boot_addr (LSW)			
w[3]	resource_mu		resource_cpu	
w[4]	undefined	undefined	resource_dev	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.23 sc_pm_reboot()

Send

w[0]	func=9U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	type

10.6.24 sc_pm_reboot_partition()

Send

w[0]	func=12U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	type	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.25 sc_pm_reboot_continue()

Send

w[0]	func=25U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.26 sc_pm_cpu_start()

Send

w[0]	func=11U	svc=2U	size=4U	ver=1U
w[1]	address (MSW)			
w[2]	address (LSW)			
w[3]	undefined	enable	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.27 sc_pm_cpu_reset()

Send

w[0]	func=23U	svc=2U	size=4U	ver=1U
w[1]	address (MSW)			
w[2]	address (LSW)			
w[3]	undefined	undefined	resource	

10.6.28 sc_pm_resource_reset()

Send

w[0]	func=29U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.29 sc_pm_is_partition_started()

Send

w[0]	func=24U	svc=2U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.30 sc_rm_partition_alloc()

Send

w[0]	func=1U	svc=3U	size=3U	ver=1U
w[1]	grant	restricted	isolated	secure
w[2]	undefined	undefined	undefined	coherent

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

10.6.31 sc_rm_set_confidential()

Send

w[0]	func=31U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	retro	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.32 sc_rm_partition_free()

Send

w[0]	func=2U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.33 sc_rm_get_did()

Send

w[0]	func=26U	svc=3U	size=1U	ver=1U

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.34 sc_rm_partition_static()

Send

w[0]	func=3U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	did	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.35 sc_rm_partition_lock()

Send

w[0]	func=4U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.36 sc_rm_get_partition()

Send

w[0]	func=5U	svc=3U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

10.6.37 sc_rm_set_parent()

Send

w[0]	func=6U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	pt_parent	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.38 sc_rm_move_all()

Send

w[0]	func=7U	svc=3U	size=2U	ver=1U
w[1]	move_pads	move_rsrc	pt_dst	pt_src

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.39 sc_rm_assign_resource()

Send

w[0]	func=8U	svc=3U	size=2U	ver=1U
w[1]	undefined	pt	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.40 sc_rm_set_resource_movable()

Send

w[0]	func=9U	svc=3U	size=3U	ver=1U
w[1]	resource_lst		resource_fst	
w[2]	undefined	undefined	undefined	movable

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.41 sc_rm_set_subsys_rsrc_movable()

Send

w[0]	func=28U	svc=3U	size=2U	ver=1U
w[1]	undefined	movable	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.42 sc_rm_set_master_attributes()

Send

w[0]	func=10U	svc=3U	size=3U	ver=1U
w[1]	pa	sa	resource	
w[2]	undefined	undefined	undefined	smmu_bypass

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.43 sc_rm_set_master_sid()

Send

w[0]	func=11U	svc=3U	size=2U	ver=1U
w[1]	sid		resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.44 sc_rm_set_peripheral_permissions()

Send

w[0]	func=12U	svc=3U	size=2U	ver=1U
w[1]	perm	pt	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.45 sc_rm_is_resource_owned()

Send

w[0]	func=13U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.46 sc_rm_get_resource_owner()

Send

w[0]	func=33U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

10.6.47 sc_rm_is_resource_master()

Send

w[0]	func=14U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.48 sc_rm_is_resource_peripheral()

Send

w[0]	func=15U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.49 sc_rm_get_resource_info()

Send

w[0]	func=16U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	resource	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	sid	

10.6.50 sc_rm_memreg_alloc()

Send

w[0]	func=17U	svc=3U	size=5U	ver=1U
w[1]	addr_start (MSW)			
w[2]	addr_start (LSW)			
w[3]	addr_end (MSW)			
w[4]	addr_end (LSW)			

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr

10.6.51 sc_rm_memreg_split()

Send

w[0]	func=29U	svc=3U	size=6U	ver=1U
w[1]	addr_start (MSW)			
w[2]	addr_start (LSW)			
w[3]	addr_end (MSW)			
w[4]	addr_end (LSW)			
w[5]	undefined	undefined	undefined	mr

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr_ret

10.6.52 sc_rm_memreg_frag()

Send

w[0]	func=32U	svc=3U	size=5U	ver=1U
w[1]	addr_start (MSW)			
w[2]	addr_start (LSW)			
w[3]	addr_end (MSW)			
w[4]	addr_end (LSW)			

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr_ret

10.6.53 sc_rm_memreg_free()

Send

w[0]	func=18U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.54 sc_rm_find_memreg()

Send

w[0]	func=30U	svc=3U	size=5U	ver=1U
w[1]	addr_start (MSW)			
w[2]	addr_start (LSW)			
w[3]	addr_end (MSW)			
w[4]	addr_end (LSW)			

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr

10.6.55 sc_rm_assign_memreg()

Send

w[0]	func=19U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	mr	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.56 sc_rm_set_memreg_permissions()

Send

w[0]	func=20U	svc=3U	size=2U	ver=1U
w[1]	undefined	perm	pt	mr

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.57 sc_rm_set_memreg_iee()

Send

w[0]	func=34U	svc=3U	size=2U	ver=1U
w[1]	undefined	rmsg	det	mr

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.58 sc_rm_is_memreg_owned()

Send

w[0]	func=21U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.59 sc_rm_get_memreg_info()

Send

w[0]	func=22U	svc=3U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mr

Receive

w[0]	err	svc=1U	size=5U	ver=1U
w[1]	addr_start (MSW)			
w[2]	addr_start (LSW)			
w[3]	addr_end (MSW)			
w[4]	addr_end (LSW)			

10.6.60 sc_rm_assign_pad()

Send

w[0]	func=23U	svc=3U	size=2U	ver=1U
w[1]	undefined	pt	pad	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.61 sc_rm_set_pad_movable()

Send

w[0]	func=24U	svc=3U	size=3U	ver=1U
w[1]	pad_lst		pad_fst	
w[2]	undefined	undefined	undefined	movable

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.62 sc_rm_is_pad_owned()

Send

w[0]	func=25U	svc=3U	size=2U	ver=1U

w[1]	undefined	undefined	pad

Receive

w[0]	result	svc=1U	size=1U	ver=1U

10.6.63 sc_rm_dump()

Send

w[0]	func=27U	svc=3U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=1U	ver=1U

10.6.64 sc_timer_set_wdog_timeout()

Send

w[0]	func=1U	svc=5U	size=2U	ver=1U
w[1]	timeout			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.65 sc_timer_set_wdog_pre_timeout()

Send

w[0]	func=12U	svc=5U	size=2U	ver=1U
w[1]	pre_timeout			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.66 sc_timer_set_wdog_window()

Send

w[0]	func=19U	svc=5U	size=2U	ver=1U
w[1]	window			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.67 sc_timer_start_wdog()

Send

w[0]	func=2U	svc=5U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	lock

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.68 sc_timer_stop_wdog()

Send

w[0]	func=3U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.69 sc_timer_ping_wdog()

Send

w[0]	func=4U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.70 sc_timer_get_wdog_status()

Send

w[0]	func=5U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=4U	ver=1U
w[1]	timeout			
w[2]	max_timeout			
w[3]	remaining_time			

10.6.71 sc_timer_pt_get_wdog_status()

Send

w[0]	func=13U	svc=5U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	pt

Receive

w[0]	err	svc=1U	size=4U	ver=1U
w[1]	timeout			
w[2]	remaining_time			
w[3]	undefined	undefined	undefined	enb

10.6.72 sc_timer_set_wdog_action()

Send

w[0]	func=10U	svc=5U	size=2U	ver=1U
w[1]	undefined	undefined	action	pt

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.73 sc_timer_set_rtc_time()

Send

w[0]	func=6U	svc=5U	size=3U	ver=1U
w[1]	day	mon	year	
w[2]	undefined	sec	min	hour

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.74 sc_timer_get_rtc_time()

Send

w[0]	func=7U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=3U	ver=1U
w[1]	day	mon	year	
w[2]	undefined	sec	min	hour

10.6.75 sc_timer_get_rtc_sec1970()

Send

w[0]	func=9U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	sec			

10.6.76 sc_timer_set_rtc_alarm()

Send

w[0]	func=8U	svc=5U	size=3U	ver=1U
w[1]	day	mon	year	
w[2]	undefined	sec	min	hour

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.77 sc_timer_set_rtc_periodic_alarm()

Send

w[0]	func=14U	svc=5U	size=2U	ver=1U
w[1]	sec			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.78 sc_timer_cancel_rtc_alarm()

Send

w[0]	func=15U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.79 sc_timer_set_rtc_calb()

Send

w[0]	func=11U	svc=5U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	count

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.80 sc_timer_set_sysctr_alarm()

Send

w[0]	func=16U	svc=5U	size=3U	ver=1U
w[1]	ticks (MSW)			
w[2]	ticks (LSW)			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.81 sc_timer_set_sysctr_periodic_alarm()

Send

w[0]	func=17U	svc=5U	size=3U	ver=1U
w[1]	ticks (MSW)			
w[2]	ticks (LSW)			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.82 sc_timer_cancel_sysctr_alarm()

Send

w[0]	func=18U	svc=5U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.83 sc_pad_set_mux()

Send

w[0]	func=1U	svc=6U	size=3U	ver=1U
w[1]	config	mux	pad	
w[2]	undefined	undefined	undefined	iso

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.84 sc_pad_get_mux()

Send

w[0]	func=6U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	iso	config	mux

10.6.85 sc_pad_set_gp()

Send

w[0]	func=2U	svc=6U	size=3U	ver=1U
w[1]	ctrl			
w[2]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.86 sc_pad_get_gp()

Send

w[0]	func=7U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	ctrl			

10.6.87 sc_pad_set_wakeup()

Send

w[0]	func=4U	svc=6U	size=2U	ver=1U
w[1]	undefined	wakeup	pad	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.88 sc_pad_get_wakeup()

Send

w[0]	func=9U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	wakeup

10.6.89 sc_pad_set_all()

Send

w[0]	func=5U	svc=6U	size=4U	ver=1U
w[1]	ctrl			
w[2]	config	mux	pad	
w[3]	undefined	undefined	wakeup	iso

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.90 sc_pad_get_all()

Send

w[0]	func=10U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=3U	ver=1U
w[1]	ctrl			
w[2]	wakeup	iso	config	mux

10.6.91 sc_pad_set()

Send

w[0]	func=15U	svc=6U	size=3U	ver=1U
w[1]	val			
w[2]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.92 sc_pad_get()

Send

w[0]	func=16U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	val			

10.6.93 sc_pad_config()

Send

w[0]	func=17U	svc=6U	size=3U	ver=1U
w[1]	val			

w[2]	undefined	undefined	pad

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.94 sc_pad_set_gp_28fdsoi()

Send

w[0]	func=11U	svc=6U	size=2U	ver=1U
w[1]	ps	dse	pad	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.95 sc_pad_get_gp_28fdsoi()

Send

w[0]	func=12U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	ps	dse

10.6.96 sc_pad_set_gp_28fdsoi_hsic()

Send

w[0]	func=3U	svc=6U	size=3U	ver=1U
w[1]	pus	dse	pad	
w[2]	undefined	pue	pke	hys

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.97 sc_pad_get_gp_28fdsoi_hsic()

Send

w[0]	func=8U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=3U	ver=1U
w[1]	pke	hys	pus	dse
w[2]	undefined	undefined	undefined	pue

10.6.98 sc_pad_set_gp_28fdsoi_comp()

Send

w[0]	func=13U	svc=6U	size=3U	ver=1U
w[1]	rasrcp	compen	pad	
w[2]	psw_ovr	nasrc_sel	fastfrz	rasrcn

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.99 sc_pad_get_gp_28fdsoi_comp()

Send

w[0]	func=14U	svc=6U	size=2U	ver=1U
w[1]	undefined	undefined	pad	

Receive

w[0]	err	svc=1U	size=3U	ver=1U
w[1]	nasrc	rasrcn	rasrcp	compen
w[2]	psw_ovr	compok	nasrc_sel	fastfrz

10.6.100 sc_misc_set_control()

Send

w[0]	func=1U	svc=7U	size=4U	ver=1U

w[1]	ctrl
w[2]	val
w[3]	undefined | undefined | resource

Receive

w[0]	err | svc=1U | size=1U | ver=1U

10.6.101 sc_misc_get_control()

Send

w[0]	func=2U | svc=7U | size=3U | ver=1U
w[1]	ctrl
w[2]	undefined | undefined | resource

Receive

w[0]	err | svc=1U | size=2U | ver=1U
w[1]	val

10.6.102 sc_misc_set_max_dma_group()

Send

w[0]	func=4U | svc=7U | size=2U | ver=1U
w[1]	undefined | undefined | max | pt

Receive

w[0]	err | svc=1U | size=1U | ver=1U

10.6.103 sc_misc_set_dma_group()

Send

w[0]	func=5U | svc=7U | size=2U | ver=1U
w[1]	undefined | group | resource

Receive

w[0]	err | svc=1U | size=1U | ver=1U

10.6.104 sc_misc_debug_out()

Send

w[0]	func=10U	svc=7U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	ch

Receive

w[0]	undefined	svc=1U	size=1U	ver=1U

10.6.105 sc_misc_waveform_capture()

Send

w[0]	func=6U	svc=7U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	enable

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.106 sc_misc_build_info()

Send

w[0]	func=15U	svc=7U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=3U	ver=1U
w[1]	build			
w[2]	commit			

10.6.107 sc_misc_api_ver()

Send

w[0]	func=35U	svc=7U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=3U	ver=1U
w[1]	cl_min		cl_maj	
w[2]	sv_min		sv_maj	

10.6.108 sc_misc_unique_id()

Send

w[0]	func=19U	svc=7U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=3U	ver=1U
w[1]	id_l			
w[2]	id_h			

10.6.109 sc_misc_set_ari()

Send

w[0]	func=3U	svc=7U	size=3U	ver=1U
w[1]	resource_mst		resource	
w[2]	undefined	enable	ari	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.110 sc_misc_boot_status()

Send

w[0]	func=7U	svc=7U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	status

10.6.111 sc_misc_boot_done()

Send

w[0]	func=14U	svc=7U	size=2U	ver=1U
w[1]	undefined	undefined	cpu	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.112 sc_misc_otp_fuse_read()

Send

w[0]	func=11U	svc=7U	size=2U	ver=1U
w[1]	word			

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	val			

10.6.113 sc_misc_otp_fuse_write()

Send

w[0]	func=17U	svc=7U	size=3U	ver=1U
w[1]	word			
w[2]	val			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.114 sc_misc_set_temp()

Send

w[0]	func=12U	svc=7U	size=3U	ver=1U
w[1]	celsius		resource	
w[2]	undefined	undefined	tenths	temp

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.115 sc_misc_get_temp()

Send

w[0]	func=13U	svc=7U	size=2U	ver=1U
w[1]	undefined	temp	resource	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	tenths	celsius	

10.6.116 sc_misc_get_boot_dev()

Send

w[0]	func=16U	svc=7U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	dev	

10.6.117 sc_misc_get_boot_type()

Send

w[0]	func=33U	svc=7U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	type

10.6.118 sc_misc_get_boot_container()

Send

w[0]	func=36U	svc=7U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	idx

10.6.119 sc_misc_get_button_status()

Send

w[0]	func=18U	svc=7U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	status

10.6.120 sc_misc_rompatch_checksum()

Send

w[0]	func=26U	svc=7U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	checksum			

10.6.121 sc_misc_board_ioctl()

Send

w[0]	func=34U	svc=7U	size=4U	ver=1U
w[1]	parm1			
w[2]	parm2			
w[3]	parm3			

Receive

w[0]	err	svc=1U	size=4U	ver=1U
w[1]	parm1			
w[2]	parm2			
w[3]	parm3			

10.6.122 sc_seco_image_load()

Send

w[0]	func=1U	svc=9U	size=7U	ver=1U
w[1]	addr_src (MSW)			
w[2]	addr_src (LSW)			
w[3]	addr_dst (MSW)			
w[4]	addr_dst (LSW)			
w[5]	len			
w[6]	undefined	undefined	undefined	fw

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.123 sc_seco_authenticate()

Send

w[0]	func=2U	svc=9U	size=4U	ver=1U
w[1]	addr (MSW)			
w[2]	addr (LSW)			
w[3]	undefined	undefined	undefined	cmd

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.124 sc_seco_enh_authenticate()

Send

w[0]	func=24U	svc=9U	size=6U	ver=1U
w[1]	addr (MSW)			
w[2]	addr (LSW)			
w[3]	mask1			
w[4]	mask2			
w[5]	undefined	undefined	undefined	cmd

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.125 sc_seco_forward_lifecycle()

Send

w[0]	func=3U	svc=9U	size=2U	ver=1U
w[1]	change			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.126 sc_seco_return_lifecycle()

Send

w[0]	func=4U	svc=9U	size=3U	ver=1U
w[1]	addr (MSW)			
w[2]	addr (LSW)			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.127 sc_seco_commit()

Send

w[0]	func=5U	svc=9U	size=2U	ver=1U
w[1]	info			

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	info			

10.6.128 sc_seco_attest_mode()

Send

w[0]	func=6U	svc=9U	size=2U	ver=1U
w[1]	mode			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.129 sc_seco_attest()

Send

w[0]	func=7U	svc=9U	size=3U	ver=1U
w[1]	nonce (MSW)			
w[2]	nonce (LSW)			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.130 sc_seco_get_attest_pkey()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=8U      |      svc=9U      |     size=3U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                                addr (MSW)                                |
------------------------------------------------------------------------------
| w[2] |                                addr (LSW)                                |
------------------------------------------------------------------------------

Receive
------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
------------------------------------------------------------------------------
```

10.6.131 sc_seco_get_attest_sign()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=9U      |      svc=9U      |     size=3U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                                addr (MSW)                                |
------------------------------------------------------------------------------
| w[2] |                                addr (LSW)                                |
------------------------------------------------------------------------------

Receive
------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
------------------------------------------------------------------------------
```

10.6.132 sc_seco_attest_verify()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=10U     |      svc=9U      |     size=3U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                                addr (MSW)                                |
------------------------------------------------------------------------------
| w[2] |                                addr (LSW)                                |
------------------------------------------------------------------------------

Receive
------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
------------------------------------------------------------------------------
```

10.6.133 sc_seco_gen_key_blob()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=11U     |      svc=9U      |     size=7U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                             load_addr (MSW)                              |
------------------------------------------------------------------------------
| w[2] |                             load_addr (LSW)                              |
------------------------------------------------------------------------------
```

```
| w[3] |                              export_addr (MSW)                              |
-------------------------------------------------------------------------------------
| w[4] |                              export_addr (LSW)                              |
-------------------------------------------------------------------------------------
| w[5] |                                    id                                       |
-------------------------------------------------------------------------------------
| w[6] |    undefined     |    undefined     |              max_size                |
-------------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------------
```

10.6.134 sc_seco_load_key()

```
Send
-------------------------------------------------------------------------------------
| w[0] |     func=12U     |      svc=9U      |     size=4U      |      ver=1U      |
-------------------------------------------------------------------------------------
| w[1] |                                addr (MSW)                                   |
-------------------------------------------------------------------------------------
| w[2] |                                addr (LSW)                                   |
-------------------------------------------------------------------------------------
| w[3] |                                   id                                        |
-------------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------------
```

10.6.135 sc_seco_get_mp_key()

```
Send
-------------------------------------------------------------------------------------
| w[0] |     func=13U     |      svc=9U      |     size=4U      |      ver=1U      |
-------------------------------------------------------------------------------------
| w[1] |                              dst_addr (MSW)                                 |
-------------------------------------------------------------------------------------
| w[2] |                              dst_addr (LSW)                                 |
-------------------------------------------------------------------------------------
| w[3] |    undefined     |    undefined     |              dst_size                |
-------------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------------
```

10.6.136 sc_seco_update_mpmr()

```
Send
-------------------------------------------------------------------------------------
| w[0] |     func=14U     |      svc=9U      |     size=4U      |      ver=1U      |
-------------------------------------------------------------------------------------
| w[1] |                                addr (MSW)                                   |
-------------------------------------------------------------------------------------
| w[2] |                                addr (LSW)                                   |
```

w[3]	undefined	undefined	lock	size

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.137 sc_seco_get_mp_sign()

Send

w[0]	func=15U	svc=9U	size=6U	ver=1U
w[1]	msg_addr (MSW)			
w[2]	msg_addr (LSW)			
w[3]	dst_addr (MSW)			
w[4]	dst_addr (LSW)			
w[5]	dst_size		msg_size	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.138 sc_seco_build_info()

Send

w[0]	func=16U	svc=9U	size=1U	ver=1U

Receive

w[0]	undefined	svc=1U	size=3U	ver=1U
w[1]	version			
w[2]	commit			

10.6.139 sc_seco_chip_info()

Send

w[0]	func=17U	svc=9U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=4U	ver=1U
w[1]	uid_l			

```
------------------------------------------------------------------------------
| w[2] |                                uid_h                                |
------------------------------------------------------------------------------
| w[3] |             monotonic             |                lc                 |
------------------------------------------------------------------------------
```

10.6.140 sc_seco_enable_debug()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=18U     |      svc=9U      |     size=3U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                               addr (MSW)                               |
------------------------------------------------------------------------------
| w[2] |                               addr (LSW)                               |
------------------------------------------------------------------------------

Receive
------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
------------------------------------------------------------------------------
```

10.6.141 sc_seco_get_event()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=19U     |      svc=9U      |     size=2U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |    undefined     |    undefined     |    undefined     |       idx        |
------------------------------------------------------------------------------

Receive
------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=2U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                                event                                 |
------------------------------------------------------------------------------
```

10.6.142 sc_seco_fuse_write()

```
Send
------------------------------------------------------------------------------
| w[0] |     func=20U     |      svc=9U      |     size=3U      |      ver=1U      |
------------------------------------------------------------------------------
| w[1] |                               addr (MSW)                               |
------------------------------------------------------------------------------
| w[2] |                               addr (LSW)                               |
------------------------------------------------------------------------------

Receive
------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
------------------------------------------------------------------------------
```

10.6.143 sc_seco_patch()

Send

w[0]	func=21U	svc=9U	size=3U	ver=1U
w[1]	addr (MSW)			
w[2]	addr (LSW)			

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.144 sc_seco_set_mono_counter_partition()

Send

w[0]	func=28U	svc=9U	size=2U	ver=1U
w[1]	undefined	undefined	she	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	undefined	undefined	she	

10.6.145 sc_seco_set_fips_mode()

Send

w[0]	func=29U	svc=9U	size=2U	ver=1U
w[1]	undefined	undefined	undefined	mode

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	reason			

10.6.146 sc_seco_start_rng()

Send

w[0]	func=22U	svc=9U	size=1U	ver=1U

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	status			

10.6.147 sc_seco_sab_msg()

```
Send
-------------------------------------------------------------------------------
| w[0] |     func=23U     |      svc=9U      |     size=3U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |                                addr (MSW)                                |
-------------------------------------------------------------------------------
| w[2] |                                addr (LSW)                                |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------
```

10.6.148 sc_seco_secvio_enable()

```
Send
-------------------------------------------------------------------------------
| w[0] |     func=25U     |      svc=9U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=1U      |      ver=1U      |
-------------------------------------------------------------------------------
```

10.6.149 sc_seco_secvio_config()

```
Send
-------------------------------------------------------------------------------
| w[0] |     func=26U     |      svc=9U      |     size=7U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |                                data0                                     |
-------------------------------------------------------------------------------
| w[2] |                                data1                                     |
-------------------------------------------------------------------------------
| w[3] |                                data2                                     |
-------------------------------------------------------------------------------
| w[4] |                                data3                                     |
-------------------------------------------------------------------------------
| w[5] |                                data4                                     |
-------------------------------------------------------------------------------
| w[6] |    undefined     |       size       |      access      |        id        |
-------------------------------------------------------------------------------

Receive
-------------------------------------------------------------------------------
| w[0] |       err        |      svc=1U      |     size=6U      |      ver=1U      |
-------------------------------------------------------------------------------
| w[1] |                                data0                                     |
-------------------------------------------------------------------------------
| w[2] |                                data1                                     |
-------------------------------------------------------------------------------
| w[3] |                                data2                                     |
-------------------------------------------------------------------------------
| w[4] |                                data3                                     |
-------------------------------------------------------------------------------
| w[5] |                                data4                                     |
-------------------------------------------------------------------------------
```

10.6.150 sc_seco_secvio_dgo_config()

Send

w[0]	func=27U	svc=9U	size=3U	ver=1U
w[1]	data			
w[2]	undefined	undefined	access	id

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	data			

10.6.151 sc_irq_enable()

Send

w[0]	func=1U	svc=8U	size=3U	ver=1U
w[1]	mask			
w[2]	enable	group	resource	

Receive

w[0]	err	svc=1U	size=1U	ver=1U

10.6.152 sc_irq_status()

Send

w[0]	func=2U	svc=8U	size=2U	ver=1U
w[1]	undefined	group	resource	

Receive

w[0]	err	svc=1U	size=2U	ver=1U
w[1]	status			

Chapter 11

Driver errors status

- kStatus_LPI2C_Busy = 900
- kStatus_LPI2C_Idle = 901
- kStatus_LPI2C_Nak = 902
- kStatus_LPI2C_FifoError = 903
- kStatus_LPI2C_BitError = 904
- kStatus_LPI2C_ArbitrationLost = 905
- kStatus_LPI2C_PinLowTimeout = 906
- kStatus_LPI2C_NoTransferInProgress = 907
- kStatus_LPI2C_DmaRequestFail = 908
- kStatus_LPI2C_Timeout = 909
- kStatus_LPUART_TxBusy = 1300
- kStatus_LPUART_RxBusy = 1301
- kStatus_LPUART_TxIdle = 1302
- kStatus_LPUART_RxIdle = 1303
- kStatus_LPUART_TxWatermarkTooLarge = 1304
- kStatus_LPUART_RxWatermarkTooLarge = 1305
- kStatus_LPUART_FlagCannotClearManually = 1306
- kStatus_LPUART_Error = 1307
- kStatus_LPUART_RxRingBufferOverrun = 1308
- kStatus_LPUART_RxHardwareOverrun = 1309
- kStatus_LPUART_NoiseError = 1310
- kStatus_LPUART_FramingError = 1311
- kStatus_LPUART_ParityError = 1312
- kStatus_LPUART_BaudrateNotSupport = 1313
- kStatus_LPUART_IdleLineDetected = 1314

Chapter 12

Deprecated List

Global FGPIO_ClearPinsOutput (FGPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by FGPIO_PortClear.

Global FGPIO_ReadPinInput (FGPIO_Type *base, uint32_t pin)

Do not use this function. It has been superceded by FGPIO_PinRead

Global FGPIO_SetPinsOutput (FGPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by FGPIO_PortSet.

Global FGPIO_TogglePinsOutput (FGPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by FGPIO_PortToggle.

Global FGPIO_WritePinOutput (FGPIO_Type *base, uint32_t pin, uint8_t output)

Do not use this function. It has been superceded by FGPIO_PinWrite.

Global GPIO_ClearPinsOutput (GPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by GPIO_PortClear.

Global GPIO_DisableInterrupts (GPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by GPIO_PortDisableInterrupts.

Global GPIO_ReadPadStatus (GPIO_Type *base, uint32_t pin)

Do not use this function. It has been superceded by GPIO_PinReadPadStatus.

Global GPIO_ReadPinInput (GPIO_Type *base, uint32_t pin)

Do not use this function. It has been superceded by GPIO_PinRead.

Global GPIO_SetPinInterruptConfig (GPIO_Type *base, uint32_t pin, gpio_interrupt_mode_t pinInterruptMode)

Do not use this function. It has been superceded by GPIO_PinSetInterruptConfig.

Global GPIO_SetPinsOutput (GPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by GPIO_PortSet.

Global GPIO_WritePinOutput (GPIO_Type *base, uint32_t pin, uint8_t output)

Do not use this function. It has been superceded by GPIO_PinWrite.

Global RGPIO_ClearPinsOutput (RGPIO_Type *base, uint32_t mask)

Do not use this function. It has been superceded by RGPIO_PortClear.

Global RGPIO_ReadPinInput (RGPIO_Type *base, uint32_t pin)

Do not use this function. It has been superceded by RGPIO_PinRead.

Global RGPIO_SetPinsOutput (RGPIO_Type ∗base, uint32_t mask)

Do not use this function. It has been superceded by RGPIO_PortSet.

Global RGPIO_TogglePinsOutput (RGPIO_Type ∗base, uint32_t mask)

Do not use this function. It has been superceded by RGPIO_PortToggle.

Global RGPIO_WritePinOutput (RGPIO_Type ∗base, uint32_t pin, uint8_t output)

Do not use this function. It has been superceded by RGPIO_PinWrite.

Chapter 13

Module Index

13.1 Modules

Here is a list of all modules:

Chapter 14

Data Structure Index

14.1 Data Structures

Here are the data structures with brief descriptions:

Chapter 15

File Index

15.1 File List

Here is a list of all documented files with brief descriptions:

Chapter 16

Module Documentation

16.1 DRC: DDR Controller Driver

Module for the DRC driver.

Files

- file fsl_drc_cbt.h
- file fsl_drc_derate.h
- file fsl_drc_rdbi_deskew.h

Functions

- void run_cbt (uint32_t phy_ptr0, uint32_t phy_ptr1, uint32_t total_num_drc)

  This function performs DDR command bus training.
- void ddrc_lpddr4_derate_init (uint32_t total_num_drc)

  This function initializes the DDR derate mechanism.
- sc_bool_t ddrc_lpddr4_derate_periodic (uint32_t total_num_drc)

  This function performs periodic DDR derate training.
- void RDBI_bit_deskew (uint32_t ddr_num)

  This function performs DDR deskew training.

16.1.1 Detailed Description

Module for the DRC driver.

It is an SDK driver for the DRC module of i.MX devices.

16.1.2 Function Documentation

16.1.2.1 run_cbt()

```
void run_cbt (
             uint32_t phy_ptr0,
             uint32_t phy_ptr1,
             uint32_t total_num_drc )
```

This function performs DDR command bus training.

Parameters

in	*phy_ptr0*	initial value of PTR0
in	*phy_ptr1*	initial value of PTR1
in	*total_num_drc*	number of DDR controllers used

16.1.2.2 ddrc_lpddr4_derate_init()

```
void ddrc_lpddr4_derate_init (
             uint32_t total_num_drc )
```

This function initializes the DDR derate mechanism.

Parameters

in	*total_num_drc*	number of DDR controllers used

Examples

board.c.

16.1.2.3 ddrc_lpddr4_derate_periodic()

```
sc_bool_t ddrc_lpddr4_derate_periodic (
             uint32_t total_num_drc )
```

This function performs periodic DDR derate training.

Parameters

in	*total_num_drc*	number of DDR controllers used

Returns

Returns SC_TRUE if timer is suppose to continue polling, otherwise SC_FALSE.

Examples

board.c.

16.1.2.4 RDBI_bit_deskew()

```
void RDBI_bit_deskew (
            uint32_t ddr_num )
```

This function performs DDR deskew training.

Parameters

in	*ddr_num*	index of DDR controller (0 or 1)

16.2 GPIO: General-Purpose Input/Output Driver

Modules

- GPIO Driver

16.2.1 Detailed Description

16.3 GPIO Driver

Files

- file fsl_gpio.h

Data Structures

- struct gpio_pin_config_t

  GPIO Init structure definition.

Enumerations

- enum gpio_pin_direction_t { kGPIO_DigitalInput = 0U, kGPIO_DigitalOutput = 1U }

  GPIO direction definition.
- enum gpio_interrupt_mode_t {
  kGPIO_NoIntmode = 0U, kGPIO_IntLowLevel = 1U, kGPIO_IntHighLevel = 2U, kGPIO_IntRisingEdge = 3U,
  kGPIO_IntFallingEdge = 4U, kGPIO_IntRisingOrFallingEdge = 5U }

  GPIO interrupt mode definition.

Driver version

- #define FSL_GPIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 3))

  GPIO driver version 2.0.3.

GPIO Initialization and Configuration functions

- void GPIO_PinInit (GPIO_Type *base, uint32_t pin, const gpio_pin_config_t *Config)

  Initializes the GPIO peripheral according to the specified parameters in the initConfig.

GPIO Reads and Write Functions

- void GPIO_PinWrite (GPIO_Type *base, uint32_t pin, uint8_t output)

  Sets the output level of the individual GPIO pin to logic 1 or 0.
- static void GPIO_WritePinOutput (GPIO_Type *base, uint32_t pin, uint8_t output)

  Sets the output level of the individual GPIO pin to logic 1 or 0.
- static void GPIO_PortSet (GPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple GPIO pins to the logic 1.
- static void GPIO_SetPinsOutput (GPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple GPIO pins to the logic 1.
- static void GPIO_PortClear (GPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple GPIO pins to the logic 0.
- static void GPIO_ClearPinsOutput (GPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple GPIO pins to the logic 0.
- static void GPIO_PortToggle (GPIO_Type *base, uint32_t mask)

  Reverses the current output logic of the multiple GPIO pins.
- static uint32_t GPIO_PinRead (GPIO_Type *base, uint32_t pin)

  Reads the current input value of the GPIO port.
- static uint32_t GPIO_ReadPinInput (GPIO_Type *base, uint32_t pin)

  Reads the current input value of the GPIO port.

GPIO Reads Pad Status Functions

- static uint8_t GPIO_PinReadPadStatus (GPIO_Type *base, uint32_t pin)

  Reads the current GPIO pin pad status.
- static uint8_t GPIO_ReadPadStatus (GPIO_Type *base, uint32_t pin)

  Reads the current GPIO pin pad status.

Interrupts and flags management functions

- void GPIO_PinSetInterruptConfig (GPIO_Type *base, uint32_t pin, gpio_interrupt_mode_t pinInterruptMode)

  Sets the current pin interrupt mode.
- static void GPIO_SetPinInterruptConfig (GPIO_Type *base, uint32_t pin, gpio_interrupt_mode_t pinInterrupt↩ Mode)

  Sets the current pin interrupt mode.
- static void GPIO_PortEnableInterrupts (GPIO_Type *base, uint32_t mask)

  Enables the specific pin interrupt.
- static void GPIO_EnableInterrupts (GPIO_Type *base, uint32_t mask)

  Enables the specific pin interrupt.
- static void GPIO_PortDisableInterrupts (GPIO_Type *base, uint32_t mask)

  Disables the specific pin interrupt.
- static void GPIO_DisableInterrupts (GPIO_Type *base, uint32_t mask)

  Disables the specific pin interrupt.
- static uint32_t GPIO_PortGetInterruptFlags (GPIO_Type *base)

  Reads individual pin interrupt status.
- static uint32_t GPIO_GetPinsInterruptFlags (GPIO_Type *base)

  Reads individual pin interrupt status.
- static void GPIO_PortClearInterruptFlags (GPIO_Type *base, uint32_t mask)

  Clears pin interrupt flag.
- static void GPIO_ClearPinsInterruptFlags (GPIO_Type *base, uint32_t mask)

  Clears pin interrupt flag.

16.3.1 Detailed Description

The MCUXpresso SDK provides a peripheral driver for the General-Purpose Input/Output (GPIO) module of MCUXpresso SDK devices.

16.3.2 Typical use case

16.3.2.1 Input Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/gpio

16.3.3 Enumeration Type Documentation

16.3.3.1 gpio_pin_direction_t

`enum gpio_pin_direction_t`

GPIO direction definition.

Enumerator

kGPIO_DigitalInput	Set current pin as digital input.
kGPIO_DigitalOutput	Set current pin as digital output.

16.3.3.2 gpio_interrupt_mode_t

```
enum gpio_interrupt_mode_t
```

GPIO interrupt mode definition.

Enumerator

kGPIO_NoIntmode	Set current pin general IO functionality.
kGPIO_IntLowLevel	Set current pin interrupt is low-level sensitive.
kGPIO_IntHighLevel	Set current pin interrupt is high-level sensitive.
kGPIO_IntRisingEdge	Set current pin interrupt is rising-edge sensitive.
kGPIO_IntFallingEdge	Set current pin interrupt is falling-edge sensitive.
kGPIO_IntRisingOrFallingEdge	Enable the edge select bit to override the ICR register's configuration.

16.3.4 Function Documentation

16.3.4.1 GPIO_PinInit()

```
void GPIO_PinInit (
            GPIO_Type * base,
            uint32_t pin,
            const gpio_pin_config_t * Config )
```

Initializes the GPIO peripheral according to the specified parameters in the initConfig.

Parameters

base	GPIO base pointer.
pin	Specifies the pin number
Config	pointer to a gpio_pin_config_t structure that contains the configuration information.

16.3.4.2 GPIO_PinWrite()

```
void GPIO_PinWrite (
            GPIO_Type * base,
```

```
            uint32_t pin,
            uint8_t output )
```

Sets the output level of the individual GPIO pin to logic 1 or 0.

Parameters

base	GPIO base pointer.
pin	GPIO port pin number.
output	GPIOpin output logic level. • 0: corresponding pin output low-logic level. • 1: corresponding pin output high-logic level.

16.3.4.3 GPIO_WritePinOutput()

```
static void GPIO_WritePinOutput (
            GPIO_Type * base,
            uint32_t pin,
            uint8_t output )  [inline], [static]
```

Sets the output level of the individual GPIO pin to logic 1 or 0.

Deprecated Do not use this function. It has been superceded by GPIO_PinWrite.

References GPIO_PinWrite().

16.3.4.4 GPIO_PortSet()

```
static void GPIO_PortSet (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple GPIO pins to the logic 1.

Parameters

base	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
mask	GPIO pin number macro

16.3.4.5 GPIO_SetPinsOutput()

```
static void GPIO_SetPinsOutput (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple GPIO pins to the logic 1.

Deprecated Do not use this function. It has been superceded by GPIO_PortSet.

References GPIO_PortSet().

16.3.4.6 GPIO_PortClear()

```
static void GPIO_PortClear (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple GPIO pins to the logic 0.

Parameters

base	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
mask	GPIO pin number macro

16.3.4.7 GPIO_ClearPinsOutput()

```
static void GPIO_ClearPinsOutput (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple GPIO pins to the logic 0.

Deprecated Do not use this function. It has been superceded by GPIO_PortClear.

References GPIO_PortClear().

16.3.4.8 GPIO_PortToggle()

```
static void GPIO_PortToggle (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Reverses the current output logic of the multiple GPIO pins.

Parameters

base	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
mask	GPIO pin number macro

16.3.4.9 GPIO_PinRead()

```
static uint32_t GPIO_PinRead (
            GPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current input value of the GPIO port.

Parameters

base	GPIO base pointer.
pin	GPIO port pin number.

Return values

GPIO	port input value.

16.3.4.10 GPIO_ReadPinInput()

```
static uint32_t GPIO_ReadPinInput (
            GPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current input value of the GPIO port.

Deprecated Do not use this function. It has been superceded by GPIO_PinRead.

References GPIO_PinRead().

16.3.4.11 GPIO_PinReadPadStatus()

```
static uint8_t GPIO_PinReadPadStatus (
            GPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current GPIO pin pad status.

Parameters

base	GPIO base pointer.
pin	GPIO port pin number.

Return values

GPIO	pin pad status value.

16.3.4.12 GPIO_ReadPadStatus()

```
static uint8_t GPIO_ReadPadStatus (
            GPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current GPIO pin pad status.

Deprecated Do not use this function. It has been superceded by GPIO_PinReadPadStatus.

References GPIO_PinReadPadStatus().

16.3.4.13 GPIO_PinSetInterruptConfig()

```
void GPIO_PinSetInterruptConfig (
            GPIO_Type * base,
            uint32_t pin,
            gpio_interrupt_mode_t pinInterruptMode )
```

Sets the current pin interrupt mode.

Parameters

base	GPIO base pointer.
pin	GPIO port pin number.
pinInterruptMode	pointer to a gpio_interrupt_mode_t structure that contains the interrupt mode information.

16.3.4.14 GPIO_SetPinInterruptConfig()

```
static void GPIO_SetPinInterruptConfig (
            GPIO_Type * base,
```

```
            uint32_t pin,
            gpio_interrupt_mode_t pinInterruptMode )  [inline], [static]
```

Sets the current pin interrupt mode.

Deprecated Do not use this function. It has been superceded by GPIO_PinSetInterruptConfig.

References GPIO_PinSetInterruptConfig().

16.3.4.15 GPIO_PortEnableInterrupts()

```
static void GPIO_PortEnableInterrupts (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Enables the specific pin interrupt.

Parameters

base	GPIO base pointer.
mask	GPIO pin number macro.

16.3.4.16 GPIO_EnableInterrupts()

```
static void GPIO_EnableInterrupts (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Enables the specific pin interrupt.

Parameters

base	GPIO base pointer.
mask	GPIO pin number macro.

References GPIO_PortEnableInterrupts().

16.3.4.17 GPIO_PortDisableInterrupts()

```
static void GPIO_PortDisableInterrupts (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Disables the specific pin interrupt.

Parameters

base	GPIO base pointer.
mask	GPIO pin number macro.

16.3.4.18 GPIO_DisableInterrupts()

```
static void GPIO_DisableInterrupts (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Disables the specific pin interrupt.

Deprecated Do not use this function. It has been superceded by GPIO_PortDisableInterrupts.

References GPIO_PortDisableInterrupts().

16.3.4.19 GPIO_PortGetInterruptFlags()

```
static uint32_t GPIO_PortGetInterruptFlags (
            GPIO_Type * base )  [inline], [static]
```

Reads individual pin interrupt status.

Parameters

base	GPIO base pointer.

Return values

current	pin interrupt status flag.

16.3.4.20 GPIO_GetPinsInterruptFlags()

```
static uint32_t GPIO_GetPinsInterruptFlags (
            GPIO_Type * base )  [inline], [static]
```

Reads individual pin interrupt status.

Parameters

base	GPIO base pointer.

Return values

current	pin interrupt status flag.

References GPIO_PortGetInterruptFlags().

16.3.4.21 GPIO_PortClearInterruptFlags()

```
static void GPIO_PortClearInterruptFlags (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Clears pin interrupt flag.

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

base	GPIO base pointer.
mask	GPIO pin number macro.

16.3.4.22 GPIO_ClearPinsInterruptFlags()

```
static void GPIO_ClearPinsInterruptFlags (
            GPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Clears pin interrupt flag.

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

base	GPIO base pointer.
mask	GPIO pin number macro.

References GPIO_PortClearInterruptFlags().

16.4 LPI2C: Low Power Inter-Integrated Circuit Driver

Modules

- LPI2C Master Driver
- LPI2C Slave Driver
- LPI2C Master DMA Driver
- LPI2C FreeRTOS Driver

Files

- file fsl_lpi2c.h

Macros

- #define I2C_RETRY_TIMES 0U /∗ Define to zero means keep waiting until the flag is assert/deassert. ∗/

  Retry times for waiting flag.

Enumerations

- enum {
  kStatus_LPI2C_Busy = MAKE_STATUS(kStatusGroup_LPI2C, 0), kStatus_LPI2C_Idle = MAKE_STATUS(k↩
  StatusGroup_LPI2C, 1), kStatus_LPI2C_Nak = MAKE_STATUS(kStatusGroup_LPI2C, 2), kStatus_LPI2C_FifoError
  = MAKE_STATUS(kStatusGroup_LPI2C, 3),
  kStatus_LPI2C_BitError = MAKE_STATUS(kStatusGroup_LPI2C, 4), kStatus_LPI2C_ArbitrationLost = MAKE↩
  _STATUS(kStatusGroup_LPI2C, 5), kStatus_LPI2C_PinLowTimeout, kStatus_LPI2C_NoTransferInProgress,
  kStatus_LPI2C_DmaRequestFail = MAKE_STATUS(kStatusGroup_LPI2C, 8), kStatus_LPI2C_Timeout = MA↩
  KE_STATUS(kStatusGroup_LPI2C, 9) }

  LPI2C status return codes.

Driver version

- #define FSL_LPI2C_DRIVER_VERSION (MAKE_VERSION(2, 1, 11))

  LPI2C driver version 2.1.11.

16.4.1 Detailed Description

16.4.2 Enumeration Type Documentation

16.4.2.1 anonymous enum

`anonymous enum`

LPI2C status return codes.

Enumerator

kStatus_LPI2C_Busy	The master is already performing a transfer.
kStatus_LPI2C_Idle	The slave driver is idle.
kStatus_LPI2C_Nak	The slave device sent a NAK in response to a byte.
kStatus_LPI2C_FifoError	FIFO under run or overrun.
kStatus_LPI2C_BitError	Transferred bit was not seen on the bus.
kStatus_LPI2C_ArbitrationLost	Arbitration lost error.
kStatus_LPI2C_PinLowTimeout	SCL or SDA were held low longer than the timeout.
kStatus_LPI2C_NoTransferInProgress	Attempt to abort a transfer when one is not in progress.
kStatus_LPI2C_DmaRequestFail	DMA request failed.
kStatus_LPI2C_Timeout	Timeout polling status flags.

16.5 LPI2C Master Driver

Data Structures

- struct lpi2c_master_config_t

  Structure with settings to initialize the LPI2C master module.
- struct lpi2c_data_match_config_t

  LPI2C master data match configuration structure.
- struct lpi2c_master_transfer_t

  Non-blocking transfer descriptor structure.
- struct lpi2c_master_handle_t

  Driver handle for master non-blocking APIs.

Typedefs

- typedef void(∗ lpi2c_master_transfer_callback_t) (LPI2C_Type ∗base, lpi2c_master_handle_t ∗handle, status_t completionStatus, void ∗userData)

  Master completion callback function pointer type.

Enumerations

- enum {
  kLPI2C_MasterTxReadyFlag = LPI2C_MSR_TDF_MASK, kLPI2C_MasterRxReadyFlag = LPI2C_MSR_RDF↩
  _MASK, kLPI2C_MasterEndOfPacketFlag = LPI2C_MSR_EPF_MASK, kLPI2C_MasterStopDetectFlag = LPI2↩
  C_MSR_SDF_MASK,
  kLPI2C_MasterNackDetectFlag = LPI2C_MSR_NDF_MASK, kLPI2C_MasterArbitrationLostFlag = LPI2C_M↩
  SR_ALF_MASK, kLPI2C_MasterFifoErrFlag = LPI2C_MSR_FEF_MASK, kLPI2C_MasterPinLowTimeoutFlag =
  LPI2C_MSR_PLTF_MASK,
  kLPI2C_MasterDataMatchFlag = LPI2C_MSR_DMF_MASK, kLPI2C_MasterBusyFlag = LPI2C_MSR_MBF_M↩
  ASK, kLPI2C_MasterBusBusyFlag = LPI2C_MSR_BBF_MASK }

  LPI2C master peripheral flags.
- enum lpi2c_direction_t { kLPI2C_Write = 0U, kLPI2C_Read = 1U }

  Direction of master and slave transfers.
- enum lpi2c_master_pin_config_t {
  kLPI2C_2PinOpenDrain = 0x0U, kLPI2C_2PinOutputOnly = 0x1U, kLPI2C_2PinPushPull = 0x2U, kLPI2C_4PinPushPull
  = 0x3U,
  kLPI2C_2PinOpenDrainWithSeparateSlave, kLPI2C_2PinOutputOnlyWithSeparateSlave, kLPI2C_2PinPushPullWithSeparateSlave
  kLPI2C_4PinPushPullWithInvertedOutput = 0x7U }

  LPI2C pin configuration.
- enum lpi2c_host_request_source_t { kLPI2C_HostRequestExternalPin = 0x0U, kLPI2C_HostRequestInputTrigger = 0x1U }

  LPI2C master host request selection.
- enum lpi2c_host_request_polarity_t { kLPI2C_HostRequestPinActiveLow = 0x0U, kLPI2C_HostRequestPinActiveHigh = 0x1U }

  LPI2C master host request pin polarity configuration.

- enum lpi2c_data_match_config_mode_t { kLPI2C_MatchDisabled = 0x0U, kLPI2C_1stWordEqualsM0OrM1 = 0x2U, kLPI2C_AnyWordEqualsM0OrM1 = 0x3U, kLPI2C_1stWordEqualsM0And2ndWordEqualsM1, kLPI2C_AnyWordEqualsM0AndNextWordEqualsM1, kLPI2C_1stWordAndM1EqualsM0AndM1, kLPI2C_AnyWordAndM1EqualsM0 }

  LPI2C master data match configuration modes.
- enum _lpi2c_master_transfer_flags { kLPI2C_TransferDefaultFlag = 0x00U, kLPI2C_TransferNoStartFlag = 0x01U, kLPI2C_TransferRepeatedStartFlag = 0x02U, kLPI2C_TransferNoStopFlag = 0x04U }

  Transfer option flags.

Initialization and deinitialization

- void LPI2C_MasterGetDefaultConfig (lpi2c_master_config_t *masterConfig)

  Provides a default configuration for the LPI2C master peripheral.
- void LPI2C_MasterInit (LPI2C_Type *base, const lpi2c_master_config_t *masterConfig, uint32_t sourceClock_Hz)

  Initializes the LPI2C master peripheral.
- void LPI2C_MasterDeinit (LPI2C_Type *base)

  Deinitializes the LPI2C master peripheral.
- void LPI2C_MasterConfigureDataMatch (LPI2C_Type *base, const lpi2c_data_match_config_t *config)

  Configures LPI2C master data match feature.
- status_t **LPI2C_MasterCheckAndClearError** (LPI2C_Type *base, uint32_t status)
- status_t **LPI2C_CheckForBusyBus** (LPI2C_Type *base)
- static void LPI2C_MasterReset (LPI2C_Type *base)

  Performs a software reset.
- static void LPI2C_MasterEnable (LPI2C_Type *base, bool enable)

  Enables or disables the LPI2C module as master.

Status

- static uint32_t LPI2C_MasterGetStatusFlags (LPI2C_Type *base)

  Gets the LPI2C master status flags.
- static void LPI2C_MasterClearStatusFlags (LPI2C_Type *base, uint32_t statusMask)

  Clears the LPI2C master status flag state.

Interrupts

- static void LPI2C_MasterEnableInterrupts (LPI2C_Type *base, uint32_t interruptMask)

  Enables the LPI2C master interrupt requests.
- static void LPI2C_MasterDisableInterrupts (LPI2C_Type *base, uint32_t interruptMask)

  Disables the LPI2C master interrupt requests.
- static uint32_t LPI2C_MasterGetEnabledInterrupts (LPI2C_Type *base)

  Returns the set of currently enabled LPI2C master interrupt requests.

DMA control

- static void LPI2C_MasterEnableDMA (LPI2C_Type *base, bool enableTx, bool enableRx)

  Enables or disables LPI2C master DMA requests.
- static uint32_t LPI2C_MasterGetTxFifoAddress (LPI2C_Type *base)

  Gets LPI2C master transmit data register address for DMA transfer.
- static uint32_t LPI2C_MasterGetRxFifoAddress (LPI2C_Type *base)

  Gets LPI2C master receive data register address for DMA transfer.

FIFO control

- static void LPI2C_MasterSetWatermarks (LPI2C_Type *base, size_t txWords, size_t rxWords)

  Sets the watermarks for LPI2C master FIFOs.
- static void LPI2C_MasterGetFifoCounts (LPI2C_Type *base, size_t *rxCount, size_t *txCount)

  Gets the current number of words in the LPI2C master FIFOs.

Bus operations

- void LPI2C_MasterSetBaudRate (LPI2C_Type *base, uint32_t sourceClock_Hz, uint32_t baudRate_Hz)

  Sets the I2C bus frequency for master transactions.
- static bool LPI2C_MasterGetBusIdleState (LPI2C_Type *base)

  Returns whether the bus is idle.
- status_t LPI2C_MasterStart (LPI2C_Type *base, uint8_t address, lpi2c_direction_t dir)

  Sends a START signal and slave address on the I2C bus.
- static status_t LPI2C_MasterRepeatedStart (LPI2C_Type *base, uint8_t address, lpi2c_direction_t dir)

  Sends a repeated START signal and slave address on the I2C bus.
- status_t LPI2C_MasterSend (LPI2C_Type *base, void *txBuff, size_t txSize)

  Performs a polling send transfer on the I2C bus.
- status_t LPI2C_MasterReceive (LPI2C_Type *base, void *rxBuff, size_t rxSize)

  Performs a polling receive transfer on the I2C bus.
- status_t LPI2C_MasterStop (LPI2C_Type *base)

  Sends a STOP signal on the I2C bus.
- status_t LPI2C_MasterTransferBlocking (LPI2C_Type *base, lpi2c_master_transfer_t *transfer)

  Performs a master polling transfer on the I2C bus.

Non-blocking

- void LPI2C_MasterTransferCreateHandle (LPI2C_Type *base, lpi2c_master_handle_t *handle, lpi2c_master_transfer_callback_t callback, void *userData)

  Creates a new handle for the LPI2C master non-blocking APIs.
- status_t LPI2C_MasterTransferNonBlocking (LPI2C_Type *base, lpi2c_master_handle_t *handle, lpi2c_master↩ _transfer_t *transfer)

  Performs a non-blocking transaction on the I2C bus.
- status_t LPI2C_MasterTransferGetCount (LPI2C_Type *base, lpi2c_master_handle_t *handle, size_t *count)

  Returns number of bytes transferred so far.
- void LPI2C_MasterTransferAbort (LPI2C_Type *base, lpi2c_master_handle_t *handle)

  Terminates a non-blocking LPI2C master transmission early.

IRQ handler

- void LPI2C_MasterTransferHandleIRQ (LPI2C_Type *base, lpi2c_master_handle_t *handle)

  Reusable routine to handle master interrupts.

16.5.1 Detailed Description

16.5.2 Typedef Documentation

16.5.2.1 lpi2c_master_transfer_callback_t

```
typedef void(* lpi2c_master_transfer_callback_t) (LPI2C_Type *base, lpi2c_master_handle_t *handle,
status_t completionStatus, void *userData)
```

Master completion callback function pointer type.

This callback is used only for the non-blocking master transfer API. Specify the callback you wish to use in the call to LPI2C_MasterTransferCreateHandle().

Parameters

base	The LPI2C peripheral base address.
completionStatus	Either kStatus_Success or an error code describing how the transfer completed.
userData	Arbitrary pointer-sized value passed from the application.

16.5.3 Enumeration Type Documentation

16.5.3.1 anonymous enum

```
anonymous enum
```

LPI2C master peripheral flags.

The following status register flags can be cleared:

- kLPI2C_MasterEndOfPacketFlag
- kLPI2C_MasterStopDetectFlag
- kLPI2C_MasterNackDetectFlag
- kLPI2C_MasterArbitrationLostFlag
- kLPI2C_MasterFifoErrFlag

- kLPI2C_MasterPinLowTimeoutFlag
- kLPI2C_MasterDataMatchFlag

All flags except kLPI2C_MasterBusyFlag and kLPI2C_MasterBusBusyFlag can be enabled as interrupts.

Note

These enums are meant to be OR'd together to form a bit mask.

Enumerator

kLPI2C_MasterTxReadyFlag	Transmit data flag.
kLPI2C_MasterRxReadyFlag	Receive data flag.
kLPI2C_MasterEndOfPacketFlag	End Packet flag.
kLPI2C_MasterStopDetectFlag	Stop detect flag.
kLPI2C_MasterNackDetectFlag	NACK detect flag.
kLPI2C_MasterArbitrationLostFlag	Arbitration lost flag.
kLPI2C_MasterFifoErrFlag	FIFO error flag.
kLPI2C_MasterPinLowTimeoutFlag	Pin low timeout flag.
kLPI2C_MasterDataMatchFlag	Data match flag.
kLPI2C_MasterBusyFlag	Master busy flag.
kLPI2C_MasterBusBusyFlag	Bus busy flag.

16.5.3.2 lpi2c_direction_t

```
enum lpi2c_direction_t
```

Direction of master and slave transfers.

Enumerator

kLPI2C_Write	Master transmit.
kLPI2C_Read	Master receive.

16.5.3.3 lpi2c_master_pin_config_t

```
enum lpi2c_master_pin_config_t
```

LPI2C pin configuration.

Enumerator

kLPI2C_2PinOpenDrain	LPI2C Configured for 2-pin open drain mode.
kLPI2C_2PinOutputOnly	LPI2C Configured for 2-pin output only mode (ultra-fast mode)
kLPI2C_2PinPushPull	LPI2C Configured for 2-pin push-pull mode.
kLPI2C_4PinPushPull	LPI2C Configured for 4-pin push-pull mode.
kLPI2C_2PinOpenDrainWithSeparateSlave	LPI2C Configured for 2-pin open drain mode with separate LPI2C slave.
kLPI2C_2PinOutputOnlyWithSeparateSlave	LPI2C Configured for 2-pin output only mode(ultra-fast mode) with separate LPI2C slave.
kLPI2C_2PinPushPullWithSeparateSlave	LPI2C Configured for 2-pin push-pull mode with separate LPI2C slave.
kLPI2C_4PinPushPullWithInvertedOutput	LPI2C Configured for 4-pin push-pull mode(inverted outputs)

16.5.3.4 lpi2c_host_request_source_t

`enum lpi2c_host_request_source_t`

LPI2C master host request selection.

Enumerator

kLPI2C_HostRequestExternalPin	Select the LPI2C_HREQ pin as the host request input.
kLPI2C_HostRequestInputTrigger	Select the input trigger as the host request input.

16.5.3.5 lpi2c_host_request_polarity_t

`enum lpi2c_host_request_polarity_t`

LPI2C master host request pin polarity configuration.

Enumerator

kLPI2C_HostRequestPinActiveLow	Configure the LPI2C_HREQ pin active low.
kLPI2C_HostRequestPinActiveHigh	Configure the LPI2C_HREQ pin active high.

16.5.3.6 lpi2c_data_match_config_mode_t

`enum lpi2c_data_match_config_mode_t`

LPI2C master data match configuration modes.

Enumerator

kLPI2C_MatchDisabled	LPI2C Match Disabled.
kLPI2C_1stWordEqualsM0OrM1	LPI2C Match Enabled and 1st data word equals MATCH0 OR MATCH1.
kLPI2C_AnyWordEqualsM0OrM1	LPI2C Match Enabled and any data word equals MATCH0 OR MATCH1.
kLPI2C_1stWordEqualsM0And2ndWordEqualsM1	LPI2C Match Enabled and 1st data word equals MATCH0, 2nd data equals MATCH1.
kLPI2C_AnyWordEqualsM0AndNextWordEqualsM1	LPI2C Match Enabled and any data word equals MATCH0, next data equals MATCH1.
kLPI2C_1stWordAndM1EqualsM0AndM1	LPI2C Match Enabled and 1st data word and MATCH0 equals MATCH0 and MATCH1.
kLPI2C_AnyWordAndM1EqualsM0AndM1	LPI2C Match Enabled and any data word and MATCH0 equals MATCH0 and MATCH1.

16.5.3.7 _lpi2c_master_transfer_flags

```
enum _lpi2c_master_transfer_flags
```

Transfer option flags.

Note

These enumerations are intended to be OR'd together to form a bit mask of options for the _lpi2c_master_transfer::flags field.

Enumerator

kLPI2C_TransferDefaultFlag	Transfer starts with a start signal, stops with a stop signal.
kLPI2C_TransferNoStartFlag	Don't send a start condition, address, and sub address.
kLPI2C_TransferRepeatedStartFlag	Send a repeated start condition.
kLPI2C_TransferNoStopFlag	Don't send a stop condition.

16.5.4 Function Documentation

16.5.4.1 LPI2C_MasterGetDefaultConfig()

```
void LPI2C_MasterGetDefaultConfig (
            lpi2c_master_config_t * masterConfig )
```

Provides a default configuration for the LPI2C master peripheral.

This function provides the following default configuration for the LPI2C master peripheral:

```
masterConfig->enableMaster            = true;
masterConfig->debugEnable             = false;
masterConfig->ignoreAck               = false;
masterConfig->pinConfig               = kLPI2C_2PinOpenDrain;
masterConfig->baudRate_Hz             = 100000U;
masterConfig->busIdleTimeout_ns       = 0;
masterConfig->pinLowTimeout_ns        = 0;
masterConfig->sdaGlitchFilterWidth_ns = 0;
masterConfig->sclGlitchFilterWidth_ns = 0;
masterConfig->hostRequest.enable      = false;
masterConfig->hostRequest.source      = kLPI2C_HostRequestExternalPin;
masterConfig->hostRequest.polarity    = kLPI2C_HostRequestPinActiveHigh;
```

After calling this function, you can override any settings in order to customize the configuration, prior to initializing the master driver with LPI2C_MasterInit().

Parameters

out	*masterConfig*	User provided configuration structure for default values. Refer to lpi2c_master_config_t.

Examples

board.c.

16.5.4.2 LPI2C_MasterInit()

```
void LPI2C_MasterInit (
            LPI2C_Type * base,
            const lpi2c_master_config_t * masterConfig,
            uint32_t sourceClock_Hz )
```

Initializes the LPI2C master peripheral.

This function enables the peripheral clock and initializes the LPI2C master peripheral as described by the user provided configuration. A software reset is performed prior to configuration.

Parameters

base	The LPI2C peripheral base address.
masterConfig	User provided peripheral configuration. Use LPI2C_MasterGetDefaultConfig() to get a set of defaults that you can override.
sourceClock_Hz	Frequency in Hertz of the LPI2C functional clock. Used to calculate the baud rate divisors, filter widths, and timeout periods.

Examples

board.c.

16.5.4.3 LPI2C_MasterDeinit()

```
void LPI2C_MasterDeinit (
            LPI2C_Type * base )
```

Deinitializes the LPI2C master peripheral.

This function disables the LPI2C master peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

Parameters

base	The LPI2C peripheral base address.

16.5.4.4 LPI2C_MasterConfigureDataMatch()

```
void LPI2C_MasterConfigureDataMatch (
            LPI2C_Type * base,
            const lpi2c_data_match_config_t * config )
```

Configures LPI2C master data match feature.

Parameters

base	The LPI2C peripheral base address.
config	Settings for the data match feature.

16.5.4.5 LPI2C_MasterReset()

```
static void LPI2C_MasterReset (
            LPI2C_Type * base )  [inline], [static]
```

Performs a software reset.

Restores the LPI2C master peripheral to reset conditions.

Parameters

base	The LPI2C peripheral base address.

16.5.4.6 LPI2C_MasterEnable()

```
static void LPI2C_MasterEnable (
```

```
            LPI2C_Type * base,
            bool enable )  [inline], [static]
```

Enables or disables the LPI2C module as master.

Parameters

base	The LPI2C peripheral base address.
enable	Pass true to enable or false to disable the specified LPI2C as master.

16.5.4.7 LPI2C_MasterGetStatusFlags()

```
static uint32_t LPI2C_MasterGetStatusFlags (
            LPI2C_Type * base )  [inline], [static]
```

Gets the LPI2C master status flags.

A bit mask with the state of all LPI2C master status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

Parameters

base	The LPI2C peripheral base address.

Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

See also

_lpi2c_master_flags

16.5.4.8 LPI2C_MasterClearStatusFlags()

```
static void LPI2C_MasterClearStatusFlags (
            LPI2C_Type * base,
            uint32_t statusMask )  [inline], [static]
```

Clears the LPI2C master status flag state.

The following status register flags can be cleared:

- kLPI2C_MasterEndOfPacketFlag

- kLPI2C_MasterStopDetectFlag
- kLPI2C_MasterNackDetectFlag
- kLPI2C_MasterArbitrationLostFlag
- kLPI2C_MasterFifoErrFlag
- kLPI2C_MasterPinLowTimeoutFlag
- kLPI2C_MasterDataMatchFlag

Attempts to clear other flags has no effect.

Parameters

base	The LPI2C peripheral base address.
statusMask	A bitmask of status flags that are to be cleared. The mask is composed of _lpi2c_master_flags enumerators OR'd together. You may pass the result of a previous call to LPI2C_MasterGetStatusFlags().

See also

_lpi2c_master_flags.

16.5.4.9 LPI2C_MasterEnableInterrupts()

```
static void LPI2C_MasterEnableInterrupts (
             LPI2C_Type * base,
             uint32_t interruptMask )  [inline], [static]
```

Enables the LPI2C master interrupt requests.

All flags except kLPI2C_MasterBusyFlag and kLPI2C_MasterBusBusyFlag can be enabled as interrupts.

Parameters

base	The LPI2C peripheral base address.
interruptMask	Bit mask of interrupts to enable. See _lpi2c_master_flags for the set of constants that should be OR'd together to form the bit mask.

16.5.4.10 LPI2C_MasterDisableInterrupts()

```
static void LPI2C_MasterDisableInterrupts (
             LPI2C_Type * base,
             uint32_t interruptMask )  [inline], [static]
```

Disables the LPI2C master interrupt requests.

All flags except kLPI2C_MasterBusyFlag and kLPI2C_MasterBusBusyFlag can be enabled as interrupts.

Parameters

base	The LPI2C peripheral base address.
interruptMask	Bit mask of interrupts to disable. See _lpi2c_master_flags for the set of constants that should be OR'd together to form the bit mask.

16.5.4.11 LPI2C_MasterGetEnabledInterrupts()

```
static uint32_t LPI2C_MasterGetEnabledInterrupts (
            LPI2C_Type * base )  [inline], [static]
```

Returns the set of currently enabled LPI2C master interrupt requests.

Parameters

base	The LPI2C peripheral base address.

Returns

A bitmask composed of _lpi2c_master_flags enumerators OR'd together to indicate the set of enabled interrupts.

16.5.4.12 LPI2C_MasterEnableDMA()

```
static void LPI2C_MasterEnableDMA (
            LPI2C_Type * base,
            bool enableTx,
            bool enableRx )  [inline], [static]
```

Enables or disables LPI2C master DMA requests.

Parameters

base	The LPI2C peripheral base address.
enableTx	Enable flag for transmit DMA request. Pass true for enable, false for disable.
enableRx	Enable flag for receive DMA request. Pass true for enable, false for disable.

16.5.4.13 LPI2C_MasterGetTxFifoAddress()

```
static uint32_t LPI2C_MasterGetTxFifoAddress (
            LPI2C_Type * base )  [inline], [static]
```

Gets LPI2C master transmit data register address for DMA transfer.

Parameters

base	The LPI2C peripheral base address.

Returns

The LPI2C Master Transmit Data Register address.

16.5.4.14 LPI2C_MasterGetRxFifoAddress()

```
static uint32_t LPI2C_MasterGetRxFifoAddress (
            LPI2C_Type * base )  [inline], [static]
```

Gets LPI2C master receive data register address for DMA transfer.

Parameters

base	The LPI2C peripheral base address.

Returns

The LPI2C Master Receive Data Register address.

16.5.4.15 LPI2C_MasterSetWatermarks()

```
static void LPI2C_MasterSetWatermarks (
            LPI2C_Type * base,
            size_t txWords,
            size_t rxWords )  [inline], [static]
```

Sets the watermarks for LPI2C master FIFOs.

Parameters

base	The LPI2C peripheral base address.

Parameters

txWords	Transmit FIFO watermark value in words. The kLPI2C_MasterTxReadyFlag flag is set whenever the number of words in the transmit FIFO is equal or less than *txWords*. Writing a value equal or greater than the FIFO size is truncated.
rxWords	Receive FIFO watermark value in words. The kLPI2C_MasterRxReadyFlag flag is set whenever the number of words in the receive FIFO is greater than *rxWords*. Writing a value equal or greater than the FIFO size is truncated.

16.5.4.16 LPI2C_MasterGetFifoCounts()

```
static void LPI2C_MasterGetFifoCounts (
            LPI2C_Type * base,
            size_t * rxCount,
            size_t * txCount )  [inline], [static]
```

Gets the current number of words in the LPI2C master FIFOs.

Parameters

	base	The LPI2C peripheral base address.
out	*txCount*	Pointer through which the current number of words in the transmit FIFO is returned. Pass NULL if this value is not required.
out	*rxCount*	Pointer through which the current number of words in the receive FIFO is returned. Pass NULL if this value is not required.

16.5.4.17 LPI2C_MasterSetBaudRate()

```
void LPI2C_MasterSetBaudRate (
            LPI2C_Type * base,
            uint32_t sourceClock_Hz,
            uint32_t baudRate_Hz )
```

Sets the I2C bus frequency for master transactions.

The LPI2C master is automatically disabled and re-enabled as necessary to configure the baud rate. Do not call this function during a transfer, or the transfer is aborted.

Note

Please note that the second parameter is the clock frequency of LPI2C module, the third parameter means user configured bus baudrate, this implementation is different from other I2C drivers which use baudrate configuration as second parameter and source clock frequency as third parameter.

Parameters

base	The LPI2C peripheral base address.
sourceClock_Hz	LPI2C functional clock frequency in Hertz.
baudRate_Hz	Requested bus frequency in Hertz.

16.5.4.18 LPI2C_MasterGetBusIdleState()

```
static bool LPI2C_MasterGetBusIdleState (
            LPI2C_Type * base )  [inline], [static]
```

Returns whether the bus is idle.

Requires the master mode to be enabled.

Parameters

base	The LPI2C peripheral base address.

Return values

true	Bus is busy.
false	Bus is idle.

16.5.4.19 LPI2C_MasterStart()

```
status_t LPI2C_MasterStart (
            LPI2C_Type * base,
            uint8_t address,
            lpi2c_direction_t dir )
```

Sends a START signal and slave address on the I2C bus.

This function is used to initiate a new master mode transfer. First, the bus state is checked to ensure that another master is not occupying the bus. Then a START signal is transmitted, followed by the 7-bit address specified in the *address* parameter. Note that this function does not actually wait until the START and address are successfully sent on the bus before returning.

Parameters

base	The LPI2C peripheral base address.
address	7-bit slave device address, in bits [6:0].
dir	Master transfer direction, either kLPI2C_Read or kLPI2C_Write. This parameter is used to set the R/w bit (bit 0) in the transmitted slave address.

Return values

kStatus_Success	START signal and address were successfully enqueued in the transmit FIFO.
kStatus_LPI2C_Busy	Another master is currently utilizing the bus.

16.5.4.20 LPI2C_MasterRepeatedStart()

```
static status_t LPI2C_MasterRepeatedStart (
            LPI2C_Type * base,
            uint8_t address,
            lpi2c_direction_t dir )  [inline], [static]
```

Sends a repeated START signal and slave address on the I2C bus.

This function is used to send a Repeated START signal when a transfer is already in progress. Like LPI2C_MasterStart(), it also sends the specified 7-bit address.

Note

This function exists primarily to maintain compatible APIs between LPI2C and I2C drivers, as well as to better document the intent of code that uses these APIs.

Parameters

base	The LPI2C peripheral base address.
address	7-bit slave device address, in bits [6:0].
dir	Master transfer direction, either kLPI2C_Read or kLPI2C_Write. This parameter is used to set the R/w bit (bit 0) in the transmitted slave address.

Return values

kStatus_Success	Repeated START signal and address were successfully enqueued in the transmit FIFO.
kStatus_LPI2C_Busy	Another master is currently utilizing the bus.

References LPI2C_MasterStart().

16.5.4.21 LPI2C_MasterSend()

```
status_t LPI2C_MasterSend (
            LPI2C_Type * base,
            void * txBuff,
            size_t txSize )
```

Performs a polling send transfer on the I2C bus.

Sends up to *txSize* number of bytes to the previously addressed slave device. The slave may reply with a NAK to any byte in order to terminate the transfer early. If this happens, this function returns kStatus_LPI2C_Nak.

Parameters

base	The LPI2C peripheral base address.
txBuff	The pointer to the data to be transferred.
txSize	The length in bytes of the data to be transferred.

Return values

kStatus_Success	Data was sent successfully.
kStatus_LPI2C_Busy	Another master is currently utilizing the bus.
kStatus_LPI2C_Nak	The slave device sent a NAK in response to a byte.
kStatus_LPI2C_FifoError	FIFO under run or over run.
kStatus_LPI2C_ArbitrationLost	Arbitration lost error.
kStatus_LPI2C_PinLowTimeout	SCL or SDA were held low longer than the timeout.

16.5.4.22 LPI2C_MasterReceive()

```
status_t LPI2C_MasterReceive (
             LPI2C_Type * base,
             void * rxBuff,
             size_t rxSize )
```

Performs a polling receive transfer on the I2C bus.

Parameters

base	The LPI2C peripheral base address.
rxBuff	The pointer to the data to be transferred.
rxSize	The length in bytes of the data to be transferred.

Return values

kStatus_Success	Data was received successfully.
kStatus_LPI2C_Busy	Another master is currently utilizing the bus.
kStatus_LPI2C_Nak	The slave device sent a NAK in response to a byte.
kStatus_LPI2C_FifoError	FIFO under run or overrun.
kStatus_LPI2C_ArbitrationLost	Arbitration lost error.
kStatus_LPI2C_PinLowTimeout	SCL or SDA were held low longer than the timeout.

16.5.4.23 LPI2C_MasterStop()

```
status_t LPI2C_MasterStop (
             LPI2C_Type * base )
```

Sends a STOP signal on the I2C bus.

This function does not return until the STOP signal is seen on the bus, or an error occurs.

Parameters

base	The LPI2C peripheral base address.

Return values

kStatus_Success	The STOP signal was successfully sent on the bus and the transaction terminated.
kStatus_LPI2C_Busy	Another master is currently utilizing the bus.
kStatus_LPI2C_Nak	The slave device sent a NAK in response to a byte.
kStatus_LPI2C_FifoError	FIFO under run or overrun.
kStatus_LPI2C_ArbitrationLost	Arbitration lost error.
kStatus_LPI2C_PinLowTimeout	SCL or SDA were held low longer than the timeout.

16.5.4.24 LPI2C_MasterTransferBlocking()

```
status_t LPI2C_MasterTransferBlocking (
             LPI2C_Type * base,
             lpi2c_master_transfer_t * transfer )
```

Performs a master polling transfer on the I2C bus.

Note

The API does not return until the transfer succeeds or fails due to error happens during transfer.

Parameters

base	The LPI2C peripheral base address.
transfer	Pointer to the transfer structure.

Return values

kStatus_Success	Data was received successfully.
kStatus_LPI2C_Busy	Another master is currently utilizing the bus.
kStatus_LPI2C_Nak	The slave device sent a NAK in response to a byte.
kStatus_LPI2C_FifoError	FIFO under run or overrun.
kStatus_LPI2C_ArbitrationLost	Arbitration lost error.
kStatus_LPI2C_PinLowTimeout	SCL or SDA were held low longer than the timeout.

16.5.4.25 LPI2C_MasterTransferCreateHandle()

```
void LPI2C_MasterTransferCreateHandle (
             LPI2C_Type * base,
             lpi2c_master_handle_t * handle,
             lpi2c_master_transfer_callback_t callback,
             void * userData )
```

Creates a new handle for the LPI2C master non-blocking APIs.

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the LPI2C_MasterTransferAbort() API shall be called.

Note

The function also enables the NVIC IRQ for the input LPI2C. Need to notice that on some SoCs the LPI2C IRQ is connected to INTMUX, in this case user needs to enable the associated INTMUX IRQ in application.

Parameters

	base	The LPI2C peripheral base address.
out	*handle*	Pointer to the LPI2C master driver handle.
	callback	User provided pointer to the asynchronous callback function.
	userData	User provided pointer to the application callback data.

16.5.4.26 LPI2C_MasterTransferNonBlocking()

```
status_t LPI2C_MasterTransferNonBlocking (
             LPI2C_Type * base,
             lpi2c_master_handle_t * handle,
             lpi2c_master_transfer_t * transfer )
```

Performs a non-blocking transaction on the I2C bus.

Parameters

base	The LPI2C peripheral base address.
handle	Pointer to the LPI2C master driver handle.
transfer	The pointer to the transfer descriptor.

Return values

kStatus_Success	The transaction was started successfully.
kStatus_LPI2C_Busy	Either another master is currently utilizing the bus, or a non-blocking transaction is already in progress.

16.5.4.27 LPI2C_MasterTransferGetCount()

```
status_t LPI2C_MasterTransferGetCount (
            LPI2C_Type * base,
            lpi2c_master_handle_t * handle,
            size_t * count )
```

Returns number of bytes transferred so far.

Parameters

	base	The LPI2C peripheral base address.
	handle	Pointer to the LPI2C master driver handle.
out	*count*	Number of bytes transferred so far by the non-blocking transaction.

Return values

kStatus_Success	
kStatus_NoTransferInProgress	There is not a non-blocking transaction currently in progress.

16.5.4.28 LPI2C_MasterTransferAbort()

```
void LPI2C_MasterTransferAbort (
            LPI2C_Type * base,
            lpi2c_master_handle_t * handle )
```

Terminates a non-blocking LPI2C master transmission early.

Note

It is not safe to call this function from an IRQ handler that has a higher priority than the LPI2C peripheral's IRQ priority.

Parameters

base	The LPI2C peripheral base address.
handle	Pointer to the LPI2C master driver handle.

Return values

kStatus_Success	A transaction was successfully aborted.
kStatus_LPI2C_Idle	There is not a non-blocking transaction currently in progress.

16.5.4.29 LPI2C_MasterTransferHandleIRQ()

```
void LPI2C_MasterTransferHandleIRQ (
            LPI2C_Type * base,
            lpi2c_master_handle_t * handle )
```

Reusable routine to handle master interrupts.

Note

This function does not need to be called unless you are reimplementing the nonblocking API's interrupt handler routines to add special functionality.

Parameters

base	The LPI2C peripheral base address.
handle	Pointer to the LPI2C master driver handle.

16.6 LPI2C Slave Driver

Data Structures

- struct lpi2c_slave_config_t

  Structure with settings to initialize the LPI2C slave module.
- struct lpi2c_slave_transfer_t

  LPI2C slave transfer structure.
- struct lpi2c_slave_handle_t

  LPI2C slave handle structure.

Typedefs

- typedef void(∗ lpi2c_slave_transfer_callback_t) (LPI2C_Type ∗base, lpi2c_slave_transfer_t ∗transfer, void ∗user↩ Data)

  Slave event callback function pointer type.

Enumerations

- enum _lpi2c_slave_flags {
  kLPI2C_SlaveTxReadyFlag = LPI2C_SSR_TDF_MASK, kLPI2C_SlaveRxReadyFlag = LPI2C_SSR_RDF_MA↩ SK, kLPI2C_SlaveAddressValidFlag = LPI2C_SSR_AVF_MASK, kLPI2C_SlaveTransmitAckFlag = LPI2C_SS↩ R_TAF_MASK,
  kLPI2C_SlaveRepeatedStartDetectFlag = LPI2C_SSR_RSF_MASK, kLPI2C_SlaveStopDetectFlag = LPI2C_↩ SSR_SDF_MASK, kLPI2C_SlaveBitErrFlag = LPI2C_SSR_BEF_MASK, kLPI2C_SlaveFifoErrFlag = LPI2C_S↩ SR_FEF_MASK,
  kLPI2C_SlaveAddressMatch0Flag = LPI2C_SSR_AM0F_MASK, kLPI2C_SlaveAddressMatch1Flag = LPI2C_↩ SSR_AM1F_MASK, kLPI2C_SlaveGeneralCallFlag = LPI2C_SSR_GCF_MASK, kLPI2C_SlaveBusyFlag = LP↩ I2C_SSR_SBF_MASK,
  kLPI2C_SlaveBusBusyFlag = LPI2C_SSR_BBF_MASK }

  LPI2C slave peripheral flags.
- enum lpi2c_slave_address_match_t { kLPI2C_MatchAddress0 = 0U, kLPI2C_MatchAddress0OrAddress1 = 2U, kLPI2C_MatchAddress0ThroughAddress1 = 6U }

  LPI2C slave address match options.
- enum lpi2c_slave_transfer_event_t {
  kLPI2C_SlaveAddressMatchEvent = 0x01U, kLPI2C_SlaveTransmitEvent = 0x02U, kLPI2C_SlaveReceiveEvent = 0x04U, kLPI2C_SlaveTransmitAckEvent = 0x08U,
  kLPI2C_SlaveRepeatedStartEvent = 0x10U, kLPI2C_SlaveCompletionEvent = 0x20U, kLPI2C_SlaveAllEvents }

  Set of events sent to the callback for non blocking slave transfers.

Slave initialization and deinitialization

- void LPI2C_SlaveGetDefaultConfig (lpi2c_slave_config_t ∗slaveConfig)

  Provides a default configuration for the LPI2C slave peripheral.
- void LPI2C_SlaveInit (LPI2C_Type ∗base, const lpi2c_slave_config_t ∗slaveConfig, uint32_t sourceClock_Hz)

  Initializes the LPI2C slave peripheral.
- void LPI2C_SlaveDeinit (LPI2C_Type ∗base)

  Deinitializes the LPI2C slave peripheral.
- static void LPI2C_SlaveReset (LPI2C_Type ∗base)

  Performs a software reset of the LPI2C slave peripheral.
- static void LPI2C_SlaveEnable (LPI2C_Type ∗base, bool enable)

  Enables or disables the LPI2C module as slave.

Slave status

- static uint32_t LPI2C_SlaveGetStatusFlags (LPI2C_Type *base)

  Gets the LPI2C slave status flags.
- static void LPI2C_SlaveClearStatusFlags (LPI2C_Type *base, uint32_t statusMask)

  Clears the LPI2C status flag state.

Slave interrupts

- static void LPI2C_SlaveEnableInterrupts (LPI2C_Type *base, uint32_t interruptMask)

  Enables the LPI2C slave interrupt requests.
- static void LPI2C_SlaveDisableInterrupts (LPI2C_Type *base, uint32_t interruptMask)

  Disables the LPI2C slave interrupt requests.
- static uint32_t LPI2C_SlaveGetEnabledInterrupts (LPI2C_Type *base)

  Returns the set of currently enabled LPI2C slave interrupt requests.

Slave DMA control

- static void LPI2C_SlaveEnableDMA (LPI2C_Type *base, bool enableAddressValid, bool enableRx, bool enable↩ Tx)

  Enables or disables the LPI2C slave peripheral DMA requests.

Slave bus operations

- static bool LPI2C_SlaveGetBusIdleState (LPI2C_Type *base)

  Returns whether the bus is idle.
- static void LPI2C_SlaveTransmitAck (LPI2C_Type *base, bool ackOrNack)

  Transmits either an ACK or NAK on the I2C bus in response to a byte from the master.
- static uint32_t LPI2C_SlaveGetReceivedAddress (LPI2C_Type *base)

  Returns the slave address sent by the I2C master.
- status_t LPI2C_SlaveSend (LPI2C_Type *base, void *txBuff, size_t txSize, size_t *actualTxSize)

  Performs a polling send transfer on the I2C bus.
- status_t LPI2C_SlaveReceive (LPI2C_Type *base, void *rxBuff, size_t rxSize, size_t *actualRxSize)

  Performs a polling receive transfer on the I2C bus.

Slave non-blocking

- void LPI2C_SlaveTransferCreateHandle (LPI2C_Type *base, lpi2c_slave_handle_t *handle, lpi2c_slave_transfer_callback_t callback, void *userData)

  Creates a new handle for the LPI2C slave non-blocking APIs.
- status_t LPI2C_SlaveTransferNonBlocking (LPI2C_Type *base, lpi2c_slave_handle_t *handle, uint32_t event↩ Mask)

  Starts accepting slave transfers.
- status_t LPI2C_SlaveTransferGetCount (LPI2C_Type *base, lpi2c_slave_handle_t *handle, size_t *count)

  Gets the slave transfer status during a non-blocking transfer.
- void LPI2C_SlaveTransferAbort (LPI2C_Type *base, lpi2c_slave_handle_t *handle)

  Aborts the slave non-blocking transfers.

Slave IRQ handler

- void LPI2C_SlaveTransferHandleIRQ (LPI2C_Type *base, lpi2c_slave_handle_t *handle)

  Reusable routine to handle slave interrupts.

16.6.1 Detailed Description

16.6.2 Typedef Documentation

16.6.2.1 lpi2c_slave_transfer_callback_t

```
typedef void(* lpi2c_slave_transfer_callback_t) (LPI2C_Type *base, lpi2c_slave_transfer_t *transfer,
void *userData)
```

Slave event callback function pointer type.

This callback is used only for the slave non-blocking transfer API. To install a callback, use the LPI2C_SlaveSetCallback() function after you have created a handle.

Parameters

base	Base address for the LPI2C instance on which the event occurred.
transfer	Pointer to transfer descriptor containing values passed to and/or from the callback.
userData	Arbitrary pointer-sized value passed from the application.

16.6.3 Enumeration Type Documentation

16.6.3.1 _lpi2c_slave_flags

```
enum _lpi2c_slave_flags
```

LPI2C slave peripheral flags.

The following status register flags can be cleared:

- kLPI2C_SlaveRepeatedStartDetectFlag
- kLPI2C_SlaveStopDetectFlag
- kLPI2C_SlaveBitErrFlag
- kLPI2C_SlaveFifoErrFlag

All flags except kLPI2C_SlaveBusyFlag and kLPI2C_SlaveBusBusyFlag can be enabled as interrupts.

Note

These enumerations are meant to be OR'd together to form a bit mask.

Enumerator

kLPI2C_SlaveTxReadyFlag	Transmit data flag.
kLPI2C_SlaveRxReadyFlag	Receive data flag.
kLPI2C_SlaveAddressValidFlag	Address valid flag.
kLPI2C_SlaveTransmitAckFlag	Transmit ACK flag.
kLPI2C_SlaveRepeatedStartDetectFlag	Repeated start detect flag.
kLPI2C_SlaveStopDetectFlag	Stop detect flag.
kLPI2C_SlaveBitErrFlag	Bit error flag.
kLPI2C_SlaveFifoErrFlag	FIFO error flag.
kLPI2C_SlaveAddressMatch0Flag	Address match 0 flag.
kLPI2C_SlaveAddressMatch1Flag	Address match 1 flag.
kLPI2C_SlaveGeneralCallFlag	General call flag.
kLPI2C_SlaveBusyFlag	Master busy flag.
kLPI2C_SlaveBusBusyFlag	Bus busy flag.

16.6.3.2 lpi2c_slave_address_match_t

`enum lpi2c_slave_address_match_t`

LPI2C slave address match options.

Enumerator

kLPI2C_MatchAddress0	Match only address 0.
kLPI2C_MatchAddress0OrAddress1	Match either address 0 or address 1.
kLPI2C_MatchAddress0ThroughAddress1	Match a range of slave addresses from address 0 through address 1.

16.6.3.3 lpi2c_slave_transfer_event_t

`enum lpi2c_slave_transfer_event_t`

Set of events sent to the callback for non blocking slave transfers.

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to LPI2C_SlaveTransferNonBlocking() in order to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

Note

These enumerations are meant to be OR'd together to form a bit mask of events.

Enumerator

kLPI2C_SlaveAddressMatchEvent	Received the slave address after a start or repeated start.
kLPI2C_SlaveTransmitEvent	Callback is requested to provide data to transmit (slave-transmitter role).
kLPI2C_SlaveReceiveEvent	Callback is requested to provide a buffer in which to place received data (slave-receiver role).
kLPI2C_SlaveTransmitAckEvent	Callback needs to either transmit an ACK or NACK.
kLPI2C_SlaveRepeatedStartEvent	A repeated start was detected.
kLPI2C_SlaveCompletionEvent	A stop was detected, completing the transfer.
kLPI2C_SlaveAllEvents	Bit mask of all available events.

16.6.4 Function Documentation

16.6.4.1 LPI2C_SlaveGetDefaultConfig()

```
void LPI2C_SlaveGetDefaultConfig (
            lpi2c_slave_config_t * slaveConfig )
```

Provides a default configuration for the LPI2C slave peripheral.

This function provides the following default configuration for the LPI2C slave peripheral:

```
slaveConfig->enableSlave               = true;
slaveConfig->address0                  = 0U;
slaveConfig->address1                  = 0U;
slaveConfig->addressMatchMode          = kLPI2C_MatchAddress0;
slaveConfig->filterDozeEnable          = true;
slaveConfig->filterEnable              = true;
slaveConfig->enableGeneralCall         = false;
slaveConfig->sclStall.enableAck        = false;
slaveConfig->sclStall.enableTx         = true;
slaveConfig->sclStall.enableRx         = true;
slaveConfig->sclStall.enableAddress    = true;
slaveConfig->ignoreAck                 = false;
slaveConfig->enableReceivedAddressRead = false;
slaveConfig->sdaGlitchFilterWidth_ns   = 0;
slaveConfig->sclGlitchFilterWidth_ns   = 0;
slaveConfig->dataValidDelay_ns         = 0;
slaveConfig->clockHoldTime_ns          = 0;
```

After calling this function, override any settings to customize the configuration, prior to initializing the master driver with LPI2C_SlaveInit(). Be sure to override at least the *address0* member of the configuration structure with the desired slave address.

Parameters

out	*slaveConfig*	User provided configuration structure that is set to default values. Refer to lpi2c_slave_config_t.

16.6.4.2 LPI2C_SlaveInit()

```
void LPI2C_SlaveInit (
            LPI2C_Type * base,
            const lpi2c_slave_config_t * slaveConfig,
            uint32_t sourceClock_Hz )
```

Initializes the LPI2C slave peripheral.

This function enables the peripheral clock and initializes the LPI2C slave peripheral as described by the user provided configuration.

Parameters

base	The LPI2C peripheral base address.
slaveConfig	User provided peripheral configuration. Use LPI2C_SlaveGetDefaultConfig() to get a set of defaults that you can override.
sourceClock_Hz	Frequency in Hertz of the LPI2C functional clock. Used to calculate the filter widths, data valid delay, and clock hold time.

16.6.4.3 LPI2C_SlaveDeinit()

```
void LPI2C_SlaveDeinit (
            LPI2C_Type * base )
```

Deinitializes the LPI2C slave peripheral.

This function disables the LPI2C slave peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

Parameters

base	The LPI2C peripheral base address.

16.6.4.4 LPI2C_SlaveReset()

```
static void LPI2C_SlaveReset (
            LPI2C_Type * base )  [inline], [static]
```

Performs a software reset of the LPI2C slave peripheral.

Parameters

base	The LPI2C peripheral base address.

16.6.4.5 LPI2C_SlaveEnable()

```
static void LPI2C_SlaveEnable (
            LPI2C_Type * base,
            bool enable )  [inline], [static]
```

Enables or disables the LPI2C module as slave.

Parameters

base	The LPI2C peripheral base address.
enable	Pass true to enable or false to disable the specified LPI2C as slave.

16.6.4.6 LPI2C_SlaveGetStatusFlags()

```
static uint32_t LPI2C_SlaveGetStatusFlags (
            LPI2C_Type * base )  [inline], [static]
```

Gets the LPI2C slave status flags.

A bit mask with the state of all LPI2C slave status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

Parameters

base	The LPI2C peripheral base address.

Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

See also

_lpi2c_slave_flags

16.6.4.7 LPI2C_SlaveClearStatusFlags()

```
static void LPI2C_SlaveClearStatusFlags (
            LPI2C_Type * base,
            uint32_t statusMask )  [inline], [static]
```

Clears the LPI2C status flag state.

The following status register flags can be cleared:

- kLPI2C_SlaveRepeatedStartDetectFlag
- kLPI2C_SlaveStopDetectFlag
- kLPI2C_SlaveBitErrFlag
- kLPI2C_SlaveFifoErrFlag

Attempts to clear other flags has no effect.

Parameters

base	The LPI2C peripheral base address.
statusMask	A bitmask of status flags that are to be cleared. The mask is composed of _lpi2c_slave_flags enumerators OR'd together. You may pass the result of a previous call to LPI2C_SlaveGetStatusFlags().

See also

_lpi2c_slave_flags.

16.6.4.8 LPI2C_SlaveEnableInterrupts()

```
static void LPI2C_SlaveEnableInterrupts (
             LPI2C_Type * base,
             uint32_t interruptMask )  [inline], [static]
```

Enables the LPI2C slave interrupt requests.

All flags except kLPI2C_SlaveBusyFlag and kLPI2C_SlaveBusBusyFlag can be enabled as interrupts.

Parameters

base	The LPI2C peripheral base address.
interruptMask	Bit mask of interrupts to enable. See _lpi2c_slave_flags for the set of constants that should be OR'd together to form the bit mask.

16.6.4.9 LPI2C_SlaveDisableInterrupts()

```
static void LPI2C_SlaveDisableInterrupts (
```

```
            LPI2C_Type * base,
            uint32_t interruptMask )  [inline], [static]
```

Disables the LPI2C slave interrupt requests.

All flags except kLPI2C_SlaveBusyFlag and kLPI2C_SlaveBusBusyFlag can be enabled as interrupts.

Parameters

base	The LPI2C peripheral base address.
interruptMask	Bit mask of interrupts to disable. See _lpi2c_slave_flags for the set of constants that should be OR'd together to form the bit mask.

16.6.4.10 LPI2C_SlaveGetEnabledInterrupts()

```
static uint32_t LPI2C_SlaveGetEnabledInterrupts (
            LPI2C_Type * base )  [inline], [static]
```

Returns the set of currently enabled LPI2C slave interrupt requests.

Parameters

base	The LPI2C peripheral base address.

Returns

A bitmask composed of _lpi2c_slave_flags enumerators OR'd together to indicate the set of enabled interrupts.

16.6.4.11 LPI2C_SlaveEnableDMA()

```
static void LPI2C_SlaveEnableDMA (
            LPI2C_Type * base,
            bool enableAddressValid,
            bool enableRx,
            bool enableTx )  [inline], [static]
```

Enables or disables the LPI2C slave peripheral DMA requests.

Parameters

base	The LPI2C peripheral base address.
enableAddressValid	Enable flag for the address valid DMA request. Pass true for enable, false for disable. The address valid DMA request is shared with the receive data DMA request.
enableRx	Enable flag for the receive data DMA request. Pass true for enable, false for disable.
enableTx	Enable flag for the transmit data DMA request. Pass true for enable, false for disable.

16.6.4.12 LPI2C_SlaveGetBusIdleState()

```
static bool LPI2C_SlaveGetBusIdleState (
            LPI2C_Type * base )  [inline], [static]
```

Returns whether the bus is idle.

Requires the slave mode to be enabled.

Parameters

base	The LPI2C peripheral base address.

Return values

true	Bus is busy.
false	Bus is idle.

16.6.4.13 LPI2C_SlaveTransmitAck()

```
static void LPI2C_SlaveTransmitAck (
            LPI2C_Type * base,
            bool ackOrNack )  [inline], [static]
```

Transmits either an ACK or NAK on the I2C bus in response to a byte from the master.

Use this function to send an ACK or NAK when the kLPI2C_SlaveTransmitAckFlag is asserted. This only happens if you enable the sclStall.enableAck field of the lpi2c_slave_config_t configuration structure used to initialize the slave peripheral.

Parameters

base	The LPI2C peripheral base address.
ackOrNack	Pass true for an ACK or false for a NAK.

16.6.4.14 LPI2C_SlaveGetReceivedAddress()

```
static uint32_t LPI2C_SlaveGetReceivedAddress (
            LPI2C_Type * base )  [inline], [static]
```

Returns the slave address sent by the I2C master.

This function should only be called if the kLPI2C_SlaveAddressValidFlag is asserted.

Parameters

base	The LPI2C peripheral base address.

Returns

The 8-bit address matched by the LPI2C slave. Bit 0 contains the R/w direction bit, and the 7-bit slave address is in the upper 7 bits.

16.6.4.15 LPI2C_SlaveSend()

```
status_t LPI2C_SlaveSend (
             LPI2C_Type * base,
             void * txBuff,
             size_t txSize,
             size_t * actualTxSize )
```

Performs a polling send transfer on the I2C bus.

Parameters

	base	The LPI2C peripheral base address.
	txBuff	The pointer to the data to be transferred.
	txSize	The length in bytes of the data to be transferred.
out	*actualTxSize*	

Returns

Error or success status returned by API.

16.6.4.16 LPI2C_SlaveReceive()

```
status_t LPI2C_SlaveReceive (
             LPI2C_Type * base,
             void * rxBuff,
             size_t rxSize,
             size_t * actualRxSize )
```

Performs a polling receive transfer on the I2C bus.

Parameters

	base	The LPI2C peripheral base address.
	rxBuff	The pointer to the data to be transferred.
	rxSize	The length in bytes of the data to be transferred.
out	*actualRxSize*	

Returns

Error or success status returned by API.

16.6.4.17 LPI2C_SlaveTransferCreateHandle()

```
void LPI2C_SlaveTransferCreateHandle (
            LPI2C_Type * base,
            lpi2c_slave_handle_t * handle,
            lpi2c_slave_transfer_callback_t callback,
            void * userData )
```

Creates a new handle for the LPI2C slave non-blocking APIs.

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the LPI2C_SlaveTransferAbort() API shall be called.

Note

The function also enables the NVIC IRQ for the input LPI2C. Need to notice that on some SoCs the LPI2C IRQ is connected to INTMUX, in this case user needs to enable the associated INTMUX IRQ in application.

Parameters

	base	The LPI2C peripheral base address.
out	*handle*	Pointer to the LPI2C slave driver handle.
	callback	User provided pointer to the asynchronous callback function.
	userData	User provided pointer to the application callback data.

16.6.4.18 LPI2C_SlaveTransferNonBlocking()

```
status_t LPI2C_SlaveTransferNonBlocking (
            LPI2C_Type * base,
            lpi2c_slave_handle_t * handle,
            uint32_t eventMask )
```

Starts accepting slave transfers.

Call this API after calling I2C_SlaveInit() and LPI2C_SlaveTransferCreateHandle() to start processing transactions driven by an I2C master. The slave monitors the I2C bus and pass events to the callback that was passed into the call to LPI2C_SlaveTransferCreateHandle(). The callback is always invoked from the interrupt context.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of lpi2c_slave_transfer_event_t enumerators for the events you wish to receive. The kLPI2C_SlaveTransmitEvent and kLPI2C_SlaveReceiveEvent events are always enabled and do not need to be included in the mask. Alternatively, you can pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the kLPI2C_SlaveAllEvents constant is provided as a convenient way to enable all events.

Parameters

base	The LPI2C peripheral base address.
handle	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.
eventMask	Bit mask formed by OR'ing together lpi2c_slave_transfer_event_t enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and kLPI2C_SlaveAllEvents to enable all events.

Return values

kStatus_Success	Slave transfers were successfully started.
kStatus_LPI2C_Busy	Slave transfers have already been started on this handle.

16.6.4.19 LPI2C_SlaveTransferGetCount()

```
status_t LPI2C_SlaveTransferGetCount (
             LPI2C_Type * base,
             lpi2c_slave_handle_t * handle,
             size_t * count )
```

Gets the slave transfer status during a non-blocking transfer.

Parameters

	base	The LPI2C peripheral base address.
	handle	Pointer to i2c_slave_handle_t structure.
out	*count*	Pointer to a value to hold the number of bytes transferred. May be NULL if the count is not required.

Return values

kStatus_Success	
kStatus_NoTransferInProgress	

16.6.4.20 LPI2C_SlaveTransferAbort()

```
void LPI2C_SlaveTransferAbort (
             LPI2C_Type * base,
             lpi2c_slave_handle_t * handle )
```

Aborts the slave non-blocking transfers.

Note

This API could be called at any time to stop slave for handling the bus events.

Parameters

base	The LPI2C peripheral base address.
handle	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.

Return values

kStatus_Success	
kStatus_LPI2C_Idle	

16.6.4.21 LPI2C_SlaveTransferHandleIRQ()

```
void LPI2C_SlaveTransferHandleIRQ (
            LPI2C_Type * base,
            lpi2c_slave_handle_t * handle )
```

Reusable routine to handle slave interrupts.

Note

This function does not need to be called unless you are reimplementing the non blocking API's interrupt handler routines to add special functionality.

Parameters

base	The LPI2C peripheral base address.
handle	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.

16.7 LPI2C Master DMA Driver

16.8 LPI2C FreeRTOS Driver

16.9 LPUART: Low Power Universal Asynchronous Receiver/Transmitter Driver

Modules

- LPUART Driver
- LPUART DMA Driver
- LPUART eDMA Driver
- LPUART FreeRTOS Driver

16.9.1 Detailed Description

16.10 LPUART Driver

Files

- file fsl_lpuart.h

Data Structures

- struct lpuart_config_t

  LPUART configuration structure.
- struct lpuart_transfer_t

  LPUART transfer structure.
- struct lpuart_handle_t

  LPUART handle structure.

Macros

- #define UART_RETRY_TIMES 0U /∗ Defining to zero means to keep waiting for the flag until it is assert/deassert. ∗/

  Retry times for waiting flag.

Typedefs

- typedef void(∗ lpuart_transfer_callback_t) (LPUART_Type ∗base, lpuart_handle_t ∗handle, status_t status, void ∗userData)

  LPUART transfer callback function.

Enumerations

- enum { kStatus_LPUART_TxBusy = MAKE_STATUS(kStatusGroup_LPUART, 0), kStatus_LPUART_RxBusy = MAKE↩ _STATUS(kStatusGroup_LPUART, 1), kStatus_LPUART_TxIdle = MAKE_STATUS(kStatusGroup_LPUART, 2), kStatus_LPUART_RxIdle = MAKE_STATUS(kStatusGroup_LPUART, 3), kStatus_LPUART_TxWatermarkTooLarge = MAKE_STATUS(kStatusGroup_LPUART, 4), kStatus_LPUART_RxWatermarkTooLarg = MAKE_STATUS(kStatusGroup_LPUART, 5), kStatus_LPUART_FlagCannotClearManually = MAKE_STAT↩ US(kStatusGroup_LPUART, 6), kStatus_LPUART_Error = MAKE_STATUS(kStatusGroup_LPUART, 7), kStatus_LPUART_RxRingBufferOverrun, kStatus_LPUART_RxHardwareOverrun = MAKE_STATUS(k↩ StatusGroup_LPUART, 9), kStatus_LPUART_NoiseError = MAKE_STATUS(kStatusGroup_LPUART, 10), kStatus_LPUART_FramingError = MAKE_STATUS(kStatusGroup_LPUART, 11), kStatus_LPUART_ParityError = MAKE_STATUS(kStatusGroup_LPUART, 12), kStatus_LPUART_BaudrateNotSupport, kStatus_LPUART_IdleLineDetected = MAKE_STATUS(kStatusGroup_LPUART, 14), kStatus_LPUART_Timeout = MAKE_STATUS(kStatusGroup_LPUART, 15) }

  Error codes for the LPUART driver.
- enum lpuart_parity_mode_t { kLPUART_ParityDisabled = 0x0U, kLPUART_ParityEven = 0x2U, kLPUART_ParityOdd = 0x3U }

  LPUART parity mode.

- enum lpuart_data_bits_t { kLPUART_EightDataBits = 0x0U }

  LPUART data bits count.
- enum lpuart_stop_bit_count_t { kLPUART_OneStopBit = 0U, kLPUART_TwoStopBit = 1U }

  LPUART stop bit count.
- enum lpuart_idle_type_select_t { kLPUART_IdleTypeStartBit = 0U, kLPUART_IdleTypeStopBit = 1U }

  LPUART idle flag type defines when the receiver starts counting.
- enum lpuart_idle_config_t {
  kLPUART_IdleCharacter1 = 0U, kLPUART_IdleCharacter2 = 1U, kLPUART_IdleCharacter4 = 2U, kLPUART_IdleCharacter8 = 3U,
  kLPUART_IdleCharacter16 = 4U, kLPUART_IdleCharacter32 = 5U, kLPUART_IdleCharacter64 = 6U, kLPUART_IdleCharacter128 = 7U }

  LPUART idle detected configuration.
- enum _lpuart_interrupt_enable {
  kLPUART_RxActiveEdgeInterruptEnable = (LPUART_BAUD_RXEDGIE_MASK >> 8), kLPUART_TxDataRegEmptyInterruptEnab = (LPUART_CTRL_TIE_MASK), kLPUART_TransmissionCompleteInterruptEnable = (LPUART_CTRL_TCIE_↩ MASK), kLPUART_RxDataRegFullInterruptEnable = (LPUART_CTRL_RIE_MASK),
  kLPUART_IdleLineInterruptEnable = (LPUART_CTRL_ILIE_MASK), kLPUART_RxOverrunInterruptEnable = (LPUART_CTRL_ORIE_MASK), kLPUART_NoiseErrorInterruptEnable = (LPUART_CTRL_NEIE_MASK), kLPUART_FramingErrorInterruptEnable = (LPUART_CTRL_FEIE_MASK),
  kLPUART_ParityErrorInterruptEnable = (LPUART_CTRL_PEIE_MASK) }

  LPUART interrupt configuration structure, default settings all disabled.
- enum _lpuart_flags {
  kLPUART_TxDataRegEmptyFlag, kLPUART_TransmissionCompleteFlag, kLPUART_RxDataRegFullFlag, kLPUART_IdleLineFlag = (LPUART_STAT_IDLE_MASK),
  kLPUART_RxOverrunFlag = (LPUART_STAT_OR_MASK), kLPUART_NoiseErrorFlag = (LPUART_STAT_N↩ F_MASK), kLPUART_FramingErrorFlag, kLPUART_ParityErrorFlag = (LPUART_STAT_PF_MASK),
  kLPUART_RxActiveEdgeFlag, kLPUART_RxActiveFlag }

  LPUART status flags.

Driver version

- #define FSL_LPUART_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))

  LPUART driver version 2.3.0.

Initialization and deinitialization

- status_t LPUART_Init (LPUART_Type *base, const lpuart_config_t *config, uint32_t srcClock_Hz)

  Initializes an LPUART instance with the user configuration structure and the peripheral clock.
- void LPUART_Deinit (LPUART_Type *base)

  Deinitializes a LPUART instance.
- void LPUART_GetDefaultConfig (lpuart_config_t *config)

  Gets the default configuration structure.
- status_t LPUART_SetBaudRate (LPUART_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)

  Sets the LPUART instance baudrate.

Status

- uint32_t LPUART_GetStatusFlags (LPUART_Type *base)

  Gets LPUART status flags.
- status_t LPUART_ClearStatusFlags (LPUART_Type *base, uint32_t mask)

  Clears status flags with a provided mask.

Interrupts

- void LPUART_EnableInterrupts (LPUART_Type *base, uint32_t mask)

  Enables LPUART interrupts according to a provided mask.
- void LPUART_DisableInterrupts (LPUART_Type *base, uint32_t mask)

  Disables LPUART interrupts according to a provided mask.
- uint32_t LPUART_GetEnabledInterrupts (LPUART_Type *base)

  Gets enabled LPUART interrupts.

Bus Operations

- uint32_t LPUART_GetInstance (LPUART_Type *base)

  Get the LPUART instance from peripheral base address.
- static void LPUART_EnableTx (LPUART_Type *base, bool enable)

  Enables or disables the LPUART transmitter.
- static void LPUART_EnableRx (LPUART_Type *base, bool enable)

  Enables or disables the LPUART receiver.
- static void LPUART_WriteByte (LPUART_Type *base, uint8_t data)

  Writes to the transmitter register.
- static uint8_t LPUART_ReadByte (LPUART_Type *base)

  Reads the receiver register.
- status_t LPUART_WriteBlocking (LPUART_Type *base, const uint8_t *data, size_t length)

  Writes to the transmitter register using a blocking method.
- status_t LPUART_ReadBlocking (LPUART_Type *base, uint8_t *data, size_t length)

  Reads the receiver data register using a blocking method.

Transactional

- void LPUART_TransferCreateHandle (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_callback_t callback, void *userData)

  Initializes the LPUART handle.
- status_t LPUART_TransferSendNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer)

  Transmits a buffer of data using the interrupt method.
- void LPUART_TransferStartRingBuffer (LPUART_Type *base, lpuart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)

  Sets up the RX ring buffer.
- void LPUART_TransferStopRingBuffer (LPUART_Type *base, lpuart_handle_t *handle)

  Aborts the background transfer and uninstalls the ring buffer.

- size_t LPUART_TransferGetRxRingBufferLength (LPUART_Type *base, lpuart_handle_t *handle)

  Get the length of received data in RX ring buffer.
- void LPUART_TransferAbortSend (LPUART_Type *base, lpuart_handle_t *handle)

  Aborts the interrupt-driven data transmit.
- status_t LPUART_TransferGetSendCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)

  Gets the number of bytes that have been sent out to bus.
- status_t LPUART_TransferReceiveNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer, size_t *receivedBytes)

  Receives a buffer of data using the interrupt method.
- void LPUART_TransferAbortReceive (LPUART_Type *base, lpuart_handle_t *handle)

  Aborts the interrupt-driven data receiving.
- status_t LPUART_TransferGetReceiveCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)

  Gets the number of bytes that have been received.
- void LPUART_TransferHandleIRQ (LPUART_Type *base, lpuart_handle_t *handle)

  LPUART IRQ handle function.
- void LPUART_TransferHandleErrorIRQ (LPUART_Type *base, lpuart_handle_t *handle)

  LPUART Error IRQ handle function.

16.10.1 Detailed Description

The MCUXpresso SDK provides a peripheral driver for the Low Power UART (LPUART) module of MCUXpresso SDK devices.

16.10.2 Typical use case

16.10.2.1 LPUART Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/lpuart

16.10.3 Enumeration Type Documentation

16.10.3.1 anonymous enum

```
anonymous enum
```

Error codes for the LPUART driver.

Enumerator

kStatus_LPUART_TxBusy	TX busy.
kStatus_LPUART_RxBusy	RX busy.
kStatus_LPUART_TxIdle	LPUART transmitter is idle.
kStatus_LPUART_RxIdle	LPUART receiver is idle.
kStatus_LPUART_TxWatermarkTooLarge	TX FIFO watermark too large

Enumerator

kStatus_LPUART_RxWatermarkTooLarge	RX FIFO watermark too large
kStatus_LPUART_FlagCannotClearManually	Some flag can't manually clear.
kStatus_LPUART_Error	Error happens on LPUART.
kStatus_LPUART_RxRingBufferOverrun	LPUART RX software ring buffer overrun.
kStatus_LPUART_RxHardwareOverrun	LPUART RX receiver overrun.
kStatus_LPUART_NoiseError	LPUART noise error.
kStatus_LPUART_FramingError	LPUART framing error.
kStatus_LPUART_ParityError	LPUART parity error.
kStatus_LPUART_BaudrateNotSupport	Baudrate is not support in current clock source.
kStatus_LPUART_IdleLineDetected	IDLE flag.
kStatus_LPUART_Timeout	LPUART times out.

16.10.3.2 lpuart_parity_mode_t

`enum lpuart_parity_mode_t`

LPUART parity mode.

Enumerator

kLPUART_ParityDisabled	Parity disabled.
kLPUART_ParityEven	Parity enabled, type even, bit setting: PE|PT = 10.
kLPUART_ParityOdd	Parity enabled, type odd, bit setting: PE|PT = 11.

16.10.3.3 lpuart_data_bits_t

`enum lpuart_data_bits_t`

LPUART data bits count.

Enumerator

kLPUART_EightDataBits	Eight data bit.

16.10.3.4 lpuart_stop_bit_count_t

`enum lpuart_stop_bit_count_t`

LPUART stop bit count.

Enumerator

kLPUART_OneStopBit	One stop bit.
kLPUART_TwoStopBit	Two stop bits.

16.10.3.5 lpuart_idle_type_select_t

`enum lpuart_idle_type_select_t`

LPUART idle flag type defines when the receiver starts counting.

Enumerator

kLPUART_IdleTypeStartBit	Start counting after a valid start bit.
kLPUART_IdleTypeStopBit	Start counting after a stop bit.

16.10.3.6 lpuart_idle_config_t

`enum lpuart_idle_config_t`

LPUART idle detected configuration.

This structure defines the number of idle characters that must be received before the IDLE flag is set.

Enumerator

kLPUART_IdleCharacter1	the number of idle characters.
kLPUART_IdleCharacter2	the number of idle characters.
kLPUART_IdleCharacter4	the number of idle characters.
kLPUART_IdleCharacter8	the number of idle characters.
kLPUART_IdleCharacter16	the number of idle characters.
kLPUART_IdleCharacter32	the number of idle characters.
kLPUART_IdleCharacter64	the number of idle characters.
kLPUART_IdleCharacter128	the number of idle characters.

16.10.3.7 _lpuart_interrupt_enable

`enum _lpuart_interrupt_enable`

LPUART interrupt configuration structure, default settings all disabled.

This structure contains the settings for all LPUART interrupt configurations.

Enumerator

kLPUART_RxActiveEdgeInterruptEnable	Receive Active Edge.
kLPUART_TxDataRegEmptyInterruptEnable	Transmit data register empty.
kLPUART_TransmissionCompleteInterruptEnable	Transmission complete.
kLPUART_RxDataRegFullInterruptEnable	Receiver data register full.
kLPUART_IdleLineInterruptEnable	Idle line.
kLPUART_RxOverrunInterruptEnable	Receiver Overrun.
kLPUART_NoiseErrorInterruptEnable	Noise error flag.
kLPUART_FramingErrorInterruptEnable	Framing error flag.
kLPUART_ParityErrorInterruptEnable	Parity error flag.

16.10.3.8 _lpuart_flags

```
enum _lpuart_flags
```

LPUART status flags.

This provides constants for the LPUART status flags for use in the LPUART functions.

Enumerator

kLPUART_TxDataRegEmptyFlag	Transmit data register empty flag, sets when transmit buffer is empty.
kLPUART_TransmissionCompleteFlag	Transmission complete flag, sets when transmission activity complete.
kLPUART_RxDataRegFullFlag	Receive data register full flag, sets when the receive data buffer is full.
kLPUART_IdleLineFlag	Idle line detect flag, sets when idle line detected.
kLPUART_RxOverrunFlag	Receive Overrun, sets when new data is received before data is read from receive register.
kLPUART_NoiseErrorFlag	Receive takes 3 samples of each received bit. If any of these samples differ, noise flag sets
kLPUART_FramingErrorFlag	Frame error flag, sets if logic 0 was detected where stop bit expected.
kLPUART_ParityErrorFlag	If parity enabled, sets upon parity error detection.
kLPUART_RxActiveEdgeFlag	Receive pin active edge interrupt flag, sets when active edge detected.
kLPUART_RxActiveFlag	Receiver Active Flag (RAF), sets at beginning of valid start bit.

16.10.4 Function Documentation

16.10.4.1 LPUART_Init()

```
status_t LPUART_Init (
            LPUART_Type * base,
```

```
            const lpuart_config_t * config,
            uint32_t srcClock_Hz )
```

Initializes an LPUART instance with the user configuration structure and the peripheral clock.

This function configures the LPUART module with user-defined settings. Call the LPUART_GetDefaultConfig() function to configure the configuration structure and get the default configuration. The example below shows how to use this API to configure the LPUART.

```
lpuart_config_t lpuartConfig;
lpuartConfig.baudRate_Bps = 115200U;
lpuartConfig.parityMode = kLPUART_ParityDisabled;
lpuartConfig.dataBitsCount = kLPUART_EightDataBits;
lpuartConfig.isMsb = false;
lpuartConfig.stopBitCount = kLPUART_OneStopBit;
lpuartConfig.txFifoWatermark = 0;
lpuartConfig.rxFifoWatermark = 1;
LPUART_Init(LPUART1, &lpuartConfig, 20000000U);
```

Parameters

base	LPUART peripheral base address.
config	Pointer to a user-defined configuration structure.
srcClock_Hz	LPUART clock source frequency in HZ.

Return values

kStatus_LPUART_BaudrateNotSupport	Baudrate is not support in current clock source.
kStatus_Success	LPUART initialize succeed

16.10.4.2 LPUART_Deinit()

```
void LPUART_Deinit (
            LPUART_Type * base )
```

Deinitializes a LPUART instance.

This function waits for transmit to complete, disables TX and RX, and disables the LPUART clock.

Parameters

base	LPUART peripheral base address.

Examples

board.c.

16.10.4.3 LPUART_GetDefaultConfig()

```
void LPUART_GetDefaultConfig (
             lpuart_config_t * config )
```

Gets the default configuration structure.

This function initializes the LPUART configuration structure to a default value. The default values are: lpuart↩Config->baudRate_Bps = 115200U; lpuartConfig->parityMode = kLPUART_ParityDisabled; lpuartConfig->dataBits↩Count = kLPUART_EightDataBits; lpuartConfig->isMsb = false; lpuartConfig->stopBitCount = kLPUART_OneStopBit; lpuartConfig->txFifoWatermark = 0; lpuartConfig->rxFifoWatermark = 1; lpuartConfig->rxIdleType = kLPUART_Idle↩TypeStartBit; lpuartConfig->rxIdleConfig = kLPUART_IdleCharacter1; lpuartConfig->enableTx = false; lpuartConfig->enableRx = false;

Parameters

config	Pointer to a configuration structure.

16.10.4.4 LPUART_SetBaudRate()

```
status_t LPUART_SetBaudRate (
             LPUART_Type * base,
             uint32_t baudRate_Bps,
             uint32_t srcClock_Hz )
```

Sets the LPUART instance baudrate.

This function configures the LPUART module baudrate. This function is used to update the LPUART module baudrate after the LPUART module is initialized by the LPUART_Init.

```
LPUART_SetBaudRate(LPUART1, 115200U, 20000000U);
```

Parameters

base	LPUART peripheral base address.
baudRate_Bps	LPUART baudrate to be set.
srcClock_Hz	LPUART clock source frequency in HZ.

Return values

kStatus_LPUART_BaudrateNotSupport	Baudrate is not supported in the current clock source.
kStatus_Success	Set baudrate succeeded.

16.10.4.5 LPUART_GetStatusFlags()

```
uint32_t LPUART_GetStatusFlags (
             LPUART_Type * base )
```

Gets LPUART status flags.

This function gets all LPUART status flags. The flags are returned as the logical OR value of the enumerators _lpuart_flags. To check for a specific status, compare the return value with enumerators in the _lpuart_flags. For example, to check whether the TX is empty:

```
if (kLPUART_TxDataRegEmptyFlag & LPUART_GetStatusFlags(LPUART1))
{
    ...
}
```

Parameters

base	LPUART peripheral base address.

Returns

LPUART status flags which are ORed by the enumerators in the _lpuart_flags.

16.10.4.6 LPUART_ClearStatusFlags()

```
status_t LPUART_ClearStatusFlags (
             LPUART_Type * base,
             uint32_t mask )
```

Clears status flags with a provided mask.

This function clears LPUART status flags with a provided mask. Automatically cleared flags can't be cleared by this function. Flags that can only cleared or set by hardware are: kLPUART_TxDataRegEmptyFlag, kLPU↩ ART_TransmissionCompleteFlag, kLPUART_RxDataRegFullFlag, kLPUART_RxActiveFlag, kLPUART_NoiseError↩ InRxDataRegFlag, kLPUART_ParityErrorInRxDataRegFlag, kLPUART_TxFifoEmptyFlag,kLPUART_RxFifoEmptyFlag Note: This API should be called when the Tx/Rx is idle, otherwise it takes no effects.

Parameters

base	LPUART peripheral base address.
mask	the status flags to be cleared. The user can use the enumerators in the _lpuart_status_flag_t to do the OR operation and get the mask.

Returns

0 succeed, others failed.

Return values

kStatus_LPUART_FlagCannotClearManually	The flag can't be cleared by this function but it is cleared automatically by hardware.
kStatus_Success	Status in the mask are cleared.

16.10.4.7 LPUART_EnableInterrupts()

```
void LPUART_EnableInterrupts (
             LPUART_Type * base,
             uint32_t mask )
```

Enables LPUART interrupts according to a provided mask.

This function enables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See the _lpuart_interrupt_enable. This examples shows how to enable TX empty interrupt and RX full interrupt:

```
LPUART_EnableInterrupts(LPUART1,kLPUART_TxDataRegEmptyInterruptEnable | kLPUART_RxDataRegFullInterruptEnable);
```

Parameters

base	LPUART peripheral base address.
mask	The interrupts to enable. Logical OR of the enumeration _uart_interrupt_enable.

16.10.4.8 LPUART_DisableInterrupts()

```
void LPUART_DisableInterrupts (
             LPUART_Type * base,
             uint32_t mask )
```

Disables LPUART interrupts according to a provided mask.

This function disables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See _lpuart_interrupt_enable. This example shows how to disable the TX empty interrupt and RX full interrupt:

```
LPUART_DisableInterrupts(LPUART1,kLPUART_TxDataRegEmptyInterruptEnable | kLPUART_RxDataRegFullInterruptEnable);
```

Parameters

base	LPUART peripheral base address.
mask	The interrupts to disable. Logical OR of _lpuart_interrupt_enable.

16.10.4.9 LPUART_GetEnabledInterrupts()

```
uint32_t LPUART_GetEnabledInterrupts (
             LPUART_Type * base )
```

Gets enabled LPUART interrupts.

This function gets the enabled LPUART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators _lpuart_interrupt_enable. To check a specific interrupt enable status, compare the return value with enumerators in _lpuart_interrupt_enable. For example, to check whether the TX empty interrupt is enabled:

```
uint32_t enabledInterrupts = LPUART_GetEnabledInterrupts(LPUART1);
if (kLPUART_TxDataRegEmptyInterruptEnable & enabledInterrupts)
{
    ...
}
```

Parameters

base	LPUART peripheral base address.

Returns

LPUART interrupt flags which are logical OR of the enumerators in _lpuart_interrupt_enable.

16.10.4.10 LPUART_GetInstance()

```
uint32_t LPUART_GetInstance (
             LPUART_Type * base )
```

Get the LPUART instance from peripheral base address.

Parameters

base	LPUART peripheral base address.

Returns

LPUART instance.

16.10.4.11 LPUART_EnableTx()

```
static void LPUART_EnableTx (
             LPUART_Type * base,
             bool enable )  [inline], [static]
```

Enables or disables the LPUART transmitter.

This function enables or disables the LPUART transmitter.

Parameters

base	LPUART peripheral base address.
enable	True to enable, false to disable.

16.10.4.12 LPUART_EnableRx()

```
static void LPUART_EnableRx (
            LPUART_Type * base,
            bool enable )  [inline], [static]
```

Enables or disables the LPUART receiver.

This function enables or disables the LPUART receiver.

Parameters

base	LPUART peripheral base address.
enable	True to enable, false to disable.

16.10.4.13 LPUART_WriteByte()

```
static void LPUART_WriteByte (
            LPUART_Type * base,
            uint8_t data )  [inline], [static]
```

Writes to the transmitter register.

This function writes data to the transmitter register directly. The upper layer must ensure that the TX register is empty or that the TX FIFO has room before calling this function.

Parameters

base	LPUART peripheral base address.
data	Data write to the TX register.

16.10.4.14 LPUART_ReadByte()

```
static uint8_t LPUART_ReadByte (
            LPUART_Type * base )  [inline], [static]
```

Reads the receiver register.

This function reads data from the receiver register directly. The upper layer must ensure that the receiver register is full or that the RX FIFO has data before calling this function.

Parameters

base	LPUART peripheral base address.

Returns

Data read from data register.

16.10.4.15 LPUART_WriteBlocking()

```
status_t LPUART_WriteBlocking (
             LPUART_Type * base,
             const uint8_t * data,
             size_t length )
```

Writes to the transmitter register using a blocking method.

This function polls the transmitter register, first waits for the register to be empty or TX FIFO to have room, and writes data to the transmitter buffer, then waits for the dat to be sent out to the bus.

Parameters

base	LPUART peripheral base address.
data	Start address of the data to write.
length	Size of the data to write.

Return values

kStatus_LPUART_Timeout	Transmission timed out and was aborted.
kStatus_Success	Successfully wrote all data.

16.10.4.16 LPUART_ReadBlocking()

```
status_t LPUART_ReadBlocking (
             LPUART_Type * base,
             uint8_t * data,
             size_t length )
```

Reads the receiver data register using a blocking method.

This function polls the receiver register, waits for the receiver register full or receiver FIFO has data, and reads data from the TX register.

Parameters

base	LPUART peripheral base address.
data	Start address of the buffer to store the received data.
length	Size of the buffer.

Return values

kStatus_LPUART_RxHardwareOverrun	Receiver overrun happened while receiving data.
kStatus_LPUART_NoiseError	Noise error happened while receiving data.
kStatus_LPUART_FramingError	Framing error happened while receiving data.
kStatus_LPUART_ParityError	Parity error happened while receiving data.
kStatus_LPUART_Timeout	Transmission timed out and was aborted.
kStatus_Success	Successfully received all data.

16.10.4.17 LPUART_TransferCreateHandle()

```
void LPUART_TransferCreateHandle (
             LPUART_Type * base,
             lpuart_handle_t * handle,
             lpuart_transfer_callback_t callback,
             void * userData )
```

Initializes the LPUART handle.

This function initializes the LPUART handle, which can be used for other LPUART transactional APIs. Usually, for a specified LPUART instance, call this API once to get the initialized handle.

The LPUART driver supports the "background" receiving, which means that user can set up an RX ring buffer optionally. Data received is stored into the ring buffer even when the user doesn't call the LPUART_TransferReceiveNonBlocking() API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly. The ring buffer is disabled if passing NULL as `ringBuffer`.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.
callback	Callback function.
userData	User data.

16.10.4.18 LPUART_TransferSendNonBlocking()

```
status_t LPUART_TransferSendNonBlocking (
             LPUART_Type * base,
```

```
            lpuart_handle_t * handle,
            lpuart_transfer_t * xfer )
```

Transmits a buffer of data using the interrupt method.

This function send data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data written to the transmitter register. When all data is written to the TX register in the ISR, the LPUART driver calls the callback function and passes the kStatus_LPUART_TxIdle as status parameter.

Note

The kStatus_LPUART_TxIdle is passed to the upper layer when all data are written to the TX register. However, there is no check to ensure that all the data sent out. Before disabling the TX, check the kLPUART_Transmission↩ CompleteFlag to ensure that the transmit is finished.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.
xfer	LPUART transfer structure, see lpuart_transfer_t.

Return values

kStatus_Success	Successfully start the data transmission.
kStatus_LPUART_TxBusy	Previous transmission still not finished, data not all written to the TX register.
kStatus_InvalidArgument	Invalid argument.

16.10.4.19 LPUART_TransferStartRingBuffer()

```
void LPUART_TransferStartRingBuffer (
            LPUART_Type * base,
            lpuart_handle_t * handle,
            uint8_t * ringBuffer,
            size_t ringBufferSize )
```

Sets up the RX ring buffer.

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received is stored into the ring buffer even when the user doesn't call the UAR↩ T_TransferReceiveNonBlocking() API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly.

Note

When using RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, then only 31 bytes are used for saving data.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.
ringBuffer	Start address of ring buffer for background receiving. Pass NULL to disable the ring buffer.
ringBufferSize	size of the ring buffer.

16.10.4.20 LPUART_TransferStopRingBuffer()

```
void LPUART_TransferStopRingBuffer (
             LPUART_Type * base,
             lpuart_handle_t * handle )
```

Aborts the background transfer and uninstalls the ring buffer.

This function aborts the background transfer and uninstalls the ring buffer.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.

16.10.4.21 LPUART_TransferGetRxRingBufferLength()

```
size_t LPUART_TransferGetRxRingBufferLength (
             LPUART_Type * base,
             lpuart_handle_t * handle )
```

Get the length of received data in RX ring buffer.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.

Returns

Length of received data in RX ring buffer.

16.10.4.22 LPUART_TransferAbortSend()

```
void LPUART_TransferAbortSend (
             LPUART_Type * base,
             lpuart_handle_t * handle )
```

Aborts the interrupt-driven data transmit.

This function aborts the interrupt driven data sending. The user can get the remainBtyes to find out how many bytes are not sent out.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.

16.10.4.23 LPUART_TransferGetSendCount()

```
status_t LPUART_TransferGetSendCount (
             LPUART_Type * base,
             lpuart_handle_t * handle,
             uint32_t * count )
```

Gets the number of bytes that have been sent out to bus.

This function gets the number of bytes that have been sent out to bus by an interrupt method.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.
count	Send bytes count.

Return values

kStatus_NoTransferInProgress	No send in progress.
kStatus_InvalidArgument	Parameter is invalid.
kStatus_Success	Get successfully through the parameter `count;`

16.10.4.24 LPUART_TransferReceiveNonBlocking()

```
status_t LPUART_TransferReceiveNonBlocking (
             LPUART_Type * base,
```

```
            lpuart_handle_t * handle,
            lpuart_transfer_t * xfer,
            size_t * receivedBytes )
```

Receives a buffer of data using the interrupt method.

This function receives data using an interrupt method. This is a non-blocking function which returns without waiting to ensure that all data are received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter `receivedBytes` shows how many bytes are copied from the ring buffer. After copying, if the data in the ring buffer is not enough for read, the receive request is saved by the LPUART driver. When the new data arrives, the receive request is serviced first. When all data is received, the LPUART driver notifies the upper layer through a callback function and passes a status parameter kStatus_UART_RxIdle. For example, the upper layer needs 10 bytes but there are only 5 bytes in ring buffer. The 5 bytes are copied to xfer->data, which returns with the parameter `receivedBytes` set to 5. For the remaining 5 bytes, the newly arrived data is saved from xfer->data[5]. When 5 bytes are received, the LPUART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to xfer->data. When all data is received, the upper layer is notified.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.
xfer	LPUART transfer structure, see uart_transfer_t.
receivedBytes	Bytes received from the ring buffer directly.

Return values

kStatus_Success	Successfully queue the transfer into the transmit queue.
kStatus_LPUART_RxBusy	Previous receive request is not finished.
kStatus_InvalidArgument	Invalid argument.

16.10.4.25 LPUART_TransferAbortReceive()

```
void LPUART_TransferAbortReceive (
            LPUART_Type * base,
            lpuart_handle_t * handle )
```

Aborts the interrupt-driven data receiving.

This function aborts the interrupt-driven data receiving. The user can get the remainBytes to find out how many bytes not received yet.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.

16.10.4.26 LPUART_TransferGetReceiveCount()

```
status_t LPUART_TransferGetReceiveCount (
             LPUART_Type * base,
             lpuart_handle_t * handle,
             uint32_t * count )
```

Gets the number of bytes that have been received.

This function gets the number of bytes that have been received.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.
count	Receive bytes count.

Return values

kStatus_NoTransferInProgress	No receive in progress.
kStatus_InvalidArgument	Parameter is invalid.
kStatus_Success	Get successfully through the parameter `count`;

16.10.4.27 LPUART_TransferHandleIRQ()

```
void LPUART_TransferHandleIRQ (
             LPUART_Type * base,
             lpuart_handle_t * handle )
```

LPUART IRQ handle function.

This function handles the LPUART transmit and receive IRQ request.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.

16.10.4.28 LPUART_TransferHandleErrorIRQ()

```
void LPUART_TransferHandleErrorIRQ (
             LPUART_Type * base,
             lpuart_handle_t * handle )
```

LPUART Error IRQ handle function.

This function handles the LPUART error IRQ request.

Parameters

base	LPUART peripheral base address.
handle	LPUART handle pointer.

16.11 LPUART DMA Driver

16.12 LPUART eDMA Driver

16.13 LPUART FreeRTOS Driver

16.14 PMIC: Power Management IC Driver

Module for the PMIC driver.

Files

- file fsl_pmic.h

Data Structures

- struct pmic_version_t

  Structure for ID and Revision of PMIC.

Macros

- #define **PMIC_SET_VOLTAGE** dynamic_pmic_set_voltage
- #define **PMIC_GET_VOLTAGE** dynamic_pmic_get_voltage
- #define **PMIC_SET_MODE** dynamic_pmic_set_mode
- #define **PMIC_GET_MODE** dynamic_pmic_get_mode
- #define **PMIC_IRQ_SERVICE** dynamic_pmic_irq_service
- #define **PMIC_REGISTER_ACCESS** dynamic_pmic_register_access
- #define **GET_PMIC_VERSION** dynamic_get_pmic_version
- #define **GET_PMIC_TEMP** dynamic_get_pmic_temp
- #define **SET_PMIC_TEMP_ALARM** dynamic_set_pmic_temp_alarm
- #define **i2c_error_flags**

Typedefs

- typedef uint8_t pmic_id_t

  This type is used to declare which PMIC to address.

Functions

- sc_err_t dynamic_pmic_set_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t vol_mv, uint32_t mode_to_set)

  This function sets the voltage of a corresponding voltage regulator for the supported PMIC types.
- sc_err_t dynamic_pmic_get_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t *vol_mv, uint32_t mode_to_get)

  This function gets the voltage on a corresponding voltage regulator of the PMIC.
- sc_err_t dynamic_pmic_set_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t mode)

  This function sets the mode of the specified regulator.
- sc_err_t dynamic_pmic_get_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t *mode)

  This function gets the mode of the specified regulator.
- sc_bool_t dynamic_pmic_irq_service (pmic_id_t id)

  This function services the interrupt for the temp alarm.
- sc_err_t dynamic_pmic_register_access (pmic_id_t id, uint32_t address, sc_bool_t read_write, uint8_t *value)

  This function allows access to individual registers of the PMIC.

- pmic_version_t dynamic_get_pmic_version (pmic_id_t id)

  This function returns the device ID and revision for the PMIC.
- uint32_t dynamic_get_pmic_temp (pmic_id_t id)

  This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.
- uint32_t dynamic_set_pmic_temp_alarm (pmic_id_t id, uint32_t temp)

  This function sets the temp alarm for the PMIC in Celsius.
- status_t i2c_write_sub (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function is a simple write to an i2c register on the PMIC.
- status_t i2c_write (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function writes an i2c register on the PMIC device with clock management.
- status_t i2c_read_sub (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function is a simple read of an i2c register on the PMIC.
- status_t i2c_read (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function reads an i2c register on the PMIC device with clock management.
- status_t i2c_j1850_write (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function writes an i2c register on the PMIC device with j1850 CRC appended and clock management.
- status_t i2c_j1850_read (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function reads an i2c register on the PMIC device with j1850 CRC and clock management.
- uint8_t pmic_get_device_id (uint8_t address)

  This function reads the register at address 0x0 for the Device ID.

Variables

- uint8_t PMIC_TYPE

  Global PMIC type identifier.

Defines for supported PMIC devices

- #define **PMIC_NONE** 0U
- #define **PF100** 1U
- #define **PF8100** 2U
- #define **PF8200** 3U

Defines for PMIC configuration

- #define **PF100_DEV_ID** 0x10U
- #define **PF8100_DEV_ID** 0x40U
- #define **PF8200_DEV_ID** 0x48U
- #define **PF8X00_FAM_ID** 0x40U
- #define **PF7X00_FAM_ID** 0x80U
- #define **PF8100_A0_REV** 0x10U
- #define **FAM_ID_MASK** 0xF0U

16.14.1 Detailed Description

Module for the PMIC driver.

It is an SDK driver for the PMIC module of i.MX devices. PMIC users shoud not call the PMIC driver functions directly. Instead, use the PMIC access macros. This allows for quick PMIC change and dynamic PMIC binding.

16.14.2 Macro Definition Documentation

16.14.2.1 i2c_error_flags

```
#define i2c_error_flags
```

Value:

```
(U32(kLPI2C_MasterArbitrationLostFlag) |        \
                                    U32(kLPI2C_MasterFifoErrFlag) |                \
                                    U32(kLPI2C_MasterPinLowTimeoutFlag) |          \
                                    U32(kLPI2C_MasterDataMatchFlag) |              \
                                    U32(kLPI2C_MasterBusyFlag) |                   \
                                    U32(kLPI2C_MasterBusBusyFlag))
```

16.14.3 Function Documentation

16.14.3.1 dynamic_pmic_set_voltage()

```
sc_err_t dynamic_pmic_set_voltage (
             pmic_id_t id,
             uint32_t pmic_reg,
             uint32_t vol_mv,
             uint32_t mode_to_set )
```

This function sets the voltage of a corresponding voltage regulator for the supported PMIC types.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator e.g pf8100_vregs_t
in	*vol_mv*	New voltage setpoint for the regulator in millivolts
in	*mode_to_set*	Which mode to change setpoint for. Refer to each PMIC for valid modes

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters

- SC_ERR_FAIL if writing the register failed

16.14.3.2 dynamic_pmic_get_voltage()

```
sc_err_t dynamic_pmic_get_voltage (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t * vol_mv,
            uint32_t mode_to_get )
```

This function gets the voltage on a corresponding voltage regulator of the PMIC.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator e.g pf8100_vregs_t
out	*vol_mv*	pointer to return voltage in millivolts
in	*mode_to_get*	Mode for which to get the voltage. Refer to each PMIC for valid modes.

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters

16.14.3.3 dynamic_pmic_set_mode()

```
sc_err_t dynamic_pmic_set_mode (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t mode )
```

This function sets the mode of the specified regulator.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; e.g pf8100_vregs_t
in	*mode*	mode to set the regulator; Refer to each PMIC for valid modes.

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.14.3.4 dynamic_pmic_get_mode()

```
sc_err_t dynamic_pmic_get_mode (
             pmic_id_t id,
             uint32_t pmic_reg,
             uint32_t * mode )
```

This function gets the mode of the specified regulator.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; e.g pf8100_vregs_t
in	*mode*	pointer to return mode in raw hex form

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.14.3.5 dynamic_pmic_irq_service()

```
sc_bool_t dynamic_pmic_irq_service (
             pmic_id_t id )
```

This function services the interrupt for the temp alarm.

Parameters

in	*id*	I2C address of PMIC device

Returns

Returns SC_TRUE if there was a temperature interrupt to be cleared

16.14.3.6 dynamic_pmic_register_access()

```
sc_err_t dynamic_pmic_register_access (
            pmic_id_t id,
            uint32_t address,
            sc_bool_t read_write,
            uint8_t * value )
```

This function allows access to individual registers of the PMIC.

Parameters

in	*id*	I2C address of PMIC device
in	*address*	register address to access
in	*read_write*	bool indicating read(SC_FALSE/0) or write(SC_TRUE/1)
in,out	*value*	value to read or to set

Returns

Returns ar error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters

16.14.3.7 dynamic_get_pmic_version()

```
pmic_version_t dynamic_get_pmic_version (
            pmic_id_t id )
```

This function returns the device ID and revision for the PMIC.

Parameters

in	*id*	I2C address of PMIC device

Returns

Returns a structure with the device ID and revision.

16.14.3.8 dynamic_get_pmic_temp()

```
uint32_t dynamic_get_pmic_temp (
            pmic_id_t id )
```

This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.

Parameters

in	*id*	I2C address of PMIC device

Returns

returns the temp sensed by the PMIC in a UINT32 in Celsius

Note: Refer to Refer to each PMIC for temperature details

Return errors:

- SC_ERR_CONFIG if temperature monitor is not enabled

16.14.3.9 dynamic_set_pmic_temp_alarm()

```
uint32_t dynamic_set_pmic_temp_alarm (
            pmic_id_t id,
            uint32_t temp )
```

This function sets the temp alarm for the PMIC in Celsius.

Parameters

in	*id*	I2C address of PMIC device
in	*temp*	Temperature to set the alarm

Note: Refer to Refer to each PMIC for temperature details

Returns

Returns the temperature that the alarm is set to in Celsius

16.14.3.10 i2c_write_sub()

```
status_t i2c_write_sub (
            uint8_t device_addr,
            uint8_t reg,
            void * data,
            uint32_t dataLength )
```

This function is a simple write to an i2c register on the PMIC.

Parameters

in	*device_addr*	I2C address of device
in	*reg*	address of register on device
in	*data*	data to be written
in	*dataLength*	length of data to be written

Returns

Returns the status of the write (success = kStatus_Success)

Return errors

- kStatus_Fail if any of the transactions failed

Note there is no clock management in this function

16.14.3.11 i2c_write()

```
status_t i2c_write (
            uint8_t device_addr,
            uint8_t reg,
            void * data,
            uint32_t dataLength )
```

This function writes an i2c register on the PMIC device with clock management.

Parameters

in	*device_addr*	I2C address of device
in	*reg*	address of register on device
in	*data*	data to be written
in	*dataLength*	length of data to be written

Returns

Returns the status of the write (success = kStatus_Success)

Return errors

- kStatus_Fail if any of the transactions failed

16.14.3.12 i2c_read_sub()

```
status_t i2c_read_sub (
            uint8_t device_addr,
            uint8_t reg,
            void * data,
            uint32_t dataLength )
```

This function is a simple read of an i2c register on the PMIC.

Parameters

in	*device_addr*	I2C address of device
in	*reg*	address of register on device
out	*data*	data to be read
in	*dataLength*	length of data to be read

Returns

Returns the status of the read (success = kStatus_Success)

Return errors

- kStatus_Fail if any of the transactions failed

16.14.3.13 i2c_read()

```
status_t i2c_read (
            uint8_t device_addr,
            uint8_t reg,
            void * data,
            uint32_t dataLength )
```

This function reads an i2c register on the PMIC device with clock management.

Parameters

in	*device_addr*	I2C address of device
in	*reg*	address of register on device
out	*data*	data to be read
in	*dataLength*	length of data to be read

Returns

Returns the status of the read (success = kStatus_Success)

Return errors

- kStatus_Fail if any of the transactions failed

16.14.3.14 i2c_j1850_write()

```
status_t i2c_j1850_write (
            uint8_t device_addr,
            uint8_t reg,
            void * data,
            uint32_t dataLength )
```

This function writes an i2c register on the PMIC device with j1850 CRC appended and clock management.

Parameters

in	*device_addr*	I2C address of device
in	*reg*	address of register on device
in	*data*	data to be written
in	*dataLength*	length of data to be written

Returns

Returns the status of the write (success = kStatus_Success)

Return errors

- kStatus_Fail if any of the transactions failed

16.14.3.15 i2c_j1850_read()

```
status_t i2c_j1850_read (
            uint8_t device_addr,
            uint8_t reg,
            void * data,
            uint32_t dataLength )
```

This function reads an i2c register on the PMIC device with j1850 CRC and clock management.

Parameters

in	*device_addr*	I2C address of device
in	*reg*	address of register on device
out	*data*	data to be read
in	*dataLength*	length of data to be read

Returns

Returns the status of the read (success = kStatus_Success)

Return errors

- kStatus_Fail if any of the transactions failed

16.14.3.16 pmic_get_device_id()

```
uint8_t pmic_get_device_id (
            uint8_t address )
```

This function reads the register at address 0x0 for the Device ID.

Parameters

in	*address*	I2C address of device

Returns

Returns the device ID

Return Errors

- 0 if any error in the function

16.15 PF100: PF100 Power Management IC Driver

Module for the PF100 PMIC driver.

Files

- file fsl_pf100.h

Typedefs

- typedef uint8_t pf100_vol_regs_t

  This type is used to indicate which register to address.
- typedef uint8_t sw_pmic_mode_t

  This type is used to indicate a switching regulator mode.
- typedef uint8_t vgen_pmic_mode_t

  This type is used to indicate a VGEN (LDO) regulator mode.
- typedef uint8_t sw_vmode_reg_t

  This type encodes which voltage mode register to set when calling pf100_pmic_set_voltage().

Functions

- pmic_version_t pf100_get_pmic_version (pmic_id_t id)

  This function returns the device ID and revision for the PF100 PMIC.
- sc_err_t pf100_pmic_set_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t vol_mv, uint32_t mode_to_set)

  This function sets the voltage of a corresponding voltage regulator for the PF100 PMIC.
- sc_err_t pf100_pmic_get_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t *vol_mv, uint32_t mode_to_get)

  This function gets the voltage on a corresponding voltage regulator for the PF100 PMIC.
- sc_err_t pf100_pmic_set_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t mode)

  This function sets the mode of the specified regulator.
- uint32_t pf100_get_pmic_temp (pmic_id_t id)

  This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.
- uint32_t pf100_set_pmic_temp_alarm (pmic_id_t id, uint32_t temp)

  This function sets the temp alarm for the PMIC in Celsius.
- sc_err_t **pf100_pmic_register_access** (pmic_id_t id, uint32_t address, sc_bool_t read_write, uint8_t *value)
- sc_bool_t pf100_pmic_irq_service (pmic_id_t id)

  This function services the interrupt for the temp alarm.

Defines for pf100_vol_regs_t

- #define SW1AB 0x20U

  Base register for SW1AB control.
- #define SW1C 0x2EU

  Base register for SW1C control.
- #define SW2 0x35U

  Base register for SW2 control.
- #define SW3A 0x3cU

  Base register for SW3A control.
- #define SW3B 0x43U

  Base register for SW3B control.
- #define SW4 0x4AU

  Base register for SW4 control.
- #define VGEN1 0x6CU

  Base register for VGEN1 control.
- #define VGEN2 0x6DU

  Base register for VGEN2 control.
- #define VGEN3 0x6EU

  Base register for VGEN3 control.
- #define VGEN4 0x6FU

  Base register for VGEN4 control.
- #define VGEN5 0x70U

  Base register for VGEN5 control.
- #define VGEN6 0x71U

  Base register for VGEN6 control.

Defines for sw_pmic_mode_t

- #define SW_MODE_OFF_STBY_OFF 0x0U

  Normal Mode: OFF, Standby Mode: OFF

- #define SW_MODE_PWM_STBY_OFF 0x1U

  Normal Mode: PWM, Standby Mode: OFF

- #define SW_MODE_PFM_STBY_OFF 0x3U

  Normal Mode: PFM, Standby Mode: OFF

- #define SW_MODE_APS_STBY_OFF 0x4U

  Normal Mode: APS, Standby Mode: OFF

- #define SW_MODE_PWM_STBY_PWM 0x5U

  Normal Mode: PWM, Standby Mode: PWM

- #define SW_MODE_PWM_STBY_APS 0x6U

  Normal Mode: PWM, Standby Mode: APS

- #define SW_MODE_APS_STBY_APS 0x8U

Normal Mode: APS, Standby Mode: APS

- #define SW_MODE_APS_STBY_PFM 0xCU
  Normal Mode: APS, Standby Mode: PFM
- #define SW_MODE_PWM_STBY_PFM 0xDU
  Normal Mode: PWM, Standby Mode: PFM

Defines for vgen_pmic_mode_t

- #define VGEN_MODE_OFF (0x0U << 4U)
  VGEN always OFF.
- #define VGEN_MODE_ON (0x1U << 4U)
  VGEN always ON
- #define VGEN_MODE_STBY_OFF (0x3U << 4U)
  VGEN Run: ON STBY: OFF.
- #define VGEN_MODE_LP (0x5U << 4U)
  VGEN Run: LPWR STBY: LPWR.
- #define VGEN_MODE_LP2 (0x7U << 4U)
  VGEN Run: LPWR STBY: LPWR.

Defines for sw_vmode_reg_t

- #define SW_RUN_MODE 0U
  SW run mode voltage
- #define SW_STBY_MODE 1U
  SW standby mode voltage.
- #define SW_OFF_MODE 2U
  SW off/sleep mode voltage.

16.15.1 Detailed Description

Module for the PF100 PMIC driver.

This is an SDK driver for the NXP PF100 PMIC. For more information, see the PF100 Datasheet.

16.15.2 Typedef Documentation

16.15.2.1 pf100_vol_regs_t

```
typedef uint8_t pf100_vol_regs_t
```

This type is used to indicate which register to address.

Refer to the PF100 Datasheet for the description of regsiter.

16.15.2.2 sw_pmic_mode_t

```
typedef uint8_t sw_pmic_mode_t
```

This type is used to indicate a switching regulator mode.

Refer to the PF100 Datasheet for the description of each mode.

16.15.2.3 vgen_pmic_mode_t

```
typedef uint8_t vgen_pmic_mode_t
```

This type is used to indicate a VGEN (LDO) regulator mode.

Refer to the LDO control register description in the PF100 Datasheet for possible mode combinations.

16.15.2.4 sw_vmode_reg_t

```
typedef uint8_t sw_vmode_reg_t
```

This type encodes which voltage mode register to set when calling pf100_pmic_set_voltage().

Possible modes are Run, Standby and Off/Sleep.

16.15.3 Function Documentation

16.15.3.1 pf100_get_pmic_version()

```
pmic_version_t pf100_get_pmic_version (
            pmic_id_t id )
```

This function returns the device ID and revision for the PF100 PMIC.

Parameters

in	*id*	I2C address of PMIC device

Returns

Returns a structure with the device ID and revision.

16.15.3.2 pf100_pmic_set_voltage()

```
sc_err_t pf100_pmic_set_voltage (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t vol_mv,
            uint32_t mode_to_set )
```

This function sets the voltage of a corresponding voltage regulator for the PF100 PMIC.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf100_vol_regs_t
in	*vol_mv*	New voltage setpoint for the regulator in millivolts
in	*mode_to_set*	Mode to set the voltage for run, standby and off; only applicable to switching regulators, ignored otherwise; see sw_vmode_reg_t

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.15.3.3 pf100_pmic_get_voltage()

```
sc_err_t pf100_pmic_get_voltage (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t * vol_mv,
            uint32_t mode_to_get )
```

This function gets the voltage on a corresponding voltage regulator for the PF100 PMIC.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf8100_vregs_t
out	*vol_mv*	pointer to return voltage in millivolts
in	*mode_to_get*	Mode to get the voltage for run, standby and off; only applicable to switching regulators, ignored otherwise; see sw_vmode_reg_t

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters

16.15.3.4 pf100_pmic_set_mode()

```
sc_err_t pf100_pmic_set_mode (
             pmic_id_t id,
             uint32_t pmic_reg,
             uint32_t mode )
```

This function sets the mode of the specified regulator.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf100_vol_regs_t
in	*mode*	mode to set the regulator; see vgen_pmic_mode_t and sw_pmic_mode_t

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.15.3.5 pf100_get_pmic_temp()

```
uint32_t pf100_get_pmic_temp (
             pmic_id_t id )
```

This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.

Parameters

in	*id*	I2C address of PMIC device

Returns

returns the temp sensed by the PMIC in a UINT32 in Celsius

Return errors:

- SC_ERR_CONFIG if temperature monitor is not enabled

Note PMIC PF100 temp is returned as the highest temp sensor enabled.

16.15.3.6 pf100_set_pmic_temp_alarm()

```
uint32_t pf100_set_pmic_temp_alarm (
            pmic_id_t id,
            uint32_t temp )
```

This function sets the temp alarm for the PMIC in Celsius.

Parameters

in	*id*	I2C address of PMIC device
in	*temp*	Temperature to set the alarm

Note the granularity for PF100 PMIC only allows the following values: 110 120 125 130 135

Returns

Returns the temperature that the alarm is set to in Celsius

16.15.3.7 pf100_pmic_irq_service()

```
sc_bool_t pf100_pmic_irq_service (
            pmic_id_t id )
```

This function services the interrupt for the temp alarm.

Parameters

in	*id*	I2C address of PMIC device

Returns

Returns SC_TRUE if there was a temperature interrupt to be cleared

16.16 PF8100: PF8100 Power Management IC Driver

Module for the PF8100 PMIC driver.

Files

- file fsl_pf8100.h

Macros

- #define **I2C_WRITE** i2c_write
- #define **I2C_READ** i2c_read

Typedefs

- typedef uint8_t pf8100_vregs_t

  This type is used to indicate which register to address.
- typedef uint8_t sw_mode_t

  This type is used to indicate a switching regulator mode.
- typedef uint8_t ldo_mode_t

  This type is used to indicate an LDO regulator mode.
- typedef uint8_t vmode_reg_t

  This type is used to indicate a Switching regulator voltage setpoint.

Functions

- pmic_version_t pf8100_get_pmic_version (pmic_id_t id)

  This function returns the device ID and revision for the PF8100 PMIC.
- sc_err_t pf8100_pmic_set_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t vol_mv, uint32_t mode_to_set)

  This function sets the voltage of a corresponding voltage regulator for the PF8100 PMIC.
- sc_err_t pf8100_pmic_get_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t *vol_mv, uint32_t mode_to_get)

  This function gets the voltage on a corresponding voltage regulator for the PF8100 PMIC.
- sc_err_t pf8100_pmic_set_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t mode)

  This function sets the mode of the specified regulator.
- sc_err_t pf8100_pmic_get_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t *mode)

  This function gets the mode of the specified regulator.
- uint32_t pf8100_get_pmic_temp (pmic_id_t id)

  This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.
- uint32_t pf8100_set_pmic_temp_alarm (pmic_id_t id, uint32_t temp)

  This function sets the temp alarm for the PMIC in Celsius.
- sc_err_t **pf8100_pmic_register_access** (pmic_id_t id, uint32_t address, sc_bool_t read_write, uint8_t *value)
- sc_bool_t pf8100_pmic_irq_service (pmic_id_t id)

  This function services the interrupt for the temp alarm.
- sc_err_t **pf8100_pmic_wdog_enable** (pmic_id_t id, sc_bool_t wd_en, sc_bool_t stby_en, sc_bool_t wdi_stby↩ _active)
- sc_err_t **pf8100_pmic_wdog_disable** (pmic_id_t id, sc_bool_t wd_dis, sc_bool_t stby_en, sc_bool_t wdi_stby↩ _active)
- sc_err_t **pf8100_pmic_wdog_set_timeout** (pmic_id_t id, uint32_t *timeout)
- sc_err_t **pf8100_pmic_wdog_service** (pmic_id_t id)

Defines for pf8100_vregs_t

- #define PF8100_CTRL1 0x37U

  CTRL1 register of PF8100/PF8200.
- #define PF8100_SW1 0x4DU

  Base register for SW1 regulator control.
- #define PF8100_SW2 0x55U

  Base register for SW2 regulator control.
- #define PF8100_SW3 0x5DU

  Base register for SW3 regulator control.
- #define PF8100_SW4 0x65U

  Base register for SW4 regulator control.
- #define PF8100_SW5 0x6DU

  Base register for SW5 regulator control.
- #define PF8100_SW6 0x75U

  Base register for SW6 regulator control.
- #define PF8100_SW7 0x7DU

  Base register for SW7 regulator control.
- #define PF8100_LDO1 0x85U

  Base register for LDO1 regulator control.
- #define PF8100_LDO2 0x8BU

  Base register for LDO2 regulator control.
- #define PF8100_LDO3 0x91U

  Base register for LDO3 regulator control.
- #define PF8100_LDO4 0x97U

  Base register for LDO4 regulator control.

Defines for sw_mode_t

- #define SW_RUN_OFF 0x0U

  Run mode: OFF.
- #define SW_RUN_PWM 0x1U

  Run mode: PWM.
- #define SW_RUN_PFM 0x2U

  Run mode: PFM.
- #define SW_RUN_ASM 0x3U

  Run mode: ASM.
- #define SW_STBY_OFF (0x0U << 2U)

  Standby mode: OFF.
- #define SW_STBY_PWM (0x1U << 2U)

  Standby mode: PWM.
- #define SW_STBY_PFM (0x2U << 2U)

  Standby mode: PFM.
- #define SW_STBY_ASM (0x3U << 2U)

  Standby mode: ASM.

Defines for ldo_mode_t

- #define RUN_OFF_STBY_OFF 0x0U
  Run mode: OFF, Standby mode: OFF.
- #define RUN_OFF_STBY_EN 0x1U
  Run mode: OFF, Standby mode: ON
- #define RUN_EN_STBY_OFF 0x2U
  Run mode: ON, Standby mode: OFF.
- #define RUN_EN_STBY_EN 0x3U
  Run mode: ON, Standby mode: ON
- #define VSELECT_EN 0x8U
  Enable VSELECT input pin for LDO 2 only.

Defines for vmode_reg_t

- #define **REG_STBY_MODE** 0U
- #define **REG_RUN_MODE** 1U

16.16.1 Detailed Description

Module for the PF8100 PMIC driver.

This is an SDK driver for the NXP PF8100 PMIC. For more information, see the PF8100 Datasheet.

If CRC operations are needed PMIC_CRC must be defined globally (usually in board.h)

16.16.2 Typedef Documentation

16.16.2.1 pf8100_vregs_t

```
typedef uint8_t pf8100_vregs_t
```

This type is used to indicate which register to address.

Refer to the PF8100 Datasheet for the description of regsiter.

16.16.2.2 sw_mode_t

```
typedef uint8_t sw_mode_t
```

This type is used to indicate a switching regulator mode.

Refer to the PF8100 Datasheet for the description of each mode.

These modes are used in combination to designate a run and standby mode i.e. (SW_RUN_PWM | SW_STBY_OFF).

16.16.2.3 ldo_mode_t

```
typedef uint8_t ldo_mode_t
```

This type is used to indicate an LDO regulator mode.

Refer to the PF8100 Datasheet for the description of each mode.

16.16.2.4 vmode_reg_t

```
typedef uint8_t vmode_reg_t
```

This type is used to indicate a Switching regulator voltage setpoint.

Refer to the PF8100 Datasheet for the description of each mode.

16.16.3 Function Documentation

16.16.3.1 pf8100_get_pmic_version()

```
pmic_version_t pf8100_get_pmic_version (
            pmic_id_t id )
```

This function returns the device ID and revision for the PF8100 PMIC.

Parameters

in	*id*	I2C address of PMIC device

Returns

Returns a structure with the device ID and revision.

16.16.3.2 pf8100_pmic_set_voltage()

```
sc_err_t pf8100_pmic_set_voltage (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t vol_mv,
            uint32_t mode_to_set )
```

This function sets the voltage of a corresponding voltage regulator for the PF8100 PMIC.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf8100_vregs_t
in	*vol_mv*	New voltage setpoint for the regulator in millivolts
in	*mode_to_set*	Mode to set the voltage for run (RUN or STANDBY)

Returns

Returns an error code (SC_ERR_NONE = success)

Note *mode_to_set* is SC_TRUE for RUN and SC_FALSE for STANDBY.

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.16.3.3 pf8100_pmic_get_voltage()

```
sc_err_t pf8100_pmic_get_voltage (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t * vol_mv,
            uint32_t mode_to_get )
```

This function gets the voltage on a corresponding voltage regulator for the PF8100 PMIC.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf8100_vregs_t
out	*vol_mv*	pointer to return voltage in millivolts
in	*mode_to_get*	Mode to get the voltage for (RUN or STANDBY)

Returns

Returns an error code (SC_ERR_NONE = success)

Note *mode_to_get* is SC_TRUE for RUN and SC_FALSE for STANDBY.

Return errors:

- SC_ERR_PARM if invalid parameters

16.16.3.4 pf8100_pmic_set_mode()

```
sc_err_t pf8100_pmic_set_mode (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t mode )
```

This function sets the mode of the specified regulator.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf8100_vregs_t
in	*mode*	mode to set the regulator; see sw_mode_t and ldo_mode_t

Note SW modes are used in combination to designate a run and standby mode i.e. (SW_RUN_PWM | SW_STBY_OFF).

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.16.3.5 pf8100_pmic_get_mode()

```
sc_err_t pf8100_pmic_get_mode (
            pmic_id_t id,
            uint32_t pmic_reg,
            uint32_t * mode )
```

This function gets the mode of the specified regulator.

Parameters

in	*id*	I2C address of PMIC device
in	*pmic_reg*	Register corresponding to regulator; see pf8100_vregs_t
out	*mode*	pointer to return mode in raw hex form

Note SW modes are used in combination to designate a run and standby mode i.e. (SW_RUN_PWM | SW_STBY_OFF).

Returns

Returns an error code (SC_ERR_NONE = success)

Return errors:

- SC_ERR_PARM if invalid parameters
- SC_ERR_FAIL if writing the register failed

16.16.3.6 pf8100_get_pmic_temp()

```
uint32_t pf8100_get_pmic_temp (
            pmic_id_t id )
```

This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.

Parameters

in	*id*	I2C address of PMIC device

Returns

returns the temp sensed by the PMIC in a UINT32 in Celsius

Return errors:

- SC_ERR_CONFIG if temperature monitor is not enabled

Note PMIC PF100 temp is returned as the highest temp sensor enabled.

16.16.3.7 pf8100_set_pmic_temp_alarm()

```
uint32_t pf8100_set_pmic_temp_alarm (
            pmic_id_t id,
            uint32_t temp )
```

This function sets the temp alarm for the PMIC in Celsius.

Parameters

in	*id*	I2C address of PMIC device
in	*temp*	Temperature to set the alarm

Note the granularity for PF100 PMIC only allows the following values: 80 95 110 125 140 155

Returns

Returns the temperature that the alarm is set to in Celsius

16.16.3.8 pf8100_pmic_irq_service()

```
sc_bool_t pf8100_pmic_irq_service (
            pmic_id_t id )
```

This function services the interrupt for the temp alarm.

Parameters

in	*id*	I2C address of PMIC device

Returns

Returns SC_TRUE if the temperature interrupt was cleared

16.17 RGPIO: Rapid General-Purpose Input/Output Driver

Modules

- RGPIO Driver
- FGPIO Driver

Files

- file fsl_rgpio.h

Data Structures

- struct rgpio_pin_config_t

  The RGPIO pin configuration structure.

Enumerations

- enum rgpio_pin_direction_t { kRGPIO_DigitalInput = 0U, kRGPIO_DigitalOutput = 1U }

  RGPIO direction definition.

Driver version

- #define FSL_RGPIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 2))

  RGPIO driver version 2.0.2.

16.17.1 Detailed Description

16.17.2 Enumeration Type Documentation

16.17.2.1 rgpio_pin_direction_t

`enum rgpio_pin_direction_t`

RGPIO direction definition.

Enumerator

kRGPIO_DigitalInput	Set current pin as digital input.
kRGPIO_DigitalOutput	Set current pin as digital output.

16.18 RGPIO Driver

RGPIO Configuration

- void RGPIO_PinInit (RGPIO_Type *base, uint32_t pin, const rgpio_pin_config_t *config)

  Initializes a RGPIO pin used by the board.
- uint32_t RGPIO_GetInstance (RGPIO_Type *base)

  Gets the RGPIO instance according to the RGPIO base.

RGPIO Output Operations

- static void RGPIO_PinWrite (RGPIO_Type *base, uint32_t pin, uint8_t output)

  Sets the output level of the multiple RGPIO pins to the logic 1 or 0.
- static void RGPIO_WritePinOutput (RGPIO_Type *base, uint32_t pin, uint8_t output)

  Sets the output level of the multiple RGPIO pins to the logic 1 or 0.
- static void RGPIO_PortSet (RGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple RGPIO pins to the logic 1.
- static void RGPIO_SetPinsOutput (RGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple RGPIO pins to the logic 1.
- static void RGPIO_PortClear (RGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple RGPIO pins to the logic 0.
- static void RGPIO_ClearPinsOutput (RGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple RGPIO pins to the logic 0.
- static void RGPIO_PortToggle (RGPIO_Type *base, uint32_t mask)

  Reverses the current output logic of the multiple RGPIO pins.
- static void RGPIO_TogglePinsOutput (RGPIO_Type *base, uint32_t mask)

  Reverses the current output logic of the multiple RGPIO pins.

RGPIO Input Operations

- static uint32_t RGPIO_PinRead (RGPIO_Type *base, uint32_t pin)

  Reads the current input value of the RGPIO port.
- static uint32_t RGPIO_ReadPinInput (RGPIO_Type *base, uint32_t pin)

  Reads the current input value of the RGPIO port.

16.18.1 Detailed Description

The MCUXpresso SDK provides a peripheral driver for the Rapid General-Purpose Input/Output (RGPIO) module of MCUXpresso SDK devices.

16.18.2 Typical use case

16.18.2.1 Output Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/rgpio

16.18.2.2 Input Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/rgpio

16.18.3 Function Documentation

16.18.3.1 RGPIO_PinInit()

```
void RGPIO_PinInit (
             RGPIO_Type * base,
             uint32_t pin,
             const rgpio_pin_config_t * config )
```

Initializes a RGPIO pin used by the board.

To initialize the RGPIO, define a pin configuration, as either input or output, in the user file. Then, call the RGPIO_PinInit() function.

This is an example to define an input pin or an output pin configuration.

```
 Define a digital input pin configuration,
rgpio_pin_config_t config =
{
  kRGPIO_DigitalInput,
  0,
}
Define a digital output pin configuration,
rgpio_pin_config_t config =
{
  kRGPIO_DigitalOutput,
  0,
}
```

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
pin	RGPIO port pin number
config	RGPIO pin configuration pointer

16.18.3.2 RGPIO_GetInstance()

```
uint32_t RGPIO_GetInstance (
             RGPIO_Type * base )
```

Gets the RGPIO instance according to the RGPIO base.

Parameters

base	RGPIO peripheral base pointer(PTA, PTB, PTC, etc.)

Return values

RGPIO	instance

16.18.3.3 RGPIO_PinWrite()

```
static void RGPIO_PinWrite (
             RGPIO_Type * base,
             uint32_t pin,
             uint8_t output )  [inline], [static]
```

Sets the output level of the multiple RGPIO pins to the logic 1 or 0.

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
pin	RGPIO pin number
output	RGPIO pin output logic level. • 0: corresponding pin output low-logic level. • 1: corresponding pin output high-logic level.

16.18.3.4 RGPIO_WritePinOutput()

```
static void RGPIO_WritePinOutput (
             RGPIO_Type * base,
             uint32_t pin,
             uint8_t output )  [inline], [static]
```

Sets the output level of the multiple RGPIO pins to the logic 1 or 0.

Deprecated Do not use this function. It has been superceded by RGPIO_PinWrite.

References RGPIO_PinWrite().

16.18.3.5 RGPIO_PortSet()

```
static void RGPIO_PortSet (
             RGPIO_Type * base,
             uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple RGPIO pins to the logic 1.

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
mask	RGPIO pin number macro

16.18.3.6 RGPIO_SetPinsOutput()

```
static void RGPIO_SetPinsOutput (
             RGPIO_Type * base,
             uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple RGPIO pins to the logic 1.

Deprecated Do not use this function. It has been superceded by RGPIO_PortSet.

References RGPIO_PortSet().

16.18.3.7 RGPIO_PortClear()

```
static void RGPIO_PortClear (
             RGPIO_Type * base,
             uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple RGPIO pins to the logic 0.

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
mask	RGPIO pin number macro

16.18.3.8 RGPIO_ClearPinsOutput()

```
static void RGPIO_ClearPinsOutput (
```

```
            RGPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple RGPIO pins to the logic 0.

Deprecated Do not use this function. It has been superceded by RGPIO_PortClear.

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
mask	RGPIO pin number macro

References RGPIO_PortClear().

16.18.3.9 RGPIO_PortToggle()

```
static void RGPIO_PortToggle (
            RGPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Reverses the current output logic of the multiple RGPIO pins.

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
mask	RGPIO pin number macro

16.18.3.10 RGPIO_TogglePinsOutput()

```
static void RGPIO_TogglePinsOutput (
            RGPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Reverses the current output logic of the multiple RGPIO pins.

Deprecated Do not use this function. It has been superceded by RGPIO_PortToggle.

References RGPIO_PortToggle().

16.18.3.11 RGPIO_PinRead()

```
static uint32_t RGPIO_PinRead (
             RGPIO_Type * base,
             uint32_t pin )  [inline], [static]
```

Reads the current input value of the RGPIO port.

Parameters

base	RGPIO peripheral base pointer (RGPIOA, RGPIOB, RGPIOC, and so on.)
pin	RGPIO pin number

Return values

RGPIO	port input value • 0: corresponding pin input low-logic level. • 1: corresponding pin input high-logic level.

16.18.3.12 RGPIO_ReadPinInput()

```
static uint32_t RGPIO_ReadPinInput (
            RGPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current input value of the RGPIO port.

Deprecated Do not use this function. It has been superceded by RGPIO_PinRead.

References RGPIO_PinRead().

16.19 FGPIO Driver

FGPIO Configuration

- void FGPIO_PinInit (FGPIO_Type *base, uint32_t pin, const rgpio_pin_config_t *config)

  Initializes a FGPIO pin used by the board.
- uint32_t FGPIO_GetInstance (FGPIO_Type *base)

  Gets the FGPIO instance according to the RGPIO base.

FGPIO Output Operations

- static void FGPIO_PinWrite (FGPIO_Type *base, uint32_t pin, uint8_t output)

  Sets the output level of the multiple FGPIO pins to the logic 1 or 0.
- static void FGPIO_WritePinOutput (FGPIO_Type *base, uint32_t pin, uint8_t output)

  Sets the output level of the multiple FGPIO pins to the logic 1 or 0.
- static void FGPIO_PortSet (FGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple FGPIO pins to the logic 1.
- static void FGPIO_SetPinsOutput (FGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple FGPIO pins to the logic 1.
- static void FGPIO_PortClear (FGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple FGPIO pins to the logic 0.
- static void FGPIO_ClearPinsOutput (FGPIO_Type *base, uint32_t mask)

  Sets the output level of the multiple FGPIO pins to the logic 0.
- static void FGPIO_PortToggle (FGPIO_Type *base, uint32_t mask)

  Reverses the current output logic of the multiple FGPIO pins.
- static void FGPIO_TogglePinsOutput (FGPIO_Type *base, uint32_t mask)

  Reverses the current output logic of the multiple FGPIO pins.

FGPIO Input Operations

- static uint32_t FGPIO_PinRead (FGPIO_Type *base, uint32_t pin)

  Reads the current input value of the FGPIO port.
- static uint32_t FGPIO_ReadPinInput (FGPIO_Type *base, uint32_t pin)

  Reads the current input value of the FGPIO port.

16.19.1 Detailed Description

This section describes the programming interface of the FGPIO driver. The FGPIO driver configures the FGPIO module and provides a functional interface to build the RGPIO application.

Note

FGPIO (Fast GPIO) is only available in a few MCUs. FGPIO and RGPIO share the same peripheral but use different registers. FGPIO is closer to the core than the regular RGPIO and it's faster to read and write.

16.19.2 Typical use case

16.19.2.1 Output Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/rgpio

16.19.2.2 Input Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/rgpio

16.19.3 Function Documentation

16.19.3.1 FGPIO_PinInit()

```
void FGPIO_PinInit (
             FGPIO_Type * base,
             uint32_t pin,
             const rgpio_pin_config_t * config )
```

Initializes a FGPIO pin used by the board.

To initialize the FGPIO driver, define a pin configuration, as either input or output, in the user file. Then, call the FGPIO_PinInit() function.

This is an example to define an input pin or an output pin configuration:

```
 Define a digital input pin configuration,
rgpio_pin_config_t config =
{
  kRGPIO_DigitalInput,
  0,
}
Define a digital output pin configuration,
rgpio_pin_config_t config =
{
  kRGPIO_DigitalOutput,
  0,
}
```

Parameters

base	FGPIO peripheral base pointer (FGPIOA, FGPIOB, FGPIOC, and so on.)
pin	FGPIO port pin number
config	FGPIO pin configuration pointer

Examples

board.c.

16.19.3.2 FGPIO_GetInstance()

```
uint32_t FGPIO_GetInstance (
            FGPIO_Type * base )
```

Gets the FGPIO instance according to the RGPIO base.

Parameters

base	FGPIO peripheral base pointer(PTA, PTB, PTC, etc.)

Return values

FGPIO	instance

16.19.3.3 FGPIO_PinWrite()

```
static void FGPIO_PinWrite (
            FGPIO_Type * base,
            uint32_t pin,
            uint8_t output )  [inline], [static]
```

Sets the output level of the multiple FGPIO pins to the logic 1 or 0.

Parameters

base	FGPIO peripheral base pointer (FGPIOA, FGPIOB, FGPIOC, and so on.)
pin	FGPIO pin number
output	FGPIOpin output logic level. • 0: corresponding pin output low-logic level. • 1: corresponding pin output high-logic level.

Examples

board.c.

16.19.3.4 FGPIO_WritePinOutput()

```
static void FGPIO_WritePinOutput (
            FGPIO_Type * base,
```

```
            uint32_t pin,
            uint8_t output )  [inline], [static]
```

Sets the output level of the multiple FGPIO pins to the logic 1 or 0.

Deprecated Do not use this function. It has been superceded by FGPIO_PinWrite.

References FGPIO_PinWrite().

16.19.3.5 FGPIO_PortSet()

```
static void FGPIO_PortSet (
            FGPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple FGPIO pins to the logic 1.

Parameters

base	FGPIO peripheral base pointer (FGPIOA, FGPIOB, FGPIOC, and so on.)
mask	FGPIO pin number macro

16.19.3.6 FGPIO_SetPinsOutput()

```
static void FGPIO_SetPinsOutput (
            FGPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple FGPIO pins to the logic 1.

Deprecated Do not use this function. It has been superceded by FGPIO_PortSet.

References FGPIO_PortSet().

16.19.3.7 FGPIO_PortClear()

```
static void FGPIO_PortClear (
            FGPIO_Type * base,
            uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple FGPIO pins to the logic 0.

Parameters

base	FGPIO peripheral base pointer (FGPIOA, FGPIOB, FGPIOC, and so on.)
mask	FGPIO pin number macro

16.19.3.8 FGPIO_ClearPinsOutput()

```
static void FGPIO_ClearPinsOutput (
             FGPIO_Type * base,
             uint32_t mask )  [inline], [static]
```

Sets the output level of the multiple FGPIO pins to the logic 0.

Deprecated Do not use this function. It has been superceded by FGPIO_PortClear.

References FGPIO_PortClear().

16.19.3.9 FGPIO_PortToggle()

```
static void FGPIO_PortToggle (
             FGPIO_Type * base,
             uint32_t mask )  [inline], [static]
```

Reverses the current output logic of the multiple FGPIO pins.

Parameters

base	FGPIO peripheral base pointer (FGPIOA, FGPIOB, FGPIOC, and so on.)
mask	FGPIO pin number macro

16.19.3.10 FGPIO_TogglePinsOutput()

```
static void FGPIO_TogglePinsOutput (
             FGPIO_Type * base,
             uint32_t mask )  [inline], [static]
```

Reverses the current output logic of the multiple FGPIO pins.

Deprecated Do not use this function. It has been superceded by FGPIO_PortToggle.

References FGPIO_PortToggle().

16.19.3.11 FGPIO_PinRead()

```
static uint32_t FGPIO_PinRead (
            FGPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current input value of the FGPIO port.

Parameters

base	FGPIO peripheral base pointer (FGPIOA, FGPIOB, FGPIOC, and so on.)
pin	FGPIO pin number

Return values

FGPIO	port input value • 0: corresponding pin input low-logic level. • 1: corresponding pin input high-logic level.

16.19.3.12 FGPIO_ReadPinInput()

```
static uint32_t FGPIO_ReadPinInput (
            FGPIO_Type * base,
            uint32_t pin )  [inline], [static]
```

Reads the current input value of the FGPIO port.

Deprecated Do not use this function. It has been superceded by FGPIO_PinRead

References FGPIO_PinRead().

16.20 SECO: Security Controller Driver

Module for the SECO driver.

Files

- file fsl_seco.h

Typedefs

- typedef uint16_t seco_lifecycle_t

  This type is used to return the lifecycle.
- typedef uint8_t seco_snvs_id_t

  This type is used to indicate the ID of anSNVS register to access.

Variables

- sc_err_t seco_err

  SECO error return.

Defines for seco_lifecycle_t

- #define SECO_LIFECYCLE_DEFAULT BIT(0)

  Default fab mode (early_fuses_pgrm not blown)
- #define SECO_LIFECYCLE_FAB BIT(1)

  Fab mode.
- #define SECO_LIFECYCLE_NO_SECRETS BIT(2)

  No secrets.
- #define SECO_LIFECYCLE_SECRETS BIT(3)

  With Secrets.
- #define SECO_LIFECYCLE_SC_FW_CLSD BIT(4)

  SCU FW Closed.
- #define SECO_LIFECYCLE_SECO_FW_CLSD BIT(5)

  SECO FW Closed.
- #define SECO_LIFECYCLE_CLOSED BIT(6)

  Closed.
- #define SECO_LIFECYCLE_CLOSED_FW BIT(7)

  Closed with FW.
- #define SECO_LIFECYCLE_PART_RTN BIT(8,

  Partial field return.
- #define SECO_LIFECYCLE_RTN BIT(9)

  Field return.
- #define SECO_LIFECYCLE_NO_RTN BIT(10)

  No Return.

Defines for seco_snvs_id_t

- #define AHAB_SNVS_ID_INIT 0x00U

  Init SNVS.
- #define AHAB_SNVS_ID_POWER_OFF 0x01U

  Power off the system.
- #define AHAB_SNVS_ID_SRTC 0x02U

  R/W the SRTC.
- #define AHAB_SNVS_ID_SRTC_CALB 0x03U

  R/W the SRTC calibration.
- #define AHAB_SNVS_ID_SRTC_ALRM 0x04U

  R/W the SRTC alarm.
- #define AHAB_SNVS_ID_RTC 0x05U

  R/W the RTC.
- #define AHAB_SNVS_ID_RTC_CALB 0x06U

  R/W the RTC calibration.
- #define AHAB_SNVS_ID_RTC_ALRM 0x07U

  R/W the RTC alarm.
- #define AHAB_SNVS_ID_BTN_CONFIG 0x08U

  R/W the button configuration.
- #define AHAB_SNVS_ID_BTN_MASK 0x09U

  R/W the button mask.
- #define AHAB_SNVS_ID_BTN 0x0AU

  R/W the button state.
- #define AHAB_SNVS_ID_BTN_CLEAR 0x0BU

  Clear the button IRQ.
- #define AHAB_SNVS_ID_SSM_STATE 0x0CU

  Read the SSM state.
- #define AHAB_SNVS_ID_BTN_TIME 0x0DU

  R/W the button time parameters.
- #define AHAB_SNVS_ID_WAKE_UP_IT 0x0EU

  Clear the wake IRQ.

Defines for SNVS access

- #define SECO_SNVS_READ 0U

  SNVS read operation.
- #define SECO_SNVS_WRITE 1U

  SNVS write operation.

Macros for version parsing

- #define SECO_PROD_VER(X) (((X) >> 16) & 0x7FFFUL)

  Extract SECO production ver.
- #define SECO_MAJOR_VER(X) (((X) >> 4) & 0xFFFUL)

  Extract SECO major ver.
- #define SECO_MINOR_VER(X) ((X) & 0xFUL)

  Extract SECO minor ver.

Defines for V2X state

- #define V2X_STATE_AUTH_RX 0x01U

  Authentication request received.
- #define V2X_STATE_PROV_NORMAL 0x02U

  Provisioned successfully in normal mode.
- #define V2X_STATE_PROV_DEBUG 0x04U

  Provisioned successfully in debug mode.
- #define V2X_STATE_AUTH_IP 0x08U

  Authentication on going.
- #define V2X_STATE_AUTH_SUCCESS 0x10U

  Authentication success.
- #define V2X_STATE_AUTH_FAIL 0x20U

  Authentication failure.
- #define V2X_STATE_CRYPTO_DIS 0x40U

  Crypto accelerators disabled.
- #define V2X_STATE_HOLD_EN 0x80U

  V2X provisioning on hold.

Initialization Functions

- void SECO_Init (boot_phase_t phase)

  This function initializes the SECO driver.
- void SECO_CAAM_Config (uint16_t master, sc_bool_t lock, sc_rm_spa_t sa, sc_rm_did_t did, sc_rm_sid_t sid)

  This function configures the CAAM MP.
- void SECO_ClearCache (void)

  This function clears the CAAM MP cache.
- void SECO_MU_Config (uint8_t mu, sc_rm_spa_t sa, sc_rm_did_t did)

  This function configures MU ownership.
- uint16_t SECO_SetMonoCounterPartition (uint16_t she)

  This function partitions the monotonic counter.
- uint32_t SECO_SetFipsMode (uint8_t mode)

  This function configures the SECO in FIPS mode.

Power Mangement Functions

- void SECO_Power (sc_sub_t ss, uint32_t inst, sc_bool_t up)

  This function notifies SECO that a subsystem power state has changed.
- void SECO_CAAM_PowerDown (void)

  This function notifies SECO that CAAM is powering down.
- void SECO_EnterLPM (void)

  This function notifies SECO the system is entering low power mode.
- void SECO_ExitLPM (void)

  This function notifies SECO the system is has exited low power mode.

Image Functions

- void SECO_Image_Load (sc_faddr_t addr_src, sc_faddr_t addr_dst, uint32_t len, sc_bool_t fw)

  This function loads a SECO image.
- void SECO_Authenticate (sc_seco_auth_cmd_t cmd, sc_faddr_t addr, uint32_t mask1, uint32_t mask2)

  This function is used to authenticate a SECO image or command.

Lifecycle Functions

- seco_lifecycle_t SECO_Get_Lifecycle (void)

  This function is used get the lifecycle from the ADM.
- void SECO_ForwardLifecycle (uint32_t change)

  This function updates the lifecycle of the device.
- void SECO_ReturnLifecycle (sc_faddr_t addr)

  This function updates the lifecycle to one of the return lifecycles.
- void SECO_Commit (uint32_t *info)

  This function is used to commit into the fuses any new SRK revocation and FW version information that have been found in the primary and secondary containers.

Attestation Functions

- void SECO_AttestMode (uint32_t mode)

  This function is used to set the attestation mode.
- void SECO_Attest (uint64_t nonce)

  This function is used to request atestation.
- void SECO_GetAttestPublicKey (sc_faddr_t addr)

  This function is used to retrieve the attestation public key.
- void SECO_GetAttestSign (sc_faddr_t addr)

  This function is used to retrieve attestation signature and parameters.
- void SECO_AttestVerify (sc_faddr_t addr)

  This function is used to verify attestation.

Key Functions

- void SECO_GenKeyBlob (uint32_t id, sc_faddr_t load_addr, sc_faddr_t export_addr, uint16_t max_size)

  This function is used to generate a SECO key blob.
- void SECO_LoadKey (uint32_t id, sc_faddr_t addr)

  This function is used to load a SECO key.

Manufacturing Protection Functions

- void SECO_GetMPKey (sc_faddr_t dst_addr, uint16_t dst_size)

  This function is used to get the manufacturing protection public key.
- void SECO_UpdateMPMR (sc_faddr_t addr, uint8_t size, uint8_t lock)

  This function is used to update the manufacturing protection message register.
- void SECO_GetMPSign (sc_faddr_t msg_addr, uint16_t msg_size, sc_faddr_t dst_addr, uint16_t dst_size)

  This function is used to get the manufacturing protection signature.

V2X Functions

- uint8_t SECO_V2X_Forward (uint32_t *buf)

  This function is used to forward a message received from V2X.
- void SECO_V2X_Ping (void)

  This function sends a ping to V2X through SECO.
- void SECO_V2X_Hold (uint32_t hold_value)

  This function is used to set a control variable indicating whether or not the configuration of the V2X must be done as soon as possible or should be delayed and left under the control of the SCU.
- void SECO_V2X_Provision (uint32_t provision_mode)

  This function is used to provision the V2X either in "normal" mode or in "debug" mode.
- uint32_t SECO_V2X_GetState (uint32_t *req_status)

  This function returns the v2x_state (provisioned, successfully authenticated, etc.).

Debug Functions

- void SECO_Version (uint32_t *version, uint32_t *commit, sc_bool_t *dirty)

  This function is used to return the SECO FW build info.
- void SECO_ChipInfo (uint16_t *lc, uint16_t *monotonic, uint32_t *uid_l, uint32_t *uid_h)

  This function is used to return SECO chip info.
- void SECO_AttachDebug (void)

  This function notifies SECO that a JTAG connection has been made.
- void SECO_EnableDebug (sc_faddr_t addr)

  This function securely enables debug.
- uint32_t SECO_GetEvent (uint8_t idx)

  This function is used to return an event from the SECO error log.
- void SECO_DumpDebug (void)

  This function dumps low-level SECO debug info to the SCU debug UART.
- uint32_t SECO_ErrNumber (void)

  This function return the internal SECO error number returned by the last SECO function call.

Miscellaneous Functions

- void SECO_Ping (void)

  This function sends a ping to SECO.
- void SECO_KickWdog (void)

  This function sends a a message to SECO to service the 24H watchdog.
- void SECO_WriteFuse (uint32_t word, uint32_t val)

  This function writes a given fuse word index.
- void SECO_SecureWriteFuse (sc_faddr_t addr)

  This function securely writes a group of fuse words.
- void SECO_ScuPatch (sc_faddr_t addr)

  This function applies a patch.
- sc_seco_rng_stat_t SECO_StartRNG (void)

  This function starts the random number generator.
- void SECO_SABSignedMesg (sc_faddr_t addr)

  This function is used to send a generic signed message to the SECO SHE/HSM components.

SNVS Functions

- void SECO_WriteSNVS (seco_snvs_id_t id, uint32_t val)

  This function write an SNVS parameter.
- uint32_t SECO_ReadSNVS (seco_snvs_id_t id)

  This function reads an SNVS parameter.
- void SECO_ManageSNVS (uint8_t id, uint8_t access, uint32_t *val, uint8_t size)

  This function is used to manage the SNVS.
- void SECO_ManageSNVS_DGO (uint8_t id, uint8_t access, uint32_t *val)

  This function is used to manage the SNVS DGO.

16.20.1 Detailed Description

Module for the SECO driver.

It is an MCUXpresso SDK driver for the SECO module of i.MX devices.

16.20.2 Function Documentation

16.20.2.1 SECO_Init()

```
void SECO_Init (
             boot_phase_t phase )
```

This function initializes the SECO driver.

Parameters

in	*phase*	Init phase

Called when SCFW boots.

16.20.2.2 SECO_CAAM_Config()

```
void SECO_CAAM_Config (
             uint16_t master,
             sc_bool_t lock,
             sc_rm_spa_t sa,
             sc_rm_did_t did,
             sc_rm_sid_t sid )
```

This function configures the CAAM MP.

Parameters

in	*master*	Index of job ring / out

Parameters

in	*lock*	Lock state of config
in	*sa*	Secure state
in	*did*	XRDC2 Domain ID
in	*sid*	SMMU Stream ID

Called by the Resource Manager to configure CAAM job ring access and output parameters.

See the SECO API Reference Guide for more info.

16.20.2.3 SECO_ClearCache()

```
void SECO_ClearCache (
            void  )
```

This function clears the CAAM MP cache.

It is called by the Power Manager when CAAM power state is lost.

16.20.2.4 SECO_MU_Config()

```
void SECO_MU_Config (
            uint8_t mu,
            sc_rm_spa_t sa,
            sc_rm_did_t did )
```

This function configures MU ownership.

Parameters

in	*mu*	Index of MU
in	*sa*	Secure state
in	*did*	XRDC2 Domain ID

Called by the Resource Manager to configure MU access.

See the SECO API Reference Guide for more info.

16.20.2.5 SECO_SetMonoCounterPartition()

```
uint16_t SECO_SetMonoCounterPartition (
            uint16_t she )
```

This function partitions the monotonic counter.

Parameters

in	*she*	number of SHE bits

SECO uses an OTP monotonic counter to protect the SHE and HSM key-stores from roll-back attack. This function is used to define the number of monotonic counter bits allocated to SHE use. Two monotonic counter bits are used to store this information while the remaining bits are allocated to the HSM user. This function must be called before any SHE or HSM key stores are created in the system, otherwise the default configuration is applied.

If the partition has been already configured, any attempt to re-configure the SHE partition to a different value will result in a failure response.

Returns

Returns the current number of SHE bits.

See the SECO API Reference Guide for more info.

16.20.2.6 SECO_SetFipsMode()

```
uint32_t SECO_SetFipsMode (
             uint8_t mode )
```

This function configures the SECO in FIPS mode.

Parameters

in	*mode*	FIPS mode

This function permanently configures the SECO in FIPS approved mode. When in FIPS approved mode the following services will be disabled and receive a failure response:

- Encrypted boot is not supported
- Attestation is not supported
- Manufacturing protection is not supported
- DTCP load
- SHE services are not supported
- Assign JR is not supported (all JRs owned by SECO)

Returns

Returns the failure reason.

See the SECO API Reference Guide for more info.

16.20.2.7 SECO_Power()

```
void SECO_Power (
             sc_sub_t ss,
             uint32_t inst,
             sc_bool_t up )
```

This function notifies SECO that a subsystem power state has changed.

Parameters

in	*ss*	Subsystem
in	*inst*	Subsystem instance
in	*up*	Power state

Called by the Power Manager when subsystem power state changes.

16.20.2.8 SECO_CAAM_PowerDown()

```
void SECO_CAAM_PowerDown (
            void  )
```

This function notifies SECO that CAAM is powering down.

Called by the Power Manager before powering down the CAAM.

See the SECO API Reference Guide for more info.

16.20.2.9 SECO_EnterLPM()

```
void SECO_EnterLPM (
            void  )
```

This function notifies SECO the system is entering low power mode.

Called by the Power Manager before entering LPM.

See the SECO API Reference Guide for more info.

16.20.2.10 SECO_ExitLPM()

```
void SECO_ExitLPM (
            void  )
```

This function notifies SECO the system is has exited low power mode.

Called by the Power Manager before after exiting LPM.

See the SECO API Reference Guide for more info.

16.20.2.11 SECO_Image_Load()

```
void SECO_Image_Load (
            sc_faddr_t addr_src,
            sc_faddr_t addr_dst,
            uint32_t len,
            sc_bool_t fw )
```

This function loads a SECO image.

Parameters

in	*addr_src*	address of image source
in	*addr_dst*	address of image destination
in	*len*	lenth of image to load
in	*fw*	SC_TRUE = firmware load

This is used to load images via the SECO. Examples include SECO Firmware and IVT/CSF data used for authentication. These are usually loaded into SECO TCM. *addr_src* is in secure memory.

See the SECO API Reference Guide for more info.

16.20.2.12 SECO_Authenticate()

```
void SECO_Authenticate (
            sc_seco_auth_cmd_t cmd,
            sc_faddr_t addr,
            uint32_t mask1,
            uint32_t mask2 )
```

This function is used to authenticate a SECO image or command.

Parameters

in	*cmd*	authenticate command
in	*addr*	address of/or metadata
in	*mask1*	metadata
in	*mask2*	metadata

This is used to authenticate a SECO image or issue a security command. *addr* often points to an container. It is also just data (or even unused) for some commands.

See the SECO API Reference Guide for more info.

16.20.2.13 SECO_Get_Lifecycle()

```
seco_lifecycle_t SECO_Get_Lifecycle (
            void  )
```

This function is used get the lifecycle from the ADM.

Returns

Returns the lifecycle.

16.20.2.14 SECO_ForwardLifecycle()

```
void SECO_ForwardLifecycle (
            uint32_t change )
```

This function updates the lifecycle of the device.

Parameters

in	*change*	desired lifecycle transistion

This function is used for going from Open to NXP Closed to OEM Closed. Note *change* is NOT the new desired lifecycle. It is a lifecycle transition as documented in the SECO API Reference Guide.

If any SECO request fails or only succeeds because the part is in an "OEM open" lifecycle, then a request to transition from "NXP closed" to "OEM closed" will also fail. For example, booting a signed container when the OEM SRK is not fused will succeed, but as it is an abnormal situation, a subsequent request to transition the lifecycle will return an error via seco_err.

16.20.2.15 SECO_ReturnLifecycle()

```
void SECO_ReturnLifecycle (
            sc_faddr_t addr )
```

This function updates the lifecycle to one of the return lifecycles.

Parameters

in	*addr*	address of message block

Note *addr* must be a pointer to a signed message block.

To switch back to NXP states (Full Field Return), message must be signed by NXP SRK. For OEM States (Partial Field Return), must be signed by OEM SRK.

See the SECO API Reference Guide for more info.

16.20.2.16 SECO_Commit()

```
void SECO_Commit (
            uint32_t * info )
```

This function is used to commit into the fuses any new SRK revocation and FW version information that have been found in the primary and secondary containers.

Parameters

in,out	*info*	pointer to information type to be committed

The return *info* will contain what was actually committed.

16.20.2.17 SECO_AttestMode()

```
void SECO_AttestMode (
            uint32_t mode )
```

This function is used to set the attestation mode.

Parameters

in	*mode*	mode

This is used to set the SECO attestation mode. This can be prover or verfier. See the SECO API Reference Guide for more on the suported modes, mode values, and mode behavior.

16.20.2.18 SECO_Attest()

```
void SECO_Attest (
            uint64_t nonce )
```

This function is used to request atestation.

Parameters

in	*nonce*	unique value

This is used to ask SECO to perform an attestation. The result depends on the attestation mode. After this call, the signature can be requested or a verify can be requested.

See the SECO API Reference Guide for more info.

16.20.2.19 SECO_GetAttestPublicKey()

```
void SECO_GetAttestPublicKey (
            sc_faddr_t addr )
```

This function is used to retrieve the attestation public key.

Mode must be verifier.

Parameters

in	*addr*	address to write response

Result will be written to *addr*. The *addr* parmater must point to an address SECO can access. It must be 64-bit aligned. There should be 96 bytes of space.

See the SECO API Reference Guide for more info.

16.20.2.20 SECO_GetAttestSign()

```
void SECO_GetAttestSign (
            sc_faddr_t addr )
```

This function is used to retrieve attestation signature and parameters.

Mode must be provider.

Parameters

in	*addr*	address to write response

Result will be written to *addr*. The *addr* parmater must point to an address SECO can access. It must be 64-bit aligned. There should be 120 bytes of space.

See the SECO API Reference Guide for more info.

16.20.2.21 SECO_AttestVerify()

```
void SECO_AttestVerify (
            sc_faddr_t addr )
```

This function is used to verify attestation.

Mode must be verifier.

Parameters

in	*addr*	address of signature

The *addr* parmater must point to an address SECO can access. It must be 64-bit aligned.

See the SECO API Reference Guide for more info.

16.20.2.22 SECO_GenKeyBlob()

```
void SECO_GenKeyBlob (
            uint32_t id,
            sc_faddr_t load_addr,
            sc_faddr_t export_addr,
            uint16_t max_size )
```

This function is used to generate a SECO key blob.

Parameters

in	*id*	key identifier
in	*load_addr*	load address
in	*export_addr*	export address
in	*max_size*	max export size

This function is used to encapsulate sensitive keys in a specific structure called a blob, which provides both confidentiality and integrity protection.

See the SECO API Reference Guide for more info.

16.20.2.23 SECO_LoadKey()

```
void SECO_LoadKey (
            uint32_t id,
            sc_faddr_t addr )
```

This function is used to load a SECO key.

Parameters

in	*id*	key identifier
in	*addr*	key address

This function is used to install private cryptographic keys encapsulated in a blob previously generated by SECO. The controller can be either the IEE or the VPU. The blob header carries the controller type and the key size, as provided by the user when generating the key blob.

See the SECO API Reference Guide for more info.

16.20.2.24 SECO_GetMPKey()

```
void SECO_GetMPKey (
            sc_faddr_t dst_addr,
            uint16_t dst_size )
```

This function is used to get the manufacturing protection public key.

Parameters

in	*dst_addr*	destination address
in	*dst_size*	destination size

This function is supported only in OEM-closed lifecycle. It generates the mfg public key and stores it in a specific location in the secure memory.

See the SECO API Reference Guide for more info.

16.20.2.25 SECO_UpdateMPMR()

```
void SECO_UpdateMPMR (
            sc_faddr_t addr,
            uint8_t size,
            uint8_t lock )
```

This function is used to update the manufacturing protection message register.

Parameters

in	*addr*	data address
in	*size*	size
in	*lock*	lock_reg

This function is supported only in OEM-closed lifecycle. It updates the content of the MPMR (Manufacturing Protection Message register of 256 bits). This register will be appended to the input-data message when generating the signature. Please refer to the CAAM block guide for details.

See the SECO API Reference Guide for more info.

16.20.2.26 SECO_GetMPSign()

```
void SECO_GetMPSign (
             sc_faddr_t msg_addr,
             uint16_t msg_size,
             sc_faddr_t dst_addr,
             uint16_t dst_size )
```

This function is used to get the manufacturing protection signature.

Parameters

in	*msg_addr*	message address
in	*msg_size*	message size
in	*dst_addr*	destination address
in	*dst_size*	destination size

This function is used to generate an ECDSA signature for an input-data message and to store it in a specific location in the secure memory. It is only supported in OEM-closed lifecycle. In order to get the ECDSA signature, the RNG must be initialized. In case it has not been started an error will be returned.
See the SECO API Reference Guide for more info.

16.20.2.27 SECO_V2X_Forward()

```
uint8_t SECO_V2X_Forward (
             uint32_t * buf )
```

This function is used to forward a message received from V2X.

Parameters

in	*buf*	pointer to message buffer

Returns

Returns number of words in response.

16.20.2.28 SECO_V2X_Ping()

```
void SECO_V2X_Ping (
             void  )
```

This function sends a ping to V2X through SECO.

See the SECO API Reference Guide for more info.

16.20.2.29 SECO_V2X_Hold()

```
void SECO_V2X_Hold (
            uint32_t hold_value )
```

This function is used to set a control variable indicating whether or not the configuration of the V2X must be done as soon as possible or should be delayed and left under the control of the SCU.

Parameters

in	*hold_value*	0=no delay, 1=delay

See the SECO API Reference Guide for more info.

16.20.2.30 SECO_V2X_Provision()

```
void SECO_V2X_Provision (
            uint32_t provision_mode )
```

This function is used to provision the V2X either in "normal" mode or in "debug" mode.

Provisioning for debug request will be accepted only in NXP open LC. In NXP closed LC, the SECO_EnableDebug() function must be used instead.

Parameters

in	*provision_mode*	0=normal, 1=debug

See the SECO API Reference Guide for more info.

16.20.2.31 SECO_V2X_GetState()

```
uint32_t SECO_V2X_GetState (
            uint32_t * req_status )
```

This function returns the v2x_state (provisioned, successfully authenticated, etc.).

It should be sent after the v2x_authenticate_request in order to get the result of the v2x authentication once finished.

Parameters

out	*req_status*	V2X authentication request status

Returns

Returns the V2X state.

- Bit 0: v2x authentication request received
- Bit 1: v2x provisioned successfully in normal mode
- Bit 2: v2x provisioned successfully in debug mode
- Bit 3: v2x authentication on going
- Bit 4: v2x authentication success
- Bit 5: v2x authentication failure
- Bit 6: v2x crypto disabled
- Bit 7: v2x hold enabled

See the SECO API Reference Guide for more info.

16.20.2.32 SECO_Version()

```
void SECO_Version (
             uint32_t * version,
             uint32_t * commit,
             sc_bool_t * dirty )
```

This function is used to return the SECO FW build info.

Parameters

out	*version*	pointer to return build number
out	*commit*	pointer to return commit ID (git SHA-1)
out	*dirty*	pointer to return dirty flag

See the SECO API Reference Guide for more info.

16.20.2.33 SECO_ChipInfo()

```
void SECO_ChipInfo (
             uint16_t * lc,
             uint16_t * monotonic,
             uint32_t * uid_l,
             uint32_t * uid_h )
```

This function is used to return SECO chip info.

Parameters

out	*lc*	pointer to return lifecycle

Parameters

out	*monotonic*	pointer to return monotonic counter
out	*uid_l*	pointer to return UID (lower 32 bits)
out	*uid_h*	pointer to return UID (upper 32 bits)

See the SECO API Reference Guide for more info.

16.20.2.34 SECO_AttachDebug()

```
void SECO_AttachDebug (
            void  )
```

This function notifies SECO that a JTAG connection has been made.

See the SECO API Reference Guide for more info.

16.20.2.35 SECO_EnableDebug()

```
void SECO_EnableDebug (
            sc_faddr_t addr )
```

This function securely enables debug.

Parameters

in	*addr*	address of message block

Note *addr* must be a pointer to a signed message block.

See the SECO API Reference Guide for more info.

16.20.2.36 SECO_GetEvent()

```
uint32_t SECO_GetEvent (
            uint8_t idx )
```

This function is used to return an event from the SECO error log.

Parameters

out	*idx*	index of event to return

Returns

Returns the event.

Read of *idx* 0 captures events from SECO. Loop starting with 0 until an error is returned to dump all events.

See the SECO API Reference Guide for more info.

16.20.2.37 SECO_ErrNumber()

```
uint32_t SECO_ErrNumber (
             void  )
```

This function return the internal SECO error number returned by the last SECO function call.

It is valid if seco_err != SC_R_NONE.

See the SECO API Reference Guide for a description of these internal error codes.

Returns

Returns the error number.

16.20.2.38 SECO_Ping()

```
void SECO_Ping (
             void  )
```

This function sends a ping to SECO.

See the SECO API Reference Guide for more info.

16.20.2.39 SECO_KickWdog()

```
void SECO_KickWdog (
             void  )
```

This function sends a a message to SECO to service the 24H watchdog.

SCFW sends this periodically.

See the SECO API Reference Guide for more info.

16.20.2.40 SECO_WriteFuse()

```
void SECO_WriteFuse (
             uint32_t word,
             uint32_t val )
```

This function writes a given fuse word index.

Parameters

in	*word*	fuse word index
in	*val*	fuse write value

The command is passed as is to SECO. SECO uses part of the *word* parameter to indicate if the fuse should be locked after programming. See the "Write common fuse" section of the SECO API Reference Guide for more info.

16.20.2.41 SECO_SecureWriteFuse()

```
void SECO_SecureWriteFuse (
            sc_faddr_t addr )
```

This function securely writes a group of fuse words.

Parameters

in	*addr*	address of message block

Note *addr* must be a pointer to a signed message block.

See the SECO API Reference Guide for more info.

16.20.2.42 SECO_ScuPatch()

```
void SECO_ScuPatch (
            sc_faddr_t addr )
```

This function applies a patch.

Parameters

in	*addr*	address of message block

Note *addr* must be a pointer to a signed message block.

See the SECO API Reference Guide for more info.

16.20.2.43 SECO_StartRNG()

```
sc_seco_rng_stat_t SECO_StartRNG (
            void  )
```

This function starts the random number generator.

Returns

Returns the state of RNG.

The RNG is started automatically after all CPUs are booted. This function can be used to start earlier and to check the status.

See the SECO API Reference Guide for more info.

16.20.2.44 SECO_SABSignedMesg()

```
void SECO_SABSignedMesg (
            sc_faddr_t addr )
```

This function is used to send a generic signed message to the SECO SHE/HSM components.

Parameters

in	*addr*	address of message block

Note *addr* must be a pointer to a signed message block.

See the SECO API Reference Guide for more info.

16.20.2.45 SECO_WriteSNVS()

```
void SECO_WriteSNVS (
            seco_snvs_id_t id,
            uint32_t val )
```

This function write an SNVS parameter.

Parameters

in	*id*	ID of parameter to write
in	*val*	value to write

This function is used by the SNVS driver. Users should call that driver instead of this function.

See the SECO API Reference Guide for more info.

16.20.2.46 SECO_ReadSNVS()

```
uint32_t SECO_ReadSNVS (
            seco_snvs_id_t id )
```

This function reads an SNVS parameter.

Parameters

in	*id*	ID of parameter to read

This function is used by the SNVS driver. Users should call that driver instead of this function.

Returns

Returns the value read.

See the SECO API Reference Guide for more info.

16.20.2.47 SECO_ManageSNVS()

```
void SECO_ManageSNVS (
            uint8_t id,
```

```
            uint8_t access,
            uint32_t * val,
            uint8_t size )
```

This function is used to manage the SNVS.

It allows reading and writing of various SNVS registers.

Parameters

in	*id*	ID of parameter to read
in	*access*	Access type (read or write)
in,out	*val*	pointer to value to read or write
in	*size*	number of words to read or write

For info on what the SNVS registers do, refer to the SNVS section of the SRM.

Note many aspects of the SNVS are used by SECO and not available for use (e.g. LPGPR0) and this function will not allow access to those registers/fields. See the SECO API Reference Guide for more info.

16.20.2.48 SECO_ManageSNVS_DGO()

```
void SECO_ManageSNVS_DGO (
            uint8_t id,
            uint8_t access,
            uint32_t * val )
```

This function is used to manage the SNVS DGO.

It allows reading and writing of various privileged SNVS DGO registers.

Parameters

in	*id*	ID of parameter to read
in	*access*	Access type (read or write)
in,out	*val*	pointer to value to read or write

For info on what the SNVS registers do, refer to the SNVS section of the SRM.

16.21 SNVS: Secure Non-Volatile Storage Driver

Module for the SNVS driver.

Files

- file fsl_snvs.h

Typedefs

- typedef uint8_t snvs_btn_config_t

  This type is used configure the button active state.
- typedef uint8_t snvs_btn_on_time_t

  This type is used configure the button on time.
- typedef uint8_t snvs_btn_debounce_t

  This type is used configure the button debounce time.
- typedef uint8_t snvs_btn_press_time_t

  This type is used configure the button press time.

Defines for snvs_btn_config_t

Used to configure which feature of the button (BTN) input signal constitutes "active".

BTN_CONFIG field in the SNVS_HP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_CONFIG_ACTIVELOW 0U

  Button signal is active low.
- #define SNVS_DRV_BTN_CONFIG_ACTIVEHIGH 1U

  Button signal is active high.
- #define SNVS_DRV_BTN_CONFIG_RISINGEDGE 2U

  Button signal is active on the rising edge.
- #define SNVS_DRV_BTN_CONFIG_FALLINGEDGE 3U

  Button signal is active on the falling edge.
- #define SNVS_DRV_BTN_CONFIG_ANYEDGE 4U

  Button signal is active on any edge.

Defines for snvs_btn_on_time_t

Used to configure the period of time after BTN is asserted before SoC power is turned on.

ON_TIME field in the SNVS_LP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_ON_50MS 0U

  500 msec off->on transition time
- #define SNVS_DRV_BTN_ON_100MS 1U

  50 msec off->on transition time
- #define SNVS_DRV_BTN_ON_500MS 2U

  100 msec off->on transition time
- #define SNVS_DRV_BTN_ON_0MS 3U

  0 msec off->on transition time

Defines for snvs_btn_debounce_t

Use to configure the amount of debounce time for the BTN input signal.

DEBOUNCE field in the SNVS_LP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_DEBOUNCE_50MS 0U

  50 msec debounce
- #define SNVS_DRV_BTN_DEBOUNCE_100MS 1U

  100 msec debounce
- #define SNVS_DRV_BTN_DEBOUNCE_500MS 2U

  500 msec debounce
- #define SNVS_DRV_BTN_DEBOUNCE_0MS 3U

  0 msec debounce

Defines for snvs_btn_press_time_t

Used to configure the button press time out values for the PMIC logic.

BTN_PRESS_TIME field in the SNVS_LP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_PRESS_5S 0U

  5 secs
- #define SNVS_DRV_BTN_PRESS_10S 1U

  10 secs
- #define SNVS_DRV_BTN_PRESS_15S 2U

  15 secs
- #define SNVS_DRV_BTN_PRESS_OFF 3U

  Long press disabled.

Initialization Functions

- void SNVS_Init (boot_phase_t phase)

  Initialize SNVS driver.

SRTC Functions

- sc_err_t snvs_err

  SNVS error return.
- void SNVS_PowerOff (void)

  Power off system.
- void SNVS_SetSecureRtc (uint32_t seconds)

  Set the secure RTC.
- void SNVS_GetSecureRtc (uint32_t *seconds)

  Get the secure RTC.
- void SNVS_SetSecureRtcCalb (int8_t count)

  Set the secure RTC calibration value.
- void SNVS_GetSecureRtcCalb (int8_t *count)

  Get the secure RTC calibration value.
- void SNVS_SetSecureRtcAlarm (uint32_t seconds)

  Set secure RTC alarm.
- void SNVS_GetSecureRtcAlarm (uint32_t *seconds)

  Get secure RTC alarm.
- void SNVS_SetRtc (uint32_t seconds)

  Set the RTC.
- void SNVS_GetRtc (uint32_t *seconds)

  Get the RTC.
- void SNVS_SetRtcCalb (int8_t count)

  Set the RTC calibration value.
- void SNVS_SetRtcAlarm (uint32_t seconds)

  Set RTC alarm.
- void SNVS_GetRtcAlarm (uint32_t *seconds)

  Get RTC alarm.
- void SNVS_ConfigButton (snvs_btn_config_t config, sc_bool_t enable)

  Configure the ON/OFF button.
- void SNVS_ButtonTime (snvs_btn_on_time_t on, snvs_btn_debounce_t debounce, snvs_btn_press_time_t press)

  Configure the ON/OFF button timing parameters.
- sc_bool_t SNVS_GetButtonStatus (void)

  Get button status.
- void SNVS_ClearButtonIRQ (void)

  Clear button IRQ.
- void SNVS_EnterLPM (void)

  Enter low power mode.
- void SNVS_ExitLPM (void)

  Exit low power mode.
- uint32_t SNVS_GetState (void)

  Get the SNVS System Security Monitor State (SSM).
- void SNVS_SecurityViolation_Enable (void)

  Enable SNVS Security Violation Interrupt.
- void SNVS_SecurityViolation_IRQHandler (void)

  SNVS security violation IRQ handler.

- void SNVS_PowerOff_IRQHandler (void)

  SNVS power off IRQ handler.
- uint32_t SNVS_ReadGP (uint8_t idx)

  Read a GP register.
- void SNVS_WriteGP (uint8_t idx, uint32_t val)

  Write a GP register.
- void SNVS_SecVio (uint8_t id, uint8_t access, uint32_t *data0, uint32_t *data1, uint32_t *data2, uint32_t *data3, uint32_t *data4, uint8_t size)

  Manage security violation and tamper.
- void SNVS_SecVioDgo (uint8_t id, uint8_t access, uint32_t *data)

  Manage security violation and tamper of DGO.
- void SNVS_IncTime (uint32_t secs)

  Simulation function to increment time.

16.21.1 Detailed Description

Module for the SNVS driver.

It is an MCUXpresso SDK driver for the SNVS module of i.MX devices.

16.21.2 Function Documentation

16.21.2.1 SNVS_Init()

```
void SNVS_Init (
             boot_phase_t phase )
```

Initialize SNVS driver.

This function initializes the SNVS driver.

Parameters

phase	init phase

16.21.2.2 SNVS_PowerOff()

```
void SNVS_PowerOff (
             void  )
```

Power off system.

This function asserts the signal to the PMIC to force a power off.

Examples

board.c.

16.21.2.3 SNVS_SetSecureRtc()

```
void SNVS_SetSecureRtc (
            uint32_t seconds )
```

Set the secure RTC.

This function sets the secure RTC.

Parameters

seconds	time to set

16.21.2.4 SNVS_GetSecureRtc()

```
void SNVS_GetSecureRtc (
            uint32_t * seconds )
```

Get the secure RTC.

This function returns the secure RTC time.

Parameters

seconds	pointer to return seconds

16.21.2.5 SNVS_SetSecureRtcCalb()

```
void SNVS_SetSecureRtcCalb (
            int8_t count )
```

Set the secure RTC calibration value.

This function sets the secure RTC calibration value. See the SNVS section of the SRM for more info.

Parameters

count	counts to add/subtract per 32768 ticks

16.21.2.6 SNVS_GetSecureRtcCalb()

```
void SNVS_GetSecureRtcCalb (
            int8_t * count )
```

Get the secure RTC calibration value.

This function returns the secure RTC calibration value. See the SNVS section of the SRM for more info.

Parameters

count	pointer to return count

16.21.2.7 SNVS_SetSecureRtcAlarm()

```
void SNVS_SetSecureRtcAlarm (
            uint32_t seconds )
```

Set secure RTC alarm.

This function sets the secure RTC alarm and enables it.

Parameters

seconds	alarm to set

If seconds=UINT32_MAX then disable alarm.

16.21.2.8 SNVS_GetSecureRtcAlarm()

```
void SNVS_GetSecureRtcAlarm (
            uint32_t * seconds )
```

Get secure RTC alarm.

This function returns the secure RTC alarm.

Parameters

seconds	pointer to return alarm

16.21.2.9 SNVS_SetRtc()

```
void SNVS_SetRtc (
            uint32_t seconds )
```

Set the RTC.

This function sets the RTC.

Parameters

seconds	time to set

16.21.2.10 SNVS_GetRtc()

```
void SNVS_GetRtc (
            uint32_t * seconds )
```

Get the RTC.

This function returns the RTC time.

Parameters

seconds	pointer to return seconds

16.21.2.11 SNVS_SetRtcCalb()

```
void SNVS_SetRtcCalb (
            int8_t count )
```

Set the RTC calibration value.

This function sets the RTC calibration value. See the SNVS section of the SRM for more info.

Parameters

count	counts to add/subtract per 32768 ticks

16.21.2.12 SNVS_SetRtcAlarm()

```
void SNVS_SetRtcAlarm (
            uint32_t seconds )
```

Set RTC alarm.

This function sets the RTC alarm and enables it.

Parameters

seconds	alarm to set

If seconds=UINT32_MAX then disable alarm.

16.21.2.13 SNVS_GetRtcAlarm()

```
void SNVS_GetRtcAlarm (
             uint32_t * seconds )
```

Get RTC alarm.

This function returns the RTC alarm.

Parameters

seconds	pointer to return alarm

16.21.2.14 SNVS_ConfigButton()

```
void SNVS_ConfigButton (
             snvs_btn_config_t config,
             sc_bool_t enable )
```

Configure the ON/OFF button.

This function configures the button detection and IRQ. See the SNVS section of the SRM for more info.

Parameters

config	button configuration (see BTN_CONFIG in SRM)
enable	button IRQ enable (see BTN_MASK in SRM)

For info on the arguments, see the SNVS section of the SRM.

Examples

board.c.

16.21.2.15 SNVS_ButtonTime()

```
void SNVS_ButtonTime (
             snvs_btn_on_time_t on,
             snvs_btn_debounce_t debounce,
             snvs_btn_press_time_t press )
```

Configure the ON/OFF button timing parameters.

This function configures the button timing parameters. See the SNVS section of the SRM for more info.

Parameters

on	button turn on time (see ON_TIME in SRM)
debounce	button debounce time (see DEBOUNCE in SRM)
press	button turn off time (see BTN_PRESS_TIME in SRM)

For info on the arguments, see the SNVS section of the SRM.

16.21.2.16 SNVS_GetButtonStatus()

```
sc_bool_t SNVS_GetButtonStatus (
             void  )
```

Get button status.

This function returns the status of the button. See the SNVS section of the SRM for more info. BTN in HPSR.

Returns

Returns the button status.

Examples

board.c.

16.21.2.17 SNVS_ClearButtonIRQ()

```
void SNVS_ClearButtonIRQ (
             void  )
```

Clear button IRQ.

This function clears a pending button IRQ.

Examples

board.c.

16.21.2.18 SNVS_EnterLPM()

```
void SNVS_EnterLPM (
             void  )
```

Enter low power mode.

This function prepares the SNVS for low power mode. It copies various data from the HP section to the LP section.

16.21.2.19 SNVS_ExitLPM()

```
void SNVS_ExitLPM (
             void  )
```

Exit low power mode.

This function restores SNVS data from the LP section to the HP section.

16.21.2.20 SNVS_GetState()

```
uint32_t SNVS_GetState (
             void  )
```

Get the SNVS System Security Monitor State (SSM).

This function returns the System Security Monitor State (SSM). See the SNVS section of the SRM for more info. SS↩ M_ST in HPSR.

Returns

Returns the state of the monitor.

16.21.2.21 SNVS_SecurityViolation_Enable()

```
void SNVS_SecurityViolation_Enable (
             void  )
```

Enable SNVS Security Violation Interrupt.

This function is used to re-enable the security violation interrupt. The interrupt is automatically masked when the interrupt occurs.

16.21.2.22 SNVS_SecurityViolation_IRQHandler()

```
void SNVS_SecurityViolation_IRQHandler (
             void  )
```

SNVS security violation IRQ handler.

This function is called when the security violation IRQ is asserted. It automatically masks the security violation interrupt which must then be re-enabled using SNVS_SecurityViolation_Enable().

16.21.2.23 SNVS_PowerOff_IRQHandler()

```
void SNVS_PowerOff_IRQHandler (
            void  )
```

SNVS power off IRQ handler.

This function is called when the power off IRQ is asserted.

16.21.2.24 SNVS_ReadGP()

```
uint32_t SNVS_ReadGP (
            uint8_t idx )
```

Read a GP register.

This function is called read from one of the four GP registers.

Parameters

idx	index of register to read (0-3)

Returns

Returns the stored value.

16.21.2.25 SNVS_WriteGP()

```
void SNVS_WriteGP (
            uint8_t idx,
            uint32_t val )
```

Write a GP register.

Parameters

idx	index of register to write (0-3)
val	value to write

This function is called write to one of the four GP registers.

16.21.2.26 SNVS_SecVio()

```
void SNVS_SecVio (
```

```
            uint8_t id,
            uint8_t access,
            uint32_t * data0,
            uint32_t * data1,
            uint32_t * data2,
            uint32_t * data3,
            uint32_t * data4,
            uint8_t size )
```

Manage security violation and tamper.

Parameters

id	index of register(s) to access
access	read or write
data0	value 0 to read or write
data1	value 1 to read or write
data2	value 2 to read or write
data3	value 3 to read or write
data4	value 4 to read or write
size	number of value to access

Set dataX to NULL if not used.

This function is called to read/write security violation and tamper registers. See the SECO API Reference Guide for more info.

16.21.2.27 SNVS_SecVioDgo()

```
void SNVS_SecVioDgo (
            uint8_t id,
            uint8_t access,
            uint32_t * data )
```

Manage security violation and tamper of DGO.

Parameters

id	index of register to access
access	read or write
data	value to read or write

This function is called to read/write security violation and tamper DGO registers. See the SECO API Reference Guide for more info.

16.21.2.28 SNVS_IncTime()

```
void SNVS_IncTime (
            uint32_t secs )
```

Simulation function to increment time.

Parameters

secs	seconds to increment

16.22 WDOG32: 32-bit Watchdog Timer

Files

- file fsl_wdog32.h

Data Structures

- struct wdog32_work_mode_t

  Defines WDOG32 work mode.
- struct wdog32_config_t

  Describes WDOG32 configuration structure.

Enumerations

- enum wdog32_clock_source_t { kWDOG32_ClockSource0 = 0U, kWDOG32_ClockSource1 = 1U, kWDOG32_ClockSource2 = 2U, kWDOG32_ClockSource3 = 3U }

  Describes WDOG32 clock source.
- enum wdog32_clock_prescaler_t { kWDOG32_ClockPrescalerDivide1 = 0x0U, kWDOG32_ClockPrescalerDivide256 = 0x1U }

  Describes the selection of the clock prescaler.
- enum wdog32_test_mode_t { kWDOG32_TestModeDisabled = 0U, kWDOG32_UserModeEnabled = 1U, kWDOG32_LowByteTest = 2U, kWDOG32_HighByteTest = 3U }

  Describes WDOG32 test mode.
- enum _wdog32_interrupt_enable_t { kWDOG32_InterruptEnable = WDOG_CS_INT_MASK }

  WDOG32 interrupt configuration structure.
- enum _wdog32_status_flags_t { kWDOG32_RunningFlag = WDOG_CS_EN_MASK, kWDOG32_InterruptFlag = WDOG_CS_FLG_MASK }

  WDOG32 status flags.

Unlock sequence

- #define WDOG_FIRST_WORD_OF_UNLOCK (WDOG_UPDATE_KEY & 0xFFFFU)

  First word of unlock sequence.
- #define WDOG_SECOND_WORD_OF_UNLOCK ((WDOG_UPDATE_KEY >> 16U) & 0xFFFFU)

  Second word of unlock sequence.

Refresh sequence

- #define WDOG_FIRST_WORD_OF_REFRESH (WDOG_REFRESH_KEY & 0xFFFFU)

  First word of refresh sequence.
- #define WDOG_SECOND_WORD_OF_REFRESH ((WDOG_REFRESH_KEY >> 16U) & 0xFFFFU)

  Second word of refresh sequence.

Driver version

- #define FSL_WDOG32_DRIVER_VERSION (MAKE_VERSION(2, 0, 3))

  WDOG32 driver version.

WDOG32 Initialization and De-initialization

- void WDOG32_GetDefaultConfig (wdog32_config_t *config)

  Initializes the WDOG32 configuration structure.
- AT_QUICKACCESS_SECTION_CODE (void WDOG32_Init(WDOG_Type *base, const wdog32_config_t *config))

  Initializes the WDOG32 module.
- void WDOG32_Deinit (WDOG_Type *base)

  De-initializes the WDOG32 module.

WDOG32 functional Operation

- static void WDOG32_Enable (WDOG_Type *base)

  Enables the WDOG32 module.
- static void WDOG32_Disable (WDOG_Type *base)

  Disables the WDOG32 module.
- static void WDOG32_EnableInterrupts (WDOG_Type *base, uint32_t mask)

  Enables the WDOG32 interrupt.
- static void WDOG32_DisableInterrupts (WDOG_Type *base, uint32_t mask)

  Disables the WDOG32 interrupt.
- static uint32_t WDOG32_GetStatusFlags (WDOG_Type *base)

  Gets the WDOG32 all status flags.
- AT_QUICKACCESS_SECTION_CODE (void WDOG32_ClearStatusFlags(WDOG_Type *base, uint32_t mask))

  Clears the WDOG32 flag.
- static void WDOG32_SetTimeoutValue (WDOG_Type *base, uint16_t timeoutCount)

  Sets the WDOG32 timeout value.
- static void WDOG32_SetWindowValue (WDOG_Type *base, uint16_t windowValue)

  Sets the WDOG32 window value.
- static void WDOG32_Unlock (WDOG_Type *base)

  Unlocks the WDOG32 register written.
- static void WDOG32_Refresh (WDOG_Type *base)

  Refreshes the WDOG32 timer.
- static uint16_t WDOG32_GetCounterValue (WDOG_Type *base)

  Gets the WDOG32 counter value.

16.22.1 Detailed Description

The MCUXpresso SDK provides a peripheral driver for the WDOG32 module of MCUXpresso SDK devices.

16.22.2 Typical use case

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/wdog32

16.22.3 Enumeration Type Documentation

16.22.3.1 wdog32_clock_source_t

`enum wdog32_clock_source_t`

Describes WDOG32 clock source.

Enumerator

kWDOG32_ClockSource0	Clock source 0.
kWDOG32_ClockSource1	Clock source 1.
kWDOG32_ClockSource2	Clock source 2.
kWDOG32_ClockSource3	Clock source 3.

16.22.3.2 wdog32_clock_prescaler_t

`enum wdog32_clock_prescaler_t`

Describes the selection of the clock prescaler.

Enumerator

kWDOG32_ClockPrescalerDivide1	Divided by 1.
kWDOG32_ClockPrescalerDivide256	Divided by 256.

16.22.3.3 wdog32_test_mode_t

`enum wdog32_test_mode_t`

Describes WDOG32 test mode.

Enumerator

kWDOG32_TestModeDisabled	Test Mode disabled.
kWDOG32_UserModeEnabled	User Mode enabled.
kWDOG32_LowByteTest	Test Mode enabled, only low byte is used.
kWDOG32_HighByteTest	Test Mode enabled, only high byte is used.

16.22.3.4 _wdog32_interrupt_enable_t

```
enum _wdog32_interrupt_enable_t
```

WDOG32 interrupt configuration structure.

This structure contains the settings for all of the WDOG32 interrupt configurations.

Enumerator

kWDOG32_InterruptEnable	Interrupt is generated before forcing a reset.

16.22.3.5 _wdog32_status_flags_t

```
enum _wdog32_status_flags_t
```

WDOG32 status flags.

This structure contains the WDOG32 status flags for use in the WDOG32 functions.

Enumerator

kWDOG32_RunningFlag	Running flag, set when WDOG32 is enabled.
kWDOG32_InterruptFlag	Interrupt flag, set when interrupt occurs.

16.22.4 Function Documentation

16.22.4.1 WDOG32_GetDefaultConfig()

```
void WDOG32_GetDefaultConfig (
            wdog32_config_t * config )
```

Initializes the WDOG32 configuration structure.

This function initializes the WDOG32 configuration structure to default values. The default values are:

```
wdog32Config->enableWdog32 = true;
wdog32Config->clockSource = kWDOG32_ClockSource1;
wdog32Config->prescaler = kWDOG32_ClockPrescalerDivide1;
wdog32Config->workMode.enableWait = true;
wdog32Config->workMode.enableStop = false;
wdog32Config->workMode.enableDebug = false;
wdog32Config->testMode = kWDOG32_TestModeDisabled;
wdog32Config->enableUpdate = true;
wdog32Config->enableInterrupt = false;
wdog32Config->enableWindowMode = false;
wdog32Config->windowValue = 0U;
wdog32Config->timeoutValue = 0xFFFFU;
```

Parameters

config	Pointer to the WDOG32 configuration structure.

See also

wdog32_config_t

16.22.4.2 AT_QUICKACCESS_SECTION_CODE() [1/2]

```
AT_QUICKACCESS_SECTION_CODE (
             void  WDOG32_InitWDOG_Type *base, const wdog32_config_t *config )
```

Initializes the WDOG32 module.

This function initializes the WDOG32. To reconfigure the WDOG32 without forcing a reset first, enableUpdate must be set to true in the configuration.

Example:

```
wdog32_config_t config;
WDOG32_GetDefaultConfig(&config);
config.timeoutValue = 0x7ffU;
config.enableUpdate = true;
WDOG32_Init(wdog_base,&config);
```

Parameters

base	WDOG32 peripheral base address.
config	The configuration of the WDOG32.

16.22.4.3 WDOG32_Deinit()

```
void WDOG32_Deinit (
             WDOG_Type * base )
```

De-initializes the WDOG32 module.

This function shuts down the WDOG32. Ensure that the WDOG_CS.UPDATE is 1, which means that the register update is enabled.

Parameters

base	WDOG32 peripheral base address.

16.22.4.4 WDOG32_Enable()

```
static void WDOG32_Enable (
            WDOG_Type * base )  [inline], [static]
```

Enables the WDOG32 module.

This function writes a value into the WDOG_CS register to enable the WDOG32. The WDOG_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

base	WDOG32 peripheral base address.

16.22.4.5 WDOG32_Disable()

```
static void WDOG32_Disable (
            WDOG_Type * base )  [inline], [static]
```

Disables the WDOG32 module.

This function writes a value into the WDOG_CS register to disable the WDOG32. The WDOG_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

base	WDOG32 peripheral base address

Examples

board.c.

16.22.4.6 WDOG32_EnableInterrupts()

```
static void WDOG32_EnableInterrupts (
            WDOG_Type * base,
            uint32_t mask )  [inline], [static]
```

Enables the WDOG32 interrupt.

This function writes a value into the WDOG_CS register to enable the WDOG32 interrupt. The WDOG_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

base	WDOG32 peripheral base address.
mask	The interrupts to enable. The parameter can be a combination of the following source if defined: • kWDOG32_InterruptEnable

16.22.4.7 WDOG32_DisableInterrupts()

```
static void WDOG32_DisableInterrupts (
             WDOG_Type * base,
             uint32_t mask )  [inline], [static]
```

Disables the WDOG32 interrupt.

This function writes a value into the WDOG_CS register to disable the WDOG32 interrupt. The WDOG_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

base	WDOG32 peripheral base address.
mask	The interrupts to disabled. The parameter can be a combination of the following source if defined: • kWDOG32_InterruptEnable

16.22.4.8 WDOG32_GetStatusFlags()

```
static uint32_t WDOG32_GetStatusFlags (
             WDOG_Type * base )  [inline], [static]
```

Gets the WDOG32 all status flags.

This function gets all status flags.

Example to get the running flag:

```
uint32_t status;
status = WDOG32_GetStatusFlags(wdog_base) & kWDOG32_RunningFlag;
```

Parameters

base	WDOG32 peripheral base address

Returns

State of the status flag: asserted (true) or not-asserted (false).

See also

_wdog32_status_flags_t

- true: related status flag has been set.
- false: related status flag is not set.

16.22.4.9 AT_QUICKACCESS_SECTION_CODE() [2/2]

```
AT_QUICKACCESS_SECTION_CODE (
            void  WDOG32_ClearStatusFlagsWDOG_Type *base, uint32_t mask )
```

Clears the WDOG32 flag.

This function clears the WDOG32 status flag.

Example to clear an interrupt flag:
```
WDOG32_ClearStatusFlags(wdog_base,kWDOG32_InterruptFlag);
```

Parameters

base	WDOG32 peripheral base address.
mask	The status flags to clear. The parameter can be any combination of the following values: • kWDOG32_InterruptFlag

16.22.4.10 WDOG32_SetTimeoutValue()

```
static void WDOG32_SetTimeoutValue (
            WDOG_Type * base,
            uint16_t timeoutCount )  [inline], [static]
```

Sets the WDOG32 timeout value.

This function writes a timeout value into the WDOG_TOVAL register. The WDOG_TOVAL register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

base	WDOG32 peripheral base address
timeoutCount	WDOG32 timeout value, count of WDOG32 clock ticks.

Examples

board.c.

16.22.4.11 WDOG32_SetWindowValue()

```
static void WDOG32_SetWindowValue (
             WDOG_Type * base,
             uint16_t windowValue )  [inline], [static]
```

Sets the WDOG32 window value.

This function writes a window value into the WDOG_WIN register. The WDOG_WIN register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

base	WDOG32 peripheral base address.
windowValue	WDOG32 window value.

16.22.4.12 WDOG32_Unlock()

```
static void WDOG32_Unlock (
             WDOG_Type * base )  [inline], [static]
```

Unlocks the WDOG32 register written.

This function unlocks the WDOG32 register written.

Before starting the unlock sequence and following the configuration, disable the global interrupts. Otherwise, an interrupt could effectively invalidate the unlock sequence and the WCT may expire. After the configuration finishes, re-enable the global interrupts.

Parameters

base	WDOG32 peripheral base address

Examples

board.c.

References WDOG_FIRST_WORD_OF_UNLOCK, and WDOG_SECOND_WORD_OF_UNLOCK.

16.22.4.13 WDOG32_Refresh()

```
static void WDOG32_Refresh (
            WDOG_Type * base )  [inline], [static]
```

Refreshes the WDOG32 timer.

This function feeds the WDOG32. This function should be called before the Watchdog timer is in timeout. Otherwise, a reset is asserted.

Parameters

base	WDOG32 peripheral base address

References WDOG_FIRST_WORD_OF_REFRESH, and WDOG_SECOND_WORD_OF_REFRESH.

16.22.4.14 WDOG32_GetCounterValue()

```
static uint16_t WDOG32_GetCounterValue (
            WDOG_Type * base )  [inline], [static]
```

Gets the WDOG32 counter value.

This function gets the WDOG32 counter value.

Parameters

base	WDOG32 peripheral base address.

Returns

Current WDOG32 counter value.

16.23 MISC: Miscellaneous Service

Module for the Miscellaneous (MISC) service.

Macros

- #define SC_MISC_DMA_GRP_MAX 31U

  Max DMA channel priority group.

Typedefs

- typedef uint8_t sc_misc_dma_group_t

  This type is used to store a DMA channel priority group.
- typedef uint8_t sc_misc_boot_status_t

  This type is used report boot status.
- typedef uint8_t sc_misc_temp_t

  This type is used report boot status.
- typedef uint8_t sc_misc_bt_t

  This type is used report the boot type.

Defines for type widths

- #define SC_MISC_DMA_GRP_W 5U

  Width of sc_misc_dma_group_t.

Defines for sc_misc_boot_status_t

- #define SC_MISC_BOOT_STATUS_SUCCESS 0U

  Success.
- #define SC_MISC_BOOT_STATUS_SECURITY 1U

  Security violation.

Defines for sc_misc_temp_t

- #define SC_MISC_TEMP 0U

  Temp sensor.
- #define SC_MISC_TEMP_HIGH 1U

  Temp high alarm.
- #define SC_MISC_TEMP_LOW 2U

  Temp low alarm.

Defines for sc_misc_bt_t

- #define SC_MISC_BT_PRIMARY 0U

  Primary boot.
- #define SC_MISC_BT_SECONDARY 1U

  Secondary boot.
- #define SC_MISC_BT_RECOVERY 2U

  Recovery boot.
- #define SC_MISC_BT_MANUFACTURE 3U

  Manufacture boot.
- #define SC_MISC_BT_SERIAL 4U

  Serial boot.

Control Functions

- sc_err_t sc_misc_set_control (sc_ipc_t ipc, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t val)

  This function sets a miscellaneous control value.
- sc_err_t sc_misc_get_control (sc_ipc_t ipc, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t *val)

  This function gets a miscellaneous control value.

DMA Functions

- sc_err_t sc_misc_set_max_dma_group (sc_ipc_t ipc, sc_rm_pt_t pt, sc_misc_dma_group_t max)

  This function configures the max DMA channel priority group for a partition.
- sc_err_t sc_misc_set_dma_group (sc_ipc_t ipc, sc_rsrc_t resource, sc_misc_dma_group_t group)

  This function configures the priority group for a DMA channel.

Debug Functions

- void sc_misc_debug_out (sc_ipc_t ipc, uint8_t ch)

  This function is used output a debug character from the SCU UART.
- sc_err_t sc_misc_waveform_capture (sc_ipc_t ipc, sc_bool_t enable)

  This function starts/stops emulation waveform capture.
- void sc_misc_build_info (sc_ipc_t ipc, uint32_t *build, uint32_t *commit)

  This function is used to return the SCFW build info.
- void sc_misc_api_ver (sc_ipc_t ipc, uint16_t *cl_maj, uint16_t *cl_min, uint16_t *sv_maj, uint16_t *sv_min)

  This function is used to return the SCFW API versions.
- void sc_misc_unique_id (sc_ipc_t ipc, uint32_t *id_l, uint32_t *id_h)

  This function is used to return the device's unique ID.

Other Functions

- sc_err_t sc_misc_set_ari (sc_ipc_t ipc, sc_rsrc_t resource, sc_rsrc_t resource_mst, uint16_t ari, sc_bool_t enable)

  This function configures the ARI match value for PCIe/SATA resources.
- void sc_misc_boot_status (sc_ipc_t ipc, sc_misc_boot_status_t status)

  This function reports boot status.
- sc_err_t sc_misc_boot_done (sc_ipc_t ipc, sc_rsrc_t cpu)

  This function tells the SCFW that a CPU is done booting.
- sc_err_t sc_misc_otp_fuse_read (sc_ipc_t ipc, uint32_t word, uint32_t *val)

  This function reads a given fuse word index.
- sc_err_t sc_misc_otp_fuse_write (sc_ipc_t ipc, uint32_t word, uint32_t val)

  This function writes a given fuse word index.
- sc_err_t sc_misc_set_temp (sc_ipc_t ipc, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t celsius, int8_t tenths)

  This function sets a temp sensor alarm.
- sc_err_t sc_misc_get_temp (sc_ipc_t ipc, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t *celsius, int8_t *tenths)

  This function gets a temp sensor value.
- void sc_misc_get_boot_dev (sc_ipc_t ipc, sc_rsrc_t *dev)

  This function returns the boot device.
- sc_err_t sc_misc_get_boot_type (sc_ipc_t ipc, sc_misc_bt_t *type)

  This function returns the boot type.
- sc_err_t sc_misc_get_boot_container (sc_ipc_t ipc, uint8_t *idx)

  This function returns the boot container index.
- void sc_misc_get_button_status (sc_ipc_t ipc, sc_bool_t *status)

  This function returns the current status of the ON/OFF button.
- sc_err_t sc_misc_rompatch_checksum (sc_ipc_t ipc, uint32_t *checksum)

  This function returns the ROM patch checksum.
- sc_err_t sc_misc_board_ioctl (sc_ipc_t ipc, uint32_t *parm1, uint32_t *parm2, uint32_t *parm3)

  This function calls the board IOCTL function.

Internal Functions

- void misc_init (sc_bool_t api_phase)

  Internal SC function to initializes the MISC service.
- sc_err_t misc_set_control (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t val)

  Internal SC function to set a miscellaneous control value.
- sc_err_t misc_get_control (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t *val)

  Internal SC function to get a miscellaneous control value.
- sc_err_t misc_set_ari (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rsrc_t resource_mst, uint16_t ari, sc_bool_t enable)

  Internal SC function to configure the ARI translation for PCIe/SATA resources.
- sc_err_t misc_set_max_dma_group (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_misc_dma_group_t max)

  Internal SC function to configure max DMA channel priority group for a partition.
- sc_err_t misc_set_dma_group (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_misc_dma_group_t group)

  Internal SC function to configure the priority group for a DMA channel.
- void misc_boot_status (sc_rm_pt_t caller_pt, sc_misc_boot_status_t status)

Internal SC function to report boot status.

- sc_err_t misc_boot_done (sc_rm_pt_t caller_pt, sc_rsrc_t cpu)

  Internal SC function to report a CPU has finished initialization.
- sc_err_t misc_boot_done_wait (sc_rsrc_t cpu)

  Internal SC function to wait for a CPU to be done booting.
- sc_err_t misc_waveform_capture (sc_rm_pt_t caller_pt, sc_bool_t enable)

  Internal SC function to start/stop emulation waveform capture.
- void misc_debug_out (sc_rm_pt_t caller_pt, uint8_t ch)

  Internal SC function to output a debug charcter.
- sc_err_t misc_otp_fuse_read (sc_rm_pt_t caller_pt, uint32_t word, uint32_t *val)

  Internal SC function to read otp fuse word.
- sc_err_t misc_otp_fuse_write (sc_rm_pt_t caller_pt, uint32_t word, uint32_t val)

  Internal SC function to write otp fuse word.
- sc_bool_t misc_has_temp (sc_rsrc_t resource)

  This function reports if a resource has a temp sensor.
- sc_err_t misc_set_temp (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t celsius, int8_t tenths)

  Internal SC function to set a temp sensor alarm.
- sc_err_t misc_get_temp (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t *celsius, int8_t *tenths)

  Internal SC function to get a temp sensor value.
- void misc_build_info (sc_rm_pt_t caller_pt, uint32_t *build, uint32_t *commit)

  Internal SC function to return SCFW build info.
- void misc_unique_id (sc_rm_pt_t caller_pt, uint32_t *id_l, uint32_t *id_h)

  Internal SC function to return the device unique ID.
- void misc_get_boot_dev (sc_rm_pt_t caller_pt, sc_rsrc_t *dev)

  Internal SC function to return the boot device.
- sc_err_t misc_get_boot_type (sc_rm_pt_t caller_pt, sc_misc_bt_t *type)

  Internal SC function to return the boot type.
- sc_err_t misc_get_boot_container (sc_rm_pt_t caller_pt, uint8_t *idx)

  Internal SC function to return the boot container index.
- void misc_get_button_status (sc_rm_pt_t caller_pt, sc_bool_t *status)

  Internal SC function to return the current status of the ON/OFF button.
- sc_err_t misc_rompatch_checksum (sc_rm_pt_t caller_pt, uint32_t *checksum)

  Internal SC function to return the ROM patch checksum.
- sc_err_t misc_board_ioctl (sc_rsrc_t mu, uint32_t *parm1, uint32_t *parm2, uint32_t *parm3)

  Internal SC function to call board IOCTL.
- void misc_api_ver (sc_rm_pt_t caller_pt, uint16_t *cl_maj, uint16_t *cl_min, uint16_t *sv_maj, uint16_t *sv_min)

  Internal SC function to return API version info.

16.23.1 Detailed Description

Module for the Miscellaneous (MISC) service.

16.23.2 Function Documentation

16.23.2.1 sc_misc_set_control()

```
sc_err_t sc_misc_set_control (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_ctrl_t ctrl,
             uint32_t val )
```

This function sets a miscellaneous control value.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource the control is associated with
in	*ctrl*	control to change
in	*val*	value to apply to the control

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner

Refer to the Control List for valid control values.

16.23.2.2 sc_misc_get_control()

```
sc_err_t sc_misc_get_control (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_ctrl_t ctrl,
             uint32_t * val )
```

This function gets a miscellaneous control value.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource the control is associated with
in	*ctrl*	control to get
out	*val*	pointer to return the control value

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner

Refer to the Control List for valid control values.

16.23.2.3 sc_misc_set_max_dma_group()

```
sc_err_t sc_misc_set_max_dma_group (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_misc_dma_group_t max )
```

This function configures the max DMA channel priority group for a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to assign *max*
in	*max*	max priority group (0-31)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the parent of the affected partition

Valid *max* range is 0-31 with 0 being the lowest and 31 the highest. Default is the max priority group for the parent partition of *pt*.

16.23.2.4 sc_misc_set_dma_group()

```
sc_err_t sc_misc_set_dma_group (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_misc_dma_group_t group )
```

This function configures the priority group for a DMA channel.

Parameters

in	*ipc*	IPC handle
in	*resource*	DMA channel resource
in	*group*	priority group (0-31)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the owner or parent of the owner of the DMA channel

Valid *group* range is 0-31 with 0 being the lowest and 31 the highest. The max value of *group* is limited by the partition max set using sc_misc_set_max_dma_group().

16.23.2.5 sc_misc_debug_out()

```
void sc_misc_debug_out (
            sc_ipc_t ipc,
            uint8_t ch )
```

This function is used output a debug character from the SCU UART.

Parameters

in	*ipc*	IPC handle
in	*ch*	character to output

16.23.2.6 sc_misc_waveform_capture()

```
sc_err_t sc_misc_waveform_capture (
            sc_ipc_t ipc,
            sc_bool_t enable )
```

This function starts/stops emulation waveform capture.

Parameters

in	*ipc*	IPC handle
in	*enable*	flag to enable/disable capture

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_UNAVAILABLE if not running on emulation

16.23.2.7 sc_misc_build_info()

```
void sc_misc_build_info (
            sc_ipc_t ipc,
            uint32_t * build,
            uint32_t * commit )
```

This function is used to return the SCFW build info.

Parameters

in	*ipc*	IPC handle
out	*build*	pointer to return build number
out	*commit*	pointer to return commit ID (git SHA-1)

16.23.2.8 sc_misc_api_ver()

```
void sc_misc_api_ver (
            sc_ipc_t ipc,
            uint16_t * cl_maj,
            uint16_t * cl_min,
            uint16_t * sv_maj,
            uint16_t * sv_min )
```

This function is used to return the SCFW API versions.

Parameters

in	*ipc*	IPC handle
out	*cl_maj*	pointer to return major part of client version
out	*cl_min*	pointer to return minor part of client version
out	*sv_maj*	pointer to return major part of SCFW version
out	*sv_min*	pointer to return minor part of SCFW version

Client version is the version of the API ported to and used by the caller. SCFW version is the version of the SCFW

binary running on the CPU.

Note a major version difference indicates a break in compatibility.

16.23.2.9 sc_misc_unique_id()

```
void sc_misc_unique_id (
            sc_ipc_t ipc,
            uint32_t * id_l,
            uint32_t * id_h )
```

This function is used to return the device's unique ID.

Parameters

in	*ipc*	IPC handle
out	*id_l*	pointer to return lower 32-bit of ID [31:0]
out	*id_h*	pointer to return upper 32-bits of ID [63:32]

16.23.2.10 sc_misc_set_ari()

```
sc_err_t sc_misc_set_ari (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_rsrc_t resource_mst,
            uint16_t ari,
            sc_bool_t enable )
```

This function configures the ARI match value for PCIe/SATA resources.

Parameters

in	*ipc*	IPC handle
in	*resource*	match resource
in	*resource_mst*	PCIe/SATA master to match
in	*ari*	ARI to match
in	*enable*	enable match or not

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,

- SC_ERR_NOACCESS if caller's partition is not the owner or parent of the owner of the resource and translation

For PCIe, the ARI is the 16-bit value that includes the bus number, device number, and function number. For SATA, this value includes the FISType and PM_Port.

16.23.2.11 sc_misc_boot_status()

```
void sc_misc_boot_status (
             sc_ipc_t ipc,
             sc_misc_boot_status_t status )
```

This function reports boot status.

Parameters

in	*ipc*	IPC handle
in	*status*	boot status

This is used by SW partitions to report status of boot. This is normally used to report a boot failure.

16.23.2.12 sc_misc_boot_done()

```
sc_err_t sc_misc_boot_done (
             sc_ipc_t ipc,
             sc_rsrc_t cpu )
```

This function tells the SCFW that a CPU is done booting.

Parameters

in	*ipc*	IPC handle
in	*cpu*	CPU that is done booting

This is called by early booting CPUs to report they are done with initialization. After starting early CPUs, the SCFW halts the booting process until they are done. During this time, early CPUs can call the SCFW with lower latency as the SCFW is idle.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the CPU owner

16.23.2.13 sc_misc_otp_fuse_read()

```
sc_err_t sc_misc_otp_fuse_read (
             sc_ipc_t ipc,
             uint32_t word,
             uint32_t * val )
```

This function reads a given fuse word index.

Parameters

in	*ipc*	IPC handle
in	*word*	fuse word index
out	*val*	fuse read value

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid
- SC_ERR_NOACCESS if read operation failed
- SC_ERR_LOCKED if read operation is locked

16.23.2.14 sc_misc_otp_fuse_write()

```
sc_err_t sc_misc_otp_fuse_write (
             sc_ipc_t ipc,
             uint32_t word,
             uint32_t val )
```

This function writes a given fuse word index.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can do this.

Parameters

in	*ipc*	IPC handle
in	*word*	fuse word index
in	*val*	fuse write value

The command is passed as is to SECO. SECO uses part of the *word* parameter to indicate if the fuse should be locked after programming. See the "Write common fuse" section of the SECO API Reference Guide for more info.

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid
- SC_ERR_NOACCESS if caller does not have SC_R_SYSTEM access
- SC_ERR_NOACCESS if write operation failed
- SC_ERR_LOCKED if write operation is locked

16.23.2.15 sc_misc_set_temp()

```
sc_err_t sc_misc_set_temp (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_misc_temp_t temp,
            int16_t celsius,
            int8_t tenths )
```

This function sets a temp sensor alarm.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource with sensor
in	*temp*	alarm to set
in	*celsius*	whole part of temp to set
in	*tenths*	fractional part of temp to set

Returns

Returns and error code (SC_ERR_NONE = success).

This function will enable the alarm interrupt if the temp requested is not the min/max temp. This enable automatically clears when the alarm occurs and this function has to be called again to re-enable.

Return errors codes:

- SC_ERR_PARM if parameters invalid
- SC_ERR_NOACCESS if caller does not own the resource
- SC_ERR_NOPOWER if power domain of resource not powered

16.23.2.16 sc_misc_get_temp()

```
sc_err_t sc_misc_get_temp (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_misc_temp_t temp,
             int16_t * celsius,
             int8_t * tenths )
```

This function gets a temp sensor value.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource with sensor
in	*temp*	value to get (sensor or alarm)
out	*celsius*	whole part of temp to get
out	*tenths*	fractional part of temp to get

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if parameters invalid
- SC_ERR_BUSY if temp not ready yet (time delay after power on)
- SC_ERR_NOPOWER if power domain of resource not powered

16.23.2.17 sc_misc_get_boot_dev()

```
void sc_misc_get_boot_dev (
             sc_ipc_t ipc,
             sc_rsrc_t * dev )
```

This function returns the boot device.

Parameters

in	*ipc*	IPC handle
out	*dev*	pointer to return boot device

16.23.2.18 sc_misc_get_boot_type()

```
sc_err_t sc_misc_get_boot_type (
             sc_ipc_t ipc,
             sc_misc_bt_t * type )
```

This function returns the boot type.

Parameters

in	*ipc*	IPC handle
out	*type*	pointer to return boot type

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors code:

- SC_ERR_UNAVAILABLE if type not passed by ROM

16.23.2.19 sc_misc_get_boot_container()

```
sc_err_t sc_misc_get_boot_container (
             sc_ipc_t ipc,
             uint8_t * idx )
```

This function returns the boot container index.

Parameters

in	*ipc*	IPC handle
out	*idx*	pointer to return index

Return *idx* = 1 for first container, 2 for second.

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors code:

- SC_ERR_UNAVAILABLE if index not passed by ROM

16.23.2.20 sc_misc_get_button_status()

```
void sc_misc_get_button_status (
            sc_ipc_t ipc,
            sc_bool_t * status )
```

This function returns the current status of the ON/OFF button.

Parameters

in	*ipc*	IPC handle
out	*status*	pointer to return button status

16.23.2.21 sc_misc_rompatch_checksum()

```
sc_err_t sc_misc_rompatch_checksum (
            sc_ipc_t ipc,
            uint32_t * checksum )
```

This function returns the ROM patch checksum.

Parameters

in	*ipc*	IPC handle
out	*checksum*	pointer to return checksum

Returns

Returns and error code (SC_ERR_NONE = success).

16.23.2.22 sc_misc_board_ioctl()

```
sc_err_t sc_misc_board_ioctl (
            sc_ipc_t ipc,
            uint32_t * parm1,
            uint32_t * parm2,
            uint32_t * parm3 )
```

This function calls the board IOCTL function.

Parameters

in	*ipc*	IPC handle
in,out	*parm1*	pointer to pass parameter 1
in,out	*parm2*	pointer to pass parameter 2
in,out	*parm3*	pointer to pass parameter 3

Returns

Returns and error code (SC_ERR_NONE = success).

16.23.2.23 misc_init()

```
void misc_init (
            sc_bool_t api_phase )
```

Internal SC function to initializes the MISC service.

Parameters

in	*api_phase*	init phase

Initializes the API if /a api_phase = SC_TRUE, otherwise initializes the HW managed by the MISC service. API must be initialized before anything else is done with the service.

16.23.2.24 misc_set_control()

```
sc_err_t misc_set_control (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_ctrl_t ctrl,
            uint32_t val )
```

Internal SC function to set a miscellaneous control value.

See also

sc_misc_set_control().

16.23.2.25 misc_get_control()

```
sc_err_t misc_get_control (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_ctrl_t ctrl,
            uint32_t * val )
```

Internal SC function to get a miscellaneous control value.

See also

sc_misc_get_control().

16.23.2.26 misc_set_ari()

```
sc_err_t misc_set_ari (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_rsrc_t resource_mst,
             uint16_t ari,
             sc_bool_t enable )
```

Internal SC function to configure the ARI translation for PCIe/SATA resources.

See also

sc_misc_set_ari().

16.23.2.27 misc_set_max_dma_group()

```
sc_err_t misc_set_max_dma_group (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_misc_dma_group_t max )
```

Internal SC function to configure max DMA channel priority group for a partition.

See also

sc_misc_set_max_dma_group().

16.23.2.28 misc_set_dma_group()

```
sc_err_t misc_set_dma_group (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_misc_dma_group_t group )
```

Internal SC function to configure the priority group for a DMA channel.

See also

sc_misc_set_dma_group().

16.23.2.29 misc_boot_status()

```
void misc_boot_status (
            sc_rm_pt_t caller_pt,
            sc_misc_boot_status_t status )
```

Internal SC function to report boot status.

See also

sc_misc_boot_status().

16.23.2.30 misc_boot_done()

```
sc_err_t misc_boot_done (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t cpu )
```

Internal SC function to report a CPU has finished initialization.

See also

sc_misc_boot_done().

16.23.2.31 misc_boot_done_wait()

```
sc_err_t misc_boot_done_wait (
            sc_rsrc_t cpu )
```

Internal SC function to wait for a CPU to be done booting.

Parameters

in	*cpu*	CPU to wait for

Returns

Returns an error code (SC_ERR_NONE = success).

16.23.2.32 misc_waveform_capture()

```
sc_err_t misc_waveform_capture (
            sc_rm_pt_t caller_pt,
            sc_bool_t enable )
```

Internal SC function to start/stop emulation waveform capture.

See also

sc_misc_waveform_capture().

16.23.2.33 misc_debug_out()

```
void misc_debug_out (
            sc_rm_pt_t caller_pt,
            uint8_t ch )
```

Internal SC function to output a debug charcter.

See also

sc_misc_debug_out().

16.23.2.34 misc_otp_fuse_read()

```
sc_err_t misc_otp_fuse_read (
            sc_rm_pt_t caller_pt,
            uint32_t word,
            uint32_t * val )
```

Internal SC function to read otp fuse word.

See also

sc_misc_otp_fuse_read().

16.23.2.35 misc_otp_fuse_write()

```
sc_err_t misc_otp_fuse_write (
            sc_rm_pt_t caller_pt,
            uint32_t word,
            uint32_t val )
```

Internal SC function to write otp fuse word.

See also

sc_misc_otp_fuse_write().

16.23.2.36 misc_has_temp()

```
sc_bool_t misc_has_temp (
            sc_rsrc_t resource )
```

This function reports if a resource has a temp sensor.

Parameters

in	*resource*	resource to querry

Returns

Returns SC_TRUE if the subsystem containing /a resource has a temp sensor.

16.23.2.37 misc_set_temp()

```
sc_err_t misc_set_temp (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_misc_temp_t temp,
            int16_t celsius,
            int8_t tenths )
```

Internal SC function to set a temp sensor alarm.

See also

sc_misc_set_temp().

16.23.2.38 misc_get_temp()

```
sc_err_t misc_get_temp (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_misc_temp_t temp,
             int16_t * celsius,
             int8_t * tenths )
```

Internal SC function to get a temp sensor value.

See also

sc_misc_get_temp().

16.23.2.39 misc_build_info()

```
void misc_build_info (
             sc_rm_pt_t caller_pt,
             uint32_t * build,
             uint32_t * commit )
```

Internal SC function to return SCFW build info.

See also

sc_misc_build_info().

16.23.2.40 misc_unique_id()

```
void misc_unique_id (
             sc_rm_pt_t caller_pt,
             uint32_t * id_l,
             uint32_t * id_h )
```

Internal SC function to return the device unique ID.

See also

sc_misc_unique_id().

16.23.2.41 misc_get_boot_dev()

```
void misc_get_boot_dev (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t * dev )
```

Internal SC function to return the boot device.

See also

sc_misc_get_boot_dev().

16.23.2.42 misc_get_boot_type()

```
sc_err_t misc_get_boot_type (
            sc_rm_pt_t caller_pt,
            sc_misc_bt_t * type )
```

Internal SC function to return the boot type.

See also

sc_misc_get_boot_type().

16.23.2.43 misc_get_boot_container()

```
sc_err_t misc_get_boot_container (
            sc_rm_pt_t caller_pt,
            uint8_t * idx )
```

Internal SC function to return the boot container index.

See also

sc_misc_get_boot_containere().

16.23.2.44 misc_get_button_status()

```
void misc_get_button_status (
            sc_rm_pt_t caller_pt,
            sc_bool_t * status )
```

Internal SC function to return the current status of the ON/OFF button.

See also

sc_misc_get_button_status().

16.23.2.45 misc_rompatch_checksum()

```
sc_err_t misc_rompatch_checksum (
             sc_rm_pt_t caller_pt,
             uint32_t * checksum )
```

Internal SC function to return the ROM patch checksum.

See also

sc_misc_rompatch_checksum().

16.23.2.46 misc_board_ioctl()

```
sc_err_t misc_board_ioctl (
             sc_rsrc_t mu,
             uint32_t * parm1,
             uint32_t * parm2,
             uint32_t * parm3 )
```

Internal SC function to call board IOCTL.

See also

sc_misc_board_ioctl().

16.23.2.47 misc_api_ver()

```
void misc_api_ver (
             sc_rm_pt_t caller_pt,
             uint16_t * cl_maj,
             uint16_t * cl_min,
             uint16_t * sv_maj,
             uint16_t * sv_min )
```

Internal SC function to return API version info.

See also

sc_misc_api_ver().

16.24 IRQ: Interrupt Service

Module for the Interrupt (IRQ) service.

Macros

- #define SC_IRQ_NUM_GROUP 7U

  Number of groups.

Typedefs

- typedef uint8_t sc_irq_group_t

  This type is used to declare an interrupt group.
- typedef uint8_t sc_irq_temp_t

  This type is used to declare a bit mask of temp interrupts.
- typedef uint8_t sc_irq_wdog_t

  This type is used to declare a bit mask of watchdog interrupts.
- typedef uint8_t sc_irq_rtc_t

  This type is used to declare a bit mask of RTC interrupts.
- typedef uint8_t sc_irq_wake_t

  This type is used to declare a bit mask of wakeup interrupts.

Functions

- sc_err_t sc_irq_enable (sc_ipc_t ipc, sc_rsrc_t resource, sc_irq_group_t group, uint32_t mask, sc_bool_t enable)

  This function enables/disables interrupts.
- sc_err_t sc_irq_status (sc_ipc_t ipc, sc_rsrc_t resource, sc_irq_group_t group, uint32_t *status)

  This function returns the current interrupt status (regardless if masked).
- sc_err_t irq_enable (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_irq_group_t group, uint32_t mask, sc_bool_t enable)

  Internal SC function to enable/disable interrupts.
- sc_err_t irq_status (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_irq_group_t group, uint32_t *status)

  Internal SC function to get and clear interrupt status.

Defines for sc_irq_group_t

- #define SC_IRQ_GROUP_TEMP 0U

  Temp interrupts.
- #define SC_IRQ_GROUP_WDOG 1U

  Watchdog interrupts.
- #define SC_IRQ_GROUP_RTC 2U

  RTC interrupts.
- #define SC_IRQ_GROUP_WAKE 3U

  Wakeup interrupts.
- #define SC_IRQ_GROUP_SYSCTR 4U

  System counter interrupts.
- #define SC_IRQ_GROUP_REBOOTED 5U

  Partition reboot complete.
- #define SC_IRQ_GROUP_REBOOT 6U

  Partition reboot starting.

Defines for sc_irq_temp_t

- #define SC_IRQ_TEMP_HIGH (1UL << 0U)

  Temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU0_HIGH (1UL << 1U)

  CPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU1_HIGH (1UL << 2U)

  CPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU0_HIGH (1UL << 3U)

  GPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU1_HIGH (1UL << 4U)

  GPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC0_HIGH (1UL << 5U)

  DRC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC1_HIGH (1UL << 6U)

  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_VPU_HIGH (1UL << 7U)

  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC0_HIGH (1UL << 8U)

  PMIC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC1_HIGH (1UL << 9U)

  PMIC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_LOW (1UL << 10U)

  Temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU0_LOW (1UL << 11U)

  CPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU1_LOW (1UL << 12U)

  CPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU0_LOW (1UL << 13U)

  GPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU1_LOW (1UL << 14U)

  GPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC0_LOW (1UL << 15U)

  DRC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC1_LOW (1UL << 16U)

  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_VPU_LOW (1UL << 17U)

  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC0_LOW (1UL << 18U)

  PMIC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC1_LOW (1UL << 19U)

  PMIC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC2_HIGH (1UL << 20U)

  PMIC2 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC2_LOW (1UL << 21U)

  PMIC2 temp alarm interrupt.

Defines for sc_irq_wdog_t

- #define SC_IRQ_WDOG (1U << 0U)

  Watchdog interrupt.

Defines for sc_irq_rtc_t

- #define SC_IRQ_RTC (1U << 0U)

  RTC interrupt.

Defines for sc_irq_wake_t

- #define SC_IRQ_BUTTON (1U << 0U)

  Button interrupt.
- #define SC_IRQ_PAD (1U << 1U)

  Pad wakeup.
- #define SC_IRQ_USR1 (1U << 2U)

  User defined 1.
- #define SC_IRQ_USR2 (1U << 3U)

  User defined 2.
- #define SC_IRQ_BC_PAD (1U << 4U)

  Pad wakeup (broadcast to all partitions)
- #define SC_IRQ_SW_WAKE (1U << 5U)

  Software requested wake.
- #define SC_IRQ_SECVIO (1U << 6U)

  Security violation.

Defines for sc_irq_sysctr_t

- #define SC_IRQ_SYSCTR (1U << 0U)

  SYSCTR interrupt.

16.24.1 Detailed Description

Module for the Interrupt (IRQ) service.

16.24.2 Function Documentation

16.24.2.1 sc_irq_enable()

```
sc_err_t sc_irq_enable (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_irq_group_t group,
             uint32_t mask,
             sc_bool_t enable )
```

This function enables/disables interrupts.

If pending interrupts are unmasked, an interrupt will be triggered.

Parameters

in	*ipc*	IPC handle
in	*resource*	MU channel
in	*group*	group the interrupts are in
in	*mask*	mask of interrupts to affect
in	*enable*	state to change interrupts to

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if group invalid

16.24.2.2 sc_irq_status()

```
sc_err_t sc_irq_status (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_irq_group_t group,
             uint32_t * status )
```

This function returns the current interrupt status (regardless if masked).

Automatically clears pending interrupts.

Parameters

in	*ipc*	IPC handle
in	*resource*	MU channel
in	*group*	groups the interrupts are in
in	*status*	status of interrupts

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if group invalid

The returned *status* may show interrupts pending that are currently masked.

16.24.2.3 irq_enable()

```
sc_err_t irq_enable (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_irq_group_t group,
             uint32_t mask,
             sc_bool_t enable )
```

Internal SC function to enable/disable interrupts.

See also

sc_irq_set_control().

16.24.2.4 irq_status()

```
sc_err_t irq_status (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_irq_group_t group,
             uint32_t * status )
```

Internal SC function to get and clear interrupt status.

See also

sc_irq_get_control().

16.25 PAD: Pad Service

Module for the Pad Control (PAD) service.

Typedefs

- typedef uint8_t sc_pad_config_t

  This type is used to declare a pad config.
- typedef uint8_t sc_pad_iso_t

  This type is used to declare a pad low-power isolation config.
- typedef uint8_t sc_pad_28fdsoi_dse_t

  This type is used to declare a drive strength.
- typedef uint8_t sc_pad_28fdsoi_ps_t

  This type is used to declare a pull select.
- typedef uint8_t sc_pad_28fdsoi_pus_t

  This type is used to declare a pull-up select.
- typedef uint8_t sc_pad_wakeup_t

  This type is used to declare a wakeup mode of a pad.

Defines for type widths

- #define SC_PAD_MUX_W 3U

  Width of mux parameter.

Defines for sc_pad_config_t

- #define SC_PAD_CONFIG_NORMAL 0U

  Normal.
- #define SC_PAD_CONFIG_OD 1U

  Open Drain.
- #define SC_PAD_CONFIG_OD_IN 2U

  Open Drain and input.
- #define SC_PAD_CONFIG_OUT_IN 3U

  Output and input.

Defines for sc_pad_iso_t

- #define SC_PAD_ISO_OFF 0U

  ISO latch is transparent.
- #define SC_PAD_ISO_EARLY 1U

  Follow EARLY_ISO.
- #define SC_PAD_ISO_LATE 2U

  Follow LATE_ISO.
- #define SC_PAD_ISO_ON 3U

  ISO latched data is held.

Defines for sc_pad_28fdsoi_dse_t

- #define SC_PAD_28FDSOI_DSE_18V_1MA 0U

  Drive strength of 1mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_2MA 1U

  Drive strength of 2mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_4MA 2U

  Drive strength of 4mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_6MA 3U

  Drive strength of 6mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_8MA 4U

  Drive strength of 8mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_10MA 5U

  Drive strength of 10mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_12MA 6U

  Drive strength of 12mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_HS 7U

  High-speed drive strength for 1.8v.
- #define SC_PAD_28FDSOI_DSE_33V_2MA 0U

  Drive strength of 2mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_33V_4MA 1U

  Drive strength of 4mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_33V_8MA 2U

  Drive strength of 8mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_33V_12MA 3U

  Drive strength of 12mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_DV_HIGH 0U

  High drive strength for dual volt.
- #define SC_PAD_28FDSOI_DSE_DV_LOW 1U

  Low drive strength for dual volt.

Defines for sc_pad_28fdsoi_ps_t

- #define SC_PAD_28FDSOI_PS_KEEPER 0U

  Bus-keeper (only valid for 1.8v)
- #define SC_PAD_28FDSOI_PS_PU 1U

  Pull-up.
- #define SC_PAD_28FDSOI_PS_PD 2U

  Pull-down.
- #define SC_PAD_28FDSOI_PS_NONE 3U

  No pull (disabled)

Defines for sc_pad_28fdsoi_pus_t

- #define SC_PAD_28FDSOI_PUS_30K_PD 0U

  30K pull-down
- #define SC_PAD_28FDSOI_PUS_100K_PU 1U

  100K pull-up
- #define SC_PAD_28FDSOI_PUS_3K_PU 2U

  3K pull-up
- #define SC_PAD_28FDSOI_PUS_30K_PU 3U

  30K pull-up

Defines for sc_pad_wakeup_t

- #define SC_PAD_WAKEUP_OFF 0U

  Off.
- #define SC_PAD_WAKEUP_CLEAR 1U

  Clears pending flag.
- #define SC_PAD_WAKEUP_LOW_LVL 4U

  Low level.
- #define SC_PAD_WAKEUP_FALL_EDGE 5U

  Falling edge.
- #define SC_PAD_WAKEUP_RISE_EDGE 6U

  Rising edge.
- #define SC_PAD_WAKEUP_HIGH_LVL 7U

  High-level.

Generic Functions

- sc_err_t sc_pad_set_mux (sc_ipc_t ipc, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso)

  This function configures the mux settings for a pad.
- sc_err_t sc_pad_get_mux (sc_ipc_t ipc, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso)

  This function gets the mux settings for a pad.
- sc_err_t sc_pad_set_gp (sc_ipc_t ipc, sc_pad_t pad, uint32_t ctrl)

  This function configures the general purpose pad control.
- sc_err_t sc_pad_get_gp (sc_ipc_t ipc, sc_pad_t pad, uint32_t *ctrl)

  This function gets the general purpose pad control.
- sc_err_t sc_pad_set_wakeup (sc_ipc_t ipc, sc_pad_t pad, sc_pad_wakeup_t wakeup)

  This function configures the wakeup mode of the pad.
- sc_err_t sc_pad_get_wakeup (sc_ipc_t ipc, sc_pad_t pad, sc_pad_wakeup_t *wakeup)

  This function gets the wakeup mode of a pad.
- sc_err_t sc_pad_set_all (sc_ipc_t ipc, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso, uint32_t ctrl, sc_pad_wakeup_t wakeup)

  This function configures a pad.
- sc_err_t sc_pad_get_all (sc_ipc_t ipc, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso, uint32_t *ctrl, sc_pad_wakeup_t *wakeup)

  This function gets a pad's config.

SoC Specific Functions

- sc_err_t sc_pad_set (sc_ipc_t ipc, sc_pad_t pad, uint32_t val)

  This function configures the settings for a pad.
- sc_err_t sc_pad_get (sc_ipc_t ipc, sc_pad_t pad, uint32_t *val)

  This function gets the settings for a pad.
- sc_err_t sc_pad_config (sc_ipc_t ipc, sc_pad_t pad, uint32_t val)

  This function writes a configuration register.

Technology Specific Functions

- sc_err_t sc_pad_set_gp_28fdsoi (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_pad_28fdsoi_ps_t ps)

  This function configures the pad control specific to 28FDSOI.
- sc_err_t sc_pad_get_gp_28fdsoi (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_pad_28fdsoi_ps_t *ps)

  This function gets the pad control specific to 28FDSOI.
- sc_err_t sc_pad_set_gp_28fdsoi_hsic (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_bool_t hys, sc_pad_28fdsoi_pus_t pus, sc_bool_t pke, sc_bool_t pue)

  This function configures the pad control specific to 28FDSOI.
- sc_err_t sc_pad_get_gp_28fdsoi_hsic (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_bool_t *hys, sc_pad_28fdsoi_pus_t *pus, sc_bool_t *pke, sc_bool_t *pue)

  This function gets the pad control specific to 28FDSOI.
- sc_err_t sc_pad_set_gp_28fdsoi_comp (sc_ipc_t ipc, sc_pad_t pad, uint8_t compen, sc_bool_t fastfrz, uint8_t rasrcp, uint8_t rasrcn, sc_bool_t nasrc_sel, sc_bool_t psw_ovr)

  This function configures the compensation control specific to 28FDSOI.
- sc_err_t sc_pad_get_gp_28fdsoi_comp (sc_ipc_t ipc, sc_pad_t pad, uint8_t *compen, sc_bool_t *fastfrz, uint8_t *rasrcp, uint8_t *rasrcn, sc_bool_t *nasrc_sel, sc_bool_t *compok, uint8_t *nasrc, sc_bool_t *psw_ovr)

  This function gets the compensation control specific to 28FDSOI.

Internal Functions

- void pad_init (sc_bool_t api_phase)

  Internal SC function to initializes the PAD service.
- sc_err_t pad_set (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t val)

  Internal SC function to set the pad value.
- sc_err_t pad_set_mux (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso)

  Internal SC function to set the pad mux.
- void **pad_force_mux** (sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso)
- sc_err_t pad_set_gp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t ctrl)

  Internal SC function to set the pad control.
- sc_err_t pad_set_wakeup (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_wakeup_t wakeup)

  Internal SC function to set the pad wakeup control.
- sc_err_t pad_set_all (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso, uint32_t ctrl, sc_pad_wakeup_t wakeup)

  Internal SC function to configure a pad.

- sc_err_t pad_get (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t *val)

  Internal SC function to get the pad value.
- sc_err_t pad_get_mux (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso)

  Internal SC function to get the pad mux.
- sc_err_t pad_get_gp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t *ctrl)

  Internal SC function to get the pad control.
- sc_err_t pad_get_wakeup (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_wakeup_t *wakeup)

  Internal SC function to get the pad wakeup control.
- sc_err_t pad_get_all (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso, uint32_t *ctrl, sc_pad_wakeup_t *wakeup)

  Internal SC function to get a pad's configuration.
- sc_err_t pad_set_gp_28fdsoi (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_pad_28fdsoi_ps_t ps)

  Internal SC function to set the pad control specific to 28FDSOI.
- sc_err_t pad_get_gp_28fdsoi (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_pad_28fdsoi_ps_t *ps)

  Internal SC function to get the pad control specific to 28FDSOI.
- sc_err_t pad_set_gp_28fdsoi_hsic (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_bool_t hyp, sc_pad_28fdsoi_pus_t pus, sc_bool_t pke, sc_bool_t pue)

  Internal SC function to set the pad control specific to 28FDSOI.
- sc_err_t pad_get_gp_28fdsoi_hsic (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_bool_t *hyp, sc_pad_28fdsoi_pus_t *pus, sc_bool_t *pke, sc_bool_t *pue)

  Internal SC function to get the pad control specific to 28FDSOI.
- sc_err_t pad_set_gp_28fdsoi_comp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t compen, sc_bool_t fastfrz, uint8_t rasrcp, uint8_t rasrcn, sc_bool_t nasrc_sel, sc_bool_t psw_ovr)

  Internal SC function to set the pad compensation specific to 28FDSOI.
- sc_err_t pad_get_gp_28fdsoi_comp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t *compen, sc_bool_t *fastfrz, uint8_t *rasrcp, uint8_t *rasrcn, sc_bool_t *nasrc_sel, sc_bool_t *compok, uint8_t *nasrc, sc_bool_t *psw_ovr)

  Internal SC function to get the compensation control specific to 28FDSOI.
- sc_err_t pad_config (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t val)

  Internal SC function to set a config value.
- sc_pad_t pad_map_irq (uint8_t irq, uint8_t idx)

  Internal function to map pad irq and index to pad resource.

16.25.1 Detailed Description

Module for the Pad Control (PAD) service.

Pad configuration is managed by SC firmware. The pad configuration features supported by the SC firmware include:

- Configuring the mux, input/output connection, and low-power isolation mode.
- Configuring the technology-specific pad setting such as drive strength, pullup/pulldown, etc.
- Configuring compensation for pad groups with dual voltage capability.

Pad functions fall into one of three categories. Generic functions are common to all SoCs and all process technologies. SoC functions are raw low-level functions. Technology-specific functions are specific to the process technology.

The list of pads is SoC specific. Refer to the SoC Pad List for valid pad values. Note that all pads exist on a die but may or may not be brought out by the specific package. Mapping of pads to package pins/balls is documented in the associated Data Sheet. Some pads may not be brought out because the part (die+package) is defeatured and some pads may connect to the substrate in the package.

Some pads (SC_P_COMP_*) that can be specified are not individual pads but are in fact pad groups. These groups have additional configuration that can be done using the sc_pad_set_gp_28fdsoi_comp() function. More info on these can be found in the associated Reference Manual.

Pads are managed as a resource by the Resource Manager (RM). They have assigned owners and only the owners can configure the pads. Some of the pads are reserved for use by the SCFW itself and this can be overridden with the implementation of board_config_sc(). Additionally, pads may be assigned to various other partitions via the implementation of board_system_config().

Note muxing two input pads to the same IP functional signal will result in undefined behavior.

The following SCFW pad code is an example of how to configure pads. In this example, two pads are configured for use by the i.MX8QXP I2C_0 (ADMA.I2C0). Another dual-voltge pad is configured as SPI_0 SCK (ADMA.SPI0.SCK).

The ipc parameter most functions take is a handle to the IPC channel opened to communicate to the SC. It is implementation defined. Most API ports include an sc_ipc_open() and sc_ipc_close() function to manage this. The sc_ipc_open() takes an argument to identify the communication channel (usually the MU address) and returns the IPC handle that all API calls should then use.

```
00001 /* Configure I2C_0 SCL pad */
00002 sc_pad_set_mux(ipc, SC_P_MIPI_CSI0_GPIO0_00, 1, SC_PAD_CONFIG_OD_IN, SC_PAD_ISO_OFF);
00003 sc_pad_set_gp_28fdsoi(ipc, SC_P_MIPI_CSI0_GPIO0_00, SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
00004
00005 /* Configure I2C_0 SDA pad */
00006 sc_pad_set_mux(ipc, SC_P_MIPI_CSI0_GPIO0_01, 1, SC_PAD_CONFIG_OD_IN, SC_PAD_ISO_OFF);
00007 sc_pad_set_gp_28fdsoi(ipc, SC_P_MIPI_CSI0_GPIO0_01, SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
00008
00009 /* Configure SPI0 SCK pad (dual-voltage) */
00010 sc_pad_set_mux(ipc, SC_P_SPI0_SCK, 0, SC_PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF);
00011 sc_pad_set_gp_28fdsoi(ipc, SC_P_SPI0_SCK, SC_PAD_28FDSOI_DSE_DV_LOW, SC_PAD_28FDSOI_PS_NONE);
```

The first pair of pads in question are MIPI_CSI0_GPIO0_00 (used for SCL) and MIPI_CSI0_GPIO0_01 (used for SDA). I2C_0 is mux select 1 for both pads.

The first two lines configure the SCL pad. The first configures the SCL pad for mux select 1, and as open-drain with with input. The second configures the drive strength and enables the pull-up.

The last two lines do the same for the SDA pad.

For 28FDSIO single voltage pads, SC_PAD_28FDSOI_DSE_DV_HIGH and SC_PAD_28FDSOI_DSE_DV_LOW are not valid drive strenths.

```
00000 /* Configure I2C_0 SCL pad */
00001 sc_pad_set_mux(ipc, SC_P_MIPI_CSI0_GPIO0_00, 1, SC_PAD_CONFIG_OD_IN, SC_PAD_ISO_OFF);
00002 sc_pad_set_gp_28fdsoi(ipc, SC_P_MIPI_CSI0_GPIO0_00, SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
00003
00004 /* Configure I2C_0 SDA pad */
00005 sc_pad_set_mux(ipc, SC_P_MIPI_CSI0_GPIO0_01, 1, SC_PAD_CONFIG_OD_IN, SC_PAD_ISO_OFF);
00006 sc_pad_set_gp_28fdsoi(ipc, SC_P_MIPI_CSI0_GPIO0_01, SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
```

The next pad configured is SPI0_SCK. It is configured as mux select 0. the first line configures the mux select as 0

and normal push-pull. The second line configures the drive strength and no pull-up. Note the drive strength setting is different for this dual voltage pad.

```
00007 /* Configure SPI0 SCK pad (dual-voltage) */
00009 sc_pad_set_mux(ipc, SC_P_SPI0_SCK, 0, SC_PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF);
00010 sc_pad_set_gp_28fdsoi(ipc, SC_P_SPI0_SCK, SC_PAD_28FDSOI_DSE_DV_LOW, SC_PAD_28FDSOI_PS_NONE);
```

For 28FDSIO dual voltage pads, only SC_PAD_28FDSOI_DSE_DV_HIGH and SC_PAD_28FDSOI_DSE_DV_LOW are valid drive strenths.

The voltage of the pad is determined by the supply for the pad group (the VDD_SPI_SAI_1P8_3P3 pad in this case).

16.25.2 Typedef Documentation

16.25.2.1 sc_pad_config_t

```
typedef uint8_t sc_pad_config_t
```

This type is used to declare a pad config.

It determines how the output data is driven, pull-up is controlled, and input signal is connected. Normal and OD are typical and only connect the input when the output is not driven. The IN options are less common and force an input connection even when driving the output.

16.25.2.2 sc_pad_iso_t

```
typedef uint8_t sc_pad_iso_t
```

This type is used to declare a pad low-power isolation config.

ISO_LATE is the most common setting. ISO_EARLY is only used when an output pad is directly determined by another input pad. The other two are only used when SW wants to directly control isolation.

16.25.2.3 sc_pad_28fdsoi_dse_t

```
typedef uint8_t sc_pad_28fdsoi_dse_t
```

This type is used to declare a drive strength.

Note it is specific to 28FDSOI. Also note that valid values depend on the pad type.

16.25.2.4 sc_pad_28fdsoi_ps_t

```
typedef uint8_t sc_pad_28fdsoi_ps_t
```

This type is used to declare a pull select.

Note it is specific to 28FDSOI.

16.25.2.5 sc_pad_28fdsoi_pus_t

```
typedef uint8_t sc_pad_28fdsoi_pus_t
```

This type is used to declare a pull-up select.

Note it is specific to 28FDSOI HSIC pads.

16.25.3 Function Documentation

16.25.3.1 sc_pad_set_mux()

```
sc_err_t sc_pad_set_mux (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint8_t mux,
             sc_pad_config_t config,
             sc_pad_iso_t iso )
```

This function configures the mux settings for a pad.

This includes the signal mux, pad config, and low-power isolation mode.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*mux*	mux setting
in	*config*	pad config
in	*iso*	low-power isolation mode

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Note muxing two input pads to the same IP functional signal will result in undefined behavior.

Refer to the SoC Pad List for valid pad values.

16.25.3.2 sc_pad_get_mux()

```
sc_err_t sc_pad_get_mux (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint8_t * mux,
             sc_pad_config_t * config,
             sc_pad_iso_t * iso )
```

This function gets the mux settings for a pad.

This includes the signal mux, pad config, and low-power isolation mode.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*mux*	pointer to return mux setting
out	*config*	pointer to return pad config
out	*iso*	pointer to return low-power isolation mode

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.3 sc_pad_set_gp()

```
sc_err_t sc_pad_set_gp (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint32_t ctrl )
```

This function configures the general purpose pad control.

This is technology dependent and includes things like drive strength, slew rate, pull up/down, etc. Refer to the SoC Reference Manual for bit field details.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*ctrl*	control value to set

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.4 sc_pad_get_gp()

```
sc_err_t sc_pad_get_gp (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint32_t * ctrl )
```

This function gets the general purpose pad control.

This is technology dependent and includes things like drive strength, slew rate, pull up/down, etc. Refer to the SoC Reference Manual for bit field details.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*ctrl*	pointer to return control value

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.5 sc_pad_set_wakeup()

```
sc_err_t sc_pad_set_wakeup (
             sc_ipc_t ipc,
             sc_pad_t pad,
             sc_pad_wakeup_t wakeup )
```

This function configures the wakeup mode of the pad.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*wakeup*	wakeup to set

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.6 sc_pad_get_wakeup()

```
sc_err_t sc_pad_get_wakeup (
             sc_ipc_t ipc,
             sc_pad_t pad,
             sc_pad_wakeup_t * wakeup )
```

This function gets the wakeup mode of a pad.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*wakeup*	pointer to return wakeup

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.7 sc_pad_set_all()

```
sc_err_t sc_pad_set_all (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint8_t mux,
             sc_pad_config_t config,
             sc_pad_iso_t iso,
             uint32_t ctrl,
             sc_pad_wakeup_t wakeup )
```

This function configures a pad.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*mux*	mux setting
in	*config*	pad config
in	*iso*	low-power isolation mode
in	*ctrl*	control value
in	*wakeup*	wakeup to set

See also

sc_pad_set_mux().

sc_pad_set_gp().

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Returns

Returns an error code (SC_ERR_NONE = success).

Note muxing two input pads to the same IP functional signal will result in undefined behavior.

Refer to the SoC Pad List for valid pad values.

16.25.3.8 sc_pad_get_all()

```
sc_err_t sc_pad_get_all (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint8_t * mux,
             sc_pad_config_t * config,
             sc_pad_iso_t * iso,
             uint32_t * ctrl,
             sc_pad_wakeup_t * wakeup )
```

This function gets a pad's config.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*mux*	pointer to return mux setting
out	*config*	pointer to return pad config
out	*iso*	pointer to return low-power isolation mode
out	*ctrl*	pointer to return control value
out	*wakeup*	pointer to return wakeup to set

See also

sc_pad_set_mux().

sc_pad_set_gp().

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Returns

Returns an error code (SC_ERR_NONE = success).

Refer to the SoC Pad List for valid pad values.

16.25.3.9 sc_pad_set()

```
sc_err_t sc_pad_set (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint32_t val )
```

This function configures the settings for a pad.

This setting is SoC specific.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*val*	value to set

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.10 sc_pad_get()

```
sc_err_t sc_pad_get (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint32_t * val )
```

This function gets the settings for a pad.

This setting is SoC specific.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*val*	pointer to return setting

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.11 sc_pad_config()

```
sc_err_t sc_pad_config (
             sc_ipc_t ipc,
             sc_pad_t pad,
             uint32_t val )
```

This function writes a configuration register.

This setting is SoC specific.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*val*	value to set

Use to configure various HSIC and NAND congiruation settings.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner

Refer to the SoC Pad List for valid pad values.

16.25.3.12 sc_pad_set_gp_28fdsoi()

```
sc_err_t sc_pad_set_gp_28fdsoi (
             sc_ipc_t ipc,
             sc_pad_t pad,
             sc_pad_28fdsoi_dse_t dse,
             sc_pad_28fdsoi_ps_t ps )
```

This function configures the pad control specific to 28FDSOI.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*dse*	drive strength
in	*ps*	pull select

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner,
- SC_ERR_UNAVAILABLE if process not applicable

Refer to the SoC Pad List for valid pad values.

16.25.3.13 sc_pad_get_gp_28fdsoi()

```
sc_err_t sc_pad_get_gp_28fdsoi (
            sc_ipc_t ipc,
            sc_pad_t pad,
            sc_pad_28fdsoi_dse_t * dse,
            sc_pad_28fdsoi_ps_t * ps )
```

This function gets the pad control specific to 28FDSOI.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*dse*	pointer to return drive strength
out	*ps*	pointer to return pull select

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner,
- SC_ERR_UNAVAILABLE if process not applicable

Refer to the SoC Pad List for valid pad values.

16.25.3.14 sc_pad_set_gp_28fdsoi_hsic()

```
sc_err_t sc_pad_set_gp_28fdsoi_hsic (
            sc_ipc_t ipc,
            sc_pad_t pad,
            sc_pad_28fdsoi_dse_t dse,
            sc_bool_t hys,
            sc_pad_28fdsoi_pus_t pus,
            sc_bool_t pke,
            sc_bool_t pue )
```

This function configures the pad control specific to 28FDSOI.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*dse*	drive strength
in	*hys*	hysteresis
in	*pus*	pull-up select
in	*pke*	pull keeper enable
in	*pue*	pull-up enable

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner,
- SC_ERR_UNAVAILABLE if process not applicable

Refer to the SoC Pad List for valid pad values.

16.25.3.15 sc_pad_get_gp_28fdsoi_hsic()

```
sc_err_t sc_pad_get_gp_28fdsoi_hsic (
             sc_ipc_t ipc,
             sc_pad_t pad,
             sc_pad_28fdsoi_dse_t * dse,
             sc_bool_t * hys,
             sc_pad_28fdsoi_pus_t * pus,
             sc_bool_t * pke,
             sc_bool_t * pue )
```

This function gets the pad control specific to 28FDSOI.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*dse*	pointer to return drive strength
out	*hys*	pointer to return hysteresis
out	*pus*	pointer to return pull-up select
out	*pke*	pointer to return pull keeper enable
out	*pue*	pointer to return pull-up enable

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner,
- SC_ERR_UNAVAILABLE if process not applicable

Refer to the SoC Pad List for valid pad values.

16.25.3.16 sc_pad_set_gp_28fdsoi_comp()

```
sc_err_t sc_pad_set_gp_28fdsoi_comp (
            sc_ipc_t ipc,
            sc_pad_t pad,
            uint8_t compen,
            sc_bool_t fastfrz,
            uint8_t rasrcp,
            uint8_t rasrcn,
            sc_bool_t nasrc_sel,
            sc_bool_t psw_ovr )
```

This function configures the compensation control specific to 28FDSOI.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to configure
in	*compen*	compensation/freeze mode
in	*fastfrz*	fast freeze
in	*rasrcp*	compensation code for PMOS
in	*rasrcn*	compensation code for NMOS
in	*nasrc_sel*	NASRC read select
in	*psw_ovr*	2.5v override

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner,
- SC_ERR_UNAVAILABLE if process not applicable

Refer to the SoC Pad List for valid pad values.

Note *psw_ovr* is only applicable to pads supporting 2.5 volt operation (e.g. some Ethernet pads).

16.25.3.17 sc_pad_get_gp_28fdsoi_comp()

```
sc_err_t sc_pad_get_gp_28fdsoi_comp (
            sc_ipc_t ipc,
            sc_pad_t pad,
            uint8_t * compen,
            sc_bool_t * fastfrz,
            uint8_t * rasrcp,
```

```
            uint8_t * rasrcn,
            sc_bool_t * nasrc_sel,
            sc_bool_t * compok,
            uint8_t * nasrc,
            sc_bool_t * psw_ovr )
```

This function gets the compensation control specific to 28FDSOI.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to query
out	*compen*	pointer to return compensation/freeze mode
out	*fastfrz*	pointer to return fast freeze
out	*rasrcp*	pointer to return compensation code for PMOS
out	*rasrcn*	pointer to return compensation code for NMOS
out	*nasrc_sel*	pointer to return NASRC read select
out	*compok*	pointer to return compensation status
out	*nasrc*	pointer to return NASRCP/NASRCN
out	*psw_ovr*	pointer to return the 2.5v override

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner,
- SC_ERR_UNAVAILABLE if process not applicable

Refer to the SoC Pad List for valid pad values.

16.25.3.18 pad_init()

```
void pad_init (
            sc_bool_t api_phase )
```

Internal SC function to initializes the PAD service.

Parameters

in	*api_phase*	init phase

Initializes the API if /a api_phase = SC_TRUE, otherwise initializes the HW managed by the PAD service. API must be

initialized before anything else is done with the service.

16.25.3.19 pad_set()

```
sc_err_t pad_set (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint32_t val )
```

Internal SC function to set the pad value.

See also

sc_pad_set().

16.25.3.20 pad_set_mux()

```
sc_err_t pad_set_mux (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint8_t mux,
             sc_pad_config_t config,
             sc_pad_iso_t iso )
```

Internal SC function to set the pad mux.

See also

sc_pad_set_mux().

16.25.3.21 pad_set_gp()

```
sc_err_t pad_set_gp (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint32_t ctrl )
```

Internal SC function to set the pad control.

See also

sc_pad_set_gp().

16.25.3.22 pad_set_wakeup()

```
sc_err_t pad_set_wakeup (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             sc_pad_wakeup_t wakeup )
```

Internal SC function to set the pad wakeup control.

See also

sc_pad_set_wakeup().

16.25.3.23 pad_set_all()

```
sc_err_t pad_set_all (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint8_t mux,
             sc_pad_config_t config,
             sc_pad_iso_t iso,
             uint32_t ctrl,
             sc_pad_wakeup_t wakeup )
```

Internal SC function to configure a pad.

See also

sc_pad_set_all().

16.25.3.24 pad_get()

```
sc_err_t pad_get (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint32_t * val )
```

Internal SC function to get the pad value.

See also

sc_pad_get().

16.25.3.25 pad_get_mux()

```
sc_err_t pad_get_mux (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint8_t * mux,
             sc_pad_config_t * config,
             sc_pad_iso_t * iso )
```

Internal SC function to get the pad mux.

See also

sc_pad_get_mux().

16.25.3.26 pad_get_gp()

```
sc_err_t pad_get_gp (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint32_t * ctrl )
```

Internal SC function to get the pad control.

See also

sc_pad_get_gp().

16.25.3.27 pad_get_wakeup()

```
sc_err_t pad_get_wakeup (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             sc_pad_wakeup_t * wakeup )
```

Internal SC function to get the pad wakeup control.

See also

sc_pad_get_wakeup().

16.25.3.28 pad_get_all()

```
sc_err_t pad_get_all (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint8_t * mux,
             sc_pad_config_t * config,
             sc_pad_iso_t * iso,
             uint32_t * ctrl,
             sc_pad_wakeup_t * wakeup )
```

Internal SC function to get a pad's configuration.

See also

sc_pad_get_all().

16.25.3.29 pad_set_gp_28fdsoi()

```
sc_err_t pad_set_gp_28fdsoi (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             sc_pad_28fdsoi_dse_t dse,
             sc_pad_28fdsoi_ps_t ps )
```

Internal SC function to set the pad control specific to 28FDSOI.

See also

sc_pad_set_gp_28fdsoi().

Examples

board.c.

16.25.3.30 pad_get_gp_28fdsoi()

```
sc_err_t pad_get_gp_28fdsoi (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             sc_pad_28fdsoi_dse_t * dse,
             sc_pad_28fdsoi_ps_t * ps )
```

Internal SC function to get the pad control specific to 28FDSOI.

See also

sc_pad_get_gp_28fdsoi().

16.25.3.31 pad_set_gp_28fdsoi_hsic()

```
sc_err_t pad_set_gp_28fdsoi_hsic (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             sc_pad_28fdsoi_dse_t dse,
             sc_bool_t hyp,
             sc_pad_28fdsoi_pus_t pus,
             sc_bool_t pke,
             sc_bool_t pue )
```

Internal SC function to set the pad control specific to 28FDSOI.

See also

sc_pad_set_gp_28fdsoi_hsic().

16.25.3.32 pad_get_gp_28fdsoi_hsic()

```
sc_err_t pad_get_gp_28fdsoi_hsic (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             sc_pad_28fdsoi_dse_t * dse,
             sc_bool_t * hyp,
             sc_pad_28fdsoi_pus_t * pus,
             sc_bool_t * pke,
             sc_bool_t * pue )
```

Internal SC function to get the pad control specific to 28FDSOI.

See also

sc_pad_get_gp_28fdsoi_hsic().

16.25.3.33 pad_set_gp_28fdsoi_comp()

```
sc_err_t pad_set_gp_28fdsoi_comp (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint8_t compen,
             sc_bool_t fastfrz,
             uint8_t rasrcp,
             uint8_t rasrcn,
             sc_bool_t nasrc_sel,
             sc_bool_t psw_ovr )
```

Internal SC function to set the pad compensation specific to 28FDSOI.

See also

sc_pad_set_gp_28fdsoi_comp().

16.25.3.34 pad_get_gp_28fdsoi_comp()

```
sc_err_t pad_get_gp_28fdsoi_comp (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint8_t * compen,
             sc_bool_t * fastfrz,
             uint8_t * rasrcp,
             uint8_t * rasrcn,
             sc_bool_t * nasrc_sel,
             sc_bool_t * compok,
             uint8_t * nasrc,
             sc_bool_t * psw_ovr )
```

Internal SC function to get the compensation control specific to 28FDSOI.

See also

sc_pad_get_gp_28fdsoi_comp().

16.25.3.35 pad_config()

```
sc_err_t pad_config (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad,
             uint32_t val )
```

Internal SC function to set a config value.

See also

sc_pad_config().

16.25.3.36 pad_map_irq()

```
sc_pad_t pad_map_irq (
             uint8_t irq,
             uint8_t idx )
```

Internal function to map pad irq and index to pad resource.

Parameters

in	*irq*	irq of pad
out	*idx*	index within irq

Returns

Returns the pad mapping.

If invalid irq or idx then return is >= SC_NUM_PAD.

16.26 PM: Power Management Service

Module for the Power Management (PM) service.

Typedefs

- typedef uint8_t sc_pm_power_mode_t

  This type is used to declare a power mode.
- typedef uint8_t sc_pm_clk_t

  This type is used to declare a clock.
- typedef uint8_t sc_pm_clk_parent_t

  This type is used to declare the clock parent.
- typedef uint32_t sc_pm_clock_rate_t

  This type is used to declare clock rates.
- typedef uint8_t sc_pm_reset_type_t

  This type is used to declare a desired reset type.
- typedef uint8_t sc_pm_reset_reason_t

  This type is used to declare a reason for a reset.
- typedef uint8_t sc_pm_sys_if_t

  This type is used to specify a system-level interface to be power managed.
- typedef uint8_t sc_pm_wake_src_t

  This type is used to specify a wake source for CPU resources.

Defines for type widths

- #define SC_PM_POWER_MODE_W 2U

  Width of sc_pm_power_mode_t.
- #define SC_PM_CLOCK_MODE_W 3U

  Width of sc_pm_clock_mode_t.
- #define SC_PM_RESET_TYPE_W 2U

  Width of sc_pm_reset_type_t.
- #define SC_PM_RESET_REASON_W 4U

  Width of sc_pm_reset_reason_t.

Defines for ALL parameters

- #define SC_PM_CLK_ALL ((sc_pm_clk_t) UINT8_MAX)

  All clocks.

Defines for sc_pm_power_mode_t

- #define SC_PM_PW_MODE_OFF 0U

  Power off.
- #define SC_PM_PW_MODE_STBY 1U

  Power in standby.
- #define SC_PM_PW_MODE_LP 2U

  Power in low-power.
- #define SC_PM_PW_MODE_ON 3U

  Power on.

Defines for sc_pm_clk_t

- #define SC_PM_CLK_SLV_BUS 0U

  Slave bus clock.
- #define SC_PM_CLK_MST_BUS 1U

  Master bus clock.
- #define SC_PM_CLK_PER 2U

  Peripheral clock.
- #define SC_PM_CLK_PHY 3U

  Phy clock.
- #define SC_PM_CLK_MISC 4U

  Misc clock.
- #define SC_PM_CLK_MISC0 0U

  Misc 0 clock.
- #define SC_PM_CLK_MISC1 1U

  Misc 1 clock.
- #define SC_PM_CLK_MISC2 2U

  Misc 2 clock.
- #define SC_PM_CLK_MISC3 3U

  Misc 3 clock.
- #define SC_PM_CLK_MISC4 4U

  Misc 4 clock.
- #define SC_PM_CLK_CPU 2U

  CPU clock.
- #define SC_PM_CLK_PLL 4U

  PLL.
- #define SC_PM_CLK_BYPASS 4U

  Bypass clock.

Defines for sc_pm_clk_parent_t

- #define SC_PM_PARENT_XTAL 0U

  Parent is XTAL.
- #define SC_PM_PARENT_PLL0 1U

  Parent is PLL0.
- #define SC_PM_PARENT_PLL1 2U

  Parent is PLL1 or PLL0/2.
- #define SC_PM_PARENT_PLL2 3U

  Parent in PLL2 or PLL0/4.
- #define SC_PM_PARENT_BYPS 4U

  Parent is a bypass clock.

Defines for sc_pm_reset_type_t

- #define SC_PM_RESET_TYPE_COLD 0U

  Cold reset.
- #define SC_PM_RESET_TYPE_WARM 1U

  Warm reset.
- #define SC_PM_RESET_TYPE_BOARD 2U

  Board reset.

Defines for sc_pm_reset_reason_t

- #define SC_PM_RESET_REASON_POR 0U

  Power on reset.
- #define SC_PM_RESET_REASON_JTAG 1U

  JTAG reset.
- #define SC_PM_RESET_REASON_SW 2U

  Software reset.
- #define SC_PM_RESET_REASON_WDOG 3U

  Partition watchdog reset.
- #define SC_PM_RESET_REASON_LOCKUP 4U

  SCU lockup reset.
- #define SC_PM_RESET_REASON_SNVS 5U

  SNVS reset.
- #define SC_PM_RESET_REASON_TEMP 6U

  Temp panic reset.
- #define SC_PM_RESET_REASON_MSI 7U

  MSI reset.
- #define SC_PM_RESET_REASON_UECC 8U

  ECC reset.
- #define SC_PM_RESET_REASON_SCFW_WDOG 9U

  SCFW watchdog reset.
- #define SC_PM_RESET_REASON_ROM_WDOG 10U

  SCU ROM watchdog reset.
- #define SC_PM_RESET_REASON_SECO 11U

  SECO reset.
- #define SC_PM_RESET_REASON_SCFW_FAULT 12U

  SCFW fault reset.
- #define SC_PM_RESET_REASON_V2X_DEBUG 13U

  V2X debug switch.

Defines for sc_pm_sys_if_t

- #define SC_PM_SYS_IF_INTERCONNECT 0U

  System interconnect.
- #define SC_PM_SYS_IF_MU 1U

  AP -> SCU message units.
- #define SC_PM_SYS_IF_OCMEM 2U

  On-chip memory (ROM/OCRAM)
- #define SC_PM_SYS_IF_DDR 3U

  DDR memory.

Defines for sc_pm_wake_src_t

- #define SC_PM_WAKE_SRC_NONE 0U

  No wake source, used for self-kill.
- #define SC_PM_WAKE_SRC_SCU 1U

  Wakeup from SCU to resume CPU (IRQSTEER & GIC powered down)
- #define SC_PM_WAKE_SRC_IRQSTEER 2U

  Wakeup from IRQSTEER to resume CPU (GIC powered down)
- #define SC_PM_WAKE_SRC_IRQSTEER_GIC 3U

  Wakeup from IRQSTEER+GIC to wake CPU (GIC clock gated)
- #define SC_PM_WAKE_SRC_GIC 4U

  Wakeup from GIC to wake CPU.

Power Functions

- sc_err_t sc_pm_set_sys_power_mode (sc_ipc_t ipc, sc_pm_power_mode_t mode)

  This function sets the system power mode.
- sc_err_t sc_pm_set_partition_power_mode (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_power_mode_t mode)

  This function sets the power mode of a partition.
- sc_err_t sc_pm_get_sys_power_mode (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_power_mode_t *mode)

  This function gets the power mode of a partition.
- sc_err_t sc_pm_partition_wake (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function sends a wake interrupt to a partition.
- sc_err_t sc_pm_set_resource_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  This function sets the power mode of a resource.
- sc_err_t sc_pm_set_resource_power_mode_all (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_power_mode_t mode, sc_rsrc_t exclude)

  This function sets the power mode for all the resources owned by a child partition.
- sc_err_t sc_pm_get_resource_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t *mode)

  This function gets the power mode of a resource.
- sc_err_t sc_pm_req_low_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  This function specifies the low power mode some of the resources can enter based on their state.
- sc_err_t sc_pm_req_cpu_low_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)

  This function requests low-power mode entry for CPU/cluster resources.
- sc_err_t sc_pm_set_cpu_resume_addr (sc_ipc_t ipc, sc_rsrc_t resource, sc_faddr_t address)

  This function is used to set the resume address of a CPU.
- sc_err_t sc_pm_set_cpu_resume (sc_ipc_t ipc, sc_rsrc_t resource, sc_bool_t isPrimary, sc_faddr_t address)

  This function is used to set parameters for CPU resume from low-power mode.
- sc_err_t sc_pm_req_sys_if_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_sys_if_t sys_if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)

  This function requests the power mode configuration for system-level interfaces including messaging units, interconnect, and memories.

Clock/PLL Functions

- sc_err_t sc_pm_set_clock_rate (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  This function sets the rate of a resource's clock/PLL.
- sc_err_t sc_pm_get_clock_rate (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  This function gets the rate of a resource's clock/PLL.
- sc_err_t sc_pm_clock_enable (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_bool_t enable, sc_bool_t autog)

  This function enables/disables a resource's clock.
- sc_err_t sc_pm_set_clock_parent (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t parent)

  This function sets the parent of a resource's clock.
- sc_err_t sc_pm_get_clock_parent (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t *parent)

  This function gets the parent of a resource's clock.

Reset Functions

- sc_err_t sc_pm_reset (sc_ipc_t ipc, sc_pm_reset_type_t type)

  This function is used to reset the system.
- sc_err_t sc_pm_reset_reason (sc_ipc_t ipc, sc_pm_reset_reason_t *reason)

  This function gets a caller's reset reason.
- sc_err_t sc_pm_get_reset_part (sc_ipc_t ipc, sc_rm_pt_t *pt)

  This function gets the partition that caused a reset.
- sc_err_t sc_pm_boot (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)

  This function is used to boot a partition.
- sc_err_t sc_pm_set_boot_parm (sc_ipc_t ipc, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)

  This function is used to change the boot parameters for a partition.
- void sc_pm_reboot (sc_ipc_t ipc, sc_pm_reset_type_t type)

  This function is used to reboot the caller's partition.
- sc_err_t sc_pm_reboot_partition (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_reset_type_t type)

  This function is used to reboot a partition.
- sc_err_t sc_pm_reboot_continue (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function is used to continue the reboot a partition.
- sc_err_t sc_pm_cpu_start (sc_ipc_t ipc, sc_rsrc_t resource, sc_bool_t enable, sc_faddr_t address)

  This function is used to start/stop a CPU.
- void sc_pm_cpu_reset (sc_ipc_t ipc, sc_rsrc_t resource, sc_faddr_t address)

  This function is used to reset a CPU.
- sc_err_t sc_pm_resource_reset (sc_ipc_t ipc, sc_rsrc_t resource)

  This function is used to reset a peripheral.
- sc_bool_t sc_pm_is_partition_started (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function returns a bool indicating if a partition was started.

Internal Functions

- void **pm_set_booted** (sc_rm_pt_t pt, sc_bool_t booted)
- sc_bool_t **pm_get_booted** (sc_rm_pt_t pt)
- void pm_init (sc_bool_t api_phase)

  Internal SC function to initializes the PM service.
- void pm_init_part (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  This function initializes a new partition.
- sc_err_t pm_set_sys_power_mode (sc_rm_pt_t caller_pt, sc_pm_power_mode_t mode)

  Internal SC function to set the power mode of the system.
- sc_err_t pm_set_partition_power_mode (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t mode)

  Internal SC function to set the power mode of a partition.
- sc_err_t pm_update_partition_power_mode (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t mode)

  Internal function to updates the power mode of a partition.
- sc_err_t pm_partition_wake (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  Internal SC function to send wake interrupt to a partition.
- sc_err_t pm_get_sys_power_mode (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t *mode)

  Internal SC function to get the power mode of a partition.
- void pm_update_ridx (sc_rm_idx_t idx)

  Internal SC function to update the power state of a resource.
- sc_bool_t pm_is_resource_accessible (sc_rsrc_t resource)

  Internal SC function to get the functional state of a resource.
- void pm_init_rsrc_power_mode (sc_rsrc_t rsrc, sc_pm_power_mode_t mode)

  Internal SC function to init the power mode of a resource just after ROM boot.
- sc_err_t pm_set_resource_power_mode (sc_rsrc_t mu, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to set the power mode of a resource.
- sc_err_t pm_set_resource_power_mode_all (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t mode, sc_rsrc_t exclude)

  Internal SC function to set power mode for all resources in a child partition.
- void pm_set_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t mode)

  This function sets the power mode of a resource index.
- void pm_update_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t mode)

  This function updates the power mode of a resource index.
- sc_err_t pm_force_resource_power_mode (sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to force the power mode of a resource.
- void pm_force_resource_power_mode_v (sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to force the power mode of a resource.
- sc_err_t pm_get_resource_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_power_mode_t *mode)

  Internal SC function to get the power mode of a resource.
- void pm_get_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t *mode)

  This function gets the power mode of a resource index.
- void pm_get_active_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t *mode)

  This function gets the active power mode of a resource index.
- sc_err_t pm_req_low_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to request the power mode a resource can enter in some low power conditions.
- sc_err_t pm_req_cpu_low_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)

Internal SC function to request low-power mode for a CPU.

- sc_err_t pm_set_cpu_resume_addr (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_faddr_t address)

  Internal SC function to set the resume address of a CPU.
- sc_err_t pm_set_cpu_resume (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_bool_t isPrimary, sc_faddr_t address)

  Internal SC function to set the resume parameters of a CPU.
- sc_err_t pm_req_sys_if_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_sys_if_t sys_↩ if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)

  Internal SC function to request power mode for system-level interfaces.
- sc_err_t pm_set_clock_rate (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  Internal SC function to set the rate of a resource's clock/PLL.
- sc_err_t pm_get_clock_rate (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  Internal SC function to get the rate of a resource's clock/PLL.
- sc_err_t pm_clock_enable (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_bool_t enable, sc_bool_t autog)

  Internal SC function to enable/disable a resource's clock.
- void pm_force_clock_enable (sc_rsrc_t resource, sc_pm_clk_t clk, sc_bool_t enable)

  Internal SC function to force a resource's clock to be enabled.
- sc_err_t pm_set_clock_parent (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t parent)

  Internal SC function to set a clock parent.
- sc_err_t pm_get_clock_parent (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t *parent)

  Internal SC function to get a clock parent.
- sc_err_t pm_boot (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)

  Internal SC function to boot a partition.
- sc_err_t pm_set_boot_parm (sc_rm_pt_t caller_pt, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)

  Internal SC function to set a partition's boot parameters.
- void pm_reboot (sc_rm_pt_t caller_pt, sc_pm_reset_type_t type)

  Internal SC function to reboot the caller's partition.
- sc_err_t pm_reset_reason (sc_rm_pt_t caller_pt, sc_pm_reset_reason_t *reason)

  Internal SC function to get the reset reason.
- sc_err_t pm_get_reset_part (sc_rm_pt_t caller_pt, sc_rm_pt_t *pt)

  Internal SC function to get the partition that caused a reset.
- sc_err_t pm_cpu_start (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_bool_t enable, sc_faddr_t address)

  Internal SC function to start/stop a CPU.
- void pm_cpu_reset (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_faddr_t address)

  Internal SC function to reset a CPU.
- sc_err_t pm_resource_reset (sc_rsrc_t mu, sc_rsrc_t resource)

  Internal SC function to reset a resource.
- sc_err_t pm_reboot_partition (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_reset_type_t type)

  Internal SC function to reboot a partition.
- sc_err_t pm_reboot_continue (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  Internal SC function to conntinue reboot.
- void pm_reboot_continue_all (void)

Internal SC function to force the conntinue of all reboots.

- sc_err_t pm_reset (sc_rm_pt_t caller_pt, sc_pm_reset_type_t type)

  Internal SC function to reset the system.

- sc_err_t pm_reboot_part (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_reset_type_t type, sc_pm_reset_reason_t reason, sc_pm_power_mode_t mode)

  Internal SC function used to reboot a partition.

- sc_bool_t pm_is_partition_started (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  Internal SC function to get boolean indicating that a partition was started.

16.26.1 Detailed Description

Module for the Power Management (PM) service.

The following SCFW PM code is an example of how to configure the power and clocking of a UART. All resources MUST be powered on before accessing.

The ipc parameter most functions take is a handle to the IPC channel opened to communicate to the SC. It is implementation defined. Most API ports include an sc_ipc_open() and sc_ipc_close() function to manage this. The sc_ipc_open() takes an argument to identify the communication channel (usually the MU address) and returns the IPC handle that all API calls should then use.

Refer to the SoC-specific RESOURCES for a list of resources. Refer to the SoC-specific CLOCKS for a list of clocks.

```
00001 sc_pm_clock_rate_t rate = SC_160MHZ;
00002
00003 /* Powerup UART 0 */
00004 sc_pm_set_resource_power_mode(ipc, SC_R_UART_0, SC_PM_PW_MODE_ON);
00005
00006 /* Configure UART 0 baud clock */
00007 sc_pm_set_clock_rate(ipc, SC_R_UART_0, SC_PM_CLK_PER, &rate);
00008
00009 /* Enable UART 0 clock */
00010 sc_pm_clock_enable(ipc, SC_R_UART_0, SC_PM_CLK_PER, SC_TRUE, SC_FALSE);
```

First, a variable is declared to hold the rate to request and return for the UART peripheral clock. Note this is the baud clock going into the UART which is then further divided within the UART itself.

```
00000 sc_pm_clock_rate_t rate = SC_160MHZ;
```

Then change the power state of the UART to the ON state.

```
00001 /* Powerup UART 0 */
00003 sc_pm_set_resource_power_mode(ipc, SC_R_UART_0, SC_PM_PW_MODE_ON);
```

Then configure the UART peripheral clock. Note that due to hardware limitation, the exact rate may not be what is requested. The rate is guarenteed to not be greater than the requested rate. The actual rate is returned in the varaible. The actual rate should be used when configuring the UART IP. Note that 160MHz is used as that can be divided by the UART to hit all the common UART rates within required error. Other frequencies may have issues and the caller needs to calculate the baud clock error rate. See the UART section of the SoC RM.

```
00004 /* Configure UART 0 baud clock */
00006 sc_pm_set_clock_rate(ipc, SC_R_UART_0, SC_PM_CLK_PER, &rate);
```

Then enable the clock.

```
00007 /* Enable UART 0 clock */
00009 sc_pm_clock_enable(ipc, SC_R_UART_0, SC_PM_CLK_PER, SC_TRUE, SC_FALSE);
```

At this point, the UART IP can be configured and used.

16.26.2 Typedef Documentation

16.26.2.1 sc_pm_power_mode_t

```
typedef uint8_t sc_pm_power_mode_t
```

This type is used to declare a power mode.

Note resources only use SC_PM_PW_MODE_OFF and SC_PM_PW_MODE_ON. The other modes are used only as system power modes.

16.26.3 Function Documentation

16.26.3.1 sc_pm_set_sys_power_mode()

```
sc_err_t sc_pm_set_sys_power_mode (
             sc_ipc_t ipc,
             sc_pm_power_mode_t mode )
```

This function sets the system power mode.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can do this.

Parameters

in	*ipc*	IPC handle
in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid mode,
- SC_ERR_NOACCESS if caller does not have SC_R_SYSTEM access

See also

sc_pm_set_sys_power_mode().

16.26.3.2 sc_pm_set_partition_power_mode()

```
sc_err_t sc_pm_set_partition_power_mode (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t mode )
```

This function sets the power mode of a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition
in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition or mode != SC_PM_PW_MODE_OFF,
- SC_ERR_NOACCESS if caller's partition is not the owner or parent of *pt*

This function can only be used to turn off a partition by calling with mode equal to SC_PM_PW_MODE_OFF. After turning off, the partition can be booted with sc_pm_reboot_partition() or sc_pm_boot(). It cannot be used to turn off the calling partition as the MU could not return the an error response.

For dynamic power management of a partition, use sc_pm_req_low_power_mode(), sc_pm_req_cpu_low_power_mode(), and sc_pm_req_sys_if_power_mode() with a WFI for controlled power state transitions.

16.26.3.3 sc_pm_get_sys_power_mode()

```
sc_err_t sc_pm_get_sys_power_mode (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t * mode )
```

This function gets the power mode of a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition
out	*mode*	pointer to return power mode

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition

16.26.3.4 sc_pm_partition_wake()

```
sc_err_t sc_pm_partition_wake (
             sc_ipc_t ipc,
             sc_rm_pt_t pt )
```

This function sends a wake interrupt to a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to wake

Returns

Returns an error code (SC_ERR_NONE = success).

An SC_IRQ_SW_WAKE interrupt is sent to all MUs owned by the partition that have this interrupt enabled. The CPU using an MU will exit a low-power state to service the MU interrupt.

Return errors:

- SC_ERR_PARM if invalid partition

16.26.3.5 sc_pm_set_resource_power_mode()

```
sc_err_t sc_pm_set_resource_power_mode (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_power_mode_t mode )
```

This function sets the power mode of a resource.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or mode,
- SC_ERR_PARM if resource is the MU used to make the call,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner

Resources must be at SC_PM_PW_MODE_LP mode or higher to access them, otherwise the master will get a bus error or hang.

Note some resources are still not accessible even when powered up if bus transactions go through a fabric not powered up. Examples of this are resources in display and capture subsystems which require the display controller or the imaging subsystem to be powered up first.

Note that resources are grouped into power domains by the underlying hardware. If any resource in the domain is on, the entire power domain will be on. Other power domains required to access the resource will also be turned on. Bus clocks required to access the peripheral will be turned on. Refer to the SoC RM for more info on power domains and access infrastructure (bus fabrics, clock domains, etc.).

When the resource transitions to the SC_PM_PW_MODE_OFF, all of the settings, including clock rate, will be lost; immaterial of the state of other resources in the same power domain.

16.26.3.6 sc_pm_set_resource_power_mode_all()

```
sc_err_t sc_pm_set_resource_power_mode_all (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t mode,
             sc_rsrc_t exclude )
```

This function sets the power mode for all the resources owned by a child partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of child partition
in	*mode*	power mode to apply
in	*exclude*	resource to exclude

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition or mode,
- SC_ERR_NOACCESS if caller's partition is not the parent (with grant) of *pt*

This functions loops through all the resources owned by *pt* and sets the power mode to *mode*. It will skip setting *exclude* (SC_R_LAST to skip none).

This function can only be called by the parent. It is used to implement some aspects of virtualization.

16.26.3.7 sc_pm_get_resource_power_mode()

```
sc_err_t sc_pm_get_resource_power_mode (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_power_mode_t * mode )
```

This function gets the power mode of a resource.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
out	*mode*	pointer to return power mode

Returns

Returns an error code (SC_ERR_NONE = success).

Note only SC_PM_PW_MODE_OFF and SC_PM_PW_MODE_ON are valid. The value returned does not reflect the power mode of the partition.

16.26.3.8 sc_pm_req_low_power_mode()

```
sc_err_t sc_pm_req_low_power_mode (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_power_mode_t mode )
```

This function specifies the low power mode some of the resources can enter based on their state.

This API is only valid for the following resources : SC_R_A53, SC_R_A53_0, SC_R_A53_1, SC_R_A53_2, SC_R↩_A53_3, SC_R_A72, SC_R_A72_0, SC_R_A72_1, SC_R_CC1, SC_R_A35, SC_R_A35_0, SC_R_A35_1, SC_R_↩A35_2, SC_R_A35_3. For all other resources it will return SC_ERR_PARAM. This function will set the low power mode the cores, cluster and cluster associated resources will enter when all the cores in a given cluster execute WFI.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

16.26.3.9 sc_pm_req_cpu_low_power_mode()

```
sc_err_t sc_pm_req_cpu_low_power_mode (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_power_mode_t mode,
             sc_pm_wake_src_t wake_src )
```

This function requests low-power mode entry for CPU/cluster resources.

This API is only valid for the following resources: SC_R_A53, SC_R_A53_x, SC_R_A72, SC_R_A72_x, SC_R_A35, SC_R_A35_x, SC_R_CCI. For all other resources it will return SC_ERR_PARAM. For individual core resources, the specified power mode and wake source will be applied after the core has entered WFI. For cluster resources, the specified power mode is applied after all cores in the cluster have entered low-power mode. For multicluster resources, the specified power mode is applied after all clusters have reached low-power mode.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*mode*	power mode to apply
in	*wake_src*	wake source for low-power exit

Returns

Returns an error code (SC_ERR_NONE = success).

16.26.3.10 sc_pm_set_cpu_resume_addr()

```
sc_err_t sc_pm_set_cpu_resume_addr (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_faddr_t address )
```

This function is used to set the resume address of a CPU.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the CPU resource
in	*address*	64-bit resume address

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or address,
- SC_ERR_NOACCESS if caller's partition is not the parent of the resource (CPU) owner

Note the address is limited by the hardware implementation. See the CPU Start Address section in the Porting Guide.

16.26.3.11 sc_pm_set_cpu_resume()

```
sc_err_t sc_pm_set_cpu_resume (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_bool_t isPrimary,
             sc_faddr_t address )
```

This function is used to set parameters for CPU resume from low-power mode.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the CPU resource
in	*isPrimary*	set SC_TRUE if primary wake CPU
in	*address*	64-bit resume address

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or address,
- SC_ERR_NOACCESS if caller's partition is not the parent of the resource (CPU) owner

Note the address is limited by the hardware implementation. See the CPU Start Address section in the Porting Guide.

16.26.3.12 sc_pm_req_sys_if_power_mode()

```
sc_err_t sc_pm_req_sys_if_power_mode (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_sys_if_t sys_if,
             sc_pm_power_mode_t hpm,
             sc_pm_power_mode_t lpm )
```

This function requests the power mode configuration for system-level interfaces including messaging units, interconnect, and memories.

This API is only valid for the following resources : SC_R_A53, SC_R_A72, and SC_R_M4_x_PID_y. For all other resources, it will return SC_ERR_PARAM. The requested power mode will be captured and applied to system-level resources as system conditions allow.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*sys_if*	system-level interface to be configured
in	*hpm*	high-power mode for the system interface
in	*lpm*	low-power mode for the system interface

Returns

Returns an error code (SC_ERR_NONE = success).

16.26.3.13 sc_pm_set_clock_rate()

```
sc_err_t sc_pm_set_clock_rate (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_clk_t clk,
             sc_pm_clock_rate_t * rate )
```

This function sets the rate of a resource's clock/PLL.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*clk*	clock/PLL to affect
in,out	*rate*	pointer to rate

Note the actual rate is returned in *rate*.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock/PLL,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_UNAVAILABLE if clock/PLL not applicable to this resource,
- SC_ERR_LOCKED if rate locked (usually because shared clock/PLL)

Refer to the Clock List for valid clock/PLL values.

16.26.3.14 sc_pm_get_clock_rate()

```
sc_err_t sc_pm_get_clock_rate (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_pm_clk_t clk,
            sc_pm_clock_rate_t * rate )
```

This function gets the rate of a resource's clock/PLL.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*clk*	clock/PLL to affect
out	*rate*	pointer to return rate

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock/PLL,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_UNAVAILABLE if clock/PLL not applicable to this resource

This function returns the actual clock rate of the hardware. This rate may be different from the original requested clock rate if the resource is set to a low power mode.

Refer to the Clock List for valid clock/PLL values.

16.26.3.15 sc_pm_clock_enable()

```
sc_err_t sc_pm_clock_enable (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_pm_clk_t clk,
            sc_bool_t enable,
            sc_bool_t autog )
```

This function enables/disables a resource's clock.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*clk*	clock to affect
in	*enable*	enable if SC_TRUE; otherwise disabled
in	*autog*	HW auto clock gating

If *resource* is SC_R_ALL then all resources owned will be affected. No error will be returned.

If *clk* is SC_PM_CLK_ALL, then an error will be returned if any of the available clocks returns an error.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent (with grant) of the owner,
- SC_ERR_UNAVAILABLE if clock not applicable to this resource

Refer to the Clock List for valid clock values.

16.26.3.16 sc_pm_set_clock_parent()

```
sc_err_t sc_pm_set_clock_parent (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_pm_clk_t clk,
            sc_pm_clk_parent_t parent )
```

This function sets the parent of a resource's clock.

This function should only be called when the clock is disabled.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*clk*	clock to affect
in	*parent*	New parent of the clock

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent (with grant) of the owner,
- SC_ERR_UNAVAILABLE if clock not applicable to this resource
- SC_ERR_BUSY if clock is currently enabled.
- SC_ERR_NOPOWER if resource not powered

Refer to the Clock List for valid clock values.

16.26.3.17 sc_pm_get_clock_parent()

```
sc_err_t sc_pm_get_clock_parent (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_pm_clk_t clk,
             sc_pm_clk_parent_t * parent )
```

This function gets the parent of a resource's clock.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the resource
in	*clk*	clock to affect
out	*parent*	pointer to return parent of clock

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock,

- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_UNAVAILABLE if clock not applicable to this resource

Refer to the Clock List for valid clock values.

16.26.3.18 sc_pm_reset()

```
sc_err_t sc_pm_reset (
             sc_ipc_t ipc,
             sc_pm_reset_type_t type )
```

This function is used to reset the system.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can do this.

Parameters

in	*ipc*	IPC handle
in	*type*	reset type

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid type,
- SC_ERR_NOACCESS if caller cannot access SC_R_SYSTEM

If this function returns, then the reset did not occur due to an invalid parameter.

16.26.3.19 sc_pm_reset_reason()

```
sc_err_t sc_pm_reset_reason (
             sc_ipc_t ipc,
             sc_pm_reset_reason_t * reason )
```

This function gets a caller's reset reason.

Parameters

in	*ipc*	IPC handle
out	*reason*	pointer to return the reset reason

This function returns the reason a partition was reset. If the reason is POR, then the system reset reason will be returned.

Note depending on the connection of the WDOG_OUT signal and the OTP programming of the PMIC, some resets may trigger a system POR and the original reason will be lost.

Returns

Returns an error code (SC_ERR_NONE = success).

16.26.3.20 sc_pm_get_reset_part()

```
sc_err_t sc_pm_get_reset_part (
             sc_ipc_t ipc,
             sc_rm_pt_t * pt )
```

This function gets the partition that caused a reset.

Parameters

in	*ipc*	IPC handle
out	*pt*	pointer to return the resetting partition

If the reset reason obtained via sc_pm_reset_reason() is POR then the result from this function will be 0. Some SECO causes of reset will also return 0.

Note depending on the connection of the WDOG_OUT signal and the OTP programming of the PMIC, some resets may trigger a system POR and the partition info will be lost.

Returns

Returns an error code (SC_ERR_NONE = success).

16.26.3.21 sc_pm_boot()

```
sc_err_t sc_pm_boot (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_rsrc_t resource_cpu,
             sc_faddr_t boot_addr,
             sc_rsrc_t resource_mu,
             sc_rsrc_t resource_dev )
```

This function is used to boot a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to boot
in	*resource_cpu*	ID of the CPU resource to start
in	*boot_addr*	64-bit boot address
in	*resource_mu*	ID of the MU that must be powered
in	*resource_dev*	ID of the boot device that must be powered

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition, resource, or addr,
- SC_ERR_NOACCESS if caller's partition is not the parent of the partition to boot

This must be used to boot a partition. Only a partition booted this way can be rebooted using the watchdog, sc_pm_boot() or sc_pm_reboot_partition().

Note the address is limited by the hardware implementation. See the CPU Start Address section in the Porting Guide.

16.26.3.22 sc_pm_set_boot_parm()

```
sc_err_t sc_pm_set_boot_parm (
             sc_ipc_t ipc,
             sc_rsrc_t resource_cpu,
             sc_faddr_t boot_addr,
             sc_rsrc_t resource_mu,
             sc_rsrc_t resource_dev )
```

This function is used to change the boot parameters for a partition.

Parameters

in	*ipc*	IPC handle
in	*resource_cpu*	ID of the CPU resource to start
in	*boot_addr*	64-bit boot address
in	*resource_mu*	ID of the MU that must be powered (0=none)
in	*resource_dev*	ID of the boot device that must be powered (0=none)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource, or addr

This function can be used to change the boot parameters for a partition. This can be useful if a partitions reboots differently from the initial boot done via sc_pm_boot() or via ROM.

Note the address is limited by the hardware implementation. See the CPU Start Address section in the Porting Guide.

16.26.3.23 sc_pm_reboot()

```
void sc_pm_reboot (
            sc_ipc_t ipc,
            sc_pm_reset_type_t type )
```

This function is used to reboot the caller's partition.

Parameters

in	*ipc*	IPC handle
in	*type*	reset type

If *type* is SC_PM_RESET_TYPE_COLD, then most peripherals owned by the calling partition will be reset if possible. SC state (partitions, power, clocks, etc.) is reset. The boot SW of the booting CPU must be able to handle peripherals that that are not reset.

If *type* is SC_PM_RESET_TYPE_WARM or SC_PM_RESET_TYPE_BOARD, then does nothing.

If this function returns, then the reset did not occur due to an invalid parameter.

16.26.3.24 sc_pm_reboot_partition()

```
sc_err_t sc_pm_reboot_partition (
            sc_ipc_t ipc,
            sc_rm_pt_t pt,
            sc_pm_reset_type_t type )
```

This function is used to reboot a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to reboot
in	*type*	reset type

If *type* is SC_PM_RESET_TYPE_COLD, then most peripherals owned by the calling partition will be reset if possible. SC state (partitions, power, clocks, etc.) is reset. The boot SW of the booting CPU must be able to handle peripherals that that are not reset.

If *type* is SC_PM_RESET_TYPE_WARM or SC_PM_RESET_TYPE_BOARD, then returns SC_ERR_PARM as these are not supported.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition or type
- SC_ERR_NOACCESS if caller's partition is not the parent of *pt* and the caller does not have access to SC_R_SYSTEM

Most peripherals owned by the partition will be reset if possible. SC state (partitions, power, clocks, etc.) is reset. The boot SW of the booting CPU must be able to handle peripherals that that are not reset.

If board_reboot_part() returns a non-0 mask, then the reboot will be delayed until all partitions indicated in the mask have called sc_pm_reboot_continue() to continue the boot.

16.26.3.25 sc_pm_reboot_continue()

```
sc_err_t sc_pm_reboot_continue (
             sc_ipc_t ipc,
             sc_rm_pt_t pt )
```

This function is used to continue the reboot a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to continue

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition

16.26.3.26 sc_pm_cpu_start()

```
sc_err_t sc_pm_cpu_start (
             sc_ipc_t ipc,
```

```
                sc_rsrc_t resource,
                sc_bool_t enable,
                sc_faddr_t address )
```

This function is used to start/stop a CPU.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the CPU resource
in	*enable*	start if SC_TRUE; otherwise stop
in	*address*	64-bit boot address

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or address,
- SC_ERR_NOACCESS if caller's partition is not the parent of the resource (CPU) owner

This function is usually used to start a secondary CPU in the same partition as the caller. It is not used to start the first CPU in a dedicated partition. That would be started by calling sc_pm_boot().

A CPU started with sc_pm_cpu_start() will not restart as a result of a watchdog event or calling sc_pm_reboot() or sc_pm_reboot_partition(). Those will reboot that partition which will start the CPU started with sc_pm_boot().

Note the address is limited by the hardware implementation. See the CPU Start Address section in the Porting Guide.

16.26.3.27 sc_pm_cpu_reset()

```
void sc_pm_cpu_reset (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_faddr_t address )
```

This function is used to reset a CPU.

Parameters

in	*ipc*	IPC handle
in	*resource*	ID of the CPU resource
in	*address*	64-bit boot address

This function does not return anything as the calling core may have been reset. It can still fail if the resource or address is invalid. It can also fail if the caller's partition is not the owner of the CPU, not the parent of the CPU resource owner, or has access to SC_R_SYSTEM. Will also fail if the resource is not powered on. No indication of failure is returned.

Note this just resets the CPU. None of the peripherals or bus fabric used by the CPU is reset. State configured in the SCFW is not reset. The SW running on the core has to understand and deal with this.

The address is limited by the hardware implementation. See the CPU Start Address section in the Porting Guide.

16.26.3.28 sc_pm_resource_reset()

```
sc_err_t sc_pm_resource_reset (
             sc_ipc_t ipc,
             sc_rsrc_t resource )
```

This function is used to reset a peripheral.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to reset

This function will reset a resource. Most resources cannot be reset unless the SoC design specifically allows it. In the case on MUs, the IPC/RPC protocol is also reset. Note a caller cannot reset an MU that this API call is sent on.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource,
- SC_ERR_PARM if resource is the MU used to make the call,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent (with grant) of the owner,
- SC_ERR_BUSY if the resource cannot be reset due to power state of buses,
- SC_ERR_UNAVAILABLE if the resource cannot be reset due to hardware limitations

16.26.3.29 sc_pm_is_partition_started()

```
sc_bool_t sc_pm_is_partition_started (
             sc_ipc_t ipc,
             sc_rm_pt_t pt )
```

This function returns a bool indicating if a partition was started.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to check

Returns

Returns a bool (SC_TRUE = started).

Note this indicates if a partition was started. It does not indicate if a partition is currently running or in a low power state.

16.26.3.30 pm_init()

```
void pm_init (
             sc_bool_t api_phase )
```

Internal SC function to initializes the PM service.

Parameters

in	*api_phase*	init phase

Initializes the API if /a api_phase = SC_TRUE, otherwise initializes the HW managed by the PM service. API must be initialized before anything else is done with the service.

16.26.3.31 pm_init_part()

```
void pm_init_part (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt )
```

This function initializes a new partition.

Parameters

in	*caller_pt*	handle of caller partition
in	*pt*	handle of partition

Note this function should only be called by the resource manager when a new partition is allocated. The default power mode is on.

16.26.3.32 pm_set_sys_power_mode()

```
sc_err_t pm_set_sys_power_mode (
             sc_rm_pt_t caller_pt,
             sc_pm_power_mode_t mode )
```

Internal SC function to set the power mode of the system.

See also

sc_pm_set_sys_power_mode().

16.26.3.33 pm_set_partition_power_mode()

```
sc_err_t pm_set_partition_power_mode (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t mode )
```

Internal SC function to set the power mode of a partition.

See also

sc_pm_set_partition_power_mode().

16.26.3.34 pm_update_partition_power_mode()

```
sc_err_t pm_update_partition_power_mode (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t mode )
```

Internal function to updates the power mode of a partition.

Parameters

in	*caller_pt*	handle of partition to update
in	*pt*	handle of partition
in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition or mode,
- SC_ERR_NOACCESS if caller's partition is not the owner or parent of *pt*

The power mode of the partitions is a max power any resource will be set to. Calling this will result in all resources owned by *pt* to have their power changed to the lower of *mode* or the individual resource mode set using sc_pm_set_resource_power_mode().

16.26.3.35 pm_partition_wake()

```
sc_err_t pm_partition_wake (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt )
```

Internal SC function to send wake interrupt to a partition.

See also

sc_pm_partition_wake().

16.26.3.36 pm_get_sys_power_mode()

```
sc_err_t pm_get_sys_power_mode (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t * mode )
```

Internal SC function to get the power mode of a partition.

See also

sc_pm_get_sys_power_mode().

16.26.3.37 pm_update_ridx()

```
void pm_update_ridx (
             sc_rm_idx_t idx )
```

Internal SC function to update the power state of a resource.

Parameters

in	*idx*	unified resource index

Used to update when a partition changes state or resource is moved.

16.26.3.38 pm_is_resource_accessible()

```
sc_bool_t pm_is_resource_accessible (
             sc_rsrc_t resource )
```

Internal SC function to get the functional state of a resource.

Parameters

in	*resource*	unified resource index

Returns

Returns a boolean (SC_TRUE = functional).

Used to see if a resource is ready to be used.

16.26.3.39 pm_set_resource_power_mode()

```
sc_err_t pm_set_resource_power_mode (
             sc_rsrc_t mu,
             sc_rsrc_t resource,
             sc_pm_power_mode_t mode )
```

Internal SC function to set the power mode of a resource.

See also

sc_pm_set_resource_power_mode().

16.26.3.40 pm_set_resource_power_mode_all()

```
sc_err_t pm_set_resource_power_mode_all (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_pm_power_mode_t mode,
             sc_rsrc_t exclude )
```

Internal SC function to set power mode for all resources in a child partition.

See also

sc_pm_set_resource_power_mode_all().

16.26.3.41 pm_set_rsrc_power_mode()

```
void pm_set_rsrc_power_mode (
             sc_rm_idx_t idx,
             sc_pm_power_mode_t mode )
```

This function sets the power mode of a resource index.

Parameters

in	*idx*	index of the resource
in	*mode*	power mode to apply

16.26.3.42 pm_update_rsrc_power_mode()

```
void pm_update_rsrc_power_mode (
            sc_rm_idx_t idx,
            sc_pm_power_mode_t mode )
```

This function updates the power mode of a resource index.

Parameters

in	*idx*	index of the resource
in	*mode*	power mode to apply

16.26.3.43 pm_force_resource_power_mode()

```
sc_err_t pm_force_resource_power_mode (
            sc_rsrc_t resource,
            sc_pm_power_mode_t mode )
```

Internal SC function to force the power mode of a resource.

It should only be called by the SC during initial configuration.

Parameters

in	*resource*	ID of the resource
in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or mode

Note only SC_PM_PW_MODE_OFF and SC_PM_PW_MODE_ON are valid. Other modes will return an error. Resources set to SC_PM_PW_MODE_ON will reflect the power mode of the partition and will change as that changes.

See also

sc_pm_set_partition_power_mode().

16.26.3.44 pm_force_resource_power_mode_v()

```
void pm_force_resource_power_mode_v (
            sc_rsrc_t resource,
            sc_pm_power_mode_t mode )
```

Internal SC function to force the power mode of a resource.

It should only be called by the SC during initial configuration.

Parameters

in	*resource*	ID of the resource
in	*mode*	power mode to apply

See also

sc_pm_set_partition_power_mode().

Examples

board.c.

16.26.3.45 pm_get_resource_power_mode()

```
sc_err_t pm_get_resource_power_mode (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_pm_power_mode_t * mode )
```

Internal SC function to get the power mode of a resource.

See also

sc_pm_get_resource_power_mode().

16.26.3.46 pm_get_rsrc_power_mode()

```
void pm_get_rsrc_power_mode (
            sc_rm_idx_t idx,
            sc_pm_power_mode_t * mode )
```

This function gets the power mode of a resource index.

Parameters

in	*idx*	index of the resource
in	*mode*	power mode to apply

16.26.3.47 pm_get_active_rsrc_power_mode()

```
void pm_get_active_rsrc_power_mode (
            sc_rm_idx_t idx,
            sc_pm_power_mode_t * mode )
```

This function gets the active power mode of a resource index.

Parameters

in	*idx*	index of the resource
in	*mode*	active power mode for the resource

16.26.3.48 pm_req_low_power_mode()

```
sc_err_t pm_req_low_power_mode (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_pm_power_mode_t mode )
```

Internal SC function to request the power mode a resource can enter in some low power conditions.

See also

sc_pm_req_low_power_mode().

16.26.3.49 pm_req_cpu_low_power_mode()

```
sc_err_t pm_req_cpu_low_power_mode (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_pm_power_mode_t mode,
            sc_pm_wake_src_t wake_src )
```

Internal SC function to request low-power mode for a CPU.

See also

sc_pm_req_cpu_low_power_mode().

16.26.3.50 pm_set_cpu_resume_addr()

```
sc_err_t pm_set_cpu_resume_addr (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_faddr_t address )
```

Internal SC function to set the resume address of a CPU.

See also

sc_pm_set_cpu_resume_addr().

16.26.3.51 pm_set_cpu_resume()

```
sc_err_t pm_set_cpu_resume (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_bool_t isPrimary,
             sc_faddr_t address )
```

Internal SC function to set the resume parameters of a CPU.

See also

sc_pm_set_cpu_resume().

16.26.3.52 pm_req_sys_if_power_mode()

```
sc_err_t pm_req_sys_if_power_mode (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_pm_sys_if_t sys_if,
             sc_pm_power_mode_t hpm,
             sc_pm_power_mode_t lpm )
```

Internal SC function to request power mode for system-level interfaces.

See also

pm_req_sys_if_power_mode().

16.26.3.53 pm_set_clock_rate()

```
sc_err_t pm_set_clock_rate (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_pm_clk_t clk,
             sc_pm_clock_rate_t * rate )
```

Internal SC function to set the rate of a resource's clock/PLL.

See also

sc_pm_set_clock_rate().

Examples

board.c.

16.26.3.54 pm_get_clock_rate()

```
sc_err_t pm_get_clock_rate (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_pm_clk_t clk,
             sc_pm_clock_rate_t * rate )
```

Internal SC function to get the rate of a resource's clock/PLL.

See also

sc_pm_get_clock_rate().

Examples

board.c.

16.26.3.55 pm_clock_enable()

```
sc_err_t pm_clock_enable (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_pm_clk_t clk,
             sc_bool_t enable,
             sc_bool_t autog )
```

Internal SC function to enable/disable a resource's clock.

See also

sc_pm_clock_enable().

Examples

board.c.

16.26.3.56 pm_force_clock_enable()

```
void pm_force_clock_enable (
            sc_rsrc_t resource,
            sc_pm_clk_t clk,
            sc_bool_t enable )
```

Internal SC function to force a resource's clock to be enabled.

Parameters

in	*resource*	ID of the resource
in	*clk*	clock to affect
in	*enable*	enable if SC_TRUE; otherwise depends on state from pm_clock_enable()

Refer to the Clock List for valid clock values.

Examples

board.c.

16.26.3.57 pm_set_clock_parent()

```
sc_err_t pm_set_clock_parent (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_pm_clk_t clk,
            sc_pm_clk_parent_t parent )
```

Internal SC function to set a clock parent.

See also

sc_pm_set_clock_parent().

16.26.3.58 pm_get_clock_parent()

```
sc_err_t pm_get_clock_parent (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_pm_clk_t clk,
            sc_pm_clk_parent_t * parent )
```

Internal SC function to get a clock parent.

See also

sc_pm_get_clock_parent().

16.26.3.59 pm_boot()

```
sc_err_t pm_boot (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_rsrc_t resource_cpu,
             sc_faddr_t boot_addr,
             sc_rsrc_t resource_mu,
             sc_rsrc_t resource_dev )
```

Internal SC function to boot a partition.

See also

sc_pm_boot().

16.26.3.60 pm_set_boot_parm()

```
sc_err_t pm_set_boot_parm (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource_cpu,
             sc_faddr_t boot_addr,
             sc_rsrc_t resource_mu,
             sc_rsrc_t resource_dev )
```

Internal SC function to set a partition's boot parameters.

See also

sc_pm_set_boot_parm().

16.26.3.61 pm_reboot()

```
void pm_reboot (
             sc_rm_pt_t caller_pt,
             sc_pm_reset_type_t type )
```

Internal SC function to reboot the caller's partition.

See also

sc_pm_reboot().

16.26.3.62 pm_reset_reason()

```
sc_err_t pm_reset_reason (
             sc_rm_pt_t caller_pt,
             sc_pm_reset_reason_t * reason )
```

Internal SC function to get the reset reason.

See also

sc_pm_reset_reason().

16.26.3.63 pm_get_reset_part()

```
sc_err_t pm_get_reset_part (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t * pt )
```

Internal SC function to get the partition that caused a reset.

See also

sc_pm_get_reset_part().

16.26.3.64 pm_cpu_start()

```
sc_err_t pm_cpu_start (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_bool_t enable,
             sc_faddr_t address )
```

Internal SC function to start/stop a CPU.

See also

sc_pm_cpu_start().

16.26.3.65 pm_cpu_reset()

```
void pm_cpu_reset (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_faddr_t address )
```

Internal SC function to reset a CPU.

See also

sc_pm_cpu_reset().

16.26.3.66 pm_resource_reset()

```
sc_err_t pm_resource_reset (
            sc_rsrc_t mu,
            sc_rsrc_t resource )
```

Internal SC function to reset a resource.

See also

sc_pm_resource_reset().

16.26.3.67 pm_reboot_partition()

```
sc_err_t pm_reboot_partition (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt,
            sc_pm_reset_type_t type )
```

Internal SC function to reboot a partition.

See also

sc_pm_reboot_partition().

16.26.3.68 pm_reboot_continue()

```
sc_err_t pm_reboot_continue (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt )
```

Internal SC function to conntinue reboot.

See also

sc_reboot_continue().

16.26.3.69 pm_reset()

```
sc_err_t pm_reset (
             sc_rm_pt_t caller_pt,
             sc_pm_reset_type_t type )
```

Internal SC function to reset the system.

See also

sc_pm_reset().

16.26.3.70 pm_reboot_part()

```
sc_err_t pm_reboot_part (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_pm_reset_type_t type,
             sc_pm_reset_reason_t reason,
             sc_pm_power_mode_t mode )
```

Internal SC function used to reboot a partition.

Parameters

in	*caller_pt*	calling partition
in	*pt*	handle of partition to reboot
in	*type*	reset type
in	*reason*	reset reason
in	*mode*	power mode to go down to as part of reboot

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid partition or reason

Most peripherals owned by the partition will be reset if possible. SC state (partitions, power, clocks, etc.) is reset. The boot SW of the booting CPU must be able to handle peripherals that that are not reset.

16.26.3.71 pm_is_partition_started()

```
sc_bool_t pm_is_partition_started (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt )
```

Internal SC function to get boolean indicating that a partition was started.

See also

sc_pm_is_partition_started().

16.27 SECO: Security Service

Module for the Security (SECO) service.

Typedefs

- typedef uint8_t sc_seco_auth_cmd_t

  This type is used to issue SECO authenticate commands.
- typedef uint32_t sc_seco_rng_stat_t

  This type is used to return the RNG initialization status.

Functions

- sc_err_t seco_get_mp_key (sc_rm_pt_t caller_pt, sc_faddr_t dst_addr, uint16_t dst_size)

  Internal SC function to get manufacturing protection public key.
- sc_err_t seco_update_mpmr (sc_rm_pt_t caller_pt, sc_faddr_t addr, uint8_t size, uint8_t lock)

  Internal SC function to update manufacturing protection message register.
- sc_err_t seco_get_mp_sign (sc_rm_pt_t caller_pt, sc_faddr_t msg_addr, uint16_t msg_size, sc_faddr_t dst_addr, uint16_t dst_size)

  Internal SC function to get manufacturing protection signature.
- sc_err_t seco_sab_msg (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to send a generic signed message to the SECO SHE/HSM components.
- sc_err_t seco_secvio_enable (sc_rm_pt_t caller_pt)

  Internal SC function to enable the security violation interrupt.
- sc_err_t seco_secvio_config (sc_rm_pt_t caller_pt, uint8_t id, uint8_t access, uint32_t *data0, uint32_t *data1, uint32_t *data2, uint32_t *data3, uint32_t *data4, uint8_t size)

  Internal SC function to read/write SNVS security violation and tamper registers.
- sc_err_t seco_secvio_dgo_config (sc_rm_pt_t caller_pt, uint8_t id, uint8_t access, uint32_t *data)

  Internal SC function to read/write SNVS security violation and tamper DGO registers.

Defines for sc_seco_auth_cmd_t

- #define SC_SECO_AUTH_CONTAINER 0U

  Authenticate container.
- #define SC_SECO_VERIFY_IMAGE 1U

  Verify image.
- #define SC_SECO_REL_CONTAINER 2U

  Release container.
- #define SC_SECO_AUTH_SECO_FW 3U

  SECO Firmware.
- #define SC_SECO_AUTH_HDMI_TX_FW 4U

  HDMI TX Firmware.
- #define SC_SECO_AUTH_HDMI_RX_FW 5U

  HDMI RX Firmware.
- #define SC_SECO_EVERIFY_IMAGE 6U

  Enhanced verify image.

Defines for seco_rng_stat_t

- #define SC_SECO_RNG_STAT_UNAVAILABLE 0U

  Unable to initialize the RNG.
- #define SC_SECO_RNG_STAT_INPROGRESS 1U

  Initialization is on-going.
- #define SC_SECO_RNG_STAT_READY 2U

  Initialized.

Image Functions

- sc_err_t sc_seco_image_load (sc_ipc_t ipc, sc_faddr_t addr_src, sc_faddr_t addr_dst, uint32_t len, sc_bool_t fw)

  This function loads a SECO image.
- sc_err_t sc_seco_authenticate (sc_ipc_t ipc, sc_seco_auth_cmd_t cmd, sc_faddr_t addr)

  This function is used to authenticate a SECO image or command.
- sc_err_t sc_seco_enh_authenticate (sc_ipc_t ipc, sc_seco_auth_cmd_t cmd, sc_faddr_t addr, uint32_t mask1, uint32_t mask2)

  This function is used to authenticate a SECO image or command.

Lifecycle Functions

- sc_err_t sc_seco_forward_lifecycle (sc_ipc_t ipc, uint32_t change)

  This function updates the lifecycle of the device.
- sc_err_t sc_seco_return_lifecycle (sc_ipc_t ipc, sc_faddr_t addr)

  This function updates the lifecycle to one of the return lifecycles.
- sc_err_t sc_seco_commit (sc_ipc_t ipc, uint32_t *info)

  This function is used to commit into the fuses any new SRK revocation and FW version information that have been found in the primary and secondary containers.

Attestation Functions

- sc_err_t sc_seco_attest_mode (sc_ipc_t ipc, uint32_t mode)

  This function is used to set the attestation mode.
- sc_err_t sc_seco_attest (sc_ipc_t ipc, uint64_t nonce)

  This function is used to request attestation.
- sc_err_t sc_seco_get_attest_pkey (sc_ipc_t ipc, sc_faddr_t addr)

  This function is used to retrieve the attestation public key.
- sc_err_t sc_seco_get_attest_sign (sc_ipc_t ipc, sc_faddr_t addr)

  This function is used to retrieve attestation signature and parameters.
- sc_err_t sc_seco_attest_verify (sc_ipc_t ipc, sc_faddr_t addr)

  This function is used to verify attestation.

Key Functions

- sc_err_t sc_seco_gen_key_blob (sc_ipc_t ipc, uint32_t id, sc_faddr_t load_addr, sc_faddr_t export_addr, uint16_t max_size)

  This function is used to generate a SECO key blob.
- sc_err_t sc_seco_load_key (sc_ipc_t ipc, uint32_t id, sc_faddr_t addr)

  This function is used to load a SECO key.

Manufacturing Protection Functions

- sc_err_t sc_seco_get_mp_key (sc_ipc_t ipc, sc_faddr_t dst_addr, uint16_t dst_size)

  This function is used to get the manufacturing protection public key.
- sc_err_t sc_seco_update_mpmr (sc_ipc_t ipc, sc_faddr_t addr, uint8_t size, uint8_t lock)

  This function is used to update the manufacturing protection message register.
- sc_err_t sc_seco_get_mp_sign (sc_ipc_t ipc, sc_faddr_t msg_addr, uint16_t msg_size, sc_faddr_t dst_addr, uint16_t dst_size)

  This function is used to get the manufacturing protection signature.

Debug Functions

- void sc_seco_build_info (sc_ipc_t ipc, uint32_t *version, uint32_t *commit)

  This function is used to return the SECO FW build info.
- sc_err_t sc_seco_chip_info (sc_ipc_t ipc, uint16_t *lc, uint16_t *monotonic, uint32_t *uid_l, uint32_t *uid_h)

  This function is used to return SECO chip info.
- sc_err_t sc_seco_enable_debug (sc_ipc_t ipc, sc_faddr_t addr)

  This function securely enables debug.
- sc_err_t sc_seco_get_event (sc_ipc_t ipc, uint8_t idx, uint32_t *event)

  This function is used to return an event from the SECO error log.

Miscellaneous Functions

- sc_err_t sc_seco_fuse_write (sc_ipc_t ipc, sc_faddr_t addr)

  This function securely writes a group of fuse words.
- sc_err_t sc_seco_patch (sc_ipc_t ipc, sc_faddr_t addr)

  This function applies a patch.
- sc_err_t sc_seco_set_mono_counter_partition (sc_ipc_t ipc, uint16_t *she)

  This function partitions the monotonic counter.
- sc_err_t sc_seco_set_fips_mode (sc_ipc_t ipc, uint8_t mode, uint32_t *reason)

  This function configures the SECO in FIPS mode.
- sc_err_t sc_seco_start_rng (sc_ipc_t ipc, sc_seco_rng_stat_t *status)

  This function starts the random number generator.
- sc_err_t sc_seco_sab_msg (sc_ipc_t ipc, sc_faddr_t addr)

  This function sends a generic signed message to the SECO SHE/HSM components.
- sc_err_t sc_seco_secvio_enable (sc_ipc_t ipc)

  This function is used to enable security violation and tamper interrupts.
- sc_err_t sc_seco_secvio_config (sc_ipc_t ipc, uint8_t id, uint8_t access, uint32_t *data0, uint32_t *data1, uint32_t *data2, uint32_t *data3, uint32_t *data4, uint8_t size)

  This function is used to read/write SNVS security violation and tamper registers.
- sc_err_t sc_seco_secvio_dgo_config (sc_ipc_t ipc, uint8_t id, uint8_t access, uint32_t *data)

  This function is used to read/write SNVS security violation and tamper DGO registers.

Internal Functions

- sc_err_t seco_image_load (sc_rm_pt_t caller_pt, sc_faddr_t addr_src, sc_faddr_t addr_dst, uint32_t len, sc_bool_t fw)

  Internal SC function to load a SECO image.
- sc_err_t seco_authenticate (sc_rm_pt_t caller_pt, sc_seco_auth_cmd_t cmd, sc_faddr_t addr)

  Internal SC function to authenticate a SECO image or command.
- sc_err_t seco_enh_authenticate (sc_rm_pt_t caller_pt, sc_seco_auth_cmd_t cmd, sc_faddr_t addr, uint32_t mask1, uint32_t mask2)

  Internal SC function to authenticate a SECO image or command ((enhanced version).
- sc_err_t seco_load_key (sc_rm_pt_t caller_pt, uint32_t id, sc_faddr_t addr)

  Internal SC function to load a SECO key.
- sc_err_t seco_gen_key_blob (sc_rm_pt_t caller_pt, uint32_t id, sc_faddr_t load_addr, sc_faddr_t export_addr, uint16_t max_size)

  Internal SC function to generate a key blob.
- sc_err_t seco_fuse_write (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to securely write a group of fuse words.
- sc_err_t seco_patch (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to apply a patch.
- sc_err_t seco_set_mono_counter_partition (sc_rm_pt_t caller_pt, uint16_t *she)

  Internal SC function to partition the monotonic counter.
- sc_err_t seco_set_fips_mode (sc_rm_pt_t caller_pt, uint8_t mode, uint32_t *reason)

  Internal SC function to set FIPS mode.
- sc_err_t seco_start_rng (sc_rm_pt_t caller_pt, sc_seco_rng_stat_t *status)

  Internal SC function to start the RNG.
- sc_err_t seco_enable_debug (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to securely enable debug.
- sc_err_t seco_forward_lifecycle (sc_rm_pt_t caller_pt, uint32_t change)

  Internal SC function to update the lifecycle.
- sc_err_t seco_return_lifecycle (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to securely reverse the lifecycle.
- void seco_build_info (sc_rm_pt_t caller_pt, uint32_t *version, uint32_t *commit)

  Internal SC function to return SECO FW version info.
- sc_err_t seco_chip_info (sc_rm_pt_t caller_pt, uint16_t *lc, uint16_t *monotonic, uint32_t *uid_l, uint32_t *uid_h)

  Internal SC function to return SECO chip info.
- sc_err_t seco_get_event (sc_rm_pt_t caller_pt, uint8_t idx, uint32_t *event)

  Internal SC function to return an event from the SECO error log.
- sc_err_t seco_attest_mode (sc_rm_pt_t caller_pt, uint32_t mode)

  Internal SC function to set the attestation mode.
- sc_err_t seco_attest (sc_rm_pt_t caller_pt, uint64_t nonce)

  Internal SC function to request atestation.
- sc_err_t seco_get_attest_pkey (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to retrieve attestation public key.
- sc_err_t seco_get_attest_sign (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to retrieve attestation signature and parameters.
- sc_err_t seco_attest_verify (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to verify attestation.
- sc_err_t seco_commit (sc_rm_pt_t caller_pt, uint32_t *info)

  Internal SC function to commit SRK/FW changes.

16.27.1 Detailed Description

Module for the Security (SECO) service.

SECO functions in the SCFW API communicate via a messaging protocol to the Security Controller (SECO). This messaging protocol is documented in the *SECO API Reference Guide*. There is also a *Security Reference Manual (SRM)* that documents many of the SECO features.

SECO messages contain error codes defined in the *SECO API Reference Guide*. These have to be mapped to SC↩ FW error codes. sc_seco_get_event() can be used to obtain SECO-specific error codes recorded in the SECO event log.

SCFW Error Mapping to SECO Errors

- SC_ERR_NOACCESS
  - AHAB_INVALID_LIFECYCLE
  - AHAB_PERMISSION_DENIED_IND
- SC_ERR_IPC
  - AHAB_INVALID_MESSAGE_IND
  - AHAB_CRC_ERROR
  - AHAB_INVALID_OPERATION_IND
- SC_ERR_VERSION
  - AHAB_BAD_VERSION_IND
- SC_ERR_PARM
  - AHAB_BAD_HASH_IND
  - AHAB_BAD_VALUE_IND
  - AHAB_BAD_FUSE_ID_IND
  - AHAB_BAD_CONTAINER_IND
  - AHAB_BAD_KEY_HASH_IND
  - AHAB_NO_VALID_CONTAINER_IND
  - AHAB_MUST_SIGNED_IND
  - AHAB_NO_BID_MATCHING_IND
  - AHAB_UNKNOWN_BID_IND
  - AHAB_UNALIGNED_PAYLOAD_IND
  - AHAB_WRONG_SIZE_IND
  - AHAB_OTP_INVALID_IDX_IND
  - AHAB_ADM_WRONG_LC_IND
  - AHAB_OTP_DED_IND
  - AHAB_BAD_PAYLOAD_IND
  - AHAB_WRONG_ADDRESS_IND
  - AHAB_DMA_FAILURE_IND
  - AHAB_BAD_UID_IND
  - AHAB_INCONSISTENT_PAR_IND

  - AHAB_BAD_MONOTONIC_COUNTER_IND
  - AHAB_BAD_SRK_SET_IND
  - AHAB_BAD_ID_IND
- SC_ERR_LOCKED
  - AHAB_OTP_LOCKED_IND
  - AHAB_LOCKED_REG_IND
- SC_ERR_UNAVAILABLE
  - AHAB_BID_COLLISION_IND
  - AHAB_OOM_FOR_BLOB_IND
  - AHAB_OOM_FOR_BLOB_EXPORT_IND
  - AHAB_HDCP_DISABLED_IND
  - AHAB_NON_SECURE_STATE_IND
  - AHAB_DISABLED_FEATURE_IND
- SC_ERR_BUSY
  - AHAB_ADM_NOT_READY_IND
  - AHAB_TIME_OUT_IND
- SC_ERR_FAIL
  - AHAB_BAD_BLOB_IND
  - AHAB_ENCRYPTION_FAILURE_IND
  - AHAB_DECRYPTION_FAILURE_IND
  - AHAB_BAD_CERTIFICATE_IND
  - AHAB_OTP_PROGFAIL_IND
  - AHAB_KMEK_GENERATION_FAIL_IND
  - AHAB_BAD_SIGNATURE_IND
  - AHAB_INVALID_KEY_IND
  - AHAB_MUST_ATTEST_IND
  - AHAB_RNG_NOT_STARTED_IND
  - AHAB_SECO_FATAL_FAILURE_IND
  - AHAB_RNG_INST_FAILURE_IND
  - AHAB_NO_AUTHENTICATION_IND
  - AHAB_AUTH_SKIPPED_OR_FAILED_IND
- If no mapping exists, SC_ERR_FAIL will be returned

16.27.2 Function Documentation

16.27.2.1 sc_seco_image_load()

```
sc_err_t sc_seco_image_load (
             sc_ipc_t ipc,
             sc_faddr_t addr_src,
             sc_faddr_t addr_dst,
             uint32_t len,
             sc_bool_t fw )
```

This function loads a SECO image.

Parameters

in	*ipc*	IPC handle
in	*addr_src*	address of image source
in	*addr_dst*	address of image destination
in	*len*	length of image to load
in	*fw*	SC_TRUE = firmware load

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This is used to load images via the SECO. Examples include SECO Firmware and IVT/CSF data used for authentication. These are usually loaded into SECO TCM. *addr_src* is in secure memory.

See the *SECO API Reference Guide* for more info.

16.27.2.2 sc_seco_authenticate()

```
sc_err_t sc_seco_authenticate (
            sc_ipc_t ipc,
            sc_seco_auth_cmd_t cmd,
            sc_faddr_t addr )
```

This function is used to authenticate a SECO image or command.

Parameters

in	*ipc*	IPC handle
in	*cmd*	authenticate command
in	*addr*	address of/or metadata

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_BUSY if SECO is busy with another authentication request,
- SC_ERR_FAIL if SECO response is bad,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This is used to authenticate a SECO image or issue a security command. *addr* often points to an container. It is also just data (or even unused) for some commands.

Implementation of this command depends on the underlying security architecture of the device. For example, on devices with SECO FW, the following options apply:

- cmd=SC_SECO_AUTH_CONTAINER, addr=container address (sends AHAB_AUTH_CONTAINER_REQ to SECO)
- cmd=SC_SECO_VERIFY_IMAGE, addr=image mask (sends AHAB_VERIFY_IMAGE_REQ to SECO)
- cmd=SC_SECO_REL_CONTAINER, addr unused (sends AHAB_RELEASE_CONTAINER_REQ to SECO)
- cmd=SC_SECO_AUTH_HDMI_TX_FW, addr unused (sends AHAB_ENABLE_HDMI_X_REQ with Subsystem=0 to SECO)
- cmd=SC_SECO_AUTH_HDMI_RX_FW, addr unused (sends AHAB_ENABLE_HDMI_X_REQ with Subsystem=1 to SECO)

See the *SECO API Reference Guide* for more info.

16.27.2.3 sc_seco_enh_authenticate()

```
sc_err_t sc_seco_enh_authenticate (
             sc_ipc_t ipc,
             sc_seco_auth_cmd_t cmd,
             sc_faddr_t addr,
             uint32_t mask1,
             uint32_t mask2 )
```

This function is used to authenticate a SECO image or command.

This is an enhanced version that has additional mask arguments.

Parameters

in	*ipc*	IPC handle
in	*cmd*	authenticate command
in	*addr*	address of/or metadata
in	*mask1*	metadata
in	*mask2*	metadata

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_BUSY if SECO is busy with another authentication request,
- SC_ERR_FAIL if SECO response is bad,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This supports all the commands found in sc_seco_authenticate(). Those commands should set both masks to 0 (except SC_SECO_VERIFY_IMAGE).

New commands are as follows:

- cmd=SC_SECO_VERIFY_IMAGE, addr unused, mask1=image mask, mask2 unused (sends AHAB_VERIFY↩ _IMAGE_REQ to SECO)
- cmd=SC_SECO_EVERIFY_IMAGE, addr=container address, mask1=image mask, mask2=move mask (sends AHAB_EVERIFY_IMAGE_REQ to SECO)

See the *SECO API Reference Guide* for more info.

16.27.2.4 sc_seco_forward_lifecycle()

```
sc_err_t sc_seco_forward_lifecycle (
            sc_ipc_t ipc,
            uint32_t change )
```

This function updates the lifecycle of the device.

Parameters

in	*ipc*	IPC handle
in	*change*	desired lifecycle transition

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,

- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This function is used for going from Open to NXP Closed to OEM Closed. Note *change* is NOT the new desired lifecycle. It is a lifecycle transition as documented in the *SECO API Reference Guide*.

If any SECO request fails or only succeeds because the part is in an "OEM open" lifecycle, then a request to transition from "NXP closed" to "OEM closed" will also fail. For example, booting a signed container when the OEM SRK is not fused will succeed, but as it is an abnormal situation, a subsequent request to transition the lifecycle will return an error.

16.27.2.5 sc_seco_return_lifecycle()

```
sc_err_t sc_seco_return_lifecycle (
             sc_ipc_t ipc,
             sc_faddr_t addr )
```

This function updates the lifecycle to one of the return lifecycles.

Parameters

in	*ipc*	IPC handle
in	*addr*	address of message block

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Note *addr* must be a pointer to a signed message block.

To switch back to NXP states (Full Field Return), message must be signed by NXP SRK. For OEM States (Partial Field Return), must be signed by OEM SRK.

See the *SECO API Reference Guide* for more info.

16.27.2.6 sc_seco_commit()

```
sc_err_t sc_seco_commit (
             sc_ipc_t ipc,
             uint32_t * info )
```

This function is used to commit into the fuses any new SRK revocation and FW version information that have been found in the primary and secondary containers.

Parameters

in	*ipc*	IPC handle
in,out	*info*	pointer to information type to be committed

The return *info* will contain what was actually committed.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if *info* is invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

16.27.2.7 sc_seco_attest_mode()

```
sc_err_t sc_seco_attest_mode (
             sc_ipc_t ipc,
             uint32_t mode )
```

This function is used to set the attestation mode.

Only the owner of the SC_R_ATTESTATION resource may make this call.

Parameters

in	*ipc*	IPC handle
in	*mode*	mode

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if *mode* is invalid,
- SC_ERR_NOACCESS if SC_R_ATTESTATON not owned by caller,

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This is used to set the SECO attestation mode. This can be prover or verifier. See the *SECO API Reference Guide* for more on the supported modes, mode values, and mode behavior.

16.27.2.8 sc_seco_attest()

```
sc_err_t sc_seco_attest (
             sc_ipc_t ipc,
             uint64_t nonce )
```

This function is used to request attestation.

Only the owner of the SC_R_ATTESTATION resource may make this call.

Parameters

in	*ipc*	IPC handle
in	*nonce*	unique value

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_NOACCESS if SC_R_ATTESTATON not owned by caller,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This is used to ask SECO to perform an attestation. The result depends on the attestation mode. After this call, the signature can be requested or a verify can be requested.

See the *SECO API Reference Guide* for more info.

16.27.2.9 sc_seco_get_attest_pkey()

```
sc_err_t sc_seco_get_attest_pkey (
             sc_ipc_t ipc,
             sc_faddr_t addr )
```

This function is used to retrieve the attestation public key.

Mode must be verifier. Only the owner of the SC_R_ATTESTATION resource may make this call.

Parameters

in	*ipc*	IPC handle
in	*addr*	address to write response

Result will be written to *addr*. The *addr* parameter must point to an address SECO can access. It must be 64-bit aligned. There should be 96 bytes of space.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if *addr* bad or attestation has not been requested,
- SC_ERR_NOACCESS if SC_R_ATTESTATON not owned by caller,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

See the *SECO API Reference Guide* for more info.

16.27.2.10 sc_seco_get_attest_sign()

```
sc_err_t sc_seco_get_attest_sign (
            sc_ipc_t ipc,
            sc_faddr_t addr )
```

This function is used to retrieve attestation signature and parameters.

Mode must be provider. Only the owner of the SC_R_ATTESTATION resource may make this call.

Parameters

in	*ipc*	IPC handle
in	*addr*	address to write response

Result will be written to *addr*. The *addr* parameter must point to an address SECO can access. It must be 64-bit aligned. There should be 120 bytes of space.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if *addr* bad or attestation has not been requested,
- SC_ERR_NOACCESS if SC_R_ATTESTATON not owned by caller,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

See the *SECO API Reference Guide* for more info.

16.27.2.11 sc_seco_attest_verify()

```
sc_err_t sc_seco_attest_verify (
             sc_ipc_t ipc,
             sc_faddr_t addr )
```

This function is used to verify attestation.

Mode must be verifier. Only the owner of the SC_R_ATTESTATION resource may make this call.

Parameters

in	*ipc*	IPC handle
in	*addr*	address of signature

The *addr* parameter must point to an address SECO can access. It must be 64-bit aligned.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if *addr* bad or attestation has not been requested,
- SC_ERR_NOACCESS if SC_R_ATTESTATON not owned by caller,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_FAIL if signature doesn't match,

- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

See the *SECO API Reference Guide* for more info.

16.27.2.12 sc_seco_gen_key_blob()

```
sc_err_t sc_seco_gen_key_blob (
             sc_ipc_t ipc,
             uint32_t id,
             sc_faddr_t load_addr,
             sc_faddr_t export_addr,
             uint16_t max_size )
```

This function is used to generate a SECO key blob.

Parameters

in	*ipc*	IPC handle
in	*id*	key identifier
in	*load_addr*	load address
in	*export_addr*	export address
in	*max_size*	max export size

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This function is used to encapsulate sensitive keys in a specific structure called a blob, which provides both confidentiality and integrity protection.

See the *SECO API Reference Guide* for more info.

16.27.2.13 sc_seco_load_key()

```
sc_err_t sc_seco_load_key (
             sc_ipc_t ipc,
             uint32_t id,
             sc_faddr_t addr )
```

This function is used to load a SECO key.

Parameters

in	*ipc*	IPC handle
in	*id*	key identifier
in	*addr*	key address

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This function is used to install private cryptographic keys encapsulated in a blob previously generated by SECO. The controller can be either the IEE or the VPU. The blob header carries the controller type and the key size, as provided by the user when generating the key blob.

See the *SECO API Reference Guide* for more info.

16.27.2.14 sc_seco_get_mp_key()

```
sc_err_t sc_seco_get_mp_key (
             sc_ipc_t ipc,
             sc_faddr_t dst_addr,
             uint16_t dst_size )
```

This function is used to get the manufacturing protection public key.

Parameters

in	*ipc*	IPC handle
in	*dst_addr*	destination address
in	*dst_size*	destination size

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This function is supported only in OEM-closed lifecycle. It generates the mfg public key and stores it in a specific location in the secure memory.

See the *SECO API Reference Guide* for more info.

16.27.2.15 sc_seco_update_mpmr()

```
sc_err_t sc_seco_update_mpmr (
             sc_ipc_t ipc,
             sc_faddr_t addr,
             uint8_t size,
             uint8_t lock )
```

This function is used to update the manufacturing protection message register.

Parameters

in	*ipc*	IPC handle
in	*addr*	data address
in	*size*	size
in	*lock*	lock_reg

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,

- Others, see the Security Service Detailed Description section

This function is supported only in OEM-closed lifecycle. It updates the content of the MPMR (Manufacturing Protection Message register of 256 bits). This register will be appended to the input-data message when generating the signature. Please refer to the CAAM block guide for details.

See the *SECO API Reference Guide* for more info.

16.27.2.16 sc_seco_get_mp_sign()

```
sc_err_t sc_seco_get_mp_sign (
            sc_ipc_t ipc,
            sc_faddr_t msg_addr,
            uint16_t msg_size,
            sc_faddr_t dst_addr,
            uint16_t dst_size )
```

This function is used to get the manufacturing protection signature.

Parameters

in	*ipc*	IPC handle
in	*msg_addr*	message address
in	*msg_size*	message size
in	*dst_addr*	destination address
in	*dst_size*	destination size

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_PARM if word fuse index param out of range or invalid,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

This function is used to generate an ECDSA signature for an input-data message and to store it in a specific location in the secure memory. It is only supported in OEM-closed lifecycle. In order to get the ECDSA signature, the RNG must be initialized. In case it has not been started an error will be returned.

See the *SECO API Reference Guide* for more info.

16.27.2.17 sc_seco_build_info()

```
void sc_seco_build_info (
            sc_ipc_t ipc,
            uint32_t * version,
            uint32_t * commit )
```

This function is used to return the SECO FW build info.

Parameters

in	*ipc*	IPC handle
out	*version*	pointer to return build number
out	*commit*	pointer to return commit ID (git SHA-1)

16.27.2.18 sc_seco_chip_info()

```
sc_err_t sc_seco_chip_info (
            sc_ipc_t ipc,
            uint16_t * lc,
            uint16_t * monotonic,
            uint32_t * uid_l,
            uint32_t * uid_h )
```

This function is used to return SECO chip info.

Parameters

in	*ipc*	IPC handle
out	*lc*	pointer to return lifecycle
out	*monotonic*	pointer to return monotonic counter
out	*uid_l*	pointer to return UID (lower 32 bits)
out	*uid_h*	pointer to return UID (upper 32 bits)

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

16.27.2.19 sc_seco_enable_debug()

```
sc_err_t sc_seco_enable_debug (
            sc_ipc_t ipc,
            sc_faddr_t addr )
```

This function securely enables debug.

Parameters

in	*ipc*	IPC handle
in	*addr*	address of message block

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Note *addr* must be a pointer to a signed message block.

See the *SECO API Reference Guide* for more info.

16.27.2.20 sc_seco_get_event()

```
sc_err_t sc_seco_get_event (
            sc_ipc_t ipc,
            uint8_t idx,
            uint32_t * event )
```

This function is used to return an event from the SECO error log.

Parameters

in	*ipc*	IPC handle
out	*idx*	index of event to return
out	*event*	pointer to return event

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Read of *idx* 0 captures events from SECO. Loop starting with 0 until an error is returned to dump all events.

16.27.2.21 sc_seco_fuse_write()

```
sc_err_t sc_seco_fuse_write (
             sc_ipc_t ipc,
             sc_faddr_t addr )
```

This function securely writes a group of fuse words.

Parameters

in	*ipc*	IPC handle
in	*addr*	address of message block

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Note *addr* must be a pointer to a signed message block.

See the *SECO API Reference Guide* for more info.

16.27.2.22 sc_seco_patch()

```
sc_err_t sc_seco_patch (
             sc_ipc_t ipc,
             sc_faddr_t addr )
```

This function applies a patch.

Parameters

in	*ipc*	IPC handle
in	*addr*	address of message block

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Note *addr* must be a pointer to a signed message block.

See the *SECO API Reference Guide* for more info.

16.27.2.23 sc_seco_set_mono_counter_partition()

```
sc_err_t sc_seco_set_mono_counter_partition (
            sc_ipc_t ipc,
            uint16_t * she )
```

This function partitions the monotonic counter.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can do this.

Parameters

in	*ipc*	IPC handle
in,out	*she*	pointer to number of SHE bits

SECO uses an OTP monotonic counter to protect the SHE and HSM key-stores from roll-back attack. This function is used to define the number of monotonic counter bits allocated to SHE use. Two monotonic counter bits are used to store this information while the remaining bits are allocated to the HSM user. This function must be called before any SHE or HSM key stores are created in the system, otherwise the default configuration is applied. Returns the actual number of SHE bits.

If the partition has been already configured, any attempt to re-configure the SHE partition to a different value will result in a failure response.

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_NOACCESS if caller does not have SC_R_SYSTEM access
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

See the *SECO API Reference Guide* for more info.

16.27.2.24 sc_seco_set_fips_mode()

```
sc_err_t sc_seco_set_fips_mode (
            sc_ipc_t ipc,
            uint8_t mode,
            uint32_t * reason )
```

This function configures the SECO in FIPS mode.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can do this.

Parameters

in	*ipc*	IPC handle
in	*mode*	FIPS mode
out	*reason*	pointer to return failure reason

This function permanently configures the SECO in FIPS approved mode. When in FIPS approved mode the following services will be disabled and receive a failure response:

- Encrypted boot is not supported
- Attestation is not supported
- Manufacturing protection is not supported
- DTCP load
- SHE services are not supported
- Assign JR is not supported (all JRs owned by SECO)

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_NOACCESS if caller does not have SC_R_SYSTEM access
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

See the *SECO API Reference Guide* for more info.

16.27.2.25 sc_seco_start_rng()

```
sc_err_t sc_seco_start_rng (
             sc_ipc_t ipc,
             sc_seco_rng_stat_t * status )
```

This function starts the random number generator.

Parameters

in	*ipc*	IPC handle
out	*status*	pointer to return state of RNG

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

The RNG is started automatically after all CPUs are booted. This function can be used to start earlier and to check the status.

See the *SECO API Reference Guide* for more info.

16.27.2.26 sc_seco_sab_msg()

```
sc_err_t sc_seco_sab_msg (
             sc_ipc_t ipc,
             sc_faddr_t addr )
```

This function sends a generic signed message to the SECO SHE/HSM components.

Parameters

in	*ipc*	IPC handle
in	*addr*	address of message block

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Note *addr* must be a pointer to a signed message block.

See the *SECO API Reference Guide* for more info.

16.27.2.27 sc_seco_secvio_enable()

```
sc_err_t sc_seco_secvio_enable (
             sc_ipc_t ipc )
```

This function is used to enable security violation and tamper interrupts.

These are then reported using the IRQ service via the SC_IRQ_SECVIO interrupt. Note it is automatically enabled at boot.

Parameters

in	*ipc*	IPC handle

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_NOACCESS if caller does not own SC_R_SECVIO,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,

- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

The security violation interrupt is self-masking. Once it is cleared in the SNVS it must be re-enabled using this function.

16.27.2.28 sc_seco_secvio_config()

```
sc_err_t sc_seco_secvio_config (
            sc_ipc_t ipc,
            uint8_t id,
            uint8_t access,
            uint32_t * data0,
            uint32_t * data1,
            uint32_t * data2,
            uint32_t * data3,
            uint32_t * data4,
            uint8_t size )
```

This function is used to read/write SNVS security violation and tamper registers.

Parameters

in	*ipc*	IPC handle
in	*id*	register ID
in	*access*	0=read, 1=write
in	*data0*	pointer to data to read or write
in	*data1*	pointer to data to read or write
in	*data2*	pointer to data to read or write
in	*data3*	pointer to data to read or write
in	*data4*	pointer to data to read or write
in	*size*	number of valid data words

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_NOACCESS if caller does not own SC_R_SECVIO,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

Unused data words can be passed a NULL pointer.

See AHAB_MANAGE_SNVS_REQ in the *SECO API Reference Guide* for more info.

16.27.2.29 sc_seco_secvio_dgo_config()

```
sc_err_t sc_seco_secvio_dgo_config (
            sc_ipc_t ipc,
            uint8_t id,
            uint8_t access,
            uint32_t * data )
```

This function is used to read/write SNVS security violation and tamper DGO registers.

Parameters

in	*ipc*	IPC handle
in	*id*	regsiter ID
in	*access*	0=read, 1=write
in	*data*	pointer to data to read or write

Returns

Returns and error code (SC_ERR_NONE = success).

Return errors codes:

- SC_ERR_NOACCESS if caller does not own SC_R_SECVIO,
- SC_ERR_UNAVAILABLE if SECO not available,
- SC_ERR_IPC if SECO response has bad header tag or size,
- SC_ERR_VERSION if SECO response has bad version,
- Others, see the Security Service Detailed Description section

See AHAB_MANAGE_SNVS_DGO_REQ in the *SECO API Reference Guide* for more info.

16.27.2.30 seco_image_load()

```
sc_err_t seco_image_load (
            sc_rm_pt_t caller_pt,
            sc_faddr_t addr_src,
            sc_faddr_t addr_dst,
            uint32_t len,
            sc_bool_t fw )
```

Internal SC function to load a SECO image.

See also

sc_seco_image_load().

16.27.2.31 seco_authenticate()

```
sc_err_t seco_authenticate (
             sc_rm_pt_t caller_pt,
             sc_seco_auth_cmd_t cmd,
             sc_faddr_t addr )
```

Internal SC function to authenticate a SECO image or command.

See also

sc_seco_authenticate().

16.27.2.32 seco_enh_authenticate()

```
sc_err_t seco_enh_authenticate (
             sc_rm_pt_t caller_pt,
             sc_seco_auth_cmd_t cmd,
             sc_faddr_t addr,
             uint32_t mask1,
             uint32_t mask2 )
```

Internal SC function to authenticate a SECO image or command ((enhanced version).

See also

sc_seco_enh_authenticate().

16.27.2.33 seco_load_key()

```
sc_err_t seco_load_key (
             sc_rm_pt_t caller_pt,
             uint32_t id,
             sc_faddr_t addr )
```

Internal SC function to load a SECO key.

See also

sc_seco_load_key().

16.27.2.34 seco_gen_key_blob()

```
sc_err_t seco_gen_key_blob (
             sc_rm_pt_t caller_pt,
             uint32_t id,
             sc_faddr_t load_addr,
             sc_faddr_t export_addr,
             uint16_t max_size )
```

Internal SC function to generate a key blob.

See also

sc_seco_gen_key_blob().

16.27.2.35 seco_fuse_write()

```
sc_err_t seco_fuse_write (
             sc_rm_pt_t caller_pt,
             sc_faddr_t addr )
```

Internal SC function to securely write a group of fuse words.

See also

sc_seco_fuse_write().

16.27.2.36 seco_patch()

```
sc_err_t seco_patch (
             sc_rm_pt_t caller_pt,
             sc_faddr_t addr )
```

Internal SC function to apply a patch.

See also

sc_seco_patch().

16.27.2.37 seco_set_mono_counter_partition()

```
sc_err_t seco_set_mono_counter_partition (
            sc_rm_pt_t caller_pt,
            uint16_t * she )
```

Internal SC function to partition the monotonic counter.

See also

sc_seco_set_mono_counter_partition().

16.27.2.38 seco_set_fips_mode()

```
sc_err_t seco_set_fips_mode (
            sc_rm_pt_t caller_pt,
            uint8_t mode,
            uint32_t * reason )
```

Internal SC function to set FIPS mode.

See also

sc_seco_set_fips_mode().

16.27.2.39 seco_start_rng()

```
sc_err_t seco_start_rng (
            sc_rm_pt_t caller_pt,
            sc_seco_rng_stat_t * status )
```

Internal SC function to start the RNG.

See also

sc_seco_start_rng().

16.27.2.40 seco_enable_debug()

```
sc_err_t seco_enable_debug (
             sc_rm_pt_t caller_pt,
             sc_faddr_t addr )
```

Internal SC function to securely enable debug.

See also

sc_seco_enabled_debug().

16.27.2.41 seco_forward_lifecycle()

```
sc_err_t seco_forward_lifecycle (
             sc_rm_pt_t caller_pt,
             uint32_t change )
```

Internal SC function to update the lifecycle.

See also

sc_seco_forward_lifecycle().

16.27.2.42 seco_return_lifecycle()

```
sc_err_t seco_return_lifecycle (
             sc_rm_pt_t caller_pt,
             sc_faddr_t addr )
```

Internal SC function to securely reverse the lifecycle.

See also

sc_seco_return_lifecycle().

16.27.2.43 seco_build_info()

```
void seco_build_info (
             sc_rm_pt_t caller_pt,
             uint32_t * version,
             uint32_t * commit )
```

Internal SC function to return SECO FW version info.

See also

sc_seco_build_info().

16.27.2.44 seco_chip_info()

```
sc_err_t seco_chip_info (
            sc_rm_pt_t caller_pt,
            uint16_t * lc,
            uint16_t * monotonic,
            uint32_t * uid_l,
            uint32_t * uid_h )
```

Internal SC function to return SECO chip info.

See also

sc_seco_chip_info().

16.27.2.45 seco_get_event()

```
sc_err_t seco_get_event (
            sc_rm_pt_t caller_pt,
            uint8_t idx,
            uint32_t * event )
```

Internal SC function to return an event from the SECO error log.

See also

sc_seco_get_event().

16.27.2.46 seco_attest_mode()

```
sc_err_t seco_attest_mode (
            sc_rm_pt_t caller_pt,
            uint32_t mode )
```

Internal SC function to set the attestation mode.

See also

sc_seco_attest_mode().

16.27.2.47 seco_attest()

```
sc_err_t seco_attest (
            sc_rm_pt_t caller_pt,
            uint64_t nonce )
```

Internal SC function to request atestation.

See also

sc_seco_attest().

16.27.2.48 seco_get_attest_pkey()

```
sc_err_t seco_get_attest_pkey (
            sc_rm_pt_t caller_pt,
            sc_faddr_t addr )
```

Internal SC function to retrieve attestation public key.

See also

sc_seco_get_attest_pkey().

16.27.2.49 seco_get_attest_sign()

```
sc_err_t seco_get_attest_sign (
            sc_rm_pt_t caller_pt,
            sc_faddr_t addr )
```

Internal SC function to retrieve attestation signature and parameters.

See also

sc_seco_get_attest_sign().

16.27.2.50 seco_attest_verify()

```
sc_err_t seco_attest_verify (
            sc_rm_pt_t caller_pt,
            sc_faddr_t addr )
```

Internal SC function to verify attestation.

See also

sc_seco_attest_verify().

16.27.2.51 seco_commit()

```
sc_err_t seco_commit (
             sc_rm_pt_t caller_pt,
             uint32_t * info )
```

Internal SC function to commit SRK/FW changes.

See also

sc_seco_commit().

16.27.2.52 seco_get_mp_key()

```
sc_err_t seco_get_mp_key (
             sc_rm_pt_t caller_pt,
             sc_faddr_t dst_addr,
             uint16_t dst_size )
```

Internal SC function to get manufacturing protection public key.

See also

sc_seco_get_mp_key().

16.27.2.53 seco_update_mpmr()

```
sc_err_t seco_update_mpmr (
             sc_rm_pt_t caller_pt,
             sc_faddr_t addr,
             uint8_t size,
             uint8_t lock )
```

Internal SC function to update manufacturing protection message register.

See also

sc_seco_update_mpmr().

16.27.2.54 seco_get_mp_sign()

```
sc_err_t seco_get_mp_sign (
            sc_rm_pt_t caller_pt,
            sc_faddr_t msg_addr,
            uint16_t msg_size,
            sc_faddr_t dst_addr,
            uint16_t dst_size )
```

Internal SC function to get manufacturing protection signature.

See also

sc_seco_get_mp_sign().

16.27.2.55 seco_sab_msg()

```
sc_err_t seco_sab_msg (
            sc_rm_pt_t caller_pt,
            sc_faddr_t addr )
```

Internal SC function to send a generic signed message to the SECO SHE/HSM components.

See also

sc_seco_sab_msg().

16.27.2.56 seco_secvio_enable()

```
sc_err_t seco_secvio_enable (
            sc_rm_pt_t caller_pt )
```

Internal SC function to enable the security violation interrupt.

See also

sc_seco_secvio_enable().

16.27.2.57 seco_secvio_config()

```
sc_err_t seco_secvio_config (
             sc_rm_pt_t caller_pt,
             uint8_t id,
             uint8_t access,
             uint32_t * data0,
             uint32_t * data1,
             uint32_t * data2,
             uint32_t * data3,
             uint32_t * data4,
             uint8_t size )
```

Internal SC function to read/write SNVS security violation and tamper registers.

See also

sc_seco_secvio_config().

16.27.2.58 seco_secvio_dgo_config()

```
sc_err_t seco_secvio_dgo_config (
             sc_rm_pt_t caller_pt,
             uint8_t id,
             uint8_t access,
             uint32_t * data )
```

Internal SC function to read/write SNVS security violation and tamper DGO registers.

See also

sc_seco_secvio_dgo_config().

16.28 RM: Resource Management Service

Module for the Resource Management (RM) service.

Macros

- #define SC_SS_IDX_W 8U

  Width of SS index.
- #define SC_PT_ALL SC_RM_NUM_PARTITION

  Define used to indicate function should apply to all partitions.

Typedefs

- typedef uint8_t sc_rm_pt_t

  This type is used to declare a resource partition.
- typedef uint8_t sc_rm_mr_t

  This type is used to declare a memory region.
- typedef uint8_t sc_rm_did_t

  This type is used to declare a resource domain ID used by the isolation HW.
- typedef uint16_t sc_rm_sid_t

  This type is used to declare an SMMU StreamID.
- typedef uint8_t sc_rm_spa_t

  This type is a used to declare master transaction attributes.
- typedef uint8_t sc_rm_perm_t

  This type is used to declare a resource/memory region access permission.
- typedef uint8_t sc_rm_det_t

  This type is used to indicate memory region transactions should detour to the IEE.
- typedef uint8_t sc_rm_rmsg_t

  This type is used to assign an RMSG value to a memory region.
- typedef uint8_t sc_ss_idx_t

  Type for a ss resource index.

Variables

- uint8_t rm_max_did

  Max domain used.

Defines for type widths

- #define SC_RM_PARTITION_W 5U

  Width of sc_rm_pt_t.
- #define SC_RM_MEMREG_W 6U

  Width of sc_rm_mr_t.
- #define SC_RM_DID_W 4U

  Width of sc_rm_did_t.
- #define SC_RM_SID_W 6U

  Width of sc_rm_sid_t.
- #define SC_RM_SPA_W 2U

  Width of sc_rm_spa_t.
- #define SC_RM_PERM_W 3U

  Width of sc_rm_perm_t.
- #define SC_RM_DET_W 1U

  Width of sc_rm_det_t.
- #define SC_RM_RMSG_W 4U

  Width of sc_rm_rmsg_t.

Defines for ALL parameters

- #define SC_RM_PT_ALL ((sc_rm_pt_t) UINT8_MAX)

  All partitions.
- #define SC_RM_MR_ALL ((sc_rm_mr_t) UINT8_MAX)

  All memory regions.

Defines for sc_rm_spa_t

- #define SC_RM_SPA_PASSTHRU 0U

  Pass through (attribute driven by master)
- #define SC_RM_SPA_PASSSID 1U

  Pass through and output on SID.
- #define SC_RM_SPA_ASSERT 2U

  Assert (force to be secure/privileged)
- #define SC_RM_SPA_NEGATE 3U

  Negate (force to be non-secure/user)

Defines for sc_rm_perm_t

- #define SC_RM_PERM_NONE 0U

  No access.
- #define SC_RM_PERM_SEC_R 1U

  Secure RO.
- #define SC_RM_PERM_SECPRIV_RW 2U

  Secure privilege R/W.
- #define SC_RM_PERM_SEC_RW 3U

  Secure R/W.
- #define SC_RM_PERM_NSPRIV_R 4U

  Secure R/W, non-secure privilege RO.
- #define SC_RM_PERM_NS_R 5U

  Secure R/W, non-secure RO.
- #define SC_RM_PERM_NSPRIV_RW 6U

  Secure R/W, non-secure privilege R/W.
- #define SC_RM_PERM_FULL 7U

  Full access.

Partition Functions

- sc_err_t sc_rm_partition_alloc (sc_ipc_t ipc, sc_rm_pt_t *pt, sc_bool_t secure, sc_bool_t isolated, sc_bool_t restricted, sc_bool_t grant, sc_bool_t coherent)

  This function requests that the SC create a new resource partition.
- sc_err_t sc_rm_set_confidential (sc_ipc_t ipc, sc_rm_pt_t pt, sc_bool_t retro)

  This function makes a partition confidential.
- sc_err_t sc_rm_partition_free (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function frees a partition and assigns all resources to the caller.
- sc_rm_did_t sc_rm_get_did (sc_ipc_t ipc)

  This function returns the DID of a partition.
- sc_err_t sc_rm_partition_static (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rm_did_t did)

  This function forces a partition to use a specific static DID.
- sc_err_t sc_rm_partition_lock (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function locks a partition.
- sc_err_t sc_rm_get_partition (sc_ipc_t ipc, sc_rm_pt_t *pt)

  This function gets the partition handle of the caller.
- sc_err_t sc_rm_set_parent (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rm_pt_t pt_parent)

  This function sets a new parent for a partition.
- sc_err_t sc_rm_move_all (sc_ipc_t ipc, sc_rm_pt_t pt_src, sc_rm_pt_t pt_dst, sc_bool_t move_rsrc, sc_bool_t move_pads)

  This function moves all movable resources/pads owned by a source partition to a destination partition.

Resource Functions

- sc_err_t sc_rm_assign_resource (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rsrc_t resource)

  This function assigns ownership of a resource to a partition.
- sc_err_t sc_rm_set_resource_movable (sc_ipc_t ipc, sc_rsrc_t resource_fst, sc_rsrc_t resource_lst, sc_bool_t movable)

  This function flags resources as movable or not.
- sc_err_t sc_rm_set_subsys_rsrc_movable (sc_ipc_t ipc, sc_rsrc_t resource, sc_bool_t movable)

  This function flags all of a subsystem's resources as movable or not.
- sc_err_t sc_rm_set_master_attributes (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_spa_t sa, sc_rm_spa_t pa, sc_bool_t smmu_bypass)

  This function sets attributes for a resource which is a bus master (i.e.
- sc_err_t sc_rm_set_master_sid (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_sid_t sid)

  This function sets the StreamID for a resource which is a bus master (i.e.
- sc_err_t sc_rm_set_peripheral_permissions (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_pt_t pt, sc_rm_perm_t perm)

  This function sets access permissions for a peripheral resource.
- sc_bool_t sc_rm_is_resource_owned (sc_ipc_t ipc, sc_rsrc_t resource)

  This function gets ownership status of a resource.
- sc_err_t sc_rm_get_resource_owner (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_pt_t *pt)

  This function is used to get the owner of a resource.
- sc_bool_t sc_rm_is_resource_master (sc_ipc_t ipc, sc_rsrc_t resource)

  This function is used to test if a resource is a bus master.
- sc_bool_t sc_rm_is_resource_peripheral (sc_ipc_t ipc, sc_rsrc_t resource)

  This function is used to test if a resource is a peripheral.
- sc_err_t sc_rm_get_resource_info (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_sid_t *sid)

  This function is used to obtain info about a resource.

Memory Region Functions

- sc_err_t sc_rm_memreg_alloc (sc_ipc_t ipc, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_end)

  This function requests that the SC create a new memory region.
- sc_err_t sc_rm_memreg_split (sc_ipc_t ipc, sc_rm_mr_t mr, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)

  This function requests that the SC split an existing memory region.
- sc_err_t sc_rm_memreg_frag (sc_ipc_t ipc, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)

  This function requests that the SC fragment a memory region.
- sc_err_t sc_rm_memreg_free (sc_ipc_t ipc, sc_rm_mr_t mr)

  This function frees a memory region.
- sc_err_t sc_rm_find_memreg (sc_ipc_t ipc, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_end)

  Internal SC function to find a memory region.
- sc_err_t sc_rm_assign_memreg (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rm_mr_t mr)

  This function assigns ownership of a memory region.
- sc_err_t sc_rm_set_memreg_permissions (sc_ipc_t ipc, sc_rm_mr_t mr, sc_rm_pt_t pt, sc_rm_perm_t perm)

  This function sets access permissions for a memory region.
- sc_err_t sc_rm_set_memreg_iee (sc_ipc_t ipc, sc_rm_mr_t mr, sc_rm_det_t det, sc_rm_rmsg_t rmsg)

  This function configures the IEE parameters for a memory region.
- sc_bool_t sc_rm_is_memreg_owned (sc_ipc_t ipc, sc_rm_mr_t mr)

  This function gets ownership status of a memory region.
- sc_err_t sc_rm_get_memreg_info (sc_ipc_t ipc, sc_rm_mr_t mr, sc_faddr_t *addr_start, sc_faddr_t *addr_end)

  This function is used to obtain info about a memory region.

Pad Functions

- sc_err_t sc_rm_assign_pad (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pad_t pad)

  This function assigns ownership of a pad to a partition.
- sc_err_t sc_rm_set_pad_movable (sc_ipc_t ipc, sc_pad_t pad_fst, sc_pad_t pad_lst, sc_bool_t movable)

  This function flags pads as movable or not.
- sc_bool_t sc_rm_is_pad_owned (sc_ipc_t ipc, sc_pad_t pad)

  This function gets ownership status of a pad.

Debug Functions

- void sc_rm_dump (sc_ipc_t ipc)

  This function dumps the RM state for debug.

Internal Functions

- void rm_init (sc_bool_t api_phase)

  Internal SC function to initialize the RM service.
- sc_err_t rm_reserve_static_pt (sc_rm_pt_t num)

  Internal SC function to specify the number of static partitions.
- sc_err_t rm_reserve_static_did (sc_rm_did_t num)

  Internal SC function to specify the number of static domains.
- sc_err_t rm_partition_alloc (sc_rm_pt_t caller_pt, sc_rm_pt_t *pt, sc_bool_t secure, sc_bool_t isolated, sc_bool_t restricted, sc_bool_t grant, sc_bool_t coherent)

  Internal SC function to request that the SC create a new resource partition.
- sc_err_t rm_set_confidential (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_bool_t retro)

  Internal SC function to make a partition confidential.
- sc_err_t rm_partition_free (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  Internal SC function to free a partition and assigns all resources to the caller.
- sc_err_t rm_get_partition (sc_rm_pt_t caller_pt, sc_rm_pt_t *pt)

  Internal SC function to get the partition handle of the caller.
- sc_bool_t rm_is_partition_used (sc_rm_pt_t pt)

  Internal SC function to determine if a partition is enabled (used) or not.
- sc_bool_t rm_is_secure_partition (sc_rm_pt_t caller_pt)

  Internal SC function to get the security state of partition.
- sc_bool_t rm_is_partition_isolated (sc_rm_pt_t pt)

  Internal SC function to get the isolation state of partition.
- sc_bool_t rm_is_sys_access (sc_rm_pt_t pt)

  Internal SC function to return if the partition has system access.
- sc_rm_pt_t rm_get_partition_parent (sc_rm_pt_t pt)

  Internal SC function to return the parent of a partition.
- sc_rm_did_t rm_get_did (sc_rm_pt_t caller_pt)

  Internal SC function to get the DID of the caller's partition.
- sc_err_t rm_partition_static (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rm_did_t did)

  Internal SC function to force a partition to use a specific static DID.
- sc_err_t rm_partition_lock (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

Internal SC function to lock a partition.

- sc_err_t rm_set_parent (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rm_pt_t pt_parent)

  Internal SC function to set a new parent for a partition.
- sc_bool_t rm_is_parent (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  Internal SC function to check if caller is the parent of a partition.
- sc_bool_t rm_check_ancestor (sc_rm_pt_t caller_pt, sc_rm_pt_t pt_owner)

  Internal SC function to check if caller is an ancestor of owner.
- sc_err_t rm_move_all (sc_rm_pt_t caller_pt, sc_rm_pt_t pt_src, sc_rm_pt_t pt_dst, sc_bool_t move_rsrc, sc_bool_t move_pads)

  Internal SC function to move all resources/pads owned by a source partition to a destination partition.
- sc_err_t rm_assign_resource (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rsrc_t resource)

  Internal SC function to assign ownership of a resource to a partition.
- sc_err_t rm_set_resource_movable (sc_rm_pt_t caller_pt, sc_rsrc_t resource_fst, sc_rsrc_t resource_lst, sc_bool_t movable)

  Internal SC function to flag resource as movable or not.
- sc_err_t rm_set_subsys_rsrc_movable (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_bool_t movable)

  Internal SC function to flag all of a subsystem's resources as movable or not.
- sc_err_t rm_set_master_attributes (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_spa_t sa, sc_rm_spa_t pa, sc_bool_t smmu_bypass)

  Internal SC function to set attributes for a resource which is a bus master (i.e.
- sc_err_t rm_set_master_sid (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_sid_t sid)

  Internal SC function to set the StreamID for a resource which is a bus master (i.e.
- sc_err_t rm_update_master (sc_rm_idx_t idx)

  Internal SC function to update a master resource.
- sc_err_t rm_set_peripheral_permissions (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_pt_t pt, sc_rm_perm_t perm)

  Internal SC function to set access permissions for a peripheral resource.
- sc_err_t rm_update_peripheral (sc_rm_idx_t idx)

  Internal SC function to update a peripheral resource.
- void rm_update_resource (sc_rsrc_t resource)

  Internal SC function to update a resource in HW.
- void rm_get_ridx_ss_info (sc_rm_idx_t idx, sc_sub_t *ss, sc_ss_idx_t *ss_idx)

  Internal SC function to return subsystem specific info about a resource.
- sc_bool_t rm_check_map_ridx (sc_rsrc_t resource, sc_rm_idx_t *idx)

  Internal SC function to check the validity of a resource and return the unified resource index.
- void rm_check_map_ridx_v (sc_rsrc_t resource, sc_rm_idx_t *idx)

  Internal SC function to check the validity of a resource and return the unified resource index.
- sc_bool_t rm_is_resource_owned (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function to get ownership status of a resource.
- sc_bool_t rm_is_ridx_owned (sc_rm_pt_t caller_pt, sc_rm_idx_t idx)

  Internal SC function to check if a resource is owned by the caller.
- sc_bool_t rm_is_resource_avail (sc_rsrc_t resource)

  Internal SC function to check if a resource is available.
- sc_bool_t rm_is_ridx_avail (sc_rm_idx_t idx)

  Internal SC function to check if a resource is available.
- sc_bool_t rm_is_resource_access_allowed (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function to get access rights of a resource.
- sc_bool_t rm_is_ridx_access_allowed (sc_rm_pt_t caller_pt, sc_rm_idx_t idx)

Internal SC function to check if a resource is controllable by the caller.

- sc_err_t rm_get_resource_owner (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_pt_t *pt)

  Internal SC function to return the owner partition for a resource.
- void rm_get_ridx_owner (sc_rm_idx_t idx, sc_rm_pt_t *pt)

  Internal SC function to return the ownering partition for a resource.
- sc_bool_t rm_is_resource_master (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function used to test if a resource is a bus master.
- sc_bool_t rm_is_ridx_master (sc_rm_idx_t idx)

  Internal SC function to check if a resource is a master.
- sc_bool_t rm_is_resource_peripheral (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function used to test if a resource is a peripheral.
- sc_bool_t rm_is_ridx_peripheral (sc_rm_idx_t idx)

  Internal SC function to check if a resource is a peripheral.
- sc_err_t rm_get_resource_info (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_sid_t *sid)

  Internal SC function used to obtain info about a resource.
- sc_bool_t rm_ridx_block (sc_rm_idx_t idx, sc_bool_t block)

  Internal SC function to control if a access to a resource should be blocked via HW.
- sc_err_t rm_memreg_alloc (sc_rm_pt_t caller_pt, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_end)

  Internal SC function to request that the SC create a new memory region.
- sc_err_t rm_memreg_split (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)

  Internal SC function to split a memory region.
- sc_err_t rm_memreg_frag (sc_rm_pt_t caller_pt, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr↩_end)

  Internal SC function to fragment a memory region.
- sc_err_t rm_memreg_free (sc_rm_pt_t caller_pt, sc_rm_mr_t mr)

  Internal SC function to free a memory region.
- sc_err_t rm_find_memreg (sc_rm_pt_t caller_pt, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_end)

  Internal SC function to find a memory region.
- sc_err_t rm_assign_memreg (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rm_mr_t mr)

  Internal SC function to assign ownership of a memory region.
- sc_err_t rm_set_memreg_permissions (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_rm_pt_t pt, sc_rm_perm_t perm)

  Internal SC function to set access permissions for a memory region.
- sc_err_t rm_set_memreg_iee (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_rm_det_t det, sc_rm_rmsg_t rmsg)

  Internal SC function to set configure IEE parameters for a mem region.
- sc_bool_t rm_is_memreg_owned (sc_rm_pt_t caller_pt, sc_rm_mr_t mr)

  Internal SC function to get ownership status of a memory region.
- sc_err_t rm_get_memreg_info (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_faddr_t *addr_start, sc_faddr_t *addr↩_end)

  Internal SC function used to obtain info about a memory region.
- sc_err_t rm_assign_pad (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pad_t pad)

  Internal SC function to assign ownership of a pad to a partition.
- sc_err_t rm_set_pad_movable (sc_rm_pt_t caller_pt, sc_pad_t pad_first, sc_pad_t pad_last, sc_bool_t movable)

  Internal SC function to flag pad as movable or not.
- sc_bool_t rm_is_pad_owned (sc_rm_pt_t caller_pt, sc_pad_t pad)

  Internal SC function to get ownership status of a pad.
- sc_err_t rm_get_pad_owner (sc_pad_t pad, sc_rm_pt_t *pt)

Internal SC function to get the owner of a pad.

- void rm_enable_blocking (void)

  Enable blocking of resources powered off.

- sc_err_t rm_init_subsys (sc_sub_t ss, sc_bool_t block_enb)

  Internal SC function to reload a subsystem's XRDC info after a power on.

- void rm_dump (sc_rm_pt_t caller_pt)

  Internal SC function to dump RM state for debug.

Debug Functions

- void rm_dump_partition (sc_rm_pt_t pt)

  Internal SC function to dump the internal partition state of the RM service.

- void rm_dump_resources (sc_rm_pt_t pt)

  Internal SC function to dump the internal resource state of the RM service.

- void rm_dump_memregs (sc_rm_pt_t pt)

  Internal SC function to dump the internal memory state of the RM service.

- void rm_dump_pads (sc_rm_pt_t pt)

  Internal SC function to dump the internal pad state of the RM service.

16.28.1 Detailed Description

Module for the Resource Management (RM) service.

The following SCFW resource manager (RM) code is an example of how to create a partition for an M4 core and its resources. This could be run from another core, an SCD, or be embedded into board.c.

The ipc parameter most functions take is a handle to the IPC channel opened to communicate to the SC. It is implementation defined. Most API ports include an sc_ipc_open() and sc_ipc_close() function to manage this. The sc_ipc_open() takes an argument to identify the communication channel (usually the MU address) and returns the IPC handle that all API calls should then use.

Note all this configuration can be done with the M4 subsystem powered off. It will be loaded when the M4 is powered on.

```
00001 sc_rm_pt_t pt_m4_0;
00002 sc_rm_mr_t mr_ddr1, mr_ddr2, mr_m4_0;
00003
00004 //sc_rm_dump(ipc);
00005
00006 /* Mark all resources as not movable */
00007 sc_rm_set_resource_movable(ipc, SC_R_ALL, SC_R_ALL, SC_FALSE);
00008 sc_rm_set_pad_movable(ipc, SC_P_ALL, SC_P_ALL, SC_FALSE);
00009
00010 /* Allocate M4_0 partition */
00011 sc_rm_partition_alloc(ipc, &pt_m4_0, SC_FALSE, SC_TRUE, SC_FALSE, SC_TRUE,
00012     SC_FALSE);
00013
00014 /* Mark all M4_0 subsystem resources as movable */
00015 sc_rm_set_subsys_rsrc_movable(ipc, SC_R_M4_0_PID0, SC_TRUE);
00016 sc_rm_set_pad_movable(ipc,SC_P_ADC_IN3,SC_P_ADC_IN2, SC_TRUE);
00017
00018 /* Keep some resources in the parent partition */
00019 sc_rm_set_resource_movable(ipc, SC_R_M4_0_PID1, SC_R_M4_0_PID4,
00020     SC_FALSE);
00021 sc_rm_set_resource_movable(ipc, SC_R_M4_0_MU_0A0, SC_R_M4_0_MU_0A3,
```

```
00022     SC_FALSE);
00023
00024 /* Move some resource not in the M4_0 subsystem */
00025 sc_rm_set_resource_movable(ipc, SC_R_IRQSTR_M4_0, SC_R_IRQSTR_M4_0,
00026     SC_TRUE);
00027 sc_rm_set_resource_movable(ipc, SC_R_M4_1_MU_0A0, SC_R_M4_1_MU_0A0,
00028     SC_TRUE);
00029
00030 /* Move everything flagged as movable */
00031 sc_rm_move_all(ipc, pt, pt_m4_0, SC_TRUE, SC_TRUE);
00032
00033 /* Allow all to access the SEMA42 */
00034 sc_rm_set_peripheral_permissions(ipc, pt_m4_0, SC_R_M4_0_SEMA42,
00035     SC_RM_PT_ALL, SC_RM_PERM_FULL);
00036
00037 /* Move M4 0 TCM */
00038 sc_rm_find_memreg(ipc, &mr_m4_0, 0x034FE0000, 0x034FE0000);
00039 sc_rm_assign_memreg(ipc, pt_m4_0, mr_m4_0);
00040
00041 /* Split DDR space, assign 0x88000000-0x8FFFFFFF to CM4 */
00042 sc_rm_find_memreg(ipc, &mr_ddr1, 0x080000000, 0x080000000);
00043 sc_rm_memreg_split(ipc, mr_ddr1, &mr_ddr2, 0x090000000, 0x0FFFFFFFF);
00044
00045 /* Reserve DDR for M4_0 */
00046 sc_rm_memreg_split(ipc, mr_ddr1, &mr_m4_0, 0x088000000, 0x08FFFFFFF);
00047 sc_rm_assign_memreg(ipc, pt_m4_0, mr_m4_0);
00048
00049 //sc_rm_dump(ipc);
```

First, variables are declared to hold return partition and memory region handles.

```
00000 sc_rm_pt_t pt_m4_0;
00001 sc_rm_mr_t mr_ddr1, mr_ddr2, mr_m4_0;
```

Optionally, call sc_rm_dump() to dump the state of the RM to the SCFW debug UART.

```
00002 //sc_rm_dump(ipc);
```

Mark resources and pins as movable or not movable to the new partition. By default, all resources are marked as movable. Marking all as movable or not movable first depends on how many resources are to be moved and which is the most efficient. Marking does not move the resource yet. Note, that it is also possible to assign resources individually using sc_rm_assign_resource().

```
00004 /* Mark all resources as not movable */
00006 sc_rm_set_resource_movable(ipc, SC_R_ALL, SC_R_ALL, SC_FALSE);
00007 sc_rm_set_pad_movable(ipc, SC_P_ALL, SC_P_ALL, SC_FALSE);
```

The sc_rm_partition_alloc() function call requests that the SC create a new partition to contain the M4 system. This function does not access the hardware at all. It allocates a new partition and returns a partition handle (pt_m4_0). The partition is marked non-secure as secure=SC_FALSE. Marking as non-secure prevents subsequent functions from configuring masters in this partition to assert the TZPROT signal.

```
00008 /* Allocate M4_0 partition */
00010 sc_rm_partition_alloc(ipc, &pt_m4_0, SC_FALSE, SC_TRUE, SC_FALSE, SC_TRUE,
00011     SC_FALSE);
```

Now mark some resources as movable. sc_rm_set_subsys_rsrc_movable() can be used to mark all resources in a HW subsystem. sc_rm_set_pad_movable() is used to mark some pads (i.e. pins) as movable.

```
00012 /* Mark all M4_0 subsystem resources as movable */
00014 sc_rm_set_subsys_rsrc_movable(ipc, SC_R_M4_0_PID0, SC_TRUE);
00015 sc_rm_set_pad_movable(ipc,SC_P_ADC_IN3,SC_P_ADC_IN2, SC_TRUE);
```

Then mark some resources in the M4_0 subsystem (all marked movable above) as not movable using sc_rm_set_resource_movable() In this case the process IDs used to access memory owned by other partitions as well as the MUs used for others to communicate with the M4 need to be left with the parent partition.

```
00016 /* Keep some resources in the parent partition */
```

```
00018 sc_rm_set_resource_movable(ipc, SC_R_M4_0_PID1, SC_R_M4_0_PID4,
00019     SC_FALSE);
00020 sc_rm_set_resource_movable(ipc, SC_R_M4_0_MU_0A0, SC_R_M4_0_MU_0A3,
00021     SC_FALSE);
```

Move some resources in other subsystems. The new partition will require access to the IRQ Steer module which routes interrupts to this M4's NVIC. In this example, it also needs access to one of the M4_1 MUs.

```
00022 /* Move some resource not in the M4_0 subsystem */
00024 sc_rm_set_resource_movable(ipc, SC_R_IRQSTR_M4_0, SC_R_IRQSTR_M4_0,
```

Now assign (i.e. move) everything marked as movable. At this point, all these resources are in the new partition and HW will enforce isolation.

```
00025 /* Move everything flagged as movable */
00030 sc_rm_move_all(ipc, pt, pt_m4_0, SC_TRUE, SC_TRUE);
```

Allow others to access some of the new partitions resources. In this case, the SEMA42 IP works by allowing multiple CPUs to access and acquire the semaphore.

```
00031 /* Allow all to access the SEMA42 */
00033 sc_rm_set_peripheral_permissions(ipc, pt_m4_0, SC_R_M4_0_SEMA42,
00034     SC_RM_PT_ALL, SC_RM_PERM_FULL);
```

Now assign the M4_0 TCM to the M4 partition. Note the M4 can always access its TCM. This action prevents the parent (current owner of the M4 TCM) from accessing. This should only be done after code for the M4 has been loaded into the TCM. Code loading will require the M4 subsystem already be powered on.

```
00035 /* Move M4 0 TCM */
00037 sc_rm_find_memreg(ipc, &mr_m4_0, 0x034FE0000, 0x034FE0000);
00038 sc_rm_assign_memreg(ipc, pt_m4_0, mr_m4_0);
```

Next is to carve out some DDR for the M4. In this case, the memory is in the middle of the DDR so the DDR has to be split into three regions. First is to split off the end portion and keep this with the parent. Next is then to split off the end of the remaining part and assign this to the M4.

```
00039 /* Split DDR space, assign 0x88000000-0x8FFFFFFF to CM4 */
00041 sc_rm_find_memreg(ipc, &mr_ddr1, 0x080000000, 0x080000000);
00042 sc_rm_memreg_split(ipc, mr_ddr1, &mr_ddr2, 0x090000000, 0x0FFFFFFFF);
00043
00044 /* Reserve DDR for M4_0 */
00045 sc_rm_memreg_split(ipc, mr_ddr1, &mr_m4_0, 0x088000000, 0x08FFFFFFF);
00046 sc_rm_assign_memreg(ipc, pt_m4_0, mr_m4_0);
```

Optionally, call sc_rm_dump() to dump the state of the RM to the SCFW debug UART.

```
00047 //sc_rm_dump(ipc);
```

At this point, the M4 can be powered on (if not already) and the M4 can be started using sc_pm_boot(). *Do NOT start the CPU using sc_pm_cpu_start() as that function is for starting a secondary CPU in the calling core's partition.* In this case, the core is in another partition that needs to be booted.

Refer to the SoC-specific RESOURCES for a list of resources.

16.28.2 Typedef Documentation

16.28.2.1 sc_rm_perm_t

```
typedef uint8_t sc_rm_perm_t
```

This type is used to declare a resource/memory region access permission.

Refer to the XRDC2 Block Guide for more information.

16.28.2.2 sc_rm_rmsg_t

```
typedef uint8_t sc_rm_rmsg_t
```

This type is used to assign an RMSG value to a memory region.

This value is sent to the IEE.

16.28.3 Function Documentation

16.28.3.1 sc_rm_partition_alloc()

```
sc_err_t sc_rm_partition_alloc (
             sc_ipc_t ipc,
             sc_rm_pt_t * pt,
             sc_bool_t secure,
             sc_bool_t isolated,
             sc_bool_t restricted,
             sc_bool_t grant,
             sc_bool_t coherent )
```

This function requests that the SC create a new resource partition.

Parameters

in	*ipc*	IPC handle
out	*pt*	return handle for partition; used for subsequent function calls associated with this partition
in	*secure*	boolean indicating if this partition should be secure; only valid if caller is secure
in	*isolated*	boolean indicating if this partition should be HW isolated via XRDC; set SC_TRUE if new DID is desired
in	*restricted*	boolean indicating if this partition should be restricted; set SC_TRUE if masters in this partition cannot create new partitions
in	*grant*	boolean indicating if this partition should always grant access and control to the parent
in	*coherent*	boolean indicating if this partition is coherent; set SC_TRUE if only this partition will contain both AP clusters and they will be coherent via the CCI

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_ERR_PARM if caller's partition is not secure but a new secure partition is requested,
- SC_ERR_LOCKED if caller's partition is locked,
- SC_ERR_UNAVAILABLE if partition table is full (no more allocation space)

Marking as non-secure prevents subsequent functions from configuring masters in this partition to assert the secure signal. Basically, if TrustZone SW is used, the Cortex-A cores and peripherals the TZ SW will use should be in a secure partition. Almost all other partitions (for a non-secure OS or M4 cores) should be in non-secure partitions.

Isolated should be true for almost all partitions. The exception is the non-secure partition for a Cortex-A core used to run a non-secure OS. This isn't isolated by domain but is instead isolated by the TZ security hardware.

If restricted then the new partition is limited in what functions it can call, especially those associated with managing partitions.

The grant option is usually used to isolate a bus master's traffic to specific memory without isolating the peripheral interface of the master or the API controls of that master. This is only used when creating a sub-partition with no CPU. It's useful to separate out a master and the memory it uses.

16.28.3.2 sc_rm_set_confidential()

```
sc_err_t sc_rm_set_confidential (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_bool_t retro )
```

This function makes a partition confidential.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition that is granting
in	*retro*	retroactive

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if *pt* out of range,

- SC_ERR_NOACCESS if caller's not allowed to change *pt*
- SC_ERR_LOCKED if partition *pt* is locked

Call to make a partition confidential. Confidential means only this partition should be able to grant access permissions to this partition.

If retroactive, then all resources owned by other partitions will have access rights for this partition removed, even if locked.

16.28.3.3 sc_rm_partition_free()

```
sc_err_t sc_rm_partition_free (
             sc_ipc_t ipc,
             sc_rm_pt_t pt )
```

This function frees a partition and assigns all resources to the caller.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to free

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if *pt* out of range or invalid,
- SC_ERR_NOACCESS if *pt* is the SC partition,
- SC_ERR_NOACCESS if caller's partition is not the parent of *pt*,
- SC_ERR_LOCKED if *pt* or caller's partition is locked

All resources, memory regions, and pads are assigned to the caller/parent. The partition watchdog is disabled (even if locked). DID is freed.

16.28.3.4 sc_rm_get_did()

```
sc_rm_did_t sc_rm_get_did (
             sc_ipc_t ipc )
```

This function returns the DID of a partition.

Parameters

in	*ipc*	IPC handle

Returns

Returns the domain ID (DID) of the caller's partition.

The DID is a SoC-specific internal ID used by the HW resource protection mechanism. It is only required by clients when using the SEMA42 module as the DID is sometimes connected to the master ID.

16.28.3.5 sc_rm_partition_static()

```
sc_err_t sc_rm_partition_static (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_rm_did_t did )
```

This function forces a partition to use a specific static DID.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to assign *did*
in	*did*	static DID to assign

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if *pt* or *did* out of range,
- SC_ERR_NOACCESS if caller's partition is not the parent of *pt*,
- SC_ERR_LOCKED if *pt* is locked

Assumes no assigned resources or memory regions yet! The number of static DID is fixed by the SC at boot.

16.28.3.6 sc_rm_partition_lock()

```
sc_err_t sc_rm_partition_lock (
             sc_ipc_t ipc,
             sc_rm_pt_t pt )
```

This function locks a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to lock

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if *pt* out of range,
- SC_ERR_NOACCESS if caller's partition is not the parent of *pt*

If a partition is locked it cannot be freed, have resources/pads assigned to/from it, memory regions created/assigned, DID changed, or parent changed.

16.28.3.7 sc_rm_get_partition()

```
sc_err_t sc_rm_get_partition (
             sc_ipc_t ipc,
             sc_rm_pt_t * pt )
```

This function gets the partition handle of the caller.

Parameters

in	*ipc*	IPC handle
out	*pt*	return handle for caller's partition

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.8 sc_rm_set_parent()

```
sc_err_t sc_rm_set_parent (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_rm_pt_t pt_parent )
```

This function sets a new parent for a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition for which parent is to be changed
in	*pt_parent*	handle of partition to set as parent

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the parent of *pt*,
- SC_ERR_LOCKED if either partition is locked

16.28.3.9 sc_rm_move_all()

```
sc_err_t sc_rm_move_all (
             sc_ipc_t ipc,
             sc_rm_pt_t pt_src,
             sc_rm_pt_t pt_dst,
             sc_bool_t move_rsrc,
             sc_bool_t move_pads )
```

This function moves all movable resources/pads owned by a source partition to a destination partition.

It can be used to more quickly set up a new partition if a majority of the caller's resources are to be moved to a new partition.

Parameters

in	*ipc*	IPC handle
in	*pt_src*	handle of partition from which resources should be moved from
in	*pt_dst*	handle of partition to which resources should be moved to
in	*move_rsrc*	boolean to indicate if resources should be moved
in	*move_pads*	boolean to indicate if pads should be moved

Returns

Returns an error code (SC_ERR_NONE = success).

By default, all resources are movable. This can be changed using the sc_rm_set_resource_movable() function. Note all masters defaulted to SMMU bypass.

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not *pt_src* or the parent of *pt_src*,
- SC_ERR_LOCKED if either partition is locked

16.28.3.10 sc_rm_assign_resource()

```
sc_err_t sc_rm_assign_resource (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_rsrc_t resource )
```

This function assigns ownership of a resource to a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to which resource should be assigned
in	*resource*	resource to assign

This function assigned a resource to a partition. This partition is then the owner. All resources always have an owner (one owner). The owner has various rights to make API calls affecting the resource. Ownership does not imply access to the peripheral itself (that is based on access rights).

Returns

Returns an error code (SC_ERR_NONE = success).

This action resets the resource's master and peripheral attributes. Privilege attribute will be PASSTHRU, security attribute will be ASSERT if the partition is secure and NEGATE if it is not, and masters will defaulted to SMMU bypass. Access permissions will reset to SEC_RW for the owning partition only for secure partitions, FULL for non-secure. Default is no access by other partitions.

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_LOCKED if the owning partition or *pt* is locked

16.28.3.11 sc_rm_set_resource_movable()

```
sc_err_t sc_rm_set_resource_movable (
             sc_ipc_t ipc,
             sc_rsrc_t resource_fst,
             sc_rsrc_t resource_lst,
             sc_bool_t movable )
```

This function flags resources as movable or not.

Parameters

in	*ipc*	IPC handle
in	*resource_fst*	first resource for which flag should be set
in	*resource_lst*	last resource for which flag should be set
in	*movable*	movable flag (SC_TRUE is movable)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if resources are out of range,
- SC_ERR_NOACCESS if caller's partition is not a parent of a resource owner,
- SC_ERR_LOCKED if the owning partition is locked

This function is used to determine the set of resources that will be moved using the sc_rm_move_all() function. All resources are movable by default so this function is normally used to prevent a set of resources from moving.

16.28.3.12 sc_rm_set_subsys_rsrc_movable()

```
sc_err_t sc_rm_set_subsys_rsrc_movable (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_bool_t movable )
```

This function flags all of a subsystem's resources as movable or not.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to use to identify subsystem
in	*movable*	movable flag (SC_TRUE is movable)

A subsystem is a physical grouping within the chip of related resources; this is SoC specific. This function is used to optimize moving resource for these groupings, for instance, an M4 core and its associated resources. The list of subsystems and associated resources can be found in the SoC-specific API document Resources chapter.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if a function argument is out of range

Note *resource* is used to find the associated subsystem. Only resources owned by the caller are set.

16.28.3.13 sc_rm_set_master_attributes()

```
sc_err_t sc_rm_set_master_attributes (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_rm_spa_t sa,
             sc_rm_spa_t pa,
             sc_bool_t smmu_bypass )
```

This function sets attributes for a resource which is a bus master (i.e.

capable of DMA).

Parameters

in	*ipc*	IPC handle
in	*resource*	master resource for which attributes should apply
in	*sa*	security attribute
in	*pa*	privilege attribute
in	*smmu_bypass*	SMMU bypass mode

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not a parent of the resource owner,
- SC_ERR_LOCKED if the owning partition is locked

Masters are IP blocks that generate bus transactions. This function configures how the isolation HW will define these bus transactions from the specified master. Note the security attribute will only be changed if the caller's partition is secure.

Note an IP block can be both a master and peripheral (have both a programming model and generate bus transactions).

16.28.3.14 sc_rm_set_master_sid()

```
sc_err_t sc_rm_set_master_sid (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_rm_sid_t sid )
```

This function sets the StreamID for a resource which is a bus master (i.e.

capable of DMA).

Parameters

in	*ipc*	IPC handle
in	*resource*	master resource for which attributes should apply
in	*sid*	StreamID

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_LOCKED if the owning partition is locked

This function configures the SID attribute associated with all bus transactions from this master. Note 0 is not a valid SID as it is reserved to indicate bypass.

16.28.3.15 sc_rm_set_peripheral_permissions()

```
sc_err_t sc_rm_set_peripheral_permissions (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_rm_pt_t pt,
            sc_rm_perm_t perm )
```

This function sets access permissions for a peripheral resource.

Parameters

in	*ipc*	IPC handle
in	*resource*	peripheral resource for which permissions should apply
in	*pt*	handle of partition *perm* should by applied for
in	*perm*	permissions to apply to *resource* for *pt*

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_LOCKED if the owning partition is locked
- SC_ERR_LOCKED if the *pt* is confidential and the caller isn't *pt*

Peripherals are IP blocks that have a programming model that can be accessed.

This function configures how the isolation HW will restrict access to a peripheral based on the attributes of a transaction from bus master. It also allows the access permissions of SC_R_SYSTEM to be set.

Note an IP block can be both a master and peripheral (have both a programming model and generate bus transactions).

16.28.3.16 sc_rm_is_resource_owned()

```
sc_bool_t sc_rm_is_resource_owned (
            sc_ipc_t ipc,
            sc_rsrc_t resource )
```

This function gets ownership status of a resource.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to check

Returns

Returns a boolean (SC_TRUE if caller's partition owns the resource).

If *resource* is out of range then SC_FALSE is returned.

16.28.3.17 sc_rm_get_resource_owner()

```
sc_err_t sc_rm_get_resource_owner (
             sc_ipc_t ipc,
             sc_rsrc_t resource,
             sc_rm_pt_t * pt )
```

This function is used to get the owner of a resource.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to check
out	*pt*	pointer to return owning partition

Returns

Returns a boolean (SC_TRUE if the resource is a bus master).

Return errors:

- SC_PARM if arguments out of range or invalid

If *resource* is out of range then SC_ERR_PARM is returned.

16.28.3.18 sc_rm_is_resource_master()

```
sc_bool_t sc_rm_is_resource_master (
             sc_ipc_t ipc,
             sc_rsrc_t resource )
```

This function is used to test if a resource is a bus master.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to check

Masters are IP blocks that generate bus transactions. Note an IP block can be both a master and peripheral (have both a programming model and generate bus transactions).

Returns

Returns a boolean (SC_TRUE if the resource is a bus master).

If *resource* is out of range then SC_FALSE is returned.

16.28.3.19 sc_rm_is_resource_peripheral()

```
sc_bool_t sc_rm_is_resource_peripheral (
            sc_ipc_t ipc,
            sc_rsrc_t resource )
```

This function is used to test if a resource is a peripheral.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to check

Peripherals are IP blocks that have a programming model that can be accessed. Note an IP block can be both a master and peripheral (have both a programming model and generate bus transactions)

Returns

Returns a boolean (SC_TRUE if the resource is a peripheral).

If *resource* is out of range then SC_FALSE is returned.

16.28.3.20 sc_rm_get_resource_info()

```
sc_err_t sc_rm_get_resource_info (
            sc_ipc_t ipc,
            sc_rsrc_t resource,
            sc_rm_sid_t * sid )
```

This function is used to obtain info about a resource.

Parameters

in	*ipc*	IPC handle
in	*resource*	resource to inquire about
out	*sid*	pointer to return StreamID

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if *resource* is out of range

16.28.3.21 sc_rm_memreg_alloc()

```
sc_err_t sc_rm_memreg_alloc (
             sc_ipc_t ipc,
             sc_rm_mr_t * mr,
             sc_faddr_t addr_start,
             sc_faddr_t addr_end )
```

This function requests that the SC create a new memory region.

Parameters

in	*ipc*	IPC handle
out	*mr*	return handle for region; used for subsequent function calls associated with this region
in	*addr_start*	start address of region (physical)
in	*addr_end*	end address of region (physical)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if the new memory region is misaligned,
- SC_ERR_LOCKED if caller's partition is locked,
- SC_ERR_PARM if the new memory region spans multiple existing regions,
- SC_ERR_NOACCESS if caller's partition does not own the memory containing the new region,
- SC_ERR_UNAVAILABLE if memory region table is full (no more allocation space)

This function will create a new memory region. The area covered by the new region must already exist in a memory region owned by the caller. The result will be two memory regions, the new one overlapping the existing one. The new region has higher priority. See the XRDC2 MRC documentation for how it resolves access permissions in this case. By default, permissions will mirror the parent region.

16.28.3.22 sc_rm_memreg_split()

```
sc_err_t sc_rm_memreg_split (
             sc_ipc_t ipc,
             sc_rm_mr_t mr,
             sc_rm_mr_t * mr_ret,
             sc_faddr_t addr_start,
             sc_faddr_t addr_end )
```

This function requests that the SC split an existing memory region.

Parameters

in	*ipc*	IPC handle
in	*mr*	handle of memory region to split
out	*mr_ret*	return handle for new region; used for subsequent function calls associated with this region
in	*addr_start*	start address of region (physical)
in	*addr_end*	end address of region (physical)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if the new memory region is not start/end part of mr,
- SC_ERR_LOCKED if caller's partition is locked,
- SC_ERR_PARM if the new memory region spans multiple existing regions,
- SC_ERR_NOACCESS if caller's partition does not own the memory containing the new region,
- SC_ERR_BUSY if the region is coincident with another region,
- SC_ERR_UNAVAILABLE if memory region table is full (no more allocation space)

This function will take an existing region and split it into two, non-overlapping regions. Note the new region must start or end on the split region. Permissions will mirror the parent region.

16.28.3.23 sc_rm_memreg_frag()

```
sc_err_t sc_rm_memreg_frag (
             sc_ipc_t ipc,
             sc_rm_mr_t * mr_ret,
             sc_faddr_t addr_start,
             sc_faddr_t addr_end )
```

This function requests that the SC fragment a memory region.

Parameters

in	*ipc*	IPC handle
out	*mr_ret*	return handle for new region; used for subsequent function calls associated with this region
in	*addr_start*	start address of region (physical)
in	*addr_end*	end address of region (physical)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_LOCKED if caller's partition is locked,
- SC_ERR_PARM if the new memory region spans multiple existing regions,
- SC_ERR_NOACCESS if caller's partition does not own the memory containing the new region,
- SC_ERR_BUSY if the region is coincident with another region,
- SC_ERR_UNAVAILABLE if memory region table is full (no more allocation space)

This function finds the memory region containing the address range. It then splits it as required and returns the extracted region. The result is 2-3 non-overlapping regions, depending on how the new region aligns with existing regions. Permissions will mirror the parent region.

16.28.3.24 sc_rm_memreg_free()

```
sc_err_t sc_rm_memreg_free (
             sc_ipc_t ipc,
             sc_rm_mr_t mr )
```

This function frees a memory region.

Parameters

in	*ipc*	IPC handle
in	*mr*	handle of memory region to free

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if *mr* out of range or invalid,

- SC_ERR_NOACCESS if caller's partition is not a parent of *mr*,
- SC_ERR_LOCKED if the owning partition of *mr* is locked

16.28.3.25 sc_rm_find_memreg()

```
sc_err_t sc_rm_find_memreg (
             sc_ipc_t ipc,
             sc_rm_mr_t * mr,
             sc_faddr_t addr_start,
             sc_faddr_t addr_end )
```

Internal SC function to find a memory region.

See also

sc_rm_find_memreg().

This function finds a memory region.

Parameters

in	*ipc*	IPC handle
out	*mr*	return handle for region; used for subsequent function calls associated with this region
in	*addr_start*	start address of region to search for
in	*addr_end*	end address of region to search for

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOTFOUND if region not found,

Searches only for regions owned by the caller. Finds first region containing the range specified.

16.28.3.26 sc_rm_assign_memreg()

```
sc_err_t sc_rm_assign_memreg (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_rm_mr_t mr )
```

This function assigns ownership of a memory region.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to which memory region should be assigned
in	*mr*	handle of memory region to assign

Returns

Returns an error code (SC_ERR_NONE = success).

This function assigns a memory region to a partition. This partition is then the owner. All regions always have an owner (one owner). The owner has various rights to make API calls affecting the region. Ownership does not imply access to the memory itself (that is based on access rights).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the *mr* owner or parent of the owner,
- SC_ERR_LOCKED if the owning partition or *pt* is locked

16.28.3.27 sc_rm_set_memreg_permissions()

```
sc_err_t sc_rm_set_memreg_permissions (
             sc_ipc_t ipc,
             sc_rm_mr_t mr,
             sc_rm_pt_t pt,
             sc_rm_perm_t perm )
```

This function sets access permissions for a memory region.

Parameters

in	*ipc*	IPC handle
in	*mr*	handle of memory region for which permissions should apply
in	*pt*	handle of partition *perm* should by applied for
in	*perm*	permissions to apply to *mr* for *pt*

This operates on the memory region specified. If SC_RM_PT_ALL is specified then it operates on all the regions owned by the caller that exist at the time of the call.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the region owner or parent of the owner,
- SC_ERR_LOCKED if the owning partition is locked
- SC_ERR_LOCKED if the *pt* is confidential and the caller isn't *pt*

This function configures how the HW isolation will restrict access to a memory region based on the attributes of a transaction from bus master.

16.28.3.28 sc_rm_set_memreg_iee()

```
sc_err_t sc_rm_set_memreg_iee (
             sc_ipc_t ipc,
             sc_rm_mr_t mr,
             sc_rm_det_t det,
             sc_rm_rmsg_t rmsg )
```

This function configures the IEE parameters for a memory region.

Parameters

in	*ipc*	IPC handle
in	*mr*	handle of memory region to check
in	*det*	0 = normal, 1 = encrypted
in	*rmsg*	IEE region (0-7)

Caller must own SC_R_IEE_Rn where n is rmsg.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if arguments out of range or invalid,
- SC_ERR_LOCKED if the owning partition is locked
- SC_ERR_NOACCESS if caller's partition is not the region owner or parent of the owner
- SC_ERR_UNAVAILABLE if caller's partition is not the IEE region resource owner

16.28.3.29 sc_rm_is_memreg_owned()

```
sc_bool_t sc_rm_is_memreg_owned (
            sc_ipc_t ipc,
            sc_rm_mr_t mr )
```

This function gets ownership status of a memory region.

Parameters

in	*ipc*	IPC handle
in	*mr*	handle of memory region to check

Returns

Returns a boolean (SC_TRUE if caller's partition owns the memory region).

If *mr* is out of range then SC_FALSE is returned.

16.28.3.30 sc_rm_get_memreg_info()

```
sc_err_t sc_rm_get_memreg_info (
            sc_ipc_t ipc,
            sc_rm_mr_t mr,
            sc_faddr_t * addr_start,
            sc_faddr_t * addr_end )
```

This function is used to obtain info about a memory region.

Parameters

in	*ipc*	IPC handle
in	*mr*	handle of memory region to inquire about
out	*addr_start*	pointer to return start address
out	*addr_end*	pointer to return end address

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if *mr* is out of range

16.28.3.31 sc_rm_assign_pad()

```
sc_err_t sc_rm_assign_pad (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_pad_t pad )
```

This function assigns ownership of a pad to a partition.

Parameters

in	*ipc*	IPC handle
in	*pt*	handle of partition to which pad should be assigned
in	*pad*	pad to assign

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is restricted,
- SC_PARM if arguments out of range or invalid,
- SC_ERR_NOACCESS if caller's partition is not the pad owner or parent of the owner,
- SC_ERR_LOCKED if the owning partition or *pt* is locked

16.28.3.32 sc_rm_set_pad_movable()

```
sc_err_t sc_rm_set_pad_movable (
             sc_ipc_t ipc,
             sc_pad_t pad_fst,
             sc_pad_t pad_lst,
             sc_bool_t movable )
```

This function flags pads as movable or not.

Parameters

in	*ipc*	IPC handle
in	*pad_fst*	first pad for which flag should be set
in	*pad_lst*	last pad for which flag should be set
in	*movable*	movable flag (SC_TRUE is movable)

This function assigned a pad to a partition. This partition is then the owner. All pads always have an owner (one owner). The owner has various rights to make API calls affecting the pad.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if pads are out of range,
- SC_ERR_NOACCESS if caller's partition is not a parent of a pad owner,
- SC_ERR_LOCKED if the owning partition is locked

This function is used to determine the set of pads that will be moved using the sc_rm_move_all() function. All pads are movable by default so this function is normally used to prevent a set of pads from moving.

16.28.3.33 sc_rm_is_pad_owned()

```
sc_bool_t sc_rm_is_pad_owned (
            sc_ipc_t ipc,
            sc_pad_t pad )
```

This function gets ownership status of a pad.

Parameters

in	*ipc*	IPC handle
in	*pad*	pad to check

Returns

Returns a boolean (SC_TRUE if caller's partition owns the pad).

If *pad* is out of range then SC_FALSE is returned.

16.28.3.34 sc_rm_dump()

```
void sc_rm_dump (
            sc_ipc_t ipc )
```

This function dumps the RM state for debug.

Parameters

in	*ipc*	IPC handle

16.28.3.35 rm_init()

```
void rm_init (
            sc_bool_t api_phase )
```

Internal SC function to initialize the RM service.

Parameters

in	*api_phase*	init phase

Initializes the API if /a api_phase = SC_TRUE, otherwise initializes the HW managed by the RM service. API must be initialized before anything else is done with the service.

16.28.3.36 rm_reserve_static_pt()

```
sc_err_t rm_reserve_static_pt (
            sc_rm_pt_t num )
```

Internal SC function to specify the number of static partitions.

Parameters

in	*num*	number of static partitions

Returns

Returns an error code (SC_ERR_NONE = success).

Static partitions will be skipped when a new partition is allocated. The minimum possible is 0 and the max possible is SC_RM_NUM_PARTITION.

16.28.3.37 rm_reserve_static_did()

```
sc_err_t rm_reserve_static_did (
            sc_rm_did_t num )
```

Internal SC function to specify the number of static domains.

Parameters

in	*num*	number of static domains

Returns

Returns an error code (SC_ERR_NONE = success).

Static domains will be skipped when a new partition is allocated. The minimum possible is 0 and the max possible is SC_RM_NUM_DOMAIN.

16.28.3.38 rm_partition_alloc()

```
sc_err_t rm_partition_alloc (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t * pt,
             sc_bool_t secure,
             sc_bool_t isolated,
             sc_bool_t restricted,
             sc_bool_t grant,
             sc_bool_t coherent )
```

Internal SC function to request that the SC create a new resource partition.

See also

sc_rm_partition_alloc().

Examples

board.c.

16.28.3.39 rm_set_confidential()

```
sc_err_t rm_set_confidential (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_bool_t retro )
```

Internal SC function to make a partition confidential.

See also

sc_rm_set_confidential().

16.28.3.40 rm_partition_free()

```
sc_err_t rm_partition_free (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt )
```

Internal SC function to free a partition and assigns all resources to the caller.

See also

sc_rm_partition_free().

16.28.3.41 rm_get_partition()

```
sc_err_t rm_get_partition (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t * pt )
```

Internal SC function to get the partition handle of the caller.

See also

sc_rm_get_partition().

16.28.3.42 rm_is_partition_used()

```
sc_bool_t rm_is_partition_used (
             sc_rm_pt_t pt )
```

Internal SC function to determine if a partition is enabled (used) or not.

Parameters

in	*pt*	partition to check

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.43 rm_is_secure_partition()

```
sc_bool_t rm_is_secure_partition (
             sc_rm_pt_t caller_pt )
```

Internal SC function to get the security state of partition.

Returns

Returns SC_TRUE if *caller's* partition is secure.

16.28.3.44 rm_is_partition_isolated()

```
sc_bool_t rm_is_partition_isolated (
            sc_rm_pt_t pt )
```

Internal SC function to get the isolation state of partition.

Returns

Returns SC_TRUE if *caller's* partition is isolated.

16.28.3.45 rm_is_sys_access()

```
sc_bool_t rm_is_sys_access (
            sc_rm_pt_t pt )
```

Internal SC function to return if the partition has system access.

Parameters

in	*pt*	partition to check

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.46 rm_get_partition_parent()

```
sc_rm_pt_t rm_get_partition_parent (
            sc_rm_pt_t pt )
```

Internal SC function to return the parent of a partition.

Parameters

in	*pt*	partition to check

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.47 rm_get_did()

```
sc_rm_did_t rm_get_did (
            sc_rm_pt_t caller_pt )
```

Internal SC function to get the DID of the caller's partition.

See also

sc_rm_get_did().

16.28.3.48 rm_partition_static()

```
sc_err_t rm_partition_static (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt,
            sc_rm_did_t did )
```

Internal SC function to force a partition to use a specific static DID.

See also

sc_rm_partition_static().

16.28.3.49 rm_partition_lock()

```
sc_err_t rm_partition_lock (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt )
```

Internal SC function to lock a partition.

See also

sc_rm_partition_lock().

16.28.3.50 rm_set_parent()

```
sc_err_t rm_set_parent (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt,
            sc_rm_pt_t pt_parent )
```

Internal SC function to set a new parent for a partition.

See also

sc_rm_set_parent().

Examples

board.c.

16.28.3.51 rm_is_parent()

```
sc_bool_t rm_is_parent (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt )
```

Internal SC function to check if caller is the parent of a partition.

Parameters

in	*caller_pt*	handle of caller partition
in	*pt*	handle of partition to check

Returns SC_TRUE of the caller is the parent of another partition. Used to check access permissions on functions that affect a partition.

16.28.3.52 rm_check_ancestor()

```
sc_bool_t rm_check_ancestor (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt_owner )
```

Internal SC function to check if caller is an ancestor of owner.

Parameters

in	*caller_pt*	handle of caller partition
in	*pt_owner*	handle of owner partition

Returns SC_TRUE of the caller is the owner or is an ancestor of the owner. Used to check access permissions on functions that affect a partition.

16.28.3.53 rm_move_all()

```
sc_err_t rm_move_all (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt_src,
             sc_rm_pt_t pt_dst,
             sc_bool_t move_rsrc,
             sc_bool_t move_pads )
```

Internal SC function to move all resources/pads owned by a source partition to a destination partition.

See also

sc_rm_move_all().

Examples

board.c.

16.28.3.54 rm_assign_resource()

```
sc_err_t rm_assign_resource (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_rsrc_t resource )
```

Internal SC function to assign ownership of a resource to a partition.

See also

sc_rm_assign_resource().

Examples

board.c.

16.28.3.55 rm_set_resource_movable()

```
sc_err_t rm_set_resource_movable (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource_fst,
             sc_rsrc_t resource_lst,
             sc_bool_t movable )
```

Internal SC function to flag resource as movable or not.

See also

sc_rm_set_resource_movable().

Examples

board.c.

16.28.3.56 rm_set_subsys_rsrc_movable()

```
sc_err_t rm_set_subsys_rsrc_movable (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_bool_t movable )
```

Internal SC function to flag all of a subsystem's resources as movable or not.

See also

sc_rm_set_subsys_rsrc_movable().

Examples

board.c.

16.28.3.57 rm_set_master_attributes()

```
sc_err_t rm_set_master_attributes (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_rm_spa_t sa,
             sc_rm_spa_t pa,
             sc_bool_t smmu_bypass )
```

Internal SC function to set attributes for a resource which is a bus master (i.e.

capable of DMA).

See also

sc_rm_set_master_attributes().

16.28.3.58 rm_set_master_sid()

```
sc_err_t rm_set_master_sid (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_rm_sid_t sid )
```

Internal SC function to set the StreamID for a resource which is a bus master (i.e.

capable of DMA).

See also

sc_rm_set_master_sid().

16.28.3.59 rm_update_master()

```
sc_err_t rm_update_master (
             sc_rm_idx_t idx )
```

Internal SC function to update a master resource.

It takes a resource index as an argument.

Parameters

in	*idx*	unified resource index

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.60 rm_set_peripheral_permissions()

```
sc_err_t rm_set_peripheral_permissions (
             sc_rm_pt_t caller_pt,
             sc_rsrc_t resource,
             sc_rm_pt_t pt,
             sc_rm_perm_t perm )
```

Internal SC function to set access permissions for a peripheral resource.

See also

sc_rm_set_peripheral_permissions().

Examples

board.c.

16.28.3.61 rm_update_peripheral()

```
sc_err_t rm_update_peripheral (
             sc_rm_idx_t idx )
```

Internal SC function to update a peripheral resource.

It takes a resource index as an argument.

Parameters

in	*idx*	unified resource index

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.62 rm_update_resource()

```
void rm_update_resource (
             sc_rsrc_t resource )
```

Internal SC function to update a resource in HW.

Parameters

in	*resource*	resource to update

16.28.3.63 rm_get_ridx_ss_info()

```
void rm_get_ridx_ss_info (
             sc_rm_idx_t idx,
```

```
            sc_sub_t * ss,
            sc_ss_idx_t * ss_idx )
```

Internal SC function to return subsystem specific info about a resource.

It takes a resource index as an argument.

Parameters

in	*idx*	unified resource index
out	*ss*	subsystem
out	*ss_idx*	subsystem relative resource index

16.28.3.64 rm_check_map_ridx()

```
sc_bool_t rm_check_map_ridx (
            sc_rsrc_t resource,
            sc_rm_idx_t * idx )
```

Internal SC function to check the validity of a resource and return the unified resource index.

Parameters

in	*resource*	resource to check
out	*idx*	unified resource index

Returns

Returns SC_TRUE if *resource* is valid.

The index can be used to index into any resource array of size SC_NUM_RSRCS. It is also used for most private RM functions.

16.28.3.65 rm_check_map_ridx_v()

```
void rm_check_map_ridx_v (
            sc_rsrc_t resource,
            sc_rm_idx_t * idx )
```

Internal SC function to check the validity of a resource and return the unified resource index.

Parameters

in	*resource*	resource to check
out	*idx*	unified resource index

The index can be used to index into any resource array of size SC_NUM_RSRCS. It is also used for most private RM functions.

16.28.3.66 rm_is_resource_owned()

```
sc_bool_t rm_is_resource_owned (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource )
```

Internal SC function to get ownership status of a resource.

See also

sc_rm_is_resource_owned().

16.28.3.67 rm_is_ridx_owned()

```
sc_bool_t rm_is_ridx_owned (
            sc_rm_pt_t caller_pt,
            sc_rm_idx_t idx )
```

Internal SC function to check if a resource is owned by the caller.

It takes a resource index as an argument.

Parameters

in	*caller_pt*	handle of caller partition
in	*idx*	unified resource index

Returns

Returns SC_TRUE if *idx* is owned.

16.28.3.68 rm_is_resource_avail()

```
sc_bool_t rm_is_resource_avail (
            sc_rsrc_t resource )
```

Internal SC function to check if a resource is available.

It takes a resource as an argument. Resource availability is based in hardware, fuses, and board. Not based on partition ownership.

Parameters

in	*resource*	resource to check

Returns

Returns SC_TRUE if *resource* is available.

Examples

board.c.

16.28.3.69 rm_is_ridx_avail()

```
sc_bool_t rm_is_ridx_avail (
            sc_rm_idx_t idx )
```

Internal SC function to check if a resource is available.

It takes a resource index as an argument. Resource availability is based in hardware, fuses, and board. Not based on partition ownership.

Parameters

in	*idx*	unified resource index

Returns

Returns SC_TRUE if *idx* is available.

16.28.3.70 rm_is_resource_access_allowed()

```
sc_bool_t rm_is_resource_access_allowed (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource )
```

Internal SC function to get access rights of a resource.

Parameters

in	*caller_pt*	handle of caller partition
in	*resource*	resource to check

Returns

Returns SC_TRUE if *resource* is accessible.

16.28.3.71 rm_is_ridx_access_allowed()

```
sc_bool_t rm_is_ridx_access_allowed (
            sc_rm_pt_t caller_pt,
            sc_rm_idx_t idx )
```

Internal SC function to check if a resource is controllable by the caller.

It takes a resource index as an argument.

Parameters

in	*caller_pt*	handle of caller partition
in	*idx*	unified resource index

Returns

Returns SC_TRUE if *idx* access is allowed.

16.28.3.72 rm_get_resource_owner()

```
sc_err_t rm_get_resource_owner (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_rm_pt_t * pt )
```

Internal SC function to return the owner partition for a resource.

See also

sc_rm_get_resource_owner().

16.28.3.73 rm_get_ridx_owner()

```
void rm_get_ridx_owner (
            sc_rm_idx_t idx,
            sc_rm_pt_t * pt )
```

Internal SC function to return the owning partition for a resource.

It takes a resource index as an argument.

Parameters

in	*idx*	unified resource index
out	*pt*	return handle for partition

16.28.3.74 rm_is_resource_master()

```
sc_bool_t rm_is_resource_master (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource )
```

Internal SC function used to test if a resource is a bus master.

See also

sc_rm_is_resource_master().

16.28.3.75 rm_is_ridx_master()

```
sc_bool_t rm_is_ridx_master (
            sc_rm_idx_t idx )
```

Internal SC function to check if a resource is a master.

It takes a resource index as an argument.

Parameters

in	*idx*	unified resource index

Returns

Returns SC_TRUE if *idx* is a master.

16.28.3.76 rm_is_resource_peripheral()

```
sc_bool_t rm_is_resource_peripheral (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource )
```

Internal SC function used to test if a resource is a peripheral.

See also

sc_rm_is_resource_peripheral().

16.28.3.77 rm_is_ridx_peripheral()

```
sc_bool_t rm_is_ridx_peripheral (
            sc_rm_idx_t idx )
```

Internal SC function to check if a resource is a peripheral.

It takes a resource index as an argument.

Parameters

in	*idx*	unified resource index

Returns

Returns SC_TRUE if *idx* is a peripheral.

16.28.3.78 rm_get_resource_info()

```
sc_err_t rm_get_resource_info (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t resource,
            sc_rm_sid_t * sid )
```

Internal SC function used to obtain info about a resource.

See also

sc_rm_get_resource_info().

16.28.3.79 rm_ridx_block()

```
sc_bool_t rm_ridx_block (
            sc_rm_idx_t idx,
            sc_bool_t block )
```

Internal SC function to control if a access to a resource should be blocked via HW.

Parameters

in	*idx*	unified resource index
in	*block*	block state (SC_TRUE to block)

Returns

Returns current block state.

16.28.3.80 rm_memreg_alloc()

```
sc_err_t rm_memreg_alloc (
             sc_rm_pt_t caller_pt,
             sc_rm_mr_t * mr,
             sc_faddr_t addr_start,
             sc_faddr_t addr_end )
```

Internal SC function to request that the SC create a new memory region.

See also

sc_rm_memreg_alloc().

16.28.3.81 rm_memreg_split()

```
sc_err_t rm_memreg_split (
             sc_rm_pt_t caller_pt,
             sc_rm_mr_t mr,
             sc_rm_mr_t * mr_ret,
             sc_faddr_t addr_start,
             sc_faddr_t addr_end )
```

Internal SC function to split a memory region.

See also

sc_rm_memreg_split().

16.28.3.82 rm_memreg_frag()

```
sc_err_t rm_memreg_frag (
            sc_rm_pt_t caller_pt,
            sc_rm_mr_t * mr_ret,
            sc_faddr_t addr_start,
            sc_faddr_t addr_end )
```

Internal SC function to fragment a memory region.

See also

sc_rm_memreg_frag().

Examples

board.c.

16.28.3.83 rm_memreg_free()

```
sc_err_t rm_memreg_free (
            sc_rm_pt_t caller_pt,
            sc_rm_mr_t mr )
```

Internal SC function to free a memory region.

See also

sc_rm_memreg_free().

Examples

board.c.

16.28.3.84 rm_find_memreg()

```
sc_err_t rm_find_memreg (
            sc_rm_pt_t caller_pt,
            sc_rm_mr_t * mr,
            sc_faddr_t addr_start,
            sc_faddr_t addr_end )
```

Internal SC function to find a memory region.

See also

sc_rm_find_memreg().

Examples

board.c.

16.28.3.85 rm_assign_memreg()

```
sc_err_t rm_assign_memreg (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_rm_mr_t mr )
```

Internal SC function to assign ownership of a memory region.

See also

sc_rm_assign_memreg().

Examples

board.c.

16.28.3.86 rm_set_memreg_permissions()

```
sc_err_t rm_set_memreg_permissions (
             sc_rm_pt_t caller_pt,
             sc_rm_mr_t mr,
             sc_rm_pt_t pt,
             sc_rm_perm_t perm )
```

Internal SC function to set access permissions for a memory region.

See also

sc_rm_set_memreg_permissions().

Examples

board.c.

16.28.3.87 rm_set_memreg_iee()

```
sc_err_t rm_set_memreg_iee (
             sc_rm_pt_t caller_pt,
             sc_rm_mr_t mr,
             sc_rm_det_t det,
             sc_rm_rmsg_t rmsg )
```

Internal SC function to set configure IEE parameters for a mem region.

See also

sc_rm_set_memreg_iee().

16.28.3.88 rm_is_memreg_owned()

```
sc_bool_t rm_is_memreg_owned (
            sc_rm_pt_t caller_pt,
            sc_rm_mr_t mr )
```

Internal SC function to get ownership status of a memory region.

See also

sc_rm_is_memreg_owned().

16.28.3.89 rm_get_memreg_info()

```
sc_err_t rm_get_memreg_info (
            sc_rm_pt_t caller_pt,
            sc_rm_mr_t mr,
            sc_faddr_t * addr_start,
            sc_faddr_t * addr_end )
```

Internal SC function used to obtain info about a memory region.

See also

sc_rm_get_memreg_info().

16.28.3.90 rm_assign_pad()

```
sc_err_t rm_assign_pad (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt,
            sc_pad_t pad )
```

Internal SC function to assign ownership of a pad to a partition.

See also

sc_rm_assign_pad().

16.28.3.91 rm_set_pad_movable()

```
sc_err_t rm_set_pad_movable (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad_first,
             sc_pad_t pad_last,
             sc_bool_t movable )
```

Internal SC function to flag pad as movable or not.

See also

sc_rm_set_pad_movable().

Examples

board.c.

16.28.3.92 rm_is_pad_owned()

```
sc_bool_t rm_is_pad_owned (
             sc_rm_pt_t caller_pt,
             sc_pad_t pad )
```

Internal SC function to get ownership status of a pad.

See also

sc_rm_is_pad_owned().

16.28.3.93 rm_get_pad_owner()

```
sc_err_t rm_get_pad_owner (
             sc_pad_t pad,
             sc_rm_pt_t * pt )
```

Internal SC function to get the owner of a pad.

Parameters

in	*pad*	pad to get
out	*pt*	pointer to return partition

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.94 rm_init_subsys()

```
sc_err_t rm_init_subsys (
             sc_sub_t ss,
             sc_bool_t block_enb )
```

Internal SC function to reload a subsystem's XRDC info after a power on.

Parameters

in	*ss*	subsystem
in	*block_enb*	flag to skip SCU, skip mem

Returns

Returns an error code (SC_ERR_NONE = success).

16.28.3.95 rm_dump()

```
void rm_dump (
             sc_rm_pt_t caller_pt )
```

Internal SC function to dump RM state for debug.

See also

sc_rm_set_pad_movable().

Examples

board.c.

16.28.3.96 rm_dump_partition()

```
void rm_dump_partition (
             sc_rm_pt_t pt )
```

Internal SC function to dump the internal partition state of the RM service.

Parameters

in	*pt*	partition to dump

16.28.3.97 rm_dump_resources()

```
void rm_dump_resources (
             sc_rm_pt_t pt )
```

Internal SC function to dump the internal resource state of the RM service.

Parameters

in	*pt*	partition to dump

16.28.3.98 rm_dump_memregs()

```
void rm_dump_memregs (
             sc_rm_pt_t pt )
```

Internal SC function to dump the internal memory state of the RM service.

Parameters

in	*pt*	partition to dump

16.28.3.99 rm_dump_pads()

```
void rm_dump_pads (
             sc_rm_pt_t pt )
```

Internal SC function to dump the internal pad state of the RM service.

Parameters

in	*pt*	partition to dump

16.29 TIMER: Timer Service

Module for the Timer service.

Typedefs

- typedef uint8_t sc_timer_wdog_action_t

  This type is used to configure the watchdog action.
- typedef uint32_t sc_timer_wdog_time_t

  This type is used to declare a watchdog time value in milliseconds.

Defines for type widths

- #define SC_TIMER_ACTION_W 3U

  Width of sc_timer_wdog_action_t.

Defines for sc_timer_wdog_action_t

- #define SC_TIMER_WDOG_ACTION_PARTITION 0U

  Reset partition.
- #define SC_TIMER_WDOG_ACTION_WARM 1U

  Warm reset system.
- #define SC_TIMER_WDOG_ACTION_COLD 2U

  Cold reset system.
- #define SC_TIMER_WDOG_ACTION_BOARD 3U

  Reset board.
- #define SC_TIMER_WDOG_ACTION_IRQ 4U

  Only generate IRQs.

Watchdog Functions

- sc_err_t sc_timer_set_wdog_timeout (sc_ipc_t ipc, sc_timer_wdog_time_t timeout)

  This function sets the watchdog timeout in milliseconds.
- sc_err_t sc_timer_set_wdog_pre_timeout (sc_ipc_t ipc, sc_timer_wdog_time_t pre_timeout)

  This function sets the watchdog pre-timeout in milliseconds.
- sc_err_t sc_timer_set_wdog_window (sc_ipc_t ipc, sc_timer_wdog_time_t window)

  This function sets the watchdog window in milliseconds.
- sc_err_t sc_timer_start_wdog (sc_ipc_t ipc, sc_bool_t lock)

  This function starts the watchdog.
- sc_err_t sc_timer_stop_wdog (sc_ipc_t ipc)

  This function stops the watchdog if it is not locked.
- sc_err_t sc_timer_ping_wdog (sc_ipc_t ipc)

  This function pings (services, kicks) the watchdog resetting the time before expiration back to the timeout.
- sc_err_t sc_timer_get_wdog_status (sc_ipc_t ipc, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *max_timeout, sc_timer_wdog_time_t *remaining_time)

  This function gets the status of the watchdog.
- sc_err_t sc_timer_pt_get_wdog_status (sc_ipc_t ipc, sc_rm_pt_t pt, sc_bool_t *enb, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *remaining_time)

  This function gets the status of the watchdog of a partition.
- sc_err_t sc_timer_set_wdog_action (sc_ipc_t ipc, sc_rm_pt_t pt, sc_timer_wdog_action_t action)

  This function configures the action to be taken when a watchdog expires.

Real-Time Clock (RTC) Functions

- sc_err_t sc_timer_set_rtc_time (sc_ipc_t ipc, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)

  This function sets the RTC time.
- sc_err_t sc_timer_get_rtc_time (sc_ipc_t ipc, uint16_t *year, uint8_t *mon, uint8_t *day, uint8_t *hour, uint8_t *min, uint8_t *sec)

  This function gets the RTC time.
- sc_err_t sc_timer_get_rtc_sec1970 (sc_ipc_t ipc, uint32_t *sec)

  This function gets the RTC time in seconds since 1/1/1970.
- sc_err_t sc_timer_set_rtc_alarm (sc_ipc_t ipc, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)

  This function sets the RTC alarm.
- sc_err_t sc_timer_set_rtc_periodic_alarm (sc_ipc_t ipc, uint32_t sec)

  This function sets the RTC alarm (periodic mode).
- sc_err_t sc_timer_cancel_rtc_alarm (sc_ipc_t ipc)

  This function cancels the RTC alarm.
- sc_err_t sc_timer_set_rtc_calb (sc_ipc_t ipc, int8_t count)

  This function sets the RTC calibration value.

System Counter (SYSCTR) Functions

- sc_err_t sc_timer_set_sysctr_alarm (sc_ipc_t ipc, uint64_t ticks)

  This function sets the SYSCTR alarm.
- sc_err_t sc_timer_set_sysctr_periodic_alarm (sc_ipc_t ipc, uint64_t ticks)

  This function sets the SYSCTR alarm (periodic mode).
- sc_err_t sc_timer_cancel_sysctr_alarm (sc_ipc_t ipc)

  This function cancels the SYSCTR alarm.

Internal Functions

- void timer_init (sc_bool_t api_phase)

  Internal SC function to initializes the TIMER service.
- void timer_init_part (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  This function initializes a new partition.
- sc_err_t timer_set_wdog_timeout (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t timeout)

  Internal SC function to set the watchdog timeout in milliseconds.
- sc_err_t timer_set_wdog_pre_timeout (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t pre_timeout)

  Internal SC function to set the watchdog pre-timeout in milliseconds.
- sc_err_t timer_set_wdog_window (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t window)

  Internal SC function to set the watchdog window in milliseconds.
- sc_err_t timer_start_wdog (sc_rm_pt_t caller_pt, sc_bool_t lock)

  Internal SC function to start the watchdog.
- sc_err_t timer_stop_wdog (sc_rm_pt_t caller_pt)

  Internal SC function to stop the watchdog (if not locked).
- void timer_halt_wdog (sc_rm_pt_t pt)

Internal SC function to stop halt the wdog when the partition is deleted.

- sc_err_t timer_ping_wdog (sc_rm_pt_t caller_pt)

  Internal SC function to ping (services, kicks) the watchdog resetting the time before expiration back to the timeout.

- sc_err_t timer_get_wdog_status (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *max_timeout, sc_timer_wdog_time_t *remaining_time)

  Internal SC function to get the status of the watchdog.

- sc_err_t timer_pt_get_wdog_status (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_bool_t *enb, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *remaining_time)

  Internal SC function to get the status of the watchdog of a partition.

- sc_err_t timer_set_wdog_action (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_timer_wdog_action_t action)

  Internal SC function to configure the action to be taken when a watchdog expires.

- sc_err_t timer_take_wdog_action (sc_rm_pt_t pt)

  Internal SC function to take the wdog action specified.

- sc_err_t timer_set_rtc_time (sc_rm_pt_t caller_pt, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)

  Internal SC function to set the RTC time.

- sc_err_t timer_get_rtc_time (sc_rm_pt_t caller_pt, uint16_t *year, uint8_t *mon, uint8_t *day, uint8_t *hour, uint8_t *min, uint8_t *sec)

  Internal SC function to get the RTC time.

- sc_err_t timer_set_rtc_alarm (sc_rm_pt_t caller_pt, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)

  Internal SC function to set the RTC alarm.

- sc_err_t timer_set_rtc_periodic_alarm (sc_rm_pt_t caller_pt, uint32_t sec)

  Internal SC function to set a periodic RTC alarm.

- sc_err_t timer_cancel_rtc_alarm (sc_rm_pt_t caller_pt)

  Internal SC function to cancel an RTC alarm.

- void timer_query_rtc_alarm (sc_rm_pt_t pt, uint32_t *alarm, uint32_t *period)

  Internal SC function to query an RTC alarm.

- void timer_restore_rtc_alarm (sc_rm_pt_t pt, uint32_t alarm, uint32_t period)

  Internal SC function to restore an RTC alarm.

- sc_err_t timer_get_rtc_sec1970 (sc_rm_pt_t caller_pt, uint32_t *sec)

  Internal SC function to get the RTC time in seconds since 1/1/1970.

- sc_err_t timer_set_rtc_calb (sc_rm_pt_t caller_pt, int8_t count)

  Internal SC function to set the RTC calibration.

- void timer_tick (uint16_t msec)

  Internal SC function to increment the RTC.

- sc_err_t timer_set_sysctr_alarm (sc_rm_pt_t caller_pt, uint64_t ticks)

  Internal SC function to set the sysctr alarm.

- sc_err_t timer_set_sysctr_periodic_alarm (sc_rm_pt_t caller_pt, uint64_t ticks)

  Internal SC function to set the periodic sysctr alarm.

- sc_err_t timer_cancel_sysctr_alarm (sc_rm_pt_t caller_pt)

  Internal SC function to cancel the sysctr alarm.

16.29.1 Detailed Description

Module for the Timer service.

This includes support for the watchdog, RTC, and system counter. Note every resource partition has a watchdog it can use.

16.29.2 Function Documentation

16.29.2.1 sc_timer_set_wdog_timeout()

```
sc_err_t sc_timer_set_wdog_timeout (
             sc_ipc_t ipc,
             sc_timer_wdog_time_t timeout )
```

This function sets the watchdog timeout in milliseconds.

If not set then the timeout defaults to the max. Once locked this value cannot be changed.

Parameters

in	*ipc*	IPC handle
in	*timeout*	timeout period for the watchdog

Returns

Returns an error code (SC_ERR_NONE = success, SC_ERR_LOCKED = locked).

16.29.2.2 sc_timer_set_wdog_pre_timeout()

```
sc_err_t sc_timer_set_wdog_pre_timeout (
             sc_ipc_t ipc,
             sc_timer_wdog_time_t pre_timeout )
```

This function sets the watchdog pre-timeout in milliseconds.

If not set then the pre-timeout defaults to the max. Once locked this value cannot be changed.

Parameters

in	*ipc*	IPC handle
in	*pre_timeout*	pre-timeout period for the watchdog

When the pre-timout expires an IRQ will be generated. Note this timeout clears when the IRQ is triggered. An IRQ is generated for the failing partition and all of its child partitions.

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.3 sc_timer_set_wdog_window()

```
sc_err_t sc_timer_set_wdog_window (
             sc_ipc_t ipc,
             sc_timer_wdog_time_t window )
```

This function sets the watchdog window in milliseconds.

If not set then the window defaults to the 0. Once locked this value cannot be changed.

Parameters

in	*ipc*	IPC handle
in	*window*	window period for the watchdog

Returns

Returns an error code (SC_ERR_NONE = success, SC_ERR_LOCKED = locked).

Calling sc_timer_ping_wdog() before the window time has expired will result in the watchdog action being taken.

16.29.2.4 sc_timer_start_wdog()

```
sc_err_t sc_timer_start_wdog (
             sc_ipc_t ipc,
             sc_bool_t lock )
```

This function starts the watchdog.

Parameters

in	*ipc*	IPC handle
in	*lock*	boolean indicating the lock status

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_NOACCESS if caller's partition is not isolated,
- SC_ERR_BUSY if already started

If *lock* is set then the watchdog cannot be stopped or the timeout period changed.

If the calling partition is not isolated then the wdog cannot be used. This is always the case if a non-secure partition is running on the same CPU as a secure partition (e.g. Linux under TZ). See sc_rm_partition_alloc().

16.29.2.5 sc_timer_stop_wdog()

```
sc_err_t sc_timer_stop_wdog (
             sc_ipc_t ipc )
```

This function stops the watchdog if it is not locked.

Parameters

in	*ipc*	IPC handle

Returns

Returns an error code (SC_ERR_NONE = success, SC_ERR_LOCKED = locked).

16.29.2.6 sc_timer_ping_wdog()

```
sc_err_t sc_timer_ping_wdog (
             sc_ipc_t ipc )
```

This function pings (services, kicks) the watchdog resetting the time before expiration back to the timeout.

Parameters

in	*ipc*	IPC handle

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.7 sc_timer_get_wdog_status()

```
sc_err_t sc_timer_get_wdog_status (
             sc_ipc_t ipc,
```

```
                sc_timer_wdog_time_t * timeout,
                sc_timer_wdog_time_t * max_timeout,
                sc_timer_wdog_time_t * remaining_time )
```

This function gets the status of the watchdog.

All arguments are in milliseconds.

Parameters

in	*ipc*	IPC handle
out	*timeout*	pointer to return the timeout
out	*max_timeout*	pointer to return the max timeout
out	*remaining_time*	pointer to return the time remaining until trigger

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.8 sc_timer_pt_get_wdog_status()

```
sc_err_t sc_timer_pt_get_wdog_status (
                sc_ipc_t ipc,
                sc_rm_pt_t pt,
                sc_bool_t * enb,
                sc_timer_wdog_time_t * timeout,
                sc_timer_wdog_time_t * remaining_time )
```

This function gets the status of the watchdog of a partition.

All arguments are in milliseconds.

Parameters

in	*ipc*	IPC handle
in	*pt*	partition to query
out	*enb*	pointer to return enable status
out	*timeout*	pointer to return the timeout
out	*remaining_time*	pointer to return the time remaining until trigger

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.9 sc_timer_set_wdog_action()

```
sc_err_t sc_timer_set_wdog_action (
             sc_ipc_t ipc,
             sc_rm_pt_t pt,
             sc_timer_wdog_action_t action )
```

This function configures the action to be taken when a watchdog expires.

Parameters

in	*ipc*	IPC handle
in	*pt*	partition to affect
in	*action*	action to take

Default action is inherited from the parent.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid parameters,
- SC_ERR_NOACCESS if caller's partition is not the SYSTEM owner,
- SC_ERR_LOCKED if the watchdog is locked

16.29.2.10 sc_timer_set_rtc_time()

```
sc_err_t sc_timer_set_rtc_time (
             sc_ipc_t ipc,
             uint16_t year,
             uint8_t mon,
             uint8_t day,
             uint8_t hour,
             uint8_t min,
             uint8_t sec )
```

This function sets the RTC time.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can set the time.

Parameters

in	*ipc*	IPC handle
in	*year*	year (min 1970)
in	*mon*	month (1-12)
in	*day*	day of the month (1-31)
in	*hour*	hour (0-23)
in	*min*	minute (0-59)
in	*sec*	second (0-59)

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid time/date parameters,
- SC_ERR_NOACCESS if caller's partition cannot access SC_R_SYSTEM

16.29.2.11 sc_timer_get_rtc_time()

```
sc_err_t sc_timer_get_rtc_time (
             sc_ipc_t ipc,
             uint16_t * year,
             uint8_t * mon,
             uint8_t * day,
             uint8_t * hour,
             uint8_t * min,
             uint8_t * sec )
```

This function gets the RTC time.

Parameters

in	*ipc*	IPC handle
out	*year*	pointer to return year (min 1970)
out	*mon*	pointer to return month (1-12)
out	*day*	pointer to return day of the month (1-31)
out	*hour*	pointer to return hour (0-23)
out	*min*	pointer to return minute (0-59)
out	*sec*	pointer to return second (0-59)

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.12 sc_timer_get_rtc_sec1970()

```
sc_err_t sc_timer_get_rtc_sec1970 (
            sc_ipc_t ipc,
            uint32_t * sec )
```

This function gets the RTC time in seconds since 1/1/1970.

Parameters

in	*ipc*	IPC handle
out	*sec*	pointer to return seconds

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.13 sc_timer_set_rtc_alarm()

```
sc_err_t sc_timer_set_rtc_alarm (
            sc_ipc_t ipc,
            uint16_t year,
            uint8_t mon,
            uint8_t day,
            uint8_t hour,
            uint8_t min,
            uint8_t sec )
```

This function sets the RTC alarm.

Parameters

in	*ipc*	IPC handle
in	*year*	year (min 1970)
in	*mon*	month (1-12)
in	*day*	day of the month (1-31)
in	*hour*	hour (0-23)
in	*min*	minute (0-59)
in	*sec*	second (0-59)

Note this alarm setting clears when the alarm is triggered. This is an absolute time.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid time/date parameters

16.29.2.14 sc_timer_set_rtc_periodic_alarm()

```
sc_err_t sc_timer_set_rtc_periodic_alarm (
            sc_ipc_t ipc,
            uint32_t sec )
```

This function sets the RTC alarm (periodic mode).

Parameters

in	*ipc*	IPC handle
in	*sec*	period in seconds

Returns

Returns an error code (SC_ERR_NONE = success).

Note this is a relative time.

Return errors:

- SC_ERR_PARM if invalid time/date parameters

16.29.2.15 sc_timer_cancel_rtc_alarm()

```
sc_err_t sc_timer_cancel_rtc_alarm (
            sc_ipc_t ipc )
```

This function cancels the RTC alarm.

Parameters

in	*ipc*	IPC handle

Note this alarm setting clears when the alarm is triggered.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid time/date parameters

16.29.2.16 sc_timer_set_rtc_calb()

```
sc_err_t sc_timer_set_rtc_calb (
            sc_ipc_t ipc,
            int8_t count )
```

This function sets the RTC calibration value.

Only the owner of the SC_R_SYSTEM resource or a partition with access permissions to SC_R_SYSTEM can set the calibration.

Parameters

in	*ipc*	IPC handle
in	*count*	calibration count (-16 to 15)

The calibration value is a 5-bit value including the sign bit, which is implemented in 2's complement. It is added or subtracted from the RTC on a periodic basis, once per 32768 cycles of the RTC clock.

Returns

Returns an error code (SC_ERR_NONE = success).

16.29.2.17 sc_timer_set_sysctr_alarm()

```
sc_err_t sc_timer_set_sysctr_alarm (
            sc_ipc_t ipc,
            uint64_t ticks )
```

This function sets the SYSCTR alarm.

Parameters

in	*ipc*	IPC handle
in	*ticks*	number of 8MHz cycles

Note the *ticks* parameter is an absolute time. This alarm setting clears when the alarm is triggered.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid time/date parameters

16.29.2.18 sc_timer_set_sysctr_periodic_alarm()

```
sc_err_t sc_timer_set_sysctr_periodic_alarm (
            sc_ipc_t ipc,
            uint64_t ticks )
```

This function sets the SYSCTR alarm (periodic mode).

Parameters

in	*ipc*	IPC handle
in	*ticks*	number of 8MHz cycles

Note the *ticks* parameter is a relative time.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid time/date parameters

16.29.2.19 sc_timer_cancel_sysctr_alarm()

```
sc_err_t sc_timer_cancel_sysctr_alarm (
            sc_ipc_t ipc )
```

This function cancels the SYSCTR alarm.

Parameters

in	*ipc*	IPC handle

Note this alarm setting clears when the alarm is triggered.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid time/date parameters

16.29.2.20 timer_init()

```
void timer_init (
            sc_bool_t api_phase )
```

Internal SC function to initializes the TIMER service.

Parameters

in	*api_phase*	init phase

Initializes the API if /a api_phase = SC_TRUE, otherwise initializes the HW managed by the timer service. API must be initialized before anything else is done with the service.

16.29.2.21 timer_init_part()

```
void timer_init_part (
            sc_rm_pt_t caller_pt,
            sc_rm_pt_t pt )
```

This function initializes a new partition.

Parameters

in	*caller_pt*	handle of caller partition
in	*pt*	handle of partition

Note this function should only be called by the resource manager when a new partition is allocated.

16.29.2.22 timer_set_wdog_timeout()

```
sc_err_t timer_set_wdog_timeout (
            sc_rm_pt_t caller_pt,
            sc_timer_wdog_time_t timeout )
```

Internal SC function to set the watchdog timeout in milliseconds.

See also

sc_timer_set_wdog_timeout().

16.29.2.23 timer_set_wdog_pre_timeout()

```
sc_err_t timer_set_wdog_pre_timeout (
            sc_rm_pt_t caller_pt,
            sc_timer_wdog_time_t pre_timeout )
```

Internal SC function to set the watchdog pre-timeout in milliseconds.

See also

sc_timer_set_wdog_pre_timeout().

16.29.2.24 timer_set_wdog_window()

```
sc_err_t timer_set_wdog_window (
            sc_rm_pt_t caller_pt,
            sc_timer_wdog_time_t window )
```

Internal SC function to set the watchdog window in milliseconds.

See also

sc_timer_set_wdog_window().

16.29.2.25 timer_start_wdog()

```
sc_err_t timer_start_wdog (
            sc_rm_pt_t caller_pt,
            sc_bool_t lock )
```

Internal SC function to start the watchdog.

See also

sc_timer_start_wdog().

16.29.2.26 timer_stop_wdog()

```
sc_err_t timer_stop_wdog (
             sc_rm_pt_t caller_pt )
```

Internal SC function to stop the watchdog (if not locked).

See also

sc_timer_stop_wdog().

16.29.2.27 timer_halt_wdog()

```
void timer_halt_wdog (
             sc_rm_pt_t pt )
```

Internal SC function to stop halt the wdog when the partition is deleted.

Parameters

in	*pt*	partition whose wdog should be halted

Returns

Returns an error code (SC_ERR_NONE = success).

This function will halt the wdog even if locked.

16.29.2.28 timer_ping_wdog()

```
sc_err_t timer_ping_wdog (
             sc_rm_pt_t caller_pt )
```

Internal SC function to ping (services, kicks) the watchdog resetting the time before expiration back to the timeout.

See also

sc_timer_ping_wdog().

16.29.2.29 timer_get_wdog_status()

```
sc_err_t timer_get_wdog_status (
             sc_rm_pt_t caller_pt,
             sc_timer_wdog_time_t * timeout,
             sc_timer_wdog_time_t * max_timeout,
             sc_timer_wdog_time_t * remaining_time )
```

Internal SC function to get the status of the watchdog.

All arguments are in milliseconds.

See also

sc_timer_get_wdog_status().

16.29.2.30 timer_pt_get_wdog_status()

```
sc_err_t timer_pt_get_wdog_status (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_bool_t * enb,
             sc_timer_wdog_time_t * timeout,
             sc_timer_wdog_time_t * remaining_time )
```

Internal SC function to get the status of the watchdog of a partition.

All arguments are in milliseconds.

See also

sc_timer_pt_get_wdog_status().

16.29.2.31 timer_set_wdog_action()

```
sc_err_t timer_set_wdog_action (
             sc_rm_pt_t caller_pt,
             sc_rm_pt_t pt,
             sc_timer_wdog_action_t action )
```

Internal SC function to configure the action to be taken when a watchdog expires.

See also

sc_timer_set_wdog_action().

16.29.2.32 timer_take_wdog_action()

```
sc_err_t timer_take_wdog_action (
             sc_rm_pt_t pt )
```

Internal SC function to take the wdog action specified.

Parameters

in	*pt*	partition to affect

Returns

Returns an error code (SC_ERR_NONE = success).

Reboots the partition, board, and/or generate IRQs.

16.29.2.33 timer_set_rtc_time()

```
sc_err_t timer_set_rtc_time (
             sc_rm_pt_t caller_pt,
             uint16_t year,
             uint8_t mon,
             uint8_t day,
             uint8_t hour,
             uint8_t min,
             uint8_t sec )
```

Internal SC function to set the RTC time.

See also

sc_timer_set_rtc_time().

16.29.2.34 timer_get_rtc_time()

```
sc_err_t timer_get_rtc_time (
             sc_rm_pt_t caller_pt,
             uint16_t * year,
             uint8_t * mon,
             uint8_t * day,
             uint8_t * hour,
             uint8_t * min,
             uint8_t * sec )
```

Internal SC function to get the RTC time.

See also

sc_timer_get_rtc_time().

16.29.2.35 timer_set_rtc_alarm()

```
sc_err_t timer_set_rtc_alarm (
            sc_rm_pt_t caller_pt,
            uint16_t year,
            uint8_t mon,
            uint8_t day,
            uint8_t hour,
            uint8_t min,
            uint8_t sec )
```

Internal SC function to set the RTC alarm.

See also

sc_timer_set_rtc_alarm().

16.29.2.36 timer_set_rtc_periodic_alarm()

```
sc_err_t timer_set_rtc_periodic_alarm (
            sc_rm_pt_t caller_pt,
            uint32_t sec )
```

Internal SC function to set a periodic RTC alarm.

See also

sc_timer_set_rtc_periodic_alarm().

16.29.2.37 timer_cancel_rtc_alarm()

```
sc_err_t timer_cancel_rtc_alarm (
            sc_rm_pt_t caller_pt )
```

Internal SC function to cancel an RTC alarm.

See also

sc_timer_cancel_rtc_alarm().

16.29.2.38 timer_query_rtc_alarm()

```
void timer_query_rtc_alarm (
            sc_rm_pt_t pt,
            uint32_t * alarm,
            uint32_t * period )
```

Internal SC function to query an RTC alarm.

Parameters

in	*pt*	partition to query
out	*alarm*	pointer to return alarm
out	*period*	pointer to return period

Companion function to timer_restore_rtc_alarm().

16.29.2.39 timer_restore_rtc_alarm()

```
void timer_restore_rtc_alarm (
            sc_rm_pt_t pt,
            uint32_t alarm,
            uint32_t period )
```

Internal SC function to restore an RTC alarm.

Parameters

in	*pt*	partition to restore
in	*alarm*	alarm
in	*period*	period

Companion function to timer_query_rtc_alarm().

16.29.2.40 timer_get_rtc_sec1970()

```
sc_err_t timer_get_rtc_sec1970 (
            sc_rm_pt_t caller_pt,
            uint32_t * sec )
```

Internal SC function to get the RTC time in seconds since 1/1/1970.

See also

sc_timer_get_rtc_sec1970().

16.29.2.41 timer_set_rtc_calb()

```
sc_err_t timer_set_rtc_calb (
            sc_rm_pt_t caller_pt,
            int8_t count )
```

Internal SC function to set the RTC calibration.

See also

sc_timer_set_rtc_calb().

16.30 BRD: Board Interface

Module for the Board interface.

Macros

- #define BOARD_PARM_RTN_NOT_USED 0U

  Feature not used.
- #define BOARD_PARM_RTN_USED 1U

  Feature used.
- #define BOARD_PARM_RTN_EXTERNAL 2U

  Return value for BOARD_PARM_PCIE_PLL.
- #define BOARD_PARM_RTN_INTERNAL 3U

  Return value for BOARD_PARM_PCIE_PLL.
- #define BOARD_PARM_RTN_INTERNAL_DPLL 4U

  Return value for BOARD_PARM_PCIE_PLL (DXL only)
- #define BOARD_PARM_RTN_DPLL_SS_0_5 0U

  0.5% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_DPLL_SS_1 1U

  1% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_DPLL_SS_1_5 2U

  1.5% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_DPLL_SS_2 3U

  2% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_VDD_MEMC_NOM 0U

  MEMC Nominal.
- #define BOARD_PARM_RTN_VDD_MEMC_OD 1U

  MEMC Overdrive.
- #define BOARD_PARM_KS1_RETENTION_DISABLE 0U

  Disable retention during KS1.
- #define BOARD_PARM_KS1_RETENTION_ENABLE 1U

  Enable retention during KS1.
- #define BOARD_PARM_KS1_ONOFF_WAKE_DISABLE 0U

  Disable ONOFF wakeup during KS1.
- #define BOARD_PARM_KS1_ONOFF_WAKE_ENABLE 1U

  Enable ONOFF wakeup during KS1.
- #define BOARD_PARM_KS1_WDOG_WAKE_ENABLE 0U

  Enable SC WDOG service during KS1 (required for ON_OFF wakeup on some devices)
- #define BOARD_PARM_KS1_WDOG_WAKE_DISABLE 1U

  Disable SC WDOG service during KS1 (SC WDOG disabled during KS1)
- #define BOARD_PARM_SSC_N_0P4 4U

  Return 0.4% fspread for PLL spread spectrum.
- #define BOARD_PARM_SSC_N_1P0 10U

  Return 1.0% fspread for PLL spread spectrum.
- #define BOARD_PARM_SSC_N_1P4 14U

  Return 1.4% fspread for PLL spread spectrum.
- #define BOARD_PARM_SSC_N_2P0 20U

  Return 2.0% fspread for PLL spread spectrum.
- #define BRD_ERR(X)

  Macro for debug of board calls.

Typedefs

- typedef uint32_t board_parm_rtn_t

  Board config parameter returns.

Enumerations

- enum board_parm_t {
  BOARD_PARM_PCIE_PLL = 0, BOARD_PARM_KS1_RESUME_USEC = 1, BOARD_PARM_KS1_RETENTION = 2, BOARD_PARM_KS1_ONOFF_WAKE = 3,
  BOARD_PARM_REBOOT_TIME = 4, BOARD_PARM_DC0_PLL0_SSC = 5, BOARD_PARM_DC0_PLL1_SSC = 6, BOARD_PARM_DC1_PLL0_SSC = 7,
  BOARD_PARM_DC1_PLL1_SSC = 8, BOARD_PARM_ISI_PIX_FREQ = 9, BOARD_PARM_VDD_MEMC = 10,
  BOARD_PARM_KS1_WDOG_WAKE = 11,
  BOARD_PARM_PCIE_DPLL_SS = 12 }

  Board config parameter types.
- enum sc_bfault_t {
  BOARD_BFAULT_COMMON = 0, BOARD_BFAULT_CPU = 1, BOARD_BFAULT_EXIT = 2, BOARD_BFAULT_DDR_RET = 3,
  BOARD_BFAULT_REBOOT = 4, BOARD_BFAULT_BAD_CONTAINER = 5, BOARD_BFAULT_BRD_FAIL = 6,
  BOARD_BFAULT_TEST_FAIL = 7,
  BOARD_BFAULT_DDR_INIT_FAIL = 8 }

  Board fault types.
- enum board_reboot_to_t { BOARD_REBOOT_TO_NONE = 0, BOARD_REBOOT_TO_FORCE = 1, BOARD_REBOOT_TO_FAULT = 2 }

  Board reboot timeout actions.
- enum board_cpu_rst_ev_t { **BOARD_CPU_RESET_SELF** = 0, **BOARD_CPU_RESET_WDOG** = 1, **BOARD_CPU_RESET_LOCKUP** = 2, **BOARD_CPU_RESET_MEM_ERR** = 3 }

  Board reset event types for CPUs.
- enum board_ddr_action_t {
  BOARD_DDR_COLD_INIT = 0, BOARD_DDR_PERIODIC = 1, BOARD_DDR_SR_DRC_ON_ENTER = 2, BOARD_DDR_SR_DRC_ON_EXIT = 3,
  BOARD_DDR_SR_DRC_OFF_ENTER = 4, BOARD_DDR_SR_DRC_OFF_EXIT = 5, BOARD_DDR_PERIODIC_HALT = 6, BOARD_DDR_PERIODIC_RESTART = 7,
  BOARD_DDR_DERATE_PERIODIC = 8, BOARD_DDR0_VREF = 9, BOARD_DDR1_VREF = 10 }

  DDR actions (power state transitions, etc.)

Functions

- sc_err_t test_drv (sc_bool_t *const stop)

  Shim test function (to allow test inclusion from object packages)
- sc_err_t test_sc (sc_bool_t *const stop)

  Shim test function (to allow test inclusion from object packages)
- sc_err_t test_ap (sc_bool_t *const stop)

  Shim test function (to allow test inclusion from object packages)
- void board_monitor (void)

  Shim monitor function (to allow monitor inclusion from object packages)
- void board_exit (int32_t status)

Shim for exit()

- void board_stdio (void)

  Shim for setvbuf()
- void board_printf (const char *fmt,...)

  Conditional printf.
- void board_ddr_periodic_enable (sc_bool_t enb)

  Enable/disable the DDR periodic tick.
- void board_ddr_derate_periodic_enable (sc_bool_t enb)

  Enable/disable the DDR derate periodic tick.
- void board_common_tick (uint16_t msec)

  Common function to tick the board.

Variables

- const sc_rm_idx_t board_num_rsrc

  External variable for accessing the number of board resources.
- const sc_rsrc_map_t board_rsrc_map [BRD_NUM_RSRC_BRD]

  External variable for accessing the board resource map.
- const uint32_t board_ddr_period_ms

  External variable for specing DDR periodic training.
- const uint32_t board_ddr_derate_period_ms

  External variable for DDR periodic derate.
- sc_bool_t debug

  Shim debug variable (to allow object package config)
- sc_bool_t has_test

  Shim has_test variable (to allow object package config)
- sc_bool_t test_all

  Shim test_all variable (to allow object package config)
- sc_bool_t has_monitor

  Shim has_monitor variable (to allow object package config)
- sc_bool_t xrdc_nocheck

  Shim xrdc_nocheck variable (to allow object package config)

Macros for DCD processing

- #define **DATA4**(A, V) *((volatile uint32_t*)(A)) = U32(V)
- #define **SET_BIT4**(A, V) *((volatile uint32_t*)(A)) |= U32(V)
- #define **CLR_BIT4**(A, V) *((volatile uint32_t*)(A)) &= ~(U32(V))
- #define **CHECK_BITS_SET4**(A, M)
- #define **CHECK_BITS_CLR4**(A, M)
- #define **CHECK_ANY_BIT_SET4**(A, M)
- #define **CHECK_ANY_BIT_CLR4**(A, M)

Initialization Functions

- void board_init (boot_phase_t phase)

  This function initalizes the board.
- LPUART_Type * board_get_debug_uart (uint8_t *inst, uint32_t *baud)

  This function returns the debug UART info.
- void board_config_debug_uart (sc_bool_t early_phase)

  This function initalizes the debug UART.
- void board_disable_debug_uart (void)

  This function powers off the debug UART.
- void board_config_sc (sc_rm_pt_t pt_sc)

  This function configures SCU resources.
- board_parm_rtn_t board_parameter (board_parm_t parm)

  This function returns board configuration info.
- sc_bool_t board_rsrc_avail (sc_rsrc_t rsrc)

  This function returns resource availability info.
- sc_err_t board_init_ddr (sc_bool_t early, sc_bool_t ddr_initialized)

  This function initalizes DDR.
- sc_err_t board_ddr_config (bool rom_caller, board_ddr_action_t action)

  This function cinfigures the DDR.
- void board_system_config (sc_bool_t early, sc_rm_pt_t pt_boot)

  This function allows the board file to do SCFW configuration.
- sc_bool_t board_early_cpu (sc_rsrc_t cpu)

  This function returns SC_TRUE for early CPUs.

Power Functions

- void board_set_power_mode (sc_sub_t ss, uint8_t pd, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)

  This function transitions the power state for an external board- level supply which goes to the i.MX8.
- sc_err_t board_set_voltage (sc_sub_t ss, uint32_t new_volt, uint32_t old_volt)

  This function sets the voltage for a PMIC controlled SS.
- void board_lpm (sc_pm_power_mode_t mode)

  This function is used to set power supplies of the board when entering and exiting low power mode.
- void board_trans_resource_power (sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)

  This function transitions the power state for an external board- level supply which goes to a board component.
- void board_rsrc_reset (sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, sc_rm_pt_t pt)

  This function resets a board resource.

Misc Functions

- sc_err_t board_power (sc_pm_power_mode_t mode)

  This function is used to set the board power.
- sc_err_t board_reset (sc_pm_reset_type_t type, sc_pm_reset_reason_t reason, sc_rm_pt_t pt)

  This function is used to reset the system.
- void board_cpu_reset (sc_rsrc_t resource, board_cpu_rst_ev_t reset_event, sc_rm_pt_t pt)

  This function is called when a CPU encounters a reset event.
- void board_reboot_part (sc_rm_pt_t pt, sc_pm_reset_type_t *type, sc_pm_reset_reason_t *reason, sc_pm_power_mode_t *mode, uint32_t *mask)

  This function is called when a partition reboot is requested.
- void board_reboot_part_cont (sc_rm_pt_t pt, sc_rsrc_t *boot_cpu, sc_rsrc_t *boot_mu, sc_rsrc_t *boot_dev, sc_faddr_t *boot_addr)

  This function is called when a partition reboot is has powered off the partition but has not yet powered it back on.
- board_reboot_to_t board_reboot_timeout (sc_rm_pt_t pt)

  This function is called when a partition reboot times out.
- void board_panic (sc_dsc_t dsc)

  This function is called when a SS (other than SCU) reports a panic temp alarm.
- void board_fault (sc_bool_t restarted, sc_bfault_t reason, sc_rm_pt_t pt)

  This function is called when a fault is detected or the SCFW returns from main().
- void board_security_violation (void)

  This function is called when a security violation is reported by the SECO or SNVS.
- sc_bool_t board_get_button_status (void)

  This function is used to return the current status of the ON/OFF button.
- sc_err_t board_set_control (sc_rsrc_t resource, sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, uint32_t ctrl, uint32_t val)

  This function sets a miscellaneous control value.
- sc_err_t board_get_control (sc_rsrc_t resource, sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, uint32_t ctrl, uint32_t *val)

  This function gets a miscellaneous control value.
- void board_tick (uint16_t msec)

  This function is called periodically to tick the board.
- sc_err_t board_ioctl (sc_rm_pt_t caller_pt, sc_rsrc_t mu, uint32_t *parm1, uint32_t *parm2, uint32_t *parm3)

  This function is called when sc_misc_board_ioctl() is called.
- void PMIC_IRQHandler (void)

  Interrupt handler for the PMIC.
- void SNVS_Button_IRQHandler (void)

  Interrupt handler for the SNVS button.

16.30.1 Detailed Description

Module for the Board interface.

16.30.2 Macro Definition Documentation

16.30.2.1 CHECK_BITS_SET4

```
#define CHECK_BITS_SET4(
                A,
                M )
```

Value:

```
while((*((volatile uint32_t*)(A))          \
    & U32(M)) != ((uint32_t)(M))){}
```

16.30.2.2 CHECK_BITS_CLR4

```
#define CHECK_BITS_CLR4(
                A,
                M )
```

Value:

```
while((*((volatile uint32_t*)(A))          \
    & U32(M)) != U32(0U)){}
```

16.30.2.3 CHECK_ANY_BIT_SET4

```
#define CHECK_ANY_BIT_SET4(
                A,
                M )
```

Value:

```
while((*((volatile uint32_t*)(A))       \
    & U32(M)) == U32(0U)){}
```

16.30.2.4 CHECK_ANY_BIT_CLR4

```
#define CHECK_ANY_BIT_CLR4(
                A,
                M )
```

Value:

```
while((*((volatile uint32_t*)(A))       \
    & U32(M)) == U32(M)){}
```

16.30.2.5 BRD_ERR

```
#define BRD_ERR(
                X )
```

Value:

```
if (err == SC_ERR_NONE)                         \
                    {                                                   \
                        err = (X);                                      \
                        if (err != SC_ERR_NONE)                         \
                        {                                               \
                            board_print(3, "error @ line %d: %d\n", \
                                __LINE__, err);                         \
                            board_fault(SC_FALSE,                       \
                                BOARD_BFAULT_BRD_FAIL, SC_PT);          \
                        }                                               \
                    }
```

Macro for debug of board calls.

Examples

board.c.

16.30.3 Enumeration Type Documentation

16.30.3.1 board_parm_t

enum board_parm_t

Board config parameter types.

Enumerator

BOARD_PARM_PCIE_PLL	PCIe PLL internal or external.
BOARD_PARM_KS1_RESUME_USEC	Supply ramp delay in usec for KS1 exit.
BOARD_PARM_KS1_RETENTION	Controls if retention is applied during KS1.
BOARD_PARM_KS1_ONOFF_WAKE	Controls if ONOFF button can wake from KS1.
BOARD_PARM_REBOOT_TIME	Partition reboot timeout in mS.
BOARD_PARM_DC0_PLL0_SSC	DC0 PLL0 spread spectrum config.
BOARD_PARM_DC0_PLL1_SSC	DC0 PLL1 spread spectrum config.
BOARD_PARM_DC1_PLL0_SSC	DC1 PLL0 spread spectrum config.
BOARD_PARM_DC1_PLL1_SSC	DC1 PLL1 spread spectrum config.
BOARD_PARM_ISI_PIX_FREQ	ISI pixel clock frequency override.
BOARD_PARM_VDD_MEMC	VDD_MEMC voltage, valid only for DXL.
BOARD_PARM_KS1_WDOG_WAKE	Controls if SC WDOG configuration during KS1.
BOARD_PARM_PCIE_DPLL_SS	Spread Spectrum SPREAD value for PCIE DPLL (DXL ONLY)

16.30.3.2 sc_bfault_t

enum sc_bfault_t

Board fault types.

Enumerator

BOARD_BFAULT_COMMON	Common fault handler.
BOARD_BFAULT_CPU	Cortex-M ECC or lockup error.
BOARD_BFAULT_EXIT	SCFW exit.
BOARD_BFAULT_DDR_RET	DDR retention request without configuration.
BOARD_BFAULT_REBOOT	Undetermined partition reboot failure.
BOARD_BFAULT_BAD_CONTAINER	Bad boot container, invalid partitions/images.
BOARD_BFAULT_BRD_FAIL	Board failure - RM or PMIC, etc.
BOARD_BFAULT_TEST_FAIL	Unit test failure, exit.
BOARD_BFAULT_DDR_INIT_FAIL	board_init_ddr() returned an error

16.30.3.3 board_reboot_to_t

```
enum board_reboot_to_t
```

Board reboot timeout actions.

Enumerator

BOARD_REBOOT_TO_NONE	Reboot timeout does nothing.
BOARD_REBOOT_TO_FORCE	Reboot timeout forces reboot continue.
BOARD_REBOOT_TO_FAULT	Reboot timeout causes board fault.

16.30.3.4 board_ddr_action_t

```
enum board_ddr_action_t
```

DDR actions (power state transitions, etc.)

Enumerator

BOARD_DDR_COLD_INIT	Init DDR from POR.
BOARD_DDR_PERIODIC	Run periodic training.
BOARD_DDR_SR_DRC_ON_ENTER	Enter self-refresh (leave DRC on)
BOARD_DDR_SR_DRC_ON_EXIT	Exit self-refresh (DRC was on)
BOARD_DDR_SR_DRC_OFF_ENTER	Enter self-refresh (turn off DRC)
BOARD_DDR_SR_DRC_OFF_EXIT	Exit self-refresh (DRC was off)
BOARD_DDR_PERIODIC_HALT	Halt periodic training.
BOARD_DDR_PERIODIC_RESTART	Restart periodic training.
BOARD_DDR_DERATE_PERIODIC	Run periodic derate.
BOARD_DDR0_VREF	Run VREF training for DRC 0.
BOARD_DDR1_VREF	Run VREF training for DRC 1.

16.30.4 Function Documentation

16.30.4.1 board_init()

```
void board_init (
            boot_phase_t phase )
```

This function initalizes the board.

Parameters

in	*phase*	boot phase

There are seven phases to board initialization. The first phase is system init (*phase* = BOOT_PHASE_SYS_INIT). This happens before any HW access is possible. The second phase is the API phase (*phase* = BOOT_PHASE_API_INIT) and initializes all of the board interface data structures. The third phase (*phase* = BOOT_PHASE_HW_INIT) is the HW phase and this initializes the board hardware. The fourth phase (*phase* = BOOT_PHASE_EARLY_INIT) is just before starting early CPU. The fifth phase (*phase* = BOOT_PHASE_LATE_INIT) is just before starting the remaining CPUs. The sixth phase (*phase* = BOOT_PHASE_FINAL_INIT) is the final boot phase and is used to wrap up any needed init. A test phase (*phase* = BOOT_PHASE_TEST_INIT) is called only when an SCFW image is built with unit tests and is called just before any tests are run.

Examples

board.c.

16.30.4.2 board_get_debug_uart()

```
LPUART_Type* board_get_debug_uart (
             uint8_t * inst,
             uint32_t * baud )
```

This function returns the debug UART info.

Parameters

in	*inst*	UART instance
in	*baud*	UART baud rate

Returns

Pointer to the debug UART type.

Examples

board.c.

16.30.4.3 board_config_debug_uart()

```
void board_config_debug_uart (
             sc_bool_t early_phase )
```

This function initalizes the debug UART.

Parameters

in	*early_phase*	flag indicating phase

Examples

board.c.

16.30.4.4 board_disable_debug_uart()

```
void board_disable_debug_uart (
            void  )
```

This function powers off the debug UART.

Only called when rebooting a partition. Only needs to power down the UART if it isn't the dedicated SCU UART. board_get_debug_uart() will be called again after the reboot completes.

Examples

board.c.

16.30.4.5 board_config_sc()

```
void board_config_sc (
            sc_rm_pt_t pt_sc )
```

This function configures SCU resources.

Parameters

in	*pt_sc*	SCU partition

By default, the SCFW keeps most of the resources found in the SCU subsystem. It also keeps the SCU/PMIC pads required for the main code to function. Any additional resources or pads required for the board code to run should be kept here. This is done by marking them as not movable.

Examples

board.c.

16.30.4.6 board_parameter()

```
board_parm_rtn_t board_parameter (
            board_parm_t parm )
```

This function returns board configuration info.

Parameters

in	*parm*	parameter to return

This function is used to return board configuration info. Parameters define if various how various SoC connections are made at the board-level. For example, the external PCIe clock input.

Note this can be called at any time in the boot process. If a return value is based on run-time detection (for example reading a GPIO) great care must be take to insure the return value is correct and that infrastructure is powered to allow this.

See example code (board.c) for parameter/returns options.

Returns

Returns the paramter value.

Examples

board.c.

16.30.4.7 board_rsrc_avail()

```
sc_bool_t board_rsrc_avail (
            sc_rsrc_t rsrc )
```

This function returns resource availability info.

Parameters

in	*rsrc*	resource to check

This function is used to return board configuration info. It reports if resources are functional on this board. For example, which DDR controllers are used.

See example code (board.c) for more details.

Returns

Returns SC_TRUE if available.

Examples

board.c.

16.30.4.8 board_init_ddr()

```
sc_err_t board_init_ddr (
            sc_bool_t early,
            sc_bool_t ddr_initialized )
```

This function initalizes DDR.

Parameters

in	*early*	phase of init
in	*ddr_initialized*	True if ROM initialized the DDR

This function may be called twice. The early parameter is SC_TRUE when called prior to M4 start and SC_FALSE when called after. This allows the implementation to decide when DDR init needs to be done.

Note the first call will not occur unless SC_BD_FLAGS_EARLY_CPU_START is set in bd_flags of the boot container.

Returns

Returns an error code (SC_ERR_NONE = success).

Examples

board.c.

16.30.4.9 board_ddr_config()

```
sc_err_t board_ddr_config (
            bool rom_caller,
            board_ddr_action_t action )
```

This function cinfigures the DDR.

Parameters

in	*rom_caller*	is ROM the caller?
in	*action*	perform this action on DDR

Returns

Returns SC_ERR_NONE if successful.

This function may be called from the ROM (*rom_caller* = SC_TRUE). In this case, the SCFW startup has not yet run and it is not valid to call most SCFW function calls. DSC_AIRegisterWrite() and SYSCTR_TimeDelay() are the only two functions that have are safe to call.

Examples

board.c.

16.30.4.10 board_system_config()

```
void board_system_config (
            sc_bool_t early,
            sc_rm_pt_t pt_boot )
```

This function allows the board file to do SCFW configuration.

Parameters

in	*early*	phase of init
in	*pt_boot*	boot partition

This function may be called twice. The early parameter is SC_TRUE when called prior to M4 start and SC_FALSE when called after. This allows the implementation to decide when to do configuration processing.

Note the first call will not occur unless SC_BD_FLAGS_EARLY_CPU_START is set in bd_flags of the boot container.

Typical actions here include creating a resource partition for an M4, powering up a board component, or configuring a shared clock.

Examples

board.c.

16.30.4.11 board_early_cpu()

```
sc_bool_t board_early_cpu (
            sc_rsrc_t cpu )
```

This function returns SC_TRUE for early CPUs.

Parameters

in	*cpu*	CPU

This function should return SC_TRUE if the CPU in question may be started early. This early start is before power on of later CPU subsystems. It would normally return SC_TRUE for CM4 cores that need to run early. Only SC_R_M4_0_↩ PID0 and SC_R_M4_1_PID0 can return SC_TRUE.

Note CPUs will only get started early if SC_BD_FLAGS_EARLY_CPU_START is set in bd_flags of the boot container.

Returns

Returns SC_TRUE if CPU should start early.

Examples

board.c.

16.30.4.12 board_set_power_mode()

```
void board_set_power_mode (
            sc_sub_t ss,
            uint8_t pd,
            sc_pm_power_mode_t from_mode,
            sc_pm_power_mode_t to_mode )
```

This function transitions the power state for an external board- level supply which goes to the i.MX8.

Parameters

in	*ss*	subsystem using supply
in	*pd*	power domain
in	*from_mode*	power mode transitioning from
in	*to_mode*	power mode transitioning to

This function is used to transition a board power supply that is used by the SoC. It allows mapping of subsystem power domains to board supplies.

Note that the base code will enable/disable isolators after changing the state of internal power domains. External supplies sometimes supply a domain connected via an isolator to a domain passed here. In this case, this function needs to also control the connected domain's supply. For example, when LVDS SS PD (PD1) is powered toggled, the external supply for the LVDS PHY must be toggled here. MIPI and CSI SS PD are similar.

Examples

board.c.

16.30.4.13 board_set_voltage()

```
sc_err_t board_set_voltage (
            sc_sub_t ss,
            uint32_t new_volt,
            uint32_t old_volt )
```

This function sets the voltage for a PMIC controlled SS.

Parameters

in	*ss*	subsystem
in	*new_volt*	voltage value to be set
in	*old_volt*	current voltage

Returns

Returns an error code (SC_ERR_NONE = success).

Examples

board.c.

16.30.4.14 board_lpm()

```
void board_lpm (
            sc_pm_power_mode_t mode )
```

This function is used to set power supplies of the board when entering and exiting low power mode.

Parameters

in	*mode*	power mode to apply

Note this function is not called by sc_pm_set_sys_power_mode(). It is called when the system dynamically transitions power modes during run-time execution. It is normally used to manage the supply for the memories (MEMC).

Examples

board.c.

16.30.4.15 board_trans_resource_power()

```
void board_trans_resource_power (
            sc_rm_idx_t idx,
            sc_rm_idx_t rsrc_idx,
            sc_pm_power_mode_t from_mode,
            sc_pm_power_mode_t to_mode )
```

This function transitions the power state for an external board- level supply which goes to a board component.

Parameters

in	*idx*	board-relative resource index
in	*rsrc_idx*	unified resource index
in	*from_mode*	power mode transitioning from
in	*to_mode*	power mode transitioning to

This function is used to transition a board power supply that is used by a board component. It allows mapping of board resources (e.g. SC_R_BOARD_R0) to board supplies.

idx should be used to identify the resource. It is 0-n and is associated with the board reosurces PMIC_0 through BOARD_R7.

rsrc_idx is only useful for debug output of a resource name.

Examples

board.c.

16.30.4.16 board_rsrc_reset()

```
void board_rsrc_reset (
            sc_rm_idx_t idx,
            sc_rm_idx_t rsrc_idx,
            sc_rm_pt_t pt )
```

This function resets a board resource.

Parameters

in	*idx*	board-relative resource index
in	*rsrc_idx*	unified resource index
in	*pt*	partition

This function is used to reset resource. If pt equals SC_PT_ALL then reset all resources belonging to that partition. Otherwise, reset rsrc_idx only.

It is only called when a partition is rebooted or when the sc_pm_resource_reset() function is called. Is is usually empty unless a resource can't be powered off but can be soft reset.

idx should be used to identify the resource. It is 0-n and is associated with the board reosurces PMIC_0 through BOARD_R7.

rsrc_idx is only useful for debug output of a resource name.

Examples

board.c.

16.30.4.17 board_power()

```
sc_err_t board_power (
            sc_pm_power_mode_t mode )
```

This function is used to set the board power.

Parameters

in	*mode*	power mode to apply

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid mode

This function is only called by sc_pm_set_sys_power_mode(). It is normally used ask the PMIC to power off the board completly.

Examples

board.c.

16.30.4.18 board_reset()

```
sc_err_t board_reset (
            sc_pm_reset_type_t type,
            sc_pm_reset_reason_t reason,
            sc_rm_pt_t pt )
```

This function is used to reset the system.

Parameters

in	*type*	reset type
in	*reason*	cause of reset
in	*pt*	partition causing reset

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid type

If this function returns, then the reset did not occur due to an invalid parameter.

Examples

board.c.

16.30.4.19 board_cpu_reset()

```
void board_cpu_reset (
            sc_rsrc_t resource,
            board_cpu_rst_ev_t reset_event,
            sc_rm_pt_t pt )
```

This function is called when a CPU encounters a reset event.

Parameters

in	*resource*	CPU resource
in	*reset_event*	CPU reset event
in	*pt*	partition of CPU

Examples

board.c.

16.30.4.20 board_reboot_part()

```
void board_reboot_part (
            sc_rm_pt_t pt,
```

```
            sc_pm_reset_type_t * type,
            sc_pm_reset_reason_t * reason,
            sc_pm_power_mode_t * mode,
            uint32_t * mask )
```

This function is called when a partition reboot is requested.

It allows the port to override the parameters or take other action such as logging or reboot the board.

Parameters

in	*pt*	partition being rebooted
in,out	*type*	pointer to modify reset type
in,out	*reason*	pointer to modify reset reason
in,out	*mode*	pointer to modify power cycle mode
out	*mask*	pointer to return mask of wait partitions

Code can modify or log the parameters. Can also take another action like reset the board. After return from this function, the partition will be rebooted.

Type is cold, warm, board. Reason is SW, WDOG, etc. Reboot is accomplished by reducing power and reapplying. Mode indicates the power level to reduce to (usually off).

If *mask* is non-0 mask, then the reboot will be delayed until all partitions indicated in the mask (pt 1 = bit 1, etc.) have called sc_pm_reboot_continue() to continue the boot.

Examples

board.c.

16.30.4.21 board_reboot_part_cont()

```
void board_reboot_part_cont (
            sc_rm_pt_t pt,
            sc_rsrc_t * boot_cpu,
            sc_rsrc_t * boot_mu,
            sc_rsrc_t * boot_dev,
            sc_faddr_t * boot_addr )
```

This function is called when a partition reboot is has powered off the partition but has not yet powered it back on.

It allows the boot parameters to be changed. Could also bracket a change done in board_reboot_part().

Parameters

in	*pt*	partition being rebooted
in,out	*boot_cpu*	pointer to modify the boot CPU
in,out	*boot_mu*	pointer to modify the boot MU
in,out	*boot_dev*	pointer to modify the boot device
in,out	*boot_addr*	pointer to modify the boot address

Examples

board.c.

16.30.4.22 board_reboot_timeout()

```
board_reboot_to_t board_reboot_timeout (
            sc_rm_pt_t pt )
```

This function is called when a partition reboot times out.

Parameters

in	*pt*	partition being rebooted

Returns

Returns the desired action.

Examples

board.c.

16.30.4.23 board_panic()

```
void board_panic (
            sc_dsc_t dsc )
```

This function is called when a SS (other than SCU) reports a panic temp alarm.

Parameters

in	*dsc*	dsc reporting alarm

Note this function would normally request a board reset.

See the Porting Guide for more information.

Examples

board.c.

16.30.4.24 board_fault()

```
void board_fault (
            sc_bool_t restarted,
            sc_bfault_t reason,
            sc_rm_pt_t pt )
```

This function is called when a fault is detected or the SCFW returns from main().

Parameters

in	*restarted*	SC_TRUE if called on restart
in	*reason*	reason for the fault
in	*pt*	partition causing fault

Note this function would normally request a board reset. For debug builds it is common to disable the watchdog and loop.

The *restarted* paramter is SC_TRUE if this error is pending from the last restart.

Examples

board.c.

16.30.4.25 board_security_violation()

```
void board_security_violation (
            void  )
```

This function is called when a security violation is reported by the SECO or SNVS.

Note this function would normally request a board reset. For debug builds it is common to do nothing.

Examples

board.c.

16.30.4.26 board_get_button_status()

```
sc_bool_t board_get_button_status (
            void  )
```

This function is used to return the current status of the ON/OFF button.

Returns

Returns the status

Examples

board.c.

16.30.4.27 board_set_control()

```
sc_err_t board_set_control (
            sc_rsrc_t resource,
            sc_rm_idx_t idx,
            sc_rm_idx_t rsrc_idx,
            uint32_t ctrl,
            uint32_t val )
```

This function sets a miscellaneous control value.

Parameters

in	*resource*	resource
in	*idx*	board resource index
in	*rsrc_idx*	unified resource index
in	*ctrl*	control to write
in	*val*	value to write

Returns

Returns an error code (SC_ERR_NONE = success).

Note this function can be used to set voltages for both SoC resources and board resources (e.g. SC_R_BOARD_R0).

Examples

board.c.

16.30.4.28 board_get_control()

```
sc_err_t board_get_control (
            sc_rsrc_t resource,
            sc_rm_idx_t idx,
            sc_rm_idx_t rsrc_idx,
            uint32_t ctrl,
            uint32_t * val )
```

This function gets a miscellaneous control value.

Parameters

in	*resource*	resource
in	*idx*	board resource index
in	*rsrc_idx*	unified resource index
in	*ctrl*	control to read
out	*val*	pointer to return value

Returns

Returns an error code (SC_ERR_NONE = success).

Examples

board.c.

16.30.4.29 board_tick()

```
void board_tick (
            uint16_t msec )
```

This function is called periodically to tick the board.

Parameters

in	*msec*	number of mS to increment

Can be used to implement customer watchdogs, monitor some hardware, etc.

Examples

board.c.

16.30.4.30 board_ioctl()

```
sc_err_t board_ioctl (
            sc_rm_pt_t caller_pt,
            sc_rsrc_t mu,
            uint32_t * parm1,
            uint32_t * parm2,
            uint32_t * parm3 )
```

This function is called when sc_misc_board_ioctl() is called.

Parameters

in	*caller_pt*	handle of caller partition
in	*mu*	receiving MU via RPC/IPC
in,out	*parm1*	pointer to pass parameter 1
in,out	*parm2*	pointer to pass parameter 2
in,out	*parm3*	pointer to pass parameter 3

Can be used to implement customer watchdogs, monitor some hardware, etc.

Returns

Returns an error code (SC_ERR_NONE = success).

Examples

board.c.

16.30.4.31 test_drv()

```
sc_err_t test_drv (
            sc_bool_t *const stop )
```

Shim test function (to allow test inclusion from object packages)

Parameters

in	*stop*	flag indicating if test run should stop

Returns

Returns an error code (SC_ERR_NONE = success)

16.30.4.32 test_sc()

```
sc_err_t test_sc (
            sc_bool_t *const stop )
```

Shim test function (to allow test inclusion from object packages)

Parameters

in	*stop*	flag indicating if test run should stop

Returns

Returns an error code (SC_ERR_NONE = success)

16.30.4.33 test_ap()

```
sc_err_t test_ap (
            sc_bool_t *const stop )
```

Shim test function (to allow test inclusion from object packages)

Parameters

in	*stop*	flag indicating if test run should stop

Returns

Returns an error code (SC_ERR_NONE = success)

16.30.4.34 board_ddr_periodic_enable()

```
void board_ddr_periodic_enable (
            sc_bool_t enb )
```

Enable/disable the DDR periodic tick.

Parameters

in	*enb*	enable flag (SC_TRUE = on)

Examples

board.c.

16.30.4.35 board_ddr_derate_periodic_enable()

```
void board_ddr_derate_periodic_enable (
            sc_bool_t enb )
```

Enable/disable the DDR derate periodic tick.

Parameters

in	*enb*	enable flag (SC_TRUE = on)

Examples

board.c.

16.30.4.36 board_common_tick()

```
void board_common_tick (
            uint16_t msec )
```

Common function to tick the board.

Parameters

in	*msec*	number of mS to increment

16.31 SOC: SoC Interface

Module for the SoC Interface.

Data Structures

- struct soc_patch_area_list_t
- struct soc_freq_volt_tbl_t
- struct soc_gpu_clks_opp_t
- struct soc_cpu_state_t

  Stores CPU power state info.
- struct soc_cluster_state_t

  Stores cluster power state info.
- struct soc_multicluster_state_t

  Stores multi-cluster power state info.
- struct soc_m4_state_t

  Stores M4 sleep state info.
- struct soc_sys_if_node_t

  Stores system interface node resource info.
- struct soc_sys_if_req_t

  Stores system interface power mode reqest info.
- struct soc_hmp_node_t

  Stores HMP node power mode info.
- struct soc_fspi_ret_info_t

  Stores HMP FSPI retention info.
- struct soc_hmp_t

  Stores HMP system power mode info.
- struct soc_ddr_ret_region_t
- struct soc_ddr_ret_info_t

  Stores DDR retention info.
- struct soc_dqs2dq_sync_info_t

  Stores DQS2DQ synchronization info.
- struct soc_msi_ring_usecount_t

  Stores MSI ring usecount.

Macros

- #define STC_RCAT_SETCAT(SS, CAT, CATMASK, CMP)

  Macro to configure an STC category.
- #define STC_RCAT_SETSTARTSTOPTDM(SS, CAT, TDM, START, STOP)

  Macro to set an STC TDM.
- #define STC_RCAT_GETHPR(SS, CAT)

  Macro to get an STC HPR.
- #define STC_RCAT_SETHPR(SS, CAT, HPR)

  Macro to set an STC HPR.
- #define STC_QOS_PANIC(SS, CAT, QOS)

Macro to set an STC QoS panic.

- #define STC_UD_THRESHOLD1(SS, CAT, TH, QOS)

  Macro to set an STC threshold.
- #define STC_UD_THRESHOLD2(SS, CAT, TH, QOS)

  Macro to set an STC threshold 2.
- #define STC_UD_DIS(SS)

  Macro to disable an STC underrun detect.
- #define **SOC_SYS_IF_NO_SAVE** (SC_PM_PW_MODE_ON + 1U)
- #define SOC_RR 1U

  Reset reason SNVS persistant storage register.
- #define SOC_RR_CHECK(X) ((((X) >> 24U) & 0xFFUL) == 0xCCUL)

  Macro to check if reset reason is valid.
- #define SOC_RR_INFO(R, P) ((0xCCUL << 24U) | (U32(R) << 8U) | U32(P))

  Macro to set the reset reason.
- #define SOC_RR_REASON(X) (((X) >> 8U) & 0xFFUL)

  Macro to extract the reset reason.
- #define SOC_RR_PT(X) (((X) >> 0U) & 0xFFUL)

  Macro to extract the resetting partition.

Variables

- sc_rm_pt_t soc_reset_pt

  Global variable to hold resetting partition.
- sc_pm_reset_reason_t soc_reset_rsn

  Global variable to hold reset reason.
- uint32_t **soc_dpll_tbl_0** [ ]
- uint32_t **soc_dpll_tbl_1** [ ]
- sc_bool_t soc_clk_off_trans

  Global variable to store the state of clocks during power transition.
- soc_hmp_t soc_hmp

  Global variable to hold the SCU standalone repeater trim.
- soc_sys_if_req_t **soc_sys_if_req** [SOC_NUM_HMP_NODES][SOC_NUM_SYS_IF]
- soc_m4_state_t **soc_m4_state** [SOC_NUM_M4]
- soc_cluster_state_t **soc_cluster_state** [SOC_NUM_CLUSTER]
- soc_dqs2dq_sync_info_t * **soc_dqs2dq_sync_info**

Defines for patch ID

- #define **SC_PATCH_ID_NONE** 0x00U /* Non patch - end marker */
- #define **SC_PATCH_ID_SCU** 0x55U /* SCU ROM patch */
- #define **SC_PATCH_ID_SECO** 0x45U /* SECO ROM patch */
- #define **SC_PATCH_ID_V2X** 0x57U /* V2X primary ROM patch */
- #define **SC_PATCH_ID_V2X2** 0x59U /* V2X secondary ROM patch */
- #define **SC_PATCH_ID_C2XS** 0x5AU /* V2X ROM patch SHA value */
- #define **SC_PATCH_ID_CTRL** 0x5BU /* Patch control */
- #define **SC_PATCH_ID_ALL** 0xFFU /* All patch IDs */

Initialization Functions

- void soc_init_common (boot_phase_t phase)

  This function initalizes the parts of the SoC.
- void soc_init (boot_phase_t phase)

  This function initalizes the SoC specific parts of the chip.
- void soc_config_sc (sc_rm_pt_t pt_sc, sc_rm_pt_t pt_boot)

  This function configures SCU resources.
- void soc_config_seco (void)

  This function configures SECO resources.
- void soc_db_stc_config (void)

  Configure the STCs in the DB when it is powered up.
- void soc_init_fused_rsrc (void)

  This function fills in a bit array with info about disabled resources.
- void soc_ss_notavail (sc_sub_t ss)

  This function configures a subsystem as not available.
- void soc_init_refgen (void)

  This function initalizes the refgen trims from the fuses.
- void soc_analog_fuse_init (void)

  This function initalize regulator, repeater and osc trims from the fuses.

Info Functions

- void soc_set_reset_info (sc_pm_reset_reason_t reason, sc_rm_pt_t pt)

  This function saves reset info into persistant storage.
- sc_pm_reset_reason_t soc_reset_reason (void)

  Return reset reason.
- sc_rm_pt_t soc_reset_part (void)

  Return partition causing reset.
- sc_bool_t soc_rsrc_avail (sc_rsrc_t rsrc)

  This function returns if a resource is available.
- uint32_t soc_get_temp_trim (sc_dsc_t dsc)

  This function returns the trim value for a temp sensor.
- int8_t soc_get_temp_ofs (sc_dsc_t dsc)

  This function returns the offset value for a temp sensor.
- uint32_t soc_get_max_freq (sc_dsc_t dsc_id)

  This function returns the maximum frequency limited by the fuses for the GPU and AP cores.
- sc_bool_t soc_enet_get_freq_limit (sc_rsrc_t enet_rsrc)

  This function checks if the frequency is limited by fuse.
- void soc_get_max_freq_fuse (void)

  Initialize the maximum frequency of certain resources based on fuses.
- sc_bool_t soc_pd_switchable (sc_dsc_t dsc, uint32_t pd)

  This function identifies if the given pd has internal or external switches.
- sc_bool_t soc_pd_retention (sc_dsc_t dsc, uint32_t pd)

  This function checks if the given power domain of the given dsc supports retention.
- sc_bool_t soc_ss_has_bias (sc_sub_t ss)

  This function checks if the given subsystem has forward body-bias.

- dsc_ai_type_t soc_ss_ai_type (sc_sub_t ss)

  This function returns the subsystem AI type, mainly used to identify if an SS has temp sensor.
- uint32_t soc_mem_type (sc_dsc_t dsc, uint32_t pd)

  Return the type of memory used in the given PD of the DSC.
- uint8_t soc_mem_pwr_plane (sc_dsc_t dsc_id)

  This function returns the uniquely defined memory power plane for the given dsc id.
- void soc_dsc_clock_info (dsc_clk_type_t *clk_type, uint32_t *idx, sc_pm_clk_parent_t *parent)

  Return the DSCMIX clock slice index and type.
- uint32_t soc_get_clock_div (sc_dsc_t dsc, uint8_t *pll_div)

  Return the DSCMIX clock slice divider and pll-divided output connected to all the slices in the dsc.
- sc_bool_t soc_slice_is_dsc (const dsc_clk_info_t *clk_info)

  Checks if the given clock slice is the DSCMIX slice.
- uint8_t soc_get_avpll_ssc_n (sc_dsc_t dsc, uint8_t pll_index)

  This function returns spread spectrum info required to setup the AVPLL.
- sc_bool_t soc_gpu_freq_hw_limited (void)

  This function checks if the GPU frequency is HW limited based on fuses.
- void soc_rompatch_checksum (uint32_t *checksum, uint16_t len)

  Calculate and return the ROM patch checksum.

Analog Functions

- void soc_setup_anamix (sc_bool_t enable)

  Enable/Disable anamix in some SS during init and low power mode.
- void soc_dsc_powerup_anamix (sc_dsc_t dsc)

  This function powers up the DSC anamix.
- void soc_dsc_powerup_phymix (sc_dsc_t dsc)

  This function powers up the DSC phymix.
- void soc_dsc_powerdown_anamix (sc_dsc_t dsc)

  This function powers down the DSC anamix.
- void soc_dsc_powerdown_phymix (sc_dsc_t dsc)

  This function powers down the DSC phymix.
- void soc_setup_hsio_repeater (board_parm_rtn_t internal_clk, sc_bool_t enable)

  Setup HSIO repeaters for internal or external PCIE clock.
- void soc_set_bias (sc_sub_t ss, uint8_t bias_mask, sc_bool_t enable, uint32_t delay)

  Setup the Forward body-bias for the given subsystem.
- uint32_t soc_dpll_dco_pc (sc_dsc_t dsc, uint8_t pll_index, uint32_t rate)

  Return the DPLL DCO-P trim value.
- void soc_dpll_populate_tbl (void)

  Populate the DPLL DCO-PC values based on fuses.

Power Functions

- sc_err_t soc_set_freq_voltage (sc_sub_t ss, uint32_t old_freq, uint32_t *new_freq, sc_bool_t pmic_change)

  Set the voltage based on the frequency for SS controlled by PMIC rail.
- void soc_trans_pd (sc_sub_t ss, uint8_t pd, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)

  Handle SoC and board level power transitions required to power up or down a power domain.
- sc_bool_t soc_bias_enabled (sc_sub_t ss)

  Check if the Forward body bias is enabled for the cluster, this function is only valid for the AP clusters.
- sc_bool_t soc_ss_has_vd_detect (sc_dsc_t dsc, sc_pm_clock_rate_t rate)

  Check if the new PLL rate is below the max freq vd-detect in the SS can support.
- void soc_trans_bandgap (sc_sub_t ss, sc_rsrc_t rsrc_idx, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)

  Transition internal SOC level bandgap.
- void **soc_fabric_force_on** (sc_sub_t ss, sc_bool_t enb)
- void **soc_post_ss_reset** (sc_dsc_t dsc, DSC_Type *dsc_base)
- void **soc_gicr_quiesce** (uint8_t cluster_idx, uint32_t cpu_idx)
- void **soc_pause_ddr_traffic** (sc_bool_t pause)

HPM Functions

- void **soc_init_hmp** (boot_phase_t phase)
- sc_err_t **soc_set_cpu_resume** (uint8_t cluster_idx, uint8_t cpu_idx, sc_bool_t isPrimary, sc_faddr_t resume_addr)
- sc_err_t **soc_set_m4_resume** (uint8_t m4_idx, sc_faddr_t resume_addr)
- sc_err_t **soc_set_multicluster_power_mode** (sc_pm_power_mode_t mode)
- sc_err_t **soc_set_cluster_power_mode** (uint8_t cluster_idx, sc_pm_power_mode_t mode)
- sc_err_t **soc_set_cpu_power_mode** (uint8_t cluster_idx, uint8_t cpu_idx, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)
- void **soc_set_cpu_rst_mode** (uint8_t cluster_idx, uint8_t cpu_idx, sc_bool_t rst)
- void **soc_set_m4_sleep_mode** (uint8_t m4_idx, sc_bool_t dsm, uint8_t stopm, uint8_t pstopo)
- sc_bool_t **soc_get_m4_sleep_mode_active** (uint8_t m4_idx)
- void **soc_set_m4_rst_mode** (uint8_t m4_idx, sc_bool_t rst)
- sc_err_t **soc_req_sys_if_power_mode** (uint8_t hmp_idx, sc_pm_sys_if_t sys_if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)
- void **soc_trans_sys_if_hpm** (uint8_t hmp_idx)
- void **soc_trans_sys_if_lpm** (void)
- void **soc_sync_sys_if_pm** (void)
- void **soc_trans_cpu_power_mode** (uint8_t cluster_idx, uint8_t cpu_idx)
- void **soc_trans_m4_power_mode** (uint8_t m4_idx)
- void **soc_prewake_cpu** (void)
- void **soc_wake_cpu** (uint8_t cluster_idx, uint8_t cpu_idx)
- void **soc_wake_m4** (uint8_t m4_idx)
- void **soc_wake_lsio_mu** (void)
- void **soc_wake_m4_mu** (uint8_t m4_idx)
- void **soc_wake_sys_if_interconnect** (void)
- sc_pm_power_mode_t **soc_get_hmp_sys_power_mode** (void)
- void **soc_dump_hmp_power_state** (void)
- sc_bool_t **soc_can_hmp_enter_lpm** (void)

DDR Functions

- sc_err_t soc_init_ddr (sc_bool_t early)

  This function initalizes DDR.
- void soc_self_refresh_power_down_clk_disable_entry (void)

  This function places the DDR in SRPD (self-refresh power down) and disables DDR clocks.
- void soc_refresh_power_down_clk_disable_exit (void)

  This function enables DDR clocks and exits the DDR from SRPD (self-refresh power down).
- void soc_ddr_config_retention (soc_ddr_ret_info_t *ddr_ret_info)

  This function configures parameters for DDR low-power retention (SRPD with DRC powered down).
- void soc_ddr_enter_retention (void)

  This function places the DDR into low-power retention (SRPD with DRC powered down).
- void soc_ddr_exit_retention (void)

  This function exits the DDR from low-power retention (SRPD with DRC powered down).
- void soc_ddr_dqs2dq_init (void)

  This function initializes LPDDR4 DQS2DQ training.
- void soc_ddr_bit_deskew (void)

  This function does DDR bit deskew training.
- void soc_ddr_dqs2dq_periodic (void)

  This function invokes LPDDR4 DQS2DQ periodic training.
- void soc_ddr_dqs2dq_config (soc_dqs2dq_sync_info_t *dqs2dq_sync_info)

  This function configures parameters of LPDDR4 DQS2DQ periodic training.
- void soc_ddr_dqs2dq_sync (void)

  This function sychronizes LPDDR4 DQS2DQ periodic training to DDR traffic events (i.e.
- void soc_drc_lpcg_setup (void)

  This function enables DDR LPCG clock gating.

Misc Functions

- void soc_temp_sensor_tick (uint16_t msec)

  This function ticks the temp sensor processing.
- void **soc_setup_msi_slave_ring** (sc_sub_t cur_ss, sc_sub_t parent, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
- void **soc_msi_ring_workaround** (sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode, soc_msi_ring_usecount_t *msi_slv_ring, uint32_t num_msi_slaves, MSI_MSTR_Type *msi_reg, sc_sub_t cur_ss)

Debug Functions

- void soc_dsc_ai_dumpmodule (sc_dsc_t dsc, uint8_t tog, sc_ai_t ai)

  Dumps registers of single analog module.
- void soc_dsc_ai_dump (sc_dsc_t dsc)

  Dumps registers of analog modules in a subsystem.
- void soc_anamix_test_out (sc_dsc_t dsc)

  Allows for muxing out analog clocks and voltage levels.

16.31.1 Detailed Description

Module for the SoC Interface.

16.31.2 Macro Definition Documentation

16.31.2.1 STC_RCAT_SETCAT

```
#define STC_RCAT_SETCAT(
              SS,
              CAT,
              CATMASK,
              CMP )
```

Value:

```
STC_RCAT_SetCategorization(base_ptrs[                  \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi],                    \
    CAT, CATMASK, CMP)
```

Macro to configure an STC category.

16.31.2.2 STC_RCAT_SETSTARTSTOPTDM

```
#define STC_RCAT_SETSTARTSTOPTDM(
              SS,
              CAT,
              TDM,
              START,
              STOP )
```

Value:

```
STC_RCAT_SetStartStopTDM(base_ptrs[                    \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi],                    \
    CAT, TDM, START, STOP)
```

Macro to set an STC TDM.

16.31.2.3 STC_RCAT_GETHPR

```
#define STC_RCAT_GETHPR(
              SS,
              CAT )
```

Value:

```
STC_RCAT_GetHPR(base_ptrs[                             \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi], CAT)
```

Macro to get an STC HPR.

16.31.2.4 STC_RCAT_SETHPR

```
#define STC_RCAT_SETHPR(
                SS,
                CAT,
                HPR )
```

Value:

```
STC_RCAT_SetHPR(base_ptrs[sc_ss_info[                   \
    SC_SUBSYS_##SS].db_ssi], CAT, HPR)
```

Macro to set an STC HPR.

16.31.2.5 STC_QOS_PANIC

```
#define STC_QOS_PANIC(
                SS,
                CAT,
                QOS )
```

Value:

```
STC_QOS_Panic(base_ptrs[                                \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi],                     \
    CAT, QOS)
```

Macro to set an STC QoS panic.

16.31.2.6 STC_UD_THRESHOLD1

```
#define STC_UD_THRESHOLD1(
                SS,
                CAT,
                TH,
                QOS )
```

Value:

```
STC_UD_EnableThreshold1(base_ptrs[                      \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi],                     \
    CAT, TH, QOS)
```

Macro to set an STC threshold.

16.31.2.7 STC_UD_THRESHOLD2

```
#define STC_UD_THRESHOLD2(
                SS,
                CAT,
```

```
                TH,
                QOS )
```

Value:

```
STC_UD_EnableThreshold2(base_ptrs[                      \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi],                     \
    CAT, TH, QOS)
```

Macro to set an STC threshold 2.

16.31.2.8 STC_UD_DIS

```
#define STC_UD_DIS(
                SS )
```

Value:

```
STC_UD_DisableAll(base_ptrs[                            \
    sc_ss_info[SC_SUBSYS_##SS].db_ssi])
```

Macro to disable an STC underrun detect.

16.31.3 Function Documentation

16.31.3.1 soc_init_common()

```
void soc_init_common (
              boot_phase_t phase )
```

This function initalizes the parts of the SoC.

Parameters

in	*phase*	flag indicating phase

16.31.3.2 soc_init()

```
void soc_init (
              boot_phase_t phase )
```

This function initalizes the SoC specific parts of the chip.

Parameters

in	*phase*	flag indicating phase

16.31.3.3 soc_config_sc()

```
void soc_config_sc (
            sc_rm_pt_t pt_sc,
            sc_rm_pt_t pt_boot )
```

This function configures SCU resources.

Parameters

in	*pt_sc*	SCU partition
in	*pt_boot*	boot partition

16.31.3.4 soc_ss_notavail()

```
void soc_ss_notavail (
            sc_sub_t ss )
```

This function configures a subsystem as not available.

Parameters

in	*ss*	subsystem not available

16.31.3.5 soc_set_reset_info()

```
void soc_set_reset_info (
            sc_pm_reset_reason_t reason,
            sc_rm_pt_t pt )
```

This function saves reset info into persistant storage.

Parameters

in	*reason*	reason for reset
in	*pt*	partition that caused reset

Examples

board.c.

16.31.3.6 soc_rsrc_avail()

```
sc_bool_t soc_rsrc_avail (
            sc_rsrc_t rsrc )
```

This function returns if a resource is available.

Parameters

in	*rsrc*	resource to check

Returns

Returns SC_TRUE if the resource is available.

16.31.3.7 soc_get_temp_trim()

```
uint32_t soc_get_temp_trim (
            sc_dsc_t dsc )
```

This function returns the trim value for a temp sensor.

Parameters

in	*dsc*	DSC to check

Returns

Returns trim value.

16.31.3.8 soc_get_temp_ofs()

```
int8_t soc_get_temp_ofs (
            sc_dsc_t dsc )
```

This function returns the offset value for a temp sensor.

Parameters

in	*dsc*	DSC to check

Returns

Returns the offset value.

16.31.3.9 soc_get_max_freq()

```
uint32_t soc_get_max_freq (
            sc_dsc_t dsc_id )
```

This function returns the maximum frequency limited by the fuses for the GPU and AP cores.

Parameters

in	*dsc_id*	DSC to check

Returns

Returns the maximum frequency limited by fuse

16.31.3.10 soc_enet_get_freq_limit()

```
sc_bool_t soc_enet_get_freq_limit (
            sc_rsrc_t enet_rsrc )
```

This function checks if the frequency is limited by fuse.

Parameters

in	*enet_rsrc*	ethernet resource to check

Returns

SC_TRUE is frequency is limited

16.31.3.11 soc_pd_switchable()

```
sc_bool_t soc_pd_switchable (
            sc_dsc_t dsc,
            uint32_t pd )
```

This function identifies if the given pd has internal or external switches.

Parameters

in	*dsc*	DSC to affect
in	*pd*	pd to affect

Returns

Returns SC_TRUE if the pd is internally switched, SC_FALSE if externally switched.

16.31.3.12 soc_pd_retention()

```
sc_bool_t soc_pd_retention (
            sc_dsc_t dsc,
            uint32_t pd )
```

This function checks if the given power domain of the given dsc supports retention.

Parameters

in	*dsc*	DSC to affect
in	*pd*	pd to affect

Returns

Returns SC_TRUE if the pd supports retention

16.31.3.13 soc_ss_has_bias()

```
sc_bool_t soc_ss_has_bias (
            sc_sub_t ss )
```

This function checks if the given subsystem has forward body-bias.

Parameters

in	*ss*	subsystem to affect

Returns

Returns SC_TRUE if the pd supports forward body-bias

16.31.3.14 soc_ss_ai_type()

```
dsc_ai_type_t soc_ss_ai_type (
            sc_sub_t ss )
```

This function returns the subsystem AI type, mainly used to identify if an SS has temp sensor.

Parameters

in	*ss*	subsystem to check

Returns

Type of Analog Interface in the SS

16.31.3.15 soc_mem_type()

```
uint32_t soc_mem_type (
            sc_dsc_t dsc,
            uint32_t pd )
```

Return the type of memory used in the given PD of the DSC.

Parameters

in	*dsc*	DSC to affect
in	*pd*	pd to affect

Returns

Type of memory (ESilicon or Normal) used in the SS

16.31.3.16 soc_mem_pwr_plane()

```
uint8_t soc_mem_pwr_plane (
            sc_dsc_t dsc_id )
```

This function returns the uniquely defined memory power plane for the given dsc id.

Parameters

in	*dsc_id*	DSC to check

Returns

memory plane for the dsc_id

16.31.3.17 soc_dsc_clock_info()

```
void soc_dsc_clock_info (
            dsc_clk_type_t * clk_type,
            uint32_t * idx,
            sc_pm_clk_parent_t * parent )
```

Return the DSCMIX clock slice index and type.

Parameters

out	*clk_type*	DSC clock slice type
out	*idx*	DSC clock slice index
out	*parent*	DSC clock slice parent

16.31.3.18 soc_get_clock_div()

```
uint32_t soc_get_clock_div (
            sc_dsc_t dsc,
            uint8_t * pll_div )
```

Return the DSCMIX clock slice divider and pll-divided output connected to all the slices in the dsc.

Parameters

in	*dsc*	DSC to affect
out	*pll_div*	Pll divided output

Returns

DSCMIX clock slice divider

16.31.3.19 soc_slice_is_dsc()

```
sc_bool_t soc_slice_is_dsc (
            const dsc_clk_info_t * clk_info )
```

Checks if the given clock slice is the DSCMIX slice.

Parameters

in	*clk_info*	pointer to the clock data structure

Returns

SC_TRUE if the slice is a DSCMIX slice

16.31.3.20 soc_get_avpll_ssc_n()

```
uint8_t soc_get_avpll_ssc_n (
            sc_dsc_t dsc,
            uint8_t pll_index )
```

This function returns spread spectrum info required to setup the AVPLL.

Parameters

in	*dsc*	dsc to affect
in	*pll_index*	PLL index to affect

Returns

Spread spectrum PPM for the PLL

16.31.3.21 soc_gpu_freq_hw_limited()

```
sc_bool_t soc_gpu_freq_hw_limited (
            void  )
```

This function checks if the GPU frequency is HW limited based on fuses.

Returns

SC_TRUE if the frequency is HW limited

16.31.3.22 soc_rompatch_checksum()

```
void soc_rompatch_checksum (
            uint32_t * checksum,
            uint16_t len )
```

Calculate and return the ROM patch checksum.

Parameters

out	*checksum*	pointer to return checksum
in	*len*	length of fuse area to sum

16.31.3.23 soc_dsc_powerup_anamix()

```
void soc_dsc_powerup_anamix (
            sc_dsc_t dsc )
```

This function powers up the DSC anamix.

Parameters

in	*dsc*	DSC to affect

16.31.3.24 soc_dsc_powerup_phymix()

```
void soc_dsc_powerup_phymix (
            sc_dsc_t dsc )
```

This function powers up the DSC phymix.

Parameters

in	*dsc*	DSC to affect

16.31.3.25 soc_dsc_powerdown_anamix()

```
void soc_dsc_powerdown_anamix (
            sc_dsc_t dsc )
```

This function powers down the DSC anamix.

Parameters

in	*dsc*	DSC to affect

16.31.3.26 soc_dsc_powerdown_phymix()

```
void soc_dsc_powerdown_phymix (
            sc_dsc_t dsc )
```

This function powers down the DSC phymix.

Parameters

in	*dsc*	DSC to affect

16.31.3.27 soc_setup_hsio_repeater()

```
void soc_setup_hsio_repeater (
            board_parm_rtn_t internal_clk,
            sc_bool_t enable )
```

Setup HSIO repeaters for internal or external PCIE clock.

Parameters

in	*internal_clk*	SC_TRUE if using internal clock
in	*enable*	SC_TRUE if powering up SS

16.31.3.28 soc_set_bias()

```
void soc_set_bias (
            sc_sub_t ss,
            uint8_t bias_mask,
            sc_bool_t enable,
            uint32_t delay )
```

Setup the Forward body-bias for the given subsystem.

Parameters

in	*ss*	Subsystem to affect
in	*bias_mask*	IP within SS to enable/disable
in	*enable*	SC_TRUE if enabling forward body-bias
in	*delay*	time to wait when disabling forward body-bias

16.31.3.29 soc_dpll_dco_pc()

```
uint32_t soc_dpll_dco_pc (
            sc_dsc_t dsc,
            uint8_t pll_index,
            uint32_t rate )
```

Return the DPLL DCO-P trim value.

Parameters

in	*dsc*	Subsystem to affect
in	*pll_index*	PLL index within the SS
in	*rate*	PLL lock rate

Returns

DCO-PC trim value (default if fuse is 0)

16.31.3.30 soc_set_freq_voltage()

```
sc_err_t soc_set_freq_voltage (
            sc_sub_t ss,
            uint32_t old_freq,
            uint32_t * new_freq,
            sc_bool_t pmic_change )
```

Set the voltage based on the frequency for SS controlled by PMIC rail.

Parameters

in	*ss*	Subsystem to affect
in	*old_freq*	Freq associated with current voltage
in	*new_freq*	Freq associated with new voltage
in	*pmic_change*	SC_TRUE is pmic voltage should be changed

Returns

SC_ERR_NONE on successful voltage change else error code

16.31.3.31 soc_trans_pd()

```
void soc_trans_pd (
            sc_sub_t ss,
```

```
            uint8_t pd,
            sc_pm_power_mode_t from_mode,
            sc_pm_power_mode_t to_mode )
```

Handle SoC and board level power transitions required to power up or down a power domain.

Parameters

in	*ss*	Subsytem to affect
in	*pd*	Power domain within the SS transitioning
in	*from_mode*	Current power mode of the pd
in	*to_mode*	New power mode of the pd

16.31.3.32 soc_bias_enabled()

```
sc_bool_t soc_bias_enabled (
            sc_sub_t ss )
```

Check if the Forward body bias is enabled for the cluster, this function is only valid for the AP clusters.

Parameters

in	*ss*	Subsystem to affect

Returns

SC_TRUE if forward body-bias is enabled.

16.31.3.33 soc_ss_has_vd_detect()

```
sc_bool_t soc_ss_has_vd_detect (
            sc_dsc_t dsc,
            sc_pm_clock_rate_t rate )
```

Check if the new PLL rate is below the max freq vd-detect in the SS can support.

Parameters

in	*dsc*	DSC of subsystem to affect
in	*rate*	New pll rate

Returns

SC_TRUE if new pll rate is below the max vd-detect frequency

16.31.3.34 soc_trans_bandgap()

```
void soc_trans_bandgap (
            sc_sub_t ss,
            sc_rsrc_t rsrc_idx,
            sc_pm_power_mode_t from_mode,
            sc_pm_power_mode_t to_mode )
```

Transition internal SOC level bandgap.

Parameters

in	*ss*	Subsystem to affect
in	*rsrc_idx*	Resource to affect
in	*from_mode*	Current power mode of the resource
in	*to_mode*	New power mode of the resource.

16.31.3.35 soc_init_ddr()

```
sc_err_t soc_init_ddr (
            sc_bool_t early )
```

This function initalizes DDR.

Parameters

in	*early*	boolean for early init

Returns

Returns the sc_err_t.

16.31.3.36 soc_ddr_config_retention()

```
void soc_ddr_config_retention (
            soc_ddr_ret_info_t * ddr_ret_info )
```

This function configures parameters for DDR low-power retention (SRPD with DRC powered down).

Parameters

in	*ddr_ret_info*	pointer to retention info struct

Examples

board.c.

16.31.3.37 soc_ddr_dqs2dq_config()

```
void soc_ddr_dqs2dq_config (
            soc_dqs2dq_sync_info_t * dqs2dq_sync_info )
```

This function configures parameters of LPDDR4 DQS2DQ periodic training.

Parameters

in	*dqs2dq_sync_info*	pointer to DQS2DQ info struct

Examples

board.c.

16.31.3.38 soc_ddr_dqs2dq_sync()

```
void soc_ddr_dqs2dq_sync (
            void  )
```

This function sychronizes LPDDR4 DQS2DQ periodic training to DDR traffic events (i.e.

ISI frame completion).

16.31.3.39 soc_temp_sensor_tick()

```
void soc_temp_sensor_tick (
            uint16_t msec )
```

This function ticks the temp sensor processing.

Parameters

in	*msec*	milliseconds that have expired

16.31.3.40 soc_dsc_ai_dumpmodule()

```
void soc_dsc_ai_dumpmodule (
            sc_dsc_t dsc,
            uint8_t tog,
            sc_ai_t ai )
```

Dumps registers of single analog module.

Parameters

in	*dsc*	DSC to dump
in	*tog*	toggle to dump
in	*ai*	AI type

16.31.3.41 soc_dsc_ai_dump()

```
void soc_dsc_ai_dump (
            sc_dsc_t dsc )
```

Dumps registers of analog modules in a subsystem.

Parameters

in	*dsc*	DSC to dump

16.31.3.42 soc_anamix_test_out()

```
void soc_anamix_test_out (
            sc_dsc_t dsc )
```

Allows for muxing out analog clocks and voltage levels.

Parameters

in	*dsc*	DSC to affect

16.31.4 Variable Documentation

16.31.4.1 soc_hmp

```
soc_hmp_t soc_hmp
```

Global variable to hold the SCU standalone repeater trim.

Global variable to hold the VPU standalone repeater1 trim.

Global variable to hold the VPU standalone repeater2 trim.

16.32 INF: Subsystem Interface

Module for common subsystem access.

Data Structures

- struct sc_rsrc_map_t

  This type is used store static constant info to map resources to the containing subsystem.
- struct ss_rsrc_info_t

  This type is used store static constant info about resources in a subsystem.
- struct ss_ctrl_info_t

  This type is used store static constant info about controls in a subsystem.
- struct ss_pd_info_t

  This type is used to store static constant info about the power domains in the subsystem.
- struct ss_xexp_info_t

  This type is used to store static constant info about resources to keep assigned to the SCU or associated with another resource.
- struct ss_mdac_info_t

  This type is used to store static constant info about the MDACs in a subsystem.
- struct ss_msc_info_t

  This type is used to store static constant info about the MSCs in a subsystem.
- struct ss_mrc_info_t

  This type is used to store static constant info about the MRCs in a subsystem.
- struct ss_base_info_t

  This type is used to store static constant info about a subsystem.
- struct ss_clk_data_t

  This type is used to store dynamic data about the clocks/PLLs in the subsystem.
- struct ss_base_data_t

  This type is used to store dynamic data about a subsystem.

Macros

- #define SS_CLK_W 6U

  Width of ss_clock_t.
- #define SS_PLL_W 2U

  Width of ss_pll_t.
- #define SS_IO_W 4U

  Width of ss_io_type_t.
- #define SS_XEXP_W 8U

  Width of ss_xexp_idx_t.
- #define SS_FIELD_POS_W 16U

  Width of I/O field position.
- #define SS_FIELD_WID_W 6U

  Width of I/O field width.
- #define SS_CID_W 4U

  Width of CPU ID.

- #define SS_IDX_W 8U

  Width of SS index.
- #define SS_NUM_SSI_W 2U

  Width of num SSIs.
- #define SS_MAX_CLK 35U

  Max number of clocks per subsystem.
- #define SS_MAX_PLL 3U

  Max number of PLLs per subsystem.
- #define **SS_MAX_PM_CLKS** 5U
- #define NV ((uint8_t) UINT8_MAX)

  Define to indicate invalid power domains and clocks.
- #define RSRC(R, I, X)

  Define to fill in a sc_rsrc_map_t variable.
- #define **SS_I1** 0x8001U
- #define **XNFO_DL** {0U, 0U}
- #define BASE_INFO(XEXP_INFO, MDAC_INFO, PAC_INFO, MSC_INFO, MRC_INFO, CTRL_INFO)

  Define to fill in a ss_base_info_t variable (with XRDC)
- #define RNFO(PWD, C1, C2, C3, C4, C5, M, P, X, MI, PI, MATCHF, MASKF)

  Define to fill in a ss_rsrc_info_t variable (with XRDC)
- #define XNFO(S, N)

  Define to fill in a ss_xexp_info_t variable.
- #define TNFO(R, C, IO, B, W)

  Define to fill in a ss_ctrl_info_t variable.
- #define MNFO(P, ST, EN, AJ, M, I, SL, PWD, SB, C)

  Define to fill in a ss_mrc_info_t variable.

Typedefs

- typedef uint8_t ss_idx_t

  Type for a ss resource index.
- typedef sc_rm_idx_t ss_ridx_t

  Type for a resource index.
- typedef uint8_t ss_clock_t

  Type for a clock index.
- typedef uint8_t ss_pll_t

  Type for a PLL index.
- typedef uint8_t ss_xexp_idx_t

  Type for an XRDC expansion info index.
- typedef xrdc_pac_info_t ss_pac_info_t

  This type is used to store static constant info about the PACs in a subsystem.
- typedef sc_bool_t(* ss_dsc_l2irq_handler) (sc_dsc_t dsc, uint32_t irqIndex)

  Type for IRQ handler.

Enumerations

- enum ss_prepost_t { SS_PREAMBLE, SS_POSTAMBLE }

  This type is used to indicate pre- or post-amble function calls.
- enum ss_io_type_t {
  SS_IO_GPR_CTRL, SS_IO_GPR_STAT, SS_IO_CSR, SS_IO_CSR2,
  SS_IO_CSR3, SS_IO_AI_RW, SS_IO_AI_RO, SS_IO_RST_CTRL,
  SS_IO_BRD_CTRL, SS_IO_SW_CTRL }

  This type is used to indicate type of DSC I/O.

Variables

- const sc_ss_ep_t **sc_ss_ep** [SC_SUBSYS_LAST+1U]
- ss_base_data_t **sc_ss_data** [SC_SUBSYS_LAST+1U]

Interface Functions

- void ss_init (sc_sub_t ss, sc_bool_t api_phase)

  This function initalizes a subsystem.
- void ss_trans_power_mode (ss_ridx_t rsrc_idx, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to↩
  _mode)

  This function transitions a resource from one power mode to another.
- sc_err_t ss_rsrc_reset (ss_ridx_t rsrc_idx, sc_rm_pt_t pt, sc_bool_t pre)

  This function requests a resource be reset.
- sc_err_t ss_set_cpu_power_mode (ss_ridx_t rsrc_idx, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake↩
  _src)

  This function requests the power power mode to be entered for some resources under certain circumstances.
- sc_err_t ss_set_cpu_resume (ss_ridx_t rsrc_idx, sc_bool_t isPrimary, sc_faddr_t addr)

  This function sets the resume address of a CPU.
- sc_err_t ss_req_sys_if_power_mode (ss_ridx_t rsrc_idx, sc_pm_sys_if_t sys_if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)

  This function requests the power mode for system-level interfaces including messaging units, interconnect, and memories.
- sc_err_t ss_set_clock_rate (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  This function sets a clock rate.
- sc_err_t ss_get_clock_rate (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  This function gets a clock rate.
- sc_err_t ss_clock_enable (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_bool_t enable, sc_bool_t autog)

  This function enables a clock.
- sc_err_t ss_force_clock_enable (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_bool_t enable)

  This function enables a clock.
- sc_err_t ss_set_clock_parent (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clk_parent_t new_parent)

  This function sets the parent of a resource's clock.
- sc_err_t ss_get_clock_parent (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clk_parent_t *parent)

  This function gets the parent of a resource's clock.
- sc_bool_t ss_is_rsrc_accessible (ss_ridx_t rsrc_idx)

  This function returns the functional state of a resource.
- void ss_mu_irq (ss_ridx_t rsrc_idx, uint32_t mask)

This function triggers an interrupt on an MU.

- sc_err_t ss_cpu_start (ss_ridx_t rsrc_idx, sc_bool_t enable, sc_faddr_t addr)

  This function starts or stops a subsystem CPU.
- void ss_rdc_enable (sc_sub_t ss, sc_bool_t master)

  This function enables the subsystem hardware resource manager.
- void ss_rdc_set_master (ss_ridx_t rsrc_idx, sc_bool_t valid, sc_bool_t lock, sc_rm_spa_t sa, sc_rm_spa_t pa, sc_rm_did_t did, sc_rm_sid_t sid, uint8_t cid)

  This function configures a subsystem master.
- void ss_rdc_set_peripheral (ss_ridx_t rsrc_idx, sc_bool_t valid, sc_bool_t lock, const sc_rm_perm_t *perms, sc_bool_t no_update)

  This function configures a subsystem peripheral.
- sc_err_t ss_rdc_set_memory (sc_faddr_t start, sc_faddr_t end, sc_bool_t valid, const sc_rm_perm_t *perms, sc_rm_det_t det, sc_rm_rmsg_t rmsg, sc_faddr_t new_start, sc_faddr_t new_end)

  This function configures a memory region.
- sc_err_t ss_set_control (ss_ridx_t rsrc_idx, uint32_t ctrl, uint32_t val)

  This function sets a miscellaneous control value.
- sc_err_t ss_get_control (ss_ridx_t rsrc_idx, uint32_t ctrl, uint32_t *val)

  This function gets a miscellaneous control value.
- sc_err_t ss_irq_enable (ss_ridx_t rsrc_idx, sc_irq_group_t group, uint32_t mask, sc_bool_t enable)

  This function enables/disables interrupts.
- sc_err_t ss_irq_status (ss_ridx_t rsrc_idx, sc_irq_group_t group, uint32_t *status)

  This function returns the current interrupt status.
- void ss_irq_trigger (sc_irq_group_t group, uint32_t irq, sc_rm_pt_t pt)

  This function triggers an interrupt.
- void ss_dump (sc_sub_t ss, sc_bool_t xrdc, sc_bool_t dsc, sc_bool_t clk)

  This function dumps the state of a subsystem.

Helper Functions

- void ss_do_mem_repair (sc_sub_t ss, dsc_pdom_t pd, sc_bool_t enable)

  This function runs manual memory repair on a subsystem.
- void ss_updown (sc_sub_t ss, sc_bool_t up)

  This function is used to configure SS features after a SS is fully powered up (SSI link enabled) or before powering down.
- void ss_prepost_power_mode (sc_sub_t ss, dsc_pdom_t pd, ss_prepost_t type, sc_pm_power_mode_t from_↩ mode, sc_pm_power_mode_t to_mode, sc_bool_t rom_boot)

  This function is a pre- and post-amble for power domain power mode transitions.
- void ss_iso_disable (sc_sub_t ss, dsc_pdom_t pd, sc_bool_t enable)

  This function enables/disables the isolation in a subsystem.
- void ss_link_enable (sc_sub_t ss, dsc_pdom_t pd, sc_bool_t enable)

  This function enables/disables the interfaces in a subsystem.
- void ss_ssi_power (sc_sub_t ss, sc_bool_t enable)

  This function enables/disables a subsystems's SSI ports.
- void ss_ssi_bhole_mode (sc_sub_t ss, sc_sub_t remote, uint8_t port, sc_bool_t enable)

  This function enables/disables black hole mode of an SSI.
- void ss_ssi_pause_mode (sc_sub_t ss, sc_sub_t remote, uint8_t port, sc_bool_t enable)

  This function enables/disables pause mode of an SSI.
- void ss_ssi_wait_idle (sc_sub_t ss, sc_sub_t remote, uint8_t port)

This function waits for an SSI to become idle.

- void ss_adb_enable (sc_sub_t ss, sc_sub_t remote, sc_bool_t enable)

  This function setups an ADB interface between two ss.
- void ss_adb_wait (sc_sub_t ss, sc_sub_t remote, sc_bool_t enable)

  This function waits for the ADB to be powered up.
- void ss_prepost_clock_mode (sc_sub_t ss, ss_clock_t clk, ss_prepost_t type, sc_pm_clk_mode_t from_mode, sc_pm_clk_mode_t to_mode)

  This function is a pre- and post-amble for clock mode transitions.
- sc_bool_t ss_rdc_is_did_vld (sc_sub_t ss, const sc_rm_perm_t *perms)

  This function checks if a subsystem generates transactions matching domains.
- sc_rsrc_t ss_get_resource (sc_sub_t ss, ss_idx_t ss_idx)

  This function returns a system-wide resource from a subsystem and subsystem relative resource index.
- sc_bool_t ss_overlap (sc_faddr_t start1, sc_faddr_t end1, sc_faddr_t start2, sc_faddr_t end2)

  This function determines if two memory regions overlap.
- sc_bool_t ss_temp_sensor (ss_ridx_t rsrc_idx)

  This function gets temp sensor availability of a subsystem.

16.32.1 Detailed Description

Module for common subsystem access.

16.32.2 Macro Definition Documentation

16.32.2.1 RSRC

```
#define RSRC(
               R,
               I,
               X )
```

Value:

```
{                                   \
    .resource = U16(SC_R_##R),      \
    .inst = U8(I),                  \
    .ss_idx = U8(X)                 \
}
```

Define to fill in a sc_rsrc_map_t variable.

Examples

board.c.

16.32.2.2 BASE_INFO

```
#define BASE_INFO(
                XEXP_INFO,
                MDAC_INFO,
                PAC_INFO,
                MSC_INFO,
                MRC_INFO,
                CTRL_INFO )
```

Value:

```
.num_rsrc = SS_NUM_RSRC,            \
        .num_srsrc = SS_NUM_SRSRC,          \
        .num_prsrc = SS_NUM_PRSRC,          \
        .rsrc = ss_rsrc_info,               \
        .rsrc_map = rsrc_map,               \
        .num_pd = SS_NUM_PD,                \
        .pd_info = ss_pd_info,              \
        .pd_reboot_info = SS_PD_REBOOT_INFO,\
        .num_ctrl = SS_NUM_CTRL,            \
        .ctrl_info = (CTRL_INFO),           \
        .dsc_aon_reset_mask = SS_AON_RESET, \
        .irq_enb = SS_IRQ_ENB,              \
        .pd_dsc = SS_PD_DSC,                \
        .pd_ssi = SS_PD_SSI,                \
        .num_clks = SS_NUM_CLK,             \
        .clk_info = ss_clk_info,            \
        .ss_iso_info = ss_iso_info,         \
        .num_pll = SS_NUM_PLL,              \
        .mu_irq = SS_MU_IRQ,                \
        .dscmix = SS_DSCMIX,                \
        .ai_type = SS_AI_TYPE,              \
        .ss_phy_iso = SS_PHY_ISO,           \
        .ss_num_ssi = SS_NUM_SSI,           \
        .mtr_clk_idx = MTR_CLK_IDX,         \
        .pd_mgr = SS_PD_MGR,                \
        .xexp_info = (XEXP_INFO),           \
        .num_mdac = SS_NUM_MDAC,            \
        .mdac_info = (MDAC_INFO),           \
        .mdac_match = SS_MDAC_MATCH,        \
        .mdac_cache = SS_MDAC_CACHE,        \
        .num_pac = SS_NUM_PAC,              \
        .pac_info = (PAC_INFO),             \
        .num_msc = SS_NUM_MSC,              \
        .msc_info = (MSC_INFO),             \
        .num_mrc = SS_NUM_MRC,              \
        .mrc_info = (MRC_INFO),             \
        .mrc_mask = SS_MRC_MASK,            \
        .mrc_cache = SS_MRC_CACHE
```

Define to fill in a ss_base_info_t variable (with XRDC)

16.32.2.3 RNFO

```
#define RNFO(
                PWD,
                C1,
                C2,
                C3,
                C4,
                C5,
                M,
                P,
                X,
```

```
                MI,
                PI,
                MATCHF,
                MASKF )
```

Value:

```
{                                                   \
        .master = U2B(M),                           \
        .peripheral = U2B(P),                       \
        .pd = U8(PWD),                              \
        .clk = {U8(C1), U8(C2), U8(C3), U8(C4), U8(C5)}, \
        .xexp_idx = U8(X),                          \
        .xrdc_master_idx = U16(MI),                 \
        .xrdc_peripheral_idx = U16(PI),             \
        .xrdc_mda_match = U16(MATCHF),              \
        .xrdc_mda_mask = U16(MASKF)                 \
    }
```

Define to fill in a ss_rsrc_info_t variable (with XRDC)

Examples

board.c.

16.32.2.4 XNFO

```
#define XNFO(
                S,
                N )
```

Value:

```
{                       \
    .start = U16(S),    \
    .num = U8(N),       \
}
```

Define to fill in a ss_xexp_info_t variable.

16.32.2.5 TNFO

```
#define TNFO(
                R,
                C,
                IO,
                B,
                W )
```

Value:

```
{                               \
    .ss_idx = U8(SS_R_##R),     \
    .ctrl = U8(SC_C_##C),       \
    .io = (SS_IO_##IO),         \
    .bit = U16(B),              \
    .width = U8(W)              \
}
```

Define to fill in a ss_ctrl_info_t variable.

Examples

board.c.

16.32.2.6 MNFO

```
#define MNFO(
               P,
               ST,
               EN,
               AJ,
               M,
               I,
               SL,
               PWD,
               SB,
               C )
```

Value:

```
{                                   \
    .present = U2B(P),              \
    .start = U64(ST),               \
    .end = U64(EN),                 \
    .adjust = U64(AJ),              \
    .mrc = U16(M),                  \
    .idx = U16(I),                  \
    .num_slots = U16(SL),           \
    .pd = U8(PWD),                  \
    .sub = U8(SB),                  \
    .cache = (uint32_t*) (C)        \
}
```

Define to fill in a ss_mrc_info_t variable.

16.32.3 Enumeration Type Documentation

16.32.3.1 ss_prepost_t

```
enum ss_prepost_t
```

This type is used to indicate pre- or post-amble function calls.

Enumerator

SS_PREAMBLE	Preamble function call.
SS_POSTAMBLE	Postamble function call.

16.32.3.2 ss_io_type_t

```
enum ss_io_type_t
```

This type is used to indicate type of DSC I/O.

Enumerator

SS_IO_GPR_CTRL	GPR Control.
SS_IO_GPR_STAT	GPR Status.
SS_IO_CSR	CSR.
SS_IO_CSR2	CSR2.
SS_IO_CSR3	CSR3.
SS_IO_AI_RW	Analog Interface (RW)
SS_IO_AI_RO	Analog Interface (RO)
SS_IO_RST_CTRL	Reset control.
SS_IO_BRD_CTRL	Board control.
SS_IO_SW_CTRL	Software control.

16.32.4 Function Documentation

16.32.4.1 ss_init()

```
void ss_init (
            sc_sub_t ss,
            sc_bool_t api_phase )
```

This function initalizes a subsystem.

Parameters

in	*ss*	subsystem to initialize
in	*api_phase*	flag indicating phase

There are two phases to subsystem intialization. The fist phase is the API phase (*api_phase* = SC_TRUE) and initializes all of the subsystem interface data structures. The second phase is the HW phase and this initializes the SS hardware. Both are called from main() only.

16.32.4.2 ss_trans_power_mode()

```
void ss_trans_power_mode (
            ss_ridx_t rsrc_idx,
            sc_pm_power_mode_t from_mode,
            sc_pm_power_mode_t to_mode )
```

This function transitions a resource from one power mode to another.

Parameters

in	*rsrc_idx*	unified resource index
in	*from_mode*	current resource power mode
in	*to_mode*	requested new resource power mode

This function will be dispatched to the subsystem containing *rsrc_idx*. If required, the subsystem power domains will change (dsc, ssi, and that containing *rsrc_idx*).

16.32.4.3 ss_rsrc_reset()

```
sc_err_t ss_rsrc_reset (
             ss_ridx_t rsrc_idx,
             sc_rm_pt_t pt,
             sc_bool_t pre )
```

This function requests a resource be reset.

Parameters

in	*rsrc_idx*	unified resource index
in	*pt*	partition
in	*pre*	pre-power off reset

If pt equals SC_PT_ALL then reset all resources belonging to that partition. Otherwise, reset rsrc_idx only.

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.4 ss_set_cpu_power_mode()

```
sc_err_t ss_set_cpu_power_mode (
             ss_ridx_t rsrc_idx,
             sc_pm_power_mode_t mode,
             sc_pm_wake_src_t wake_src )
```

This function requests the power power mode to be entered for some resources under certain circumstances.

Parameters

in	*rsrc_idx*	unified resource index
in	*mode*	requested low-power mode
in	*wake_src*	low-power mode wake source

Returns

Returns an error code (SC_ERR_NONE = success).

This function will be dispatched to the subsystem containing *rsrc_idx*. If required, the subsystem power domains will change (dsc, ssi, and that containing *rsrc_idx*).

16.32.4.5 ss_set_cpu_resume()

```
sc_err_t ss_set_cpu_resume (
             ss_ridx_t rsrc_idx,
             sc_bool_t isPrimary,
             sc_faddr_t addr )
```

This function sets the resume address of a CPU.

Parameters

in	*rsrc_idx*	unified resource index of CPU
in	*isPrimary*	set SC_TRUE if primary wake CPU
in	*addr*	boot address for CPU

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.6 ss_req_sys_if_power_mode()

```
sc_err_t ss_req_sys_if_power_mode (
             ss_ridx_t rsrc_idx,
             sc_pm_sys_if_t sys_if,
             sc_pm_power_mode_t hpm,
             sc_pm_power_mode_t lpm )
```

This function requests the power mode for system-level interfaces including messaging units, interconnect, and memories.

Parameters

in	*rsrc_idx*	unified resource index
in	*sys_if*	system-level interface to be configured
in	*hpm*	high-power mode for the system interface
in	*lpm*	low-power mode for the system interface

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.7 ss_set_clock_rate()

```
sc_err_t ss_set_clock_rate (
             ss_ridx_t rsrc_idx,
```

```
            sc_pm_clk_t clk,
            sc_pm_clock_rate_t * rate )
```

This function sets a clock rate.

Parameters

in	*rsrc_idx*	unified resource index
in	*clk*	clk to set
in,out	*rate*	pointer to rate to set (Hz)

Returns

Returns an error code (SC_ERR_NONE = success).

Will return actual rate that could be achieved in *rate*.

16.32.4.8 ss_get_clock_rate()

```
sc_err_t ss_get_clock_rate (
            ss_ridx_t rsrc_idx,
            sc_pm_clk_t clk,
            sc_pm_clock_rate_t * rate )
```

This function gets a clock rate.

Parameters

in	*rsrc_idx*	unified resource index
in	*clk*	clk to get
out	*rate*	pointer to return rate (Hz)

Returns

Returns the rate of the clock in Hz.

16.32.4.9 ss_clock_enable()

```
sc_err_t ss_clock_enable (
            ss_ridx_t rsrc_idx,
            sc_pm_clk_t clk,
            sc_bool_t enable,
            sc_bool_t autog )
```

This function enables a clock.

Parameters

in	*rsrc_idx*	unified resource index
in	*clk*	clk to enable/disable
in,out	*enable*	flag indicating state (SC_TRUE = enable)
in,out	*autog*	flag indicating HW autogate mode

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.10 ss_force_clock_enable()

```
sc_err_t ss_force_clock_enable (
             ss_ridx_t rsrc_idx,
             sc_pm_clk_t clk,
             sc_bool_t enable )
```

This function enables a clock.

Parameters

in	*rsrc_idx*	unified resource index
in	*clk*	clk to enable/disable
in,out	*enable*	flag indicating state (SC_TRUE = enable)

Returns

Returns an error code (SC_ERR_NONE = success).

This function forces the clock to the desired state regardless of any other gating input (hardware, etc.).

16.32.4.11 ss_set_clock_parent()

```
sc_err_t ss_set_clock_parent (
             ss_ridx_t rsrc_idx,
             sc_pm_clk_t clk,
             sc_pm_clk_parent_t new_parent )
```

This function sets the parent of a resource's clock.

This function should only be called when the clock is disabled.

Parameters

in	*rsrc_idx*	unified resource index
in	*clk*	clock to affect
in	*new_parent*	New parent of the clock.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_UNAVAILABLE if clock not applicable to this resource
- SC_ERR_BUSY if clock is currently enabled.

Refer to the Clock List for valid clock values.

16.32.4.12 ss_get_clock_parent()

```
sc_err_t ss_get_clock_parent (
             ss_ridx_t rsrc_idx,
             sc_pm_clk_t clk,
             sc_pm_clk_parent_t * parent )
```

This function gets the parent of a resource's clock.

Parameters

in	*rsrc_idx*	unified resource index
in	*clk*	clock to affect
out	*parent*	pointer to return parent of clock.

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_ERR_PARM if invalid resource or clock,
- SC_ERR_NOACCESS if caller's partition is not the resource owner or parent of the owner,
- SC_ERR_UNAVAILABLE if clock not applicable to this resource

Refer to the Clock List for valid clock values.

16.32.4.13 ss_is_rsrc_accessible()

```
sc_bool_t ss_is_rsrc_accessible (
            ss_ridx_t rsrc_idx )
```

This function returns the functional state of a resource.

Parameters

in	*rsrc_idx*	unified resource index

Returns

Returns a boolean (SC_TRUE if resource functional).

This checks to see if the power and clocks for a resource (inc. required bus clocks) are enabled.

16.32.4.14 ss_mu_irq()

```
void ss_mu_irq (
            ss_ridx_t rsrc_idx,
            uint32_t mask )
```

This function triggers an interrupt on an MU.

Parameters

in	*rsrc_idx*	unified resource index of MU
in	*mask*	MU interrupt to trigger

16.32.4.15 ss_cpu_start()

```
sc_err_t ss_cpu_start (
            ss_ridx_t rsrc_idx,
            sc_bool_t enable,
            sc_faddr_t addr )
```

This function starts or stops a subsystem CPU.

Parameters

in	*rsrc_idx*	unified resource index of CPU
in	*enable*	enable/disable flag (SC_TRUE = enable)
in	*addr*	boot address for CPU

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.16 ss_rdc_enable()

```
void ss_rdc_enable (
            sc_sub_t ss,
            sc_bool_t master )
```

This function enables the subsystem hardware resource manager.

Parameters

in	*ss*	subsystem to affect
in	*master*	master only

16.32.4.17 ss_rdc_set_master()

```
void ss_rdc_set_master (
            ss_ridx_t rsrc_idx,
            sc_bool_t valid,
            sc_bool_t lock,
            sc_rm_spa_t sa,
            sc_rm_spa_t pa,
            sc_rm_did_t did,
            sc_rm_sid_t sid,
            uint8_t cid )
```

This function configures a subsystem master.

Parameters

in	*rsrc_idx*	unified resource index of master
in	*valid*	valid flag (SC_TRUE = valid)
in	*lock*	lock flag (SC_TRUE = lock)
in	*sa*	security attribute
in	*pa*	privilege attribute
in	*did*	domain ID
in	*sid*	StreamID
in	*cid*	CPU ID

16.32.4.18 ss_rdc_set_peripheral()

```
void ss_rdc_set_peripheral (
             ss_ridx_t rsrc_idx,
             sc_bool_t valid,
             sc_bool_t lock,
             const sc_rm_perm_t * perms,
             sc_bool_t no_update )
```

This function configures a subsystem peripheral.

Parameters

in	*rsrc_idx*	unified resource index of peripheral
in	*valid*	valid flag (SC_TRUE = valid)
in	*lock*	lock flag (SC_TRUE = lock)
in	*perms*	array of permisions
in	*no_update*	if true, don't update if already valid

16.32.4.19 ss_rdc_set_memory()

```
sc_err_t ss_rdc_set_memory (
             sc_faddr_t start,
             sc_faddr_t end,
             sc_bool_t valid,
             const sc_rm_perm_t * perms,
             sc_rm_det_t det,
             sc_rm_rmsg_t rmsg,
             sc_faddr_t new_start,
             sc_faddr_t new_end )
```

This function configures a memory region.

Parameters

in	*start*	64-bit start address
in	*end*	64-bit end address
in	*valid*	valid flag (SC_TRUE = valid)
in	*perms*	array of permisions
in	*det*	detour transaction to IEE
in	*rmsg*	IEE config
in	*new_start*	new 64-bit start address
in	*new_end*	new 64-bit end address

16.32.4.20 ss_set_control()

```
sc_err_t ss_set_control (
             ss_ridx_t rsrc_idx,
             uint32_t ctrl,
             uint32_t val )
```

This function sets a miscellaneous control value.

Parameters

in	*rsrc_idx*	unified resource index
in	*ctrl*	control to write
in	*val*	value to write

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.21 ss_get_control()

```
sc_err_t ss_get_control (
             ss_ridx_t rsrc_idx,
             uint32_t ctrl,
             uint32_t * val )
```

This function gets a miscellaneous control value.

Parameters

in	*rsrc_idx*	unified resource index
in	*ctrl*	control to read
out	*val*	pointer to return value

Returns

Returns an error code (SC_ERR_NONE = success).

16.32.4.22 ss_irq_enable()

```
sc_err_t ss_irq_enable (
             ss_ridx_t rsrc_idx,
             sc_irq_group_t group,
```

```
            uint32_t mask,
            sc_bool_t enable )
```

This function enables/disables interrupts.

Parameters

in	*rsrc_idx*	unified resource index
in	*group*	group the interrupts are in
in	*mask*	mask of interrupts to affect
in	*enable*	state to change interrupts to

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if group invalid

16.32.4.23 ss_irq_status()

```
sc_err_t ss_irq_status (
            ss_ridx_t rsrc_idx,
            sc_irq_group_t group,
            uint32_t * status )
```

This function returns the current interrupt status.

Automatically clears pending interrupts.

Parameters

in	*rsrc_idx*	unified resource index
in	*group*	groups the interrupts are in
in	*status*	status of interrupts

Returns

Returns an error code (SC_ERR_NONE = success).

Return errors:

- SC_PARM if group invalid

16.32.4.24 ss_irq_trigger()

```
void ss_irq_trigger (
            sc_irq_group_t group,
            uint32_t irq,
            sc_rm_pt_t pt )
```

This function triggers an interrupt.

Parameters

in	*group*	group the interrupt is in
in	*irq*	interrupt to trigger
in	*pt*	partition to trigger

This function results in an interrupt being triggered on all SCFW MUs owned by the specified partition that have the interrupt enabled. Use SC_PT_ALL to trigger for all partitions.

See the RPC protocol section for more information.

Examples

board.c.

16.32.4.25 ss_do_mem_repair()

```
void ss_do_mem_repair (
            sc_sub_t ss,
            dsc_pdom_t pd,
            sc_bool_t enable )
```

This function runs manual memory repair on a subsystem.

Parameters

in	*ss*	subsystem to repair
in	*pd*	power domain to repair
in	*enable*	reset state of MTR HW

This function does memory repair manually to work around HW issues.

16.32.4.26 ss_updown()

```
void ss_updown (
            sc_sub_t ss,
            sc_bool_t up )
```

This function is used to configure SS features after a SS is fully powered up (SSI link enabled) or before powering down.

Parameters

in	*ss*	subsystem transitioning
in	*up*	SC_TRUE if powered up, SC_FALSE if powering down

This function is used to customize subsystem power transitions. It can be used to control the subsystem or wait for subsystem status before/after power mode transitions.

16.32.4.27 ss_prepost_power_mode()

```
void ss_prepost_power_mode (
            sc_sub_t ss,
            dsc_pdom_t pd,
            ss_prepost_t type,
            sc_pm_power_mode_t from_mode,
            sc_pm_power_mode_t to_mode,
            sc_bool_t rom_boot )
```

This function is a pre- and post-amble for power domain power mode transitions.

Parameters

in	*ss*	subsystem transitioning
in	*pd*	power domain transitioning
in	*type*	type of notification
in	*from_mode*	current power domain mode
in	*to_mode*	new power domain mode
in	*rom_boot*	SC_TRUE if ROM has powered up SS

This function is used to customize subsystem power transitions. It can be used to control the subsystem or wait for subsystem status before/after power mode transitions.

16.32.4.28 ss_iso_disable()

```
void ss_iso_disable (
            sc_sub_t ss,
            dsc_pdom_t pd,
            sc_bool_t enable )
```

This function enables/disables the isolation in a subsystem.

Parameters

in	*ss*	subsystem to affect
in	*pd*	power domain to affect
in	*enable*	flag indicating new state (SC_TRUE = enable)

16.32.4.29 ss_link_enable()

```
void ss_link_enable (
            sc_sub_t ss,
            dsc_pdom_t pd,
            sc_bool_t enable )
```

This function enables/disables the interfaces in a subsystem.

Parameters

in	*ss*	subsystem to affect
in	*pd*	power domain to affect
in	*enable*	flag indicating new state (SC_TRUE = enable)

16.32.4.30 ss_ssi_power()

```
void ss_ssi_power (
            sc_sub_t ss,
            sc_bool_t enable )
```

This function enables/disables a subsystems's SSI ports.

Parameters

in	*ss*	subsystem to affect
in	*enable*	flag indicating new state (SC_TRUE = on)

16.32.4.31 ss_ssi_bhole_mode()

```
void ss_ssi_bhole_mode (
            sc_sub_t ss,
            sc_sub_t remote,
            uint8_t port,
            sc_bool_t enable )
```

This function enables/disables black hole mode of an SSI.

Parameters

in	*ss*	subsystem to affect
in	*remote*	affect SSI to this subsystem
in	*port*	affect this instance of the SSI
in	*enable*	flag indicating new state (SC_TRUE = enable)

16.32.4.32 ss_ssi_pause_mode()

```
void ss_ssi_pause_mode (
            sc_sub_t ss,
            sc_sub_t remote,
            uint8_t port,
            sc_bool_t enable )
```

This function enables/disables pause mode of an SSI.

Parameters

in	*ss*	subsystem to affect
in	*remote*	affect SSI to this subsystem
in	*port*	affect this instance of the SSI
in	*enable*	flag indicating new state (SC_TRUE = enable)

16.32.4.33 ss_ssi_wait_idle()

```
void ss_ssi_wait_idle (
            sc_sub_t ss,
            sc_sub_t remote,
            uint8_t port )
```

This function waits for an SSI to become idle.

Parameters

in	*ss*	subsystem to affect
in	*remote*	affect SSI to this subsystem
in	*port*	affect this instance of the SSI

16.32.4.34 ss_adb_enable()

```
void ss_adb_enable (
            sc_sub_t ss,
            sc_sub_t remote,
            sc_bool_t enable )
```

This function setups an ADB interface between two ss.

Parameters

in	*ss*	local subsystem
in	*remote*	remote subsystem
in	*enable*	powerup/powerdown the ADB link

16.32.4.35 ss_adb_wait()

```
void ss_adb_wait (
            sc_sub_t ss,
            sc_sub_t remote,
            sc_bool_t enable )
```

This function waits for the ADB to be powered up.

Parameters

in	*ss*	local subsystem
in	*remote*	remote subsystem
in	*enable*	powerup/powerdown the ADB link

16.32.4.36 ss_prepost_clock_mode()

```
void ss_prepost_clock_mode (
            sc_sub_t ss,
            ss_clock_t clk,
            ss_prepost_t type,
            sc_pm_clk_mode_t from_mode,
            sc_pm_clk_mode_t to_mode )
```

This function is a pre- and post-amble for clock mode transitions.

Parameters

in	*ss*	subsystem transitioning
in	*clk*	clock transitioning
in	*type*	type of notification
in	*from_mode*	current clock mode
in	*to_mode*	new clock mode

This function is used to customize subsystem clock transitions. It can be used to control the subsystem or wait for subsystem status before/after clock transitions.

16.32.4.37 ss_rdc_is_did_vld()

```
sc_bool_t ss_rdc_is_did_vld (
            sc_sub_t ss,
            const sc_rm_perm_t * perms )
```

This function checks if a subsystem generates transactions matching domains.

Parameters

in	*ss*	subsystem to check
in	*perms*	array of permisions

Returns

Returns SC_TRUE if the subsystem has masters in domains which have access in *perms*.

16.32.4.38 ss_get_resource()

```
sc_rsrc_t ss_get_resource (
            sc_sub_t ss,
            ss_idx_t ss_idx )
```

This function returns a system-wide resource from a subsystem and subsystem relative resource index.

Parameters

in	*ss*	subsystem containing resource
in	*ss_idx*	subsystem index of resource

Returns

Returns the system-wide resource.

16.32.4.39 ss_overlap()

```
sc_bool_t ss_overlap (
            sc_faddr_t start1,
            sc_faddr_t end1,
            sc_faddr_t start2,
            sc_faddr_t end2 )
```

This function determines if two memory regions overlap.

Parameters

in	*start1*	start address for region 1
in	*end1*	end address for region 1
in	*start2*	start address for region 2
in	*end2*	end address for region 2

Returns

Returns SC_TRUE if the memory regions overlap.

16.32.4.40 ss_temp_sensor()

```
sc_bool_t ss_temp_sensor (
            ss_ridx_t rsrc_idx )
```

This function gets temp sensor availability of a subsystem.

Parameters

in	*rsrc_idx*	any resource in the subsystem

Returns

Returns SC_TRUE if the associated subsystem has a temp sensor.

16.33 PCA6416A: PCA6416A Driver

Functions

- status_t PCA6416A_WritePinDirection (uint8_t device_addr, uint8_t port, uint8_t dir)

  This function writes the pin direction regsiter.
- status_t PCA6416A_ReadPinDirection (uint8_t device_addr, uint8_t port, uint8_t ∗dir)

  This function reads the pin direction regsiter.
- status_t PCA6416A_WritePinPolarity (uint8_t device_addr, uint8_t port, uint8_t pol)

  This function writes the pin polarity regsiter.
- status_t PCA6416A_ReadPinPolarity (uint8_t device_addr, uint8_t port, uint8_t ∗pol)

  This function reads the pin polarity regsiter.
- status_t PCA6416A_WritePinOutput (uint8_t device_addr, uint8_t port, uint8_t out)

  This function writes the pin output regsiter.
- status_t PCA6416A_ReadPinOutput (uint8_t device_addr, uint8_t port, uint8_t ∗out)

  This function reads the pin output regsiter.
- status_t PCA6416A_ReadPinInput (uint8_t device_addr, uint8_t port, uint8_t ∗in)

  This function reads the pin input regsiter.

16.33.1 Detailed Description

16.33.2 Function Documentation

16.33.2.1 PCA6416A_WritePinDirection()

```
status_t PCA6416A_WritePinDirection (
            uint8_t device_addr,
            uint8_t port,
            uint8_t dir )
```

This function writes the pin direction regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
in	*dir*	direction (0=output, 1=input)

Returns

Returns the I2C status.

16.33.2.2 PCA6416A_ReadPinDirection()

```
status_t PCA6416A_ReadPinDirection (
            uint8_t device_addr,
            uint8_t port,
            uint8_t * dir )
```

This function reads the pin direction regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
out	*dir*	pointer to return the direction (0=output, 1=input)

Returns

Returns the I2C status.

16.33.2.3 PCA6416A_WritePinPolarity()

```
status_t PCA6416A_WritePinPolarity (
            uint8_t device_addr,
            uint8_t port,
            uint8_t pol )
```

This function writes the pin polarity regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
in	*pol*	polarity (1=invert)

Returns

Returns the I2C status.

16.33.2.4 PCA6416A_ReadPinPolarity()

```
status_t PCA6416A_ReadPinPolarity (
            uint8_t device_addr,
```

```
            uint8_t port,
            uint8_t * pol )
```

This function reads the pin polarity regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
out	*pol*	pointer to return the polarity (1=invert)

Returns

Returns the I2C status.

16.33.2.5 PCA6416A_WritePinOutput()

```
status_t PCA6416A_WritePinOutput (
            uint8_t device_addr,
            uint8_t port,
            uint8_t out )
```

This function writes the pin output regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
in	*out*	output value

Returns

Returns the I2C status.

16.33.2.6 PCA6416A_ReadPinOutput()

```
status_t PCA6416A_ReadPinOutput (
            uint8_t device_addr,
            uint8_t port,
            uint8_t * out )
```

This function reads the pin output regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
out	*out*	pointer to return the output

Returns

Returns the I2C status.

16.33.2.7 PCA6416A_ReadPinInput()

```
status_t PCA6416A_ReadPinInput (
             uint8_t device_addr,
             uint8_t port,
             uint8_t * in )
```

This function reads the pin input regsiter.

Parameters

in	*device_addr*	I2C address
in	*port*	expander port
out	*in*	input

Returns

Returns the I2C status.

Chapter 17

Data Structure Documentation

17.1 gpio_pin_config_t Struct Reference

GPIO Init structure definition.

Data Fields

- gpio_pin_direction_t direction
  Specifies the pin direction.
- uint8_t outputLogic
  Set a default output logic, which has no use in input.
- gpio_interrupt_mode_t interruptMode
  Specifies the pin interrupt mode, a value of gpio_interrupt_mode_t.

17.1.1 Detailed Description

GPIO Init structure definition.

17.2 lpi2c_data_match_config_t Struct Reference

LPI2C master data match configuration structure.

Data Fields

- lpi2c_data_match_config_mode_t matchMode
  Data match configuration setting.
- bool rxDataMatchOnly
  When set to true, received data is ignored until a successful match.
- uint32_t match0
  Match value 0.
- uint32_t match1
  Match value 1.

17.2.1 Detailed Description

LPI2C master data match configuration structure.

17.3 lpi2c_master_config_t Struct Reference

Structure with settings to initialize the LPI2C master module.

Data Fields

- bool enableMaster
  Whether to enable master mode.
- bool enableDoze
  Whether master is enabled in doze mode.
- bool debugEnable
  Enable transfers to continue when halted in debug mode.
- bool ignoreAck
  Whether to ignore ACK/NACK.
- lpi2c_master_pin_config_t pinConfig
  The pin configuration option.
- uint32_t baudRate_Hz
  Desired baud rate in Hertz.
- uint32_t busIdleTimeout_ns
  Bus idle timeout in nanoseconds.
- uint32_t pinLowTimeout_ns
  Pin low timeout in nanoseconds.
- uint8_t sdaGlitchFilterWidth_ns
  Width in nanoseconds of glitch filter on SDA pin.
- uint8_t sclGlitchFilterWidth_ns
  Width in nanoseconds of glitch filter on SCL pin.
- struct {
  bool enable
  Enable host request.
  lpi2c_host_request_source_t source
  Host request source.
  lpi2c_host_request_polarity_t polarity
  Host request pin polarity.
  } hostRequest
  Host request options.

17.3.1 Detailed Description

Structure with settings to initialize the LPI2C master module.

This structure holds configuration settings for the LPI2C peripheral. To initialize this structure to reasonable defaults, call the LPI2C_MasterGetDefaultConfig() function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

Examples

board.c.

17.3.2 Field Documentation

17.3.2.1 busIdleTimeout_ns

```
uint32_t lpi2c_master_config_t::busIdleTimeout_ns
```

Bus idle timeout in nanoseconds.

Set to 0 to disable.

17.3.2.2 pinLowTimeout_ns

```
uint32_t lpi2c_master_config_t::pinLowTimeout_ns
```

Pin low timeout in nanoseconds.

Set to 0 to disable.

17.3.2.3 sdaGlitchFilterWidth_ns

```
uint8_t lpi2c_master_config_t::sdaGlitchFilterWidth_ns
```

Width in nanoseconds of glitch filter on SDA pin.

Set to 0 to disable.

Examples

board.c.

17.3.2.4 sclGlitchFilterWidth_ns

```
uint8_t lpi2c_master_config_t::sclGlitchFilterWidth_ns
```

Width in nanoseconds of glitch filter on SCL pin.

Set to 0 to disable.

Examples

board.c.

17.4 lpi2c_master_handle_t Struct Reference

Driver handle for master non-blocking APIs.

Data Fields

- uint8_t state
  Transfer state machine current state.
- uint16_t remainingBytes
  Remaining byte count in current state.
- uint8_t * buf
  Buffer pointer for current state.
- uint16_t commandBuffer [7]
  LPI2C command sequence.
- lpi2c_master_transfer_t transfer
  Copy of the current transfer info.
- lpi2c_master_transfer_callback_t completionCallback
  Callback function pointer.
- void * userData
  Application data passed to callback.

17.4.1 Detailed Description

Driver handle for master non-blocking APIs.

Note

The contents of this structure are private and subject to change.

17.5 lpi2c_master_transfer_t Struct Reference

Non-blocking transfer descriptor structure.

Data Fields

- uint32_t flags
  Bit mask of options for the transfer.
- uint16_t slaveAddress
  The 7-bit slave address.
- lpi2c_direction_t direction
  Either kLPI2C_Read or kLPI2C_Write.
- uint32_t subaddress
  Sub address.
- size_t subaddressSize
  Length of sub address to send in bytes.
- void * data
  Pointer to data to transfer.
- size_t dataSize
  Number of bytes to transfer.

17.5.1 Detailed Description

Non-blocking transfer descriptor structure.

This structure is used to pass transaction parameters to the LPI2C_MasterTransferNonBlocking() API.

17.5.2 Field Documentation

17.5.2.1 flags

```
uint32_t lpi2c_master_transfer_t::flags
```

Bit mask of options for the transfer.

See enumeration _lpi2c_master_transfer_flags for available options. Set to 0 or kLPI2C_TransferDefaultFlag for normal transfers.

17.5.2.2 subaddress

```
uint32_t lpi2c_master_transfer_t::subaddress
```

Sub address.

Transferred MSB first.

17.5.2.3 subaddressSize

```
size_t lpi2c_master_transfer_t::subaddressSize
```

Length of sub address to send in bytes.

Maximum size is 4 bytes.

17.6 lpi2c_slave_config_t Struct Reference

Structure with settings to initialize the LPI2C slave module.

Data Fields

- bool enableSlave
  Enable slave mode.
- uint8_t address0
  Slave's 7-bit address.
- uint8_t address1
  Alternate slave 7-bit address.
- lpi2c_slave_address_match_t addressMatchMode
  Address matching options.

- bool filterDozeEnable

  Enable digital glitch filter in doze mode.
- bool filterEnable

  Enable digital glitch filter.
- bool enableGeneralCall

  Enable general call address matching.
- struct {
  bool enableAck
  Enables SCL clock stretching during slave-transmit address byte(s) and slave-receiver address and data byte(s) to allow softw
  bool enableTx
  Enables SCL clock stretching when the transmit data flag is set during a slave-transmit transfer.
  bool enableRx
  Enables SCL clock stretching when receive data flag is set during a slave-receive transfer.
  bool enableAddress
  Enables SCL clock stretching when the address valid flag is asserted.
  } **sclStall**

- bool ignoreAck

  Continue transfers after a NACK is detected.
- bool enableReceivedAddressRead

  Enable reading the address received address as the first byte of data.
- uint32_t sdaGlitchFilterWidth_ns

  Width in nanoseconds of the digital filter on the SDA signal.
- uint32_t sclGlitchFilterWidth_ns

  Width in nanoseconds of the digital filter on the SCL signal.
- uint32_t dataValidDelay_ns

  Width in nanoseconds of the data valid delay.
- uint32_t clockHoldTime_ns

  Width in nanoseconds of the clock hold time.

17.6.1 Detailed Description

Structure with settings to initialize the LPI2C slave module.

This structure holds configuration settings for the LPI2C slave peripheral. To initialize this structure to reasonable defaults, call the LPI2C_SlaveGetDefaultConfig() function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

17.6.2 Field Documentation

17.6.2.1 enableAck

```
bool lpi2c_slave_config_t::enableAck
```

Enables SCL clock stretching during slave-transmit address byte(s) and slave-receiver address and data byte(s) to allow software to write the Transmit ACK Register before the ACK or NACK is transmitted.

Clock stretching occurs when transmitting the 9th bit. When enableAckSCLStall is enabled, there is no need to set either enableRxDataSCLStall or enableAddressSCLStall.

17.7 lpi2c_slave_handle_t Struct Reference

LPI2C slave handle structure.

Data Fields

- lpi2c_slave_transfer_t transfer
  LPI2C slave transfer copy.
- bool isBusy
  Whether transfer is busy.
- bool wasTransmit
  Whether the last transfer was a transmit.
- uint32_t eventMask
  Mask of enabled events.
- uint32_t transferredCount
  Count of bytes transferred.
- lpi2c_slave_transfer_callback_t callback
  Callback function called at transfer event.
- void * userData
  Callback parameter passed to callback.

17.7.1 Detailed Description

LPI2C slave handle structure.

Note

The contents of this structure are private and subject to change.

17.8 lpi2c_slave_transfer_t Struct Reference

LPI2C slave transfer structure.

Data Fields

- lpi2c_slave_transfer_event_t event
  Reason the callback is being invoked.
- uint8_t receivedAddress
  Matching address send by master.
- uint8_t * data
  Transfer buffer.
- size_t dataSize
  Transfer size.
- status_t completionStatus
  Success or error code describing how the transfer completed.
- size_t transferredCount
  Number of bytes actually transferred since start or last repeated start.

17.8.1 Detailed Description

LPI2C slave transfer structure.

17.8.2 Field Documentation

17.8.2.1 completionStatus

`status_t lpi2c_slave_transfer_t::completionStatus`

Success or error code describing how the transfer completed.

Only applies for kLPI2C_SlaveCompletionEvent.

17.9 lpuart_config_t Struct Reference

LPUART configuration structure.

Data Fields

- uint32_t baudRate_Bps
  LPUART baud rate
- lpuart_parity_mode_t parityMode
  Parity mode, disabled (default), even, odd.
- lpuart_data_bits_t dataBitsCount
  Data bits count, eight (default), seven.
- bool isMsb
  Data bits order, LSB (default), MSB.
- lpuart_idle_type_select_t rxIdleType
  RX IDLE type.
- lpuart_idle_config_t rxIdleConfig
  RX IDLE configuration.
- bool enableTx
  Enable TX.
- bool enableRx
  Enable RX.

17.9.1 Detailed Description

LPUART configuration structure.

17.10 lpuart_handle_t Struct Reference

LPUART handle structure.

Data Fields

- uint8_t *volatile txData
  Address of remaining data to send.
- volatile size_t txDataSize
  Size of the remaining data to send.
- size_t txDataSizeAll
  Size of the data to send out.
- uint8_t *volatile rxData
  Address of remaining data to receive.
- volatile size_t rxDataSize
  Size of the remaining data to receive.
- size_t rxDataSizeAll
  Size of the data to receive.
- uint8_t * rxRingBuffer
  Start address of the receiver ring buffer.
- size_t rxRingBufferSize
  Size of the ring buffer.
- volatile uint16_t rxRingBufferHead
  Index for the driver to store received data into ring buffer.
- volatile uint16_t rxRingBufferTail
  Index for the user to get data from the ring buffer.
- lpuart_transfer_callback_t callback
  Callback function.
- void * userData
  LPUART callback function parameter.
- volatile uint8_t txState
  TX transfer state.
- volatile uint8_t rxState
  RX transfer state.

17.10.1 Detailed Description

LPUART handle structure.

17.11 lpuart_transfer_t Struct Reference

LPUART transfer structure.

Data Fields

- uint8_t * data
  The buffer of data to be transfer.
- size_t dataSize
  The byte count to be transfer.

17.11.1 Detailed Description

LPUART transfer structure.

17.12 pmic_version_t Struct Reference

Structure for ID and Revision of PMIC.

Data Fields

- uint8_t device_id
  dev ID value (reg location may differ per device)
- uint8_t si_rev
  silicon revision value read from device

17.12.1 Detailed Description

Structure for ID and Revision of PMIC.

Examples

board.c.

17.13 rgpio_pin_config_t Struct Reference

The RGPIO pin configuration structure.

Data Fields

- rgpio_pin_direction_t pinDirection
  RGPIO direction, input or output.
- uint8_t outputLogic
  Set a default output logic, which has no use in input.

17.13.1 Detailed Description

The RGPIO pin configuration structure.

Each pin can only be configured as either an output pin or an input pin at a time. If configured as an input pin, leave the outputConfig unused. Note that in some use cases, the corresponding port property should be configured in advance with the PORT_SetPinConfig().

Examples

board.c.

17.14 sc_rsrc_map_t Struct Reference

This type is used store static constant info to map resources to the containing subsystem.

Data Fields

- sc_rsrc_t **resource**: SC_RSRC_W
- ss_idx_t **ss_idx**: SS_IDX_W
- sc_ss_inst_t **inst**: SC_SS_INST_W

17.14.1 Detailed Description

This type is used store static constant info to map resources to the containing subsystem.

Examples

board.c.

17.15 soc_cluster_state_t Struct Reference

Stores cluster power state info.

Data Fields

- sc_rm_idx_t **rm_idx**
- uint8_t **num_cpu**
- soc_cpu_state_t * **cpu_state**
- sc_pm_power_mode_t **req_mode**

17.15.1 Detailed Description

Stores cluster power state info.

17.16 soc_cpu_state_t Struct Reference

Stores CPU power state info.

Data Fields

- sc_rm_idx_t **rm_idx**
- sc_pm_power_mode_t **req_mode**
- sc_bool_t **lpm_active**
- sc_bool_t **rst_req**
- sc_bool_t **early_wake**
- uint8_t **wake_idx**
- sc_pm_wake_src_t **wake_src**
- sc_faddr_t **resume_addr**

17.16.1 Detailed Description

Stores CPU power state info.

17.17 soc_ddr_ret_info_t Struct Reference

Stores DDR retention info.

Data Fields

- const uint32_t num_drc
  Number of DRCs to retain.
- ddrc ∗const drc_inst
  Buffer for DRC register retention.
- ddr_phy ∗const drc_phy_inst
  Buffer for DRC PHY register retention.
- const uint32_t num_region
  Number of DDR retention regions.
- const soc_ddr_ret_region_t ∗const region
  Retention region array.
- uint32_t drc0_clk_rate
  Clock rate to restore after retention.

17.17.1 Detailed Description

Stores DDR retention info.

Examples

board.c.

17.18 soc_ddr_ret_region_t Struct Reference

Data Fields

- const uint32_t addr
  Address of DDR region to be retained.
- const uint32_t size
  Size of DDR region to be retained.
- uint32_t ∗const buf
  Pointer to SCFW buffer for DDR retention.

17.18.1 Detailed Description

Examples

board.c.

17.19 soc_dqs2dq_sync_info_t Struct Reference

Stores DQS2DQ synchronization info.

Data Fields

- const sc_rsrc_t isi_rsrc

  ISI channel used for sync.
- ISI_Type *const isi_regs

  ISI peripheral registers.
- uint32_t timeout_usec

  Sync search timeout.

17.19.1 Detailed Description

Stores DQS2DQ synchronization info.

Examples

board.c.

17.20 soc_freq_volt_tbl_t Struct Reference

Data Fields

- uint32_t **freq**
- uint32_t **volt**
- uint8_t **bias**

17.21 soc_fspi_ret_info_t Struct Reference

Stores HMP FSPI retention info.

Data Fields

- sc_pm_power_mode_t pm

  FSPI power mode to restore.
- uint32_t clk_rate

  FSPI clock rate to restore.

17.21.1 Detailed Description

Stores HMP FSPI retention info.

17.22 soc_gpu_clks_opp_t Struct Reference

Data Fields

- uint32_t **shader_clk**
- uint32_t **core_clk**
- uint32_t **ahb_clk**
- uint32_t **axi_ssi_clk**

17.23 soc_hmp_node_t Struct Reference

Stores HMP node power mode info.

Data Fields

- sc_rm_idx_t **rm_idx**
- soc_sys_if_req_t * sys_if_req

  System interface mode request array.

17.23.1 Detailed Description

Stores HMP node power mode info.

17.24 soc_hmp_t Struct Reference

Stores HMP system power mode info.

Data Fields

- uint8_t num_hmp

  Number of HMP nodes.
- soc_hmp_node_t * hmp_node

  HMP node array.
- uint8_t num_sys_if

  Number of system interace nodes.
- soc_sys_if_node_t * sys_if_node

  System interface node array.
- sc_bool_t sys_if_mgmt

  System interface managment flag.
- sc_rm_idx_t ap_gic_rm_idx

AP GIC resource index.

- sc_rm_idx_t ap_irqstr_rm_idx

  AP IRQSTR resource index.
- uint8_t ap_resume_cluster_idx

  AP resume cluster index.
- uint8_t ap_resume_cpu_idx

  AP resume cpu index.
- sc_pm_power_mode_t ocmem_mode

  On-chip memory mode for SoC.
- soc_fspi_ret_info_t fspi_ret_info

  FSPI retention info.
- sc_pm_power_mode_t ddr_mode

  DDR mode for SoC.
- sc_bool_t ddr_active

  DDR active (initialized) boolean.
- sc_bool_t lpm_active

  LPM active boolean.

17.24.1 Detailed Description

Stores HMP system power mode info.

17.25 soc_m4_state_t Struct Reference

Stores M4 sleep state info.

Data Fields

- sc_rm_idx_t **wic_rm_idx**
- sc_rm_idx_t **sc_mu_rm_idx**
- sc_bool_t **dsm_req**
- sc_bool_t **dsm_active**
- sc_bool_t **rst_req**
- uint8_t **stopm**
- uint8_t **pstopo**
- sc_faddr_t **resume_addr**

17.25.1 Detailed Description

Stores M4 sleep state info.

17.26 soc_msi_ring_usecount_t Struct Reference

Stores MSI ring usecount.

Data Fields

- const sc_rsrc_t **rsrc**
- uint16_t **count**
- uint16_t **ss_count**

17.26.1 Detailed Description

Stores MSI ring usecount.

17.27 soc_multicluster_state_t Struct Reference

Stores multi-cluster power state info.

Data Fields

- sc_rm_idx_t **rm_idx**
- soc_cluster_state_t * **cluster_state**
- sc_pm_power_mode_t **req_mode**

17.27.1 Detailed Description

Stores multi-cluster power state info.

17.28 soc_patch_area_list_t Struct Reference

Data Fields

- const uint16_t **offset**
- const uint16_t **len**

17.29 soc_sys_if_node_t Struct Reference

Stores system interface node resource info.

Data Fields

- sc_rm_idx_t num_rm_idx

  Number of resources in the node.
- const sc_rsrc_t * rsrc

  Resource array for node.
- sc_rm_idx_t * rm_idx

  Resource index array for node.
- sc_pm_power_mode_t * saved_pm

  Saved power mode array for node.

17.29.1 Detailed Description

Stores system interface node resource info.

17.30 soc_sys_if_req_t Struct Reference

Stores system interface power mode reqest info.

Data Fields

- sc_pm_power_mode_t hpm

  High-power mode for system interface.
- sc_pm_power_mode_t lpm

  Low-power mode for system interface.

17.30.1 Detailed Description

Stores system interface power mode reqest info.

17.31 ss_base_data_t Struct Reference

This type is used to store dynamic data about a subsystem.

Data Fields

- ss_clk_data_t clk_data [SS_MAX_CLK]

  Clock/PLL data.
- ss_pll_t num_pll

  number of PLLs in the SS
- uint16_t usecount [DSC_MAX_PD][SC_PM_PW_MODE_ON]

  PD use counts.
- sc_pm_power_mode_t power_mode [DSC_MAX_PD]

  Power mode of each power domain.
- uint8_t master_did [SC_RM_NUM_DOMAIN]

  Count of masters in each resource domain.

17.31.1 Detailed Description

This type is used to store dynamic data about a subsystem.

17.32 ss_base_info_t Struct Reference

This type is used to store static constant info about a subsystem.

Data Fields

- uint64_t irq_enb
  Initial DSC IRQ enables.
- const sc_faddr_t mrc_mask
  Range of MRCs in subsystem.
- const ss_rsrc_info_t * rsrc
  Pointer to resource info.
- const sc_rsrc_map_t * rsrc_map
  Pointer to resource map.
- const ss_pd_info_t * pd_info
  Pointer to power domain info.
- const ss_pd_info_t * pd_reboot_info
  Pointer to power domain info.
- const ss_ctrl_info_t * ctrl_info
  Pointer to control info.
- const dsc_clk_info_t * clk_info
  Pointer to clock info.
- const uint8_t * ss_iso_info
  SS Isolation info.
- uint32_t dsc_aon_reset_mask
  Resets associated with DSC AON.
- uint32_t ss_phy_iso
  Additional ISO control (usually phy)
- const ss_xexp_info_t * xexp_info
  Pointer to xexp info.
- const ss_mdac_info_t * mdac_info
  Pointer to MDAC info.
- const ss_pac_info_t * pac_info
  Pointer to PAC info.
- const ss_msc_info_t * msc_info
  Pointer to MSC info.
- const ss_mrc_info_t * mrc_info
  Pointer to MRC info.
- uint32_t mdac_match
  MDAC match flags.
- uint16_t mdac_cache
  Size of MDAC cache (per inst)
- uint16_t mrc_cache

Size of MRC cache (per inst)

- sc_rm_idx_t num_rsrc: SC_RM_IDX_W

  Number of resources.
- sc_rm_idx_t num_srsrc: SC_RM_IDX_W

  Number of resources with children.
- sc_rm_idx_t num_prsrc: SC_RM_IDX_W

  Number of resources with parent.
- xrdc_idx_t num_mdac: XRDC_NUM_W

  Number of XRDC MDACs.
- xrdc_idx_t num_pac: XRDC_NUM_W

  Number of XRDC PACs.
- xrdc_idx_t num_msc: XRDC_NUM_W

  Number of XRDC MSCs.
- xrdc_idx_t num_mrc: XRDC_NUM_W

  Number of XRDC MRCs.
- ss_clock_t num_clks: SS_CLK_W+1

  Number of clocks.
- sc_ctrl_t num_ctrl: SC_CTRL_W

  Number of controls.
- dsc_pdom_t num_pd: DSC_PDOM_W+1

  Number of power domains.
- dsc_pdom_t pd_dsc: DSC_PDOM_W

  Power domain of the gated DSC logic.
- dsc_pdom_t pd_ssi: DSC_PDOM_W

  Power domain of the SSI.
- dsc_pdom_t pd_mgr: DSC_PDOM_W

  Power domain of XRDC manager.
- ss_pll_t num_pll: SS_PLL_W+1

  Number of PLLs.
- dsc_ai_type_t ai_type: DSC_AI_TYPE_W

  Type of AI for this SS.
- uint8_t ss_num_ssi: SS_NUM_SSI_W

  Number of standard SSI.
- ss_clock_t **mtr_clk_idx**: SS_CLK_W
- sc_bool_t mu_irq: SC_BOOL_W

  < Clock index of the MTR clock
- sc_bool_t dscmix: SC_BOOL_W

  DSCMIX clock present.

17.32.1 Detailed Description

This type is used to store static constant info about a subsystem.

An array for all subsytems is declared in inf.c called ss_base_info. From this array info for subsystems inc. resources, XRDC components, power domains, etc. can be accessed.

17.32.2 Field Documentation

17.32.2.1 mu_irq

```
sc_bool_t ss_base_info_t::mu_irq
```

< Clock index of the MTR clock

SS has interrupt trigger MU

17.33 ss_clk_data_t Struct Reference

This type is used to store dynamic data about the clocks/PLLs in the subsystem.

Data Fields

- uint16_t usecount
  Count of peripherals using clock.
- sc_pm_clk_mode_t cur_mode: SC_PM_CLOCK_MODE_W
  Current mode of the clock.
- sc_pm_clk_parent_t parent
  Current parent of the clock.
- union {
  uint32_t rate_div
  Current rate divider for the clock.
  uint32_t parent_rate
  store rate for parent clocks (pll, byp, xtal)
  };

17.33.1 Detailed Description

This type is used to store dynamic data about the clocks/PLLs in the subsystem.

17.34 ss_ctrl_info_t Struct Reference

This type is used store static constant info about controls in a subsystem.

Data Fields

- uint16_t bit: SS_FIELD_POS_W
  Field position.
- ss_idx_t ss_idx: SS_IDX_W
  SS resource index.
- uint8_t width: SS_FIELD_WID_W
  Field width.
- sc_ctrl_t ctrl: SC_CTRL_W
  Control.
- ss_io_type_t io: SS_IO_W
  I/O type.

17.34.1 Detailed Description

This type is used store static constant info about controls in a subsystem.

A pointer to this structure can be found in the ss_base_info_t type.

17.35 ss_mdac_info_t Struct Reference

This type is used to store static constant info about the MDACs in a subsystem.

Data Fields

- xrdc_idx_t num_slots: XRDC_NUM_W
  Number of slots.
- dsc_pdom_t pd: DSC_PDOM_W
  Power domain.
- uint8_t cid: SS_CID_W
  CPU ID.
- sc_bool_t present: SC_BOOL_W
  Present.
- uint32_t * cache
  Cache pointer.

17.35.1 Detailed Description

This type is used to store static constant info about the MDACs in a subsystem.

17.36 ss_mrc_info_t Struct Reference

This type is used to store static constant info about the MRCs in a subsystem.

Data Fields

- sc_faddr_t start
  Start address.
- sc_faddr_t end
  End address.
- sc_faddr_t adjust
  Sub/mask for this MRC.
- uint32_t * cache
  Cache pointer.
- xrdc_idx_t mrc: XRDC_NUM_W
  MRC index.
- xrdc_idx_t idx: XRDC_NUM_W
  index of first entry
- xrdc_idx_t num_slots: XRDC_NUM_W
  Number of slots.
- dsc_pdom_t pd: DSC_PDOM_W
  Power domain.
- dsc_pdom_t sub: SC_BOOL_W
  Adjust by subtraction.
- sc_bool_t present: SC_BOOL_W
  Present.

17.36.1 Detailed Description

This type is used to store static constant info about the MRCs in a subsystem.

Start->end address range indicates memory space covered by an MRC.

17.37 ss_msc_info_t Struct Reference

This type is used to store static constant info about the MSCs in a subsystem.

Data Fields

- dsc_pdom_t pd: DSC_PDOM_W
  Power domain.
- sc_bool_t present: SC_BOOL_W
  Present.

17.37.1 Detailed Description

This type is used to store static constant info about the MSCs in a subsystem.

17.38 ss_pd_info_t Struct Reference

This type is used to store static constant info about the power domains in the subsystem.

Data Fields

- uint32_t reset_mask
  Resets associated with the PD.

17.38.1 Detailed Description

This type is used to store static constant info about the power domains in the subsystem.

17.39 ss_rsrc_info_t Struct Reference

This type is used store static constant info about resources in a subsystem.

Data Fields

- sc_rm_idx_t xrdc_master_idx: SC_RM_IDX_W
  XRDC MDAC MDA index.
- sc_rm_idx_t xrdc_peripheral_idx: SC_RM_IDX_W
  XRDC PAC PDAC index.

- sc_rm_match_t xrdc_mda_match: SC_RM_MATCH_W
  XRDC MDAC match.
- sc_rm_match_t xrdc_mda_mask: SC_RM_MATCH_W
  XRDC MDAC mask.
- ss_xexp_idx_t xexp_idx: SS_XEXP_W
  XRDC expansion index.
- ss_clock_t clk [SS_MAX_PM_CLKS]
  Clocks.
- dsc_pdom_t pd: DSC_PDOM_W
  Power domain.
- sc_bool_t master: SC_BOOL_W
  Master flag.
- sc_bool_t peripheral: SC_BOOL_W
  Slave flag.

17.39.1 Detailed Description

This type is used store static constant info about resources in a subsystem.

A pointer to this structure can be found in the ss_base_info_t type.

17.40 ss_xexp_info_t Struct Reference

This type is used to store static constant info about resources to keep assigned to the SCU or associated with another resource.

Data Fields

- xrdc_idx_t start
  Start slot.
- uint8_t num
  Number of slots.

17.40.1 Detailed Description

This type is used to store static constant info about resources to keep assigned to the SCU or associated with another resource.

17.41 wdog32_config_t Struct Reference

Describes WDOG32 configuration structure.

Data Fields

- bool enableWdog32

Enables or disables WDOG32.

- wdog32_clock_source_t clockSource

  Clock source select.
- wdog32_clock_prescaler_t prescaler

  Clock prescaler value.
- wdog32_work_mode_t workMode

  Configures WDOG32 work mode in debug stop and wait mode.
- wdog32_test_mode_t testMode

  Configures WDOG32 test mode.
- bool enableUpdate

  Update write-once register enable.
- bool enableInterrupt

  Enables or disables WDOG32 interrupt.
- bool enableWindowMode

  Enables or disables WDOG32 window mode.
- uint16_t windowValue

  Window value.
- uint16_t timeoutValue

  Timeout value.

17.41.1 Detailed Description

Describes WDOG32 configuration structure.

17.42 wdog32_work_mode_t Struct Reference

Defines WDOG32 work mode.

Data Fields

- bool enableWait

  Enables or disables WDOG32 in wait mode.
- bool enableStop

  Enables or disables WDOG32 in stop mode.
- bool enableDebug

  Enables or disables WDOG32 in debug mode.

17.42.1 Detailed Description

Defines WDOG32 work mode.

Chapter 18

File Documentation

18.1 platform/board/board_common.h File Reference

Header file containing some common board funtions.

Functions

- sc_err_t test_drv (sc_bool_t *const stop)

  Shim test function (to allow test inclusion from object packages)
- sc_err_t test_sc (sc_bool_t *const stop)

  Shim test function (to allow test inclusion from object packages)
- sc_err_t test_ap (sc_bool_t *const stop)

  Shim test function (to allow test inclusion from object packages)
- void board_monitor (void)

  Shim monitor function (to allow monitor inclusion from object packages)
- void board_exit (int32_t status)

  Shim for exit()
- void board_stdio (void)

  Shim for setvbuf()
- void board_printf (const char *fmt,...)

  Conditional printf.
- void board_ddr_periodic_enable (sc_bool_t enb)

  Enable/disable the DDR periodic tick.
- void board_ddr_derate_periodic_enable (sc_bool_t enb)

  Enable/disable the DDR derate periodic tick.
- void board_common_tick (uint16_t msec)

  Common function to tick the board.

Variables

- sc_bool_t debug

  Shim debug variable (to allow object package config)
- sc_bool_t has_test

  Shim has_test variable (to allow object package config)
- sc_bool_t test_all

  Shim test_all variable (to allow object package config)
- sc_bool_t has_monitor

  Shim has_monitor variable (to allow object package config)
- sc_bool_t xrdc_nocheck

  Shim xrdc_nocheck variable (to allow object package config)

18.1.1 Detailed Description

Header file containing some common board funtions.

18.2 platform/board/drivers/pca6416a/pca6416a.h File Reference

Functions for PCA6416A.

Functions

- status_t PCA6416A_WritePinDirection (uint8_t device_addr, uint8_t port, uint8_t dir)

  This function writes the pin direction regsiter.
- status_t PCA6416A_ReadPinDirection (uint8_t device_addr, uint8_t port, uint8_t *dir)

  This function reads the pin direction regsiter.
- status_t PCA6416A_WritePinPolarity (uint8_t device_addr, uint8_t port, uint8_t pol)

  This function writes the pin polarity regsiter.
- status_t PCA6416A_ReadPinPolarity (uint8_t device_addr, uint8_t port, uint8_t *pol)

  This function reads the pin polarity regsiter.
- status_t PCA6416A_WritePinOutput (uint8_t device_addr, uint8_t port, uint8_t out)

  This function writes the pin output regsiter.
- status_t PCA6416A_ReadPinOutput (uint8_t device_addr, uint8_t port, uint8_t *out)

  This function reads the pin output regsiter.
- status_t PCA6416A_ReadPinInput (uint8_t device_addr, uint8_t port, uint8_t *in)

  This function reads the pin input regsiter.

18.2.1 Detailed Description

Functions for PCA6416A.

18.3 platform/board/pmic.h File Reference

PMIC include for PMIC interface layer.

Macros

- #define **PMIC_SET_VOLTAGE** dynamic_pmic_set_voltage
- #define **PMIC_GET_VOLTAGE** dynamic_pmic_get_voltage
- #define **PMIC_SET_MODE** dynamic_pmic_set_mode
- #define **PMIC_GET_MODE** dynamic_pmic_get_mode
- #define **PMIC_IRQ_SERVICE** dynamic_pmic_irq_service
- #define **PMIC_REGISTER_ACCESS** dynamic_pmic_register_access
- #define **GET_PMIC_VERSION** dynamic_get_pmic_version
- #define **GET_PMIC_TEMP** dynamic_get_pmic_temp
- #define **SET_PMIC_TEMP_ALARM** dynamic_set_pmic_temp_alarm

Defines for supported PMIC devices

- #define **PMIC_NONE** 0U
- #define **PF100** 1U
- #define **PF8100** 2U
- #define **PF8200** 3U

Defines for PMIC configuration

- #define **PF100_DEV_ID** 0x10U
- #define **PF8100_DEV_ID** 0x40U
- #define **PF8200_DEV_ID** 0x48U
- #define **PF8X00_FAM_ID** 0x40U
- #define **PF7X00_FAM_ID** 0x80U
- #define **PF8100_A0_REV** 0x10U
- #define **FAM_ID_MASK** 0xF0U

Functions

- sc_err_t dynamic_pmic_set_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t vol_mv, uint32_t mode_to_set)

  This function sets the voltage of a corresponding voltage regulator for the supported PMIC types.
- sc_err_t dynamic_pmic_get_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t *vol_mv, uint32_t mode_to_get)

  This function gets the voltage on a corresponding voltage regulator of the PMIC.
- sc_err_t dynamic_pmic_set_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t mode)

  This function sets the mode of the specified regulator.
- sc_err_t dynamic_pmic_get_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t *mode)

  This function gets the mode of the specified regulator.
- sc_bool_t dynamic_pmic_irq_service (pmic_id_t id)

  This function services the interrupt for the temp alarm.

- sc_err_t dynamic_pmic_register_access (pmic_id_t id, uint32_t address, sc_bool_t read_write, uint8_t *value)

  This function allows access to individual registers of the PMIC.
- pmic_version_t dynamic_get_pmic_version (pmic_id_t id)

  This function returns the device ID and revision for the PMIC.
- uint32_t dynamic_get_pmic_temp (pmic_id_t id)

  This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.
- uint32_t dynamic_set_pmic_temp_alarm (pmic_id_t id, uint32_t temp)

  This function sets the temp alarm for the PMIC in Celsius.

Variables

- uint8_t PMIC_TYPE

  Global PMIC type identifier.

18.3.1 Detailed Description

PMIC include for PMIC interface layer.

This API is used to abstract the PMIC driver. It also supports dynamic PMIC identification and function binding (normally only used for dev boards).

18.4 platform/drivers/drc/fsl_drc_cbt.h File Reference

Functions

- void run_cbt (uint32_t phy_ptr0, uint32_t phy_ptr1, uint32_t total_num_drc)

  This function performs DDR command bus training.

18.5 platform/drivers/drc/fsl_drc_derate.h File Reference

Functions

- void ddrc_lpddr4_derate_init (uint32_t total_num_drc)

  This function initializes the DDR derate mechanism.
- sc_bool_t ddrc_lpddr4_derate_periodic (uint32_t total_num_drc)

  This function performs periodic DDR derate training.

18.6 platform/drivers/drc/fsl_drc_rdbi_deskew.h File Reference

Functions

- void RDBI_bit_deskew (uint32_t ddr_num)

  This function performs DDR deskew training.

18.7 platform/drivers/igpio/fsl_gpio.h File Reference

Data Structures

- struct gpio_pin_config_t
  GPIO Init structure definition.

Macros

Driver version

- #define FSL_GPIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 3))
  GPIO driver version 2.0.3.

Enumerations

- enum gpio_pin_direction_t { kGPIO_DigitalInput = 0U, kGPIO_DigitalOutput = 1U }
  GPIO direction definition.
- enum gpio_interrupt_mode_t {
  kGPIO_NoIntmode = 0U, kGPIO_IntLowLevel = 1U, kGPIO_IntHighLevel = 2U, kGPIO_IntRisingEdge = 3U,
  kGPIO_IntFallingEdge = 4U, kGPIO_IntRisingOrFallingEdge = 5U }
  GPIO interrupt mode definition.

Functions

GPIO Initialization and Configuration functions

- void GPIO_PinInit (GPIO_Type *base, uint32_t pin, const gpio_pin_config_t *Config)
  Initializes the GPIO peripheral according to the specified parameters in the initConfig.

GPIO Reads and Write Functions

- void GPIO_PinWrite (GPIO_Type *base, uint32_t pin, uint8_t output)
  Sets the output level of the individual GPIO pin to logic 1 or 0.
- static void GPIO_WritePinOutput (GPIO_Type *base, uint32_t pin, uint8_t output)
  Sets the output level of the individual GPIO pin to logic 1 or 0.
- static void GPIO_PortSet (GPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple GPIO pins to the logic 1.
- static void GPIO_SetPinsOutput (GPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple GPIO pins to the logic 1.
- static void GPIO_PortClear (GPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple GPIO pins to the logic 0.
- static void GPIO_ClearPinsOutput (GPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple GPIO pins to the logic 0.
- static void GPIO_PortToggle (GPIO_Type *base, uint32_t mask)
  Reverses the current output logic of the multiple GPIO pins.
- static uint32_t GPIO_PinRead (GPIO_Type *base, uint32_t pin)
  Reads the current input value of the GPIO port.

- static uint32_t GPIO_ReadPinInput (GPIO_Type *base, uint32_t pin)
  Reads the current input value of the GPIO port.

GPIO Reads Pad Status Functions

- static uint8_t GPIO_PinReadPadStatus (GPIO_Type *base, uint32_t pin)
  Reads the current GPIO pin pad status.
- static uint8_t GPIO_ReadPadStatus (GPIO_Type *base, uint32_t pin)
  Reads the current GPIO pin pad status.

Interrupts and flags management functions

- void GPIO_PinSetInterruptConfig (GPIO_Type *base, uint32_t pin, gpio_interrupt_mode_t pinInterruptMode)
  Sets the current pin interrupt mode.
- static void GPIO_SetPinInterruptConfig (GPIO_Type *base, uint32_t pin, gpio_interrupt_mode_t pinInterrupt↩ Mode)
  Sets the current pin interrupt mode.
- static void GPIO_PortEnableInterrupts (GPIO_Type *base, uint32_t mask)
  Enables the specific pin interrupt.
- static void GPIO_EnableInterrupts (GPIO_Type *base, uint32_t mask)
  Enables the specific pin interrupt.
- static void GPIO_PortDisableInterrupts (GPIO_Type *base, uint32_t mask)
  Disables the specific pin interrupt.
- static void GPIO_DisableInterrupts (GPIO_Type *base, uint32_t mask)
  Disables the specific pin interrupt.
- static uint32_t GPIO_PortGetInterruptFlags (GPIO_Type *base)
  Reads individual pin interrupt status.
- static uint32_t GPIO_GetPinsInterruptFlags (GPIO_Type *base)
  Reads individual pin interrupt status.
- static void GPIO_PortClearInterruptFlags (GPIO_Type *base, uint32_t mask)
  Clears pin interrupt flag.
- static void GPIO_ClearPinsInterruptFlags (GPIO_Type *base, uint32_t mask)
  Clears pin interrupt flag.

18.8 platform/drivers/lpi2c/fsl_lpi2c.h File Reference

Data Structures

- struct lpi2c_master_config_t
  Structure with settings to initialize the LPI2C master module.
- struct lpi2c_data_match_config_t
  LPI2C master data match configuration structure.
- struct lpi2c_master_transfer_t
  Non-blocking transfer descriptor structure.
- struct lpi2c_master_handle_t
  Driver handle for master non-blocking APIs.
- struct lpi2c_slave_config_t
  Structure with settings to initialize the LPI2C slave module.
- struct lpi2c_slave_transfer_t
  LPI2C slave transfer structure.
- struct lpi2c_slave_handle_t
  LPI2C slave handle structure.

Macros

- #define I2C_RETRY_TIMES 0U /∗ Define to zero means keep waiting until the flag is assert/deassert. ∗/

  Retry times for waiting flag.

Driver version

- #define FSL_LPI2C_DRIVER_VERSION (MAKE_VERSION(2, 1, 11))

  LPI2C driver version 2.1.11.

Typedefs

- typedef void(∗ lpi2c_master_transfer_callback_t) (LPI2C_Type ∗base, lpi2c_master_handle_t ∗handle, status_t completionStatus, void ∗userData)

  Master completion callback function pointer type.
- typedef void(∗ lpi2c_slave_transfer_callback_t) (LPI2C_Type ∗base, lpi2c_slave_transfer_t ∗transfer, void ∗user↩ Data)

  Slave event callback function pointer type.

Enumerations

- enum {
  kStatus_LPI2C_Busy = MAKE_STATUS(kStatusGroup_LPI2C, 0), kStatus_LPI2C_Idle = MAKE_STATUS(k↩ StatusGroup_LPI2C, 1), kStatus_LPI2C_Nak = MAKE_STATUS(kStatusGroup_LPI2C, 2), kStatus_LPI2C_FifoError = MAKE_STATUS(kStatusGroup_LPI2C, 3),
  kStatus_LPI2C_BitError = MAKE_STATUS(kStatusGroup_LPI2C, 4), kStatus_LPI2C_ArbitrationLost = MAKE↩ _STATUS(kStatusGroup_LPI2C, 5), kStatus_LPI2C_PinLowTimeout, kStatus_LPI2C_NoTransferInProgress,
  kStatus_LPI2C_DmaRequestFail = MAKE_STATUS(kStatusGroup_LPI2C, 8), kStatus_LPI2C_Timeout = MA↩ KE_STATUS(kStatusGroup_LPI2C, 9) }

  LPI2C status return codes.
- enum {
  kLPI2C_MasterTxReadyFlag = LPI2C_MSR_TDF_MASK, kLPI2C_MasterRxReadyFlag = LPI2C_MSR_RDF↩ _MASK, kLPI2C_MasterEndOfPacketFlag = LPI2C_MSR_EPF_MASK, kLPI2C_MasterStopDetectFlag = LPI2↩ C_MSR_SDF_MASK,
  kLPI2C_MasterNackDetectFlag = LPI2C_MSR_NDF_MASK, kLPI2C_MasterArbitrationLostFlag = LPI2C_M↩ SR_ALF_MASK, kLPI2C_MasterFifoErrFlag = LPI2C_MSR_FEF_MASK, kLPI2C_MasterPinLowTimeoutFlag = LPI2C_MSR_PLTF_MASK,
  kLPI2C_MasterDataMatchFlag = LPI2C_MSR_DMF_MASK, kLPI2C_MasterBusyFlag = LPI2C_MSR_MBF_M↩ ASK, kLPI2C_MasterBusBusyFlag = LPI2C_MSR_BBF_MASK }

  LPI2C master peripheral flags.
- enum lpi2c_direction_t { kLPI2C_Write = 0U, kLPI2C_Read = 1U }

  Direction of master and slave transfers.
- enum lpi2c_master_pin_config_t {
  kLPI2C_2PinOpenDrain = 0x0U, kLPI2C_2PinOutputOnly = 0x1U, kLPI2C_2PinPushPull = 0x2U, kLPI2C_4PinPushPull = 0x3U,
  kLPI2C_2PinOpenDrainWithSeparateSlave, kLPI2C_2PinOutputOnlyWithSeparateSlave, kLPI2C_2PinPushPullWithSeparateSlave
  kLPI2C_4PinPushPullWithInvertedOutput = 0x7U }

  LPI2C pin configuration.

- enum lpi2c_host_request_source_t { kLPI2C_HostRequestExternalPin = 0x0U, kLPI2C_HostRequestInputTrigger = 0x1U }

  LPI2C master host request selection.
- enum lpi2c_host_request_polarity_t { kLPI2C_HostRequestPinActiveLow = 0x0U, kLPI2C_HostRequestPinActiveHigh = 0x1U }

  LPI2C master host request pin polarity configuration.
- enum lpi2c_data_match_config_mode_t { kLPI2C_MatchDisabled = 0x0U, kLPI2C_1stWordEqualsM0OrM1 = 0x2U, kLPI2C_AnyWordEqualsM0OrM1 = 0x3U, kLPI2C_1stWordEqualsM0And2ndWordEqualsM1, kLPI2C_AnyWordEqualsM0AndNextWordEqualsM1, kLPI2C_1stWordAndM1EqualsM0AndM1, kLPI2C_AnyWordAndM1EqualsM0 }

  LPI2C master data match configuration modes.
- enum _lpi2c_master_transfer_flags { kLPI2C_TransferDefaultFlag = 0x00U, kLPI2C_TransferNoStartFlag = 0x01U, kLPI2C_TransferRepeatedStartFlag = 0x02U, kLPI2C_TransferNoStopFlag = 0x04U }

  Transfer option flags.
- enum _lpi2c_slave_flags { kLPI2C_SlaveTxReadyFlag = LPI2C_SSR_TDF_MASK, kLPI2C_SlaveRxReadyFlag = LPI2C_SSR_RDF_MA↩ SK, kLPI2C_SlaveAddressValidFlag = LPI2C_SSR_AVF_MASK, kLPI2C_SlaveTransmitAckFlag = LPI2C_SS↩ R_TAF_MASK, kLPI2C_SlaveRepeatedStartDetectFlag = LPI2C_SSR_RSF_MASK, kLPI2C_SlaveStopDetectFlag = LPI2C_↩ SSR_SDF_MASK, kLPI2C_SlaveBitErrFlag = LPI2C_SSR_BEF_MASK, kLPI2C_SlaveFifoErrFlag = LPI2C_S↩ SR_FEF_MASK, kLPI2C_SlaveAddressMatch0Flag = LPI2C_SSR_AM0F_MASK, kLPI2C_SlaveAddressMatch1Flag = LPI2C_↩ SSR_AM1F_MASK, kLPI2C_SlaveGeneralCallFlag = LPI2C_SSR_GCF_MASK, kLPI2C_SlaveBusyFlag = LP↩ I2C_SSR_SBF_MASK, kLPI2C_SlaveBusBusyFlag = LPI2C_SSR_BBF_MASK }

  LPI2C slave peripheral flags.
- enum lpi2c_slave_address_match_t { kLPI2C_MatchAddress0 = 0U, kLPI2C_MatchAddress0OrAddress1 = 2U, kLPI2C_MatchAddress0ThroughAddress1 = 6U }

  LPI2C slave address match options.
- enum lpi2c_slave_transfer_event_t { kLPI2C_SlaveAddressMatchEvent = 0x01U, kLPI2C_SlaveTransmitEvent = 0x02U, kLPI2C_SlaveReceiveEvent = 0x04U, kLPI2C_SlaveTransmitAckEvent = 0x08U, kLPI2C_SlaveRepeatedStartEvent = 0x10U, kLPI2C_SlaveCompletionEvent = 0x20U, kLPI2C_SlaveAllEvents }

  Set of events sent to the callback for non blocking slave transfers.

Functions

Initialization and deinitialization

- void LPI2C_MasterGetDefaultConfig (lpi2c_master_config_t *masterConfig)

  Provides a default configuration for the LPI2C master peripheral.
- void LPI2C_MasterInit (LPI2C_Type *base, const lpi2c_master_config_t *masterConfig, uint32_t source↩ Clock_Hz)

  Initializes the LPI2C master peripheral.
- void LPI2C_MasterDeinit (LPI2C_Type *base)

  Deinitializes the LPI2C master peripheral.
- void LPI2C_MasterConfigureDataMatch (LPI2C_Type *base, const lpi2c_data_match_config_t *config)

  Configures LPI2C master data match feature.
- status_t **LPI2C_MasterCheckAndClearError** (LPI2C_Type *base, uint32_t status)
- status_t **LPI2C_CheckForBusyBus** (LPI2C_Type *base)

- static void LPI2C_MasterReset (LPI2C_Type *base)
  Performs a software reset.
- static void LPI2C_MasterEnable (LPI2C_Type *base, bool enable)
  Enables or disables the LPI2C module as master.

Status

- static uint32_t LPI2C_MasterGetStatusFlags (LPI2C_Type *base)
  Gets the LPI2C master status flags.
- static void LPI2C_MasterClearStatusFlags (LPI2C_Type *base, uint32_t statusMask)
  Clears the LPI2C master status flag state.

Interrupts

- static void LPI2C_MasterEnableInterrupts (LPI2C_Type *base, uint32_t interruptMask)
  Enables the LPI2C master interrupt requests.
- static void LPI2C_MasterDisableInterrupts (LPI2C_Type *base, uint32_t interruptMask)
  Disables the LPI2C master interrupt requests.
- static uint32_t LPI2C_MasterGetEnabledInterrupts (LPI2C_Type *base)
  Returns the set of currently enabled LPI2C master interrupt requests.

DMA control

- static void LPI2C_MasterEnableDMA (LPI2C_Type *base, bool enableTx, bool enableRx)
  Enables or disables LPI2C master DMA requests.
- static uint32_t LPI2C_MasterGetTxFifoAddress (LPI2C_Type *base)
  Gets LPI2C master transmit data register address for DMA transfer.
- static uint32_t LPI2C_MasterGetRxFifoAddress (LPI2C_Type *base)
  Gets LPI2C master receive data register address for DMA transfer.

FIFO control

- static void LPI2C_MasterSetWatermarks (LPI2C_Type *base, size_t txWords, size_t rxWords)
  Sets the watermarks for LPI2C master FIFOs.
- static void LPI2C_MasterGetFifoCounts (LPI2C_Type *base, size_t *rxCount, size_t *txCount)
  Gets the current number of words in the LPI2C master FIFOs.

Bus operations

- void LPI2C_MasterSetBaudRate (LPI2C_Type *base, uint32_t sourceClock_Hz, uint32_t baudRate_Hz)
  Sets the I2C bus frequency for master transactions.
- static bool LPI2C_MasterGetBusIdleState (LPI2C_Type *base)
  Returns whether the bus is idle.
- status_t LPI2C_MasterStart (LPI2C_Type *base, uint8_t address, lpi2c_direction_t dir)
  Sends a START signal and slave address on the I2C bus.
- static status_t LPI2C_MasterRepeatedStart (LPI2C_Type *base, uint8_t address, lpi2c_direction_t dir)
  Sends a repeated START signal and slave address on the I2C bus.
- status_t LPI2C_MasterSend (LPI2C_Type *base, void *txBuff, size_t txSize)
  Performs a polling send transfer on the I2C bus.
- status_t LPI2C_MasterReceive (LPI2C_Type *base, void *rxBuff, size_t rxSize)
  Performs a polling receive transfer on the I2C bus.
- status_t LPI2C_MasterStop (LPI2C_Type *base)

Sends a STOP signal on the I2C bus.

- status_t LPI2C_MasterTransferBlocking (LPI2C_Type *base, lpi2c_master_transfer_t *transfer)
  Performs a master polling transfer on the I2C bus.

Non-blocking

- void LPI2C_MasterTransferCreateHandle (LPI2C_Type *base, lpi2c_master_handle_t *handle, lpi2c_master_transfer_callback_t callback, void *userData)
  Creates a new handle for the LPI2C master non-blocking APIs.
- status_t LPI2C_MasterTransferNonBlocking (LPI2C_Type *base, lpi2c_master_handle_t *handle, lpi2c_master_transfer_t *transfer)
  Performs a non-blocking transaction on the I2C bus.
- status_t LPI2C_MasterTransferGetCount (LPI2C_Type *base, lpi2c_master_handle_t *handle, size_t *count)
  Returns number of bytes transferred so far.
- void LPI2C_MasterTransferAbort (LPI2C_Type *base, lpi2c_master_handle_t *handle)
  Terminates a non-blocking LPI2C master transmission early.

IRQ handler

- void LPI2C_MasterTransferHandleIRQ (LPI2C_Type *base, lpi2c_master_handle_t *handle)
  Reusable routine to handle master interrupts.

Slave initialization and deinitialization

- void LPI2C_SlaveGetDefaultConfig (lpi2c_slave_config_t *slaveConfig)
  Provides a default configuration for the LPI2C slave peripheral.
- void LPI2C_SlaveInit (LPI2C_Type *base, const lpi2c_slave_config_t *slaveConfig, uint32_t sourceClock_Hz)
  Initializes the LPI2C slave peripheral.
- void LPI2C_SlaveDeinit (LPI2C_Type *base)
  Deinitializes the LPI2C slave peripheral.
- static void LPI2C_SlaveReset (LPI2C_Type *base)
  Performs a software reset of the LPI2C slave peripheral.
- static void LPI2C_SlaveEnable (LPI2C_Type *base, bool enable)
  Enables or disables the LPI2C module as slave.

Slave status

- static uint32_t LPI2C_SlaveGetStatusFlags (LPI2C_Type *base)
  Gets the LPI2C slave status flags.
- static void LPI2C_SlaveClearStatusFlags (LPI2C_Type *base, uint32_t statusMask)
  Clears the LPI2C status flag state.

Slave interrupts

- static void LPI2C_SlaveEnableInterrupts (LPI2C_Type *base, uint32_t interruptMask)
  Enables the LPI2C slave interrupt requests.
- static void LPI2C_SlaveDisableInterrupts (LPI2C_Type *base, uint32_t interruptMask)
  Disables the LPI2C slave interrupt requests.
- static uint32_t LPI2C_SlaveGetEnabledInterrupts (LPI2C_Type *base)
  Returns the set of currently enabled LPI2C slave interrupt requests.

Slave DMA control

- static void LPI2C_SlaveEnableDMA (LPI2C_Type *base, bool enableAddressValid, bool enableRx, bool enableTx)

  Enables or disables the LPI2C slave peripheral DMA requests.

Slave bus operations

- static bool LPI2C_SlaveGetBusIdleState (LPI2C_Type *base)

  Returns whether the bus is idle.
- static void LPI2C_SlaveTransmitAck (LPI2C_Type *base, bool ackOrNack)

  Transmits either an ACK or NAK on the I2C bus in response to a byte from the master.
- static uint32_t LPI2C_SlaveGetReceivedAddress (LPI2C_Type *base)

  Returns the slave address sent by the I2C master.
- status_t LPI2C_SlaveSend (LPI2C_Type *base, void *txBuff, size_t txSize, size_t *actualTxSize)

  Performs a polling send transfer on the I2C bus.
- status_t LPI2C_SlaveReceive (LPI2C_Type *base, void *rxBuff, size_t rxSize, size_t *actualRxSize)

  Performs a polling receive transfer on the I2C bus.

Slave non-blocking

- void LPI2C_SlaveTransferCreateHandle (LPI2C_Type *base, lpi2c_slave_handle_t *handle, lpi2c_slave_transfer_callback_t callback, void *userData)

  Creates a new handle for the LPI2C slave non-blocking APIs.
- status_t LPI2C_SlaveTransferNonBlocking (LPI2C_Type *base, lpi2c_slave_handle_t *handle, uint32_t eventMask)

  Starts accepting slave transfers.
- status_t LPI2C_SlaveTransferGetCount (LPI2C_Type *base, lpi2c_slave_handle_t *handle, size_t *count)

  Gets the slave transfer status during a non-blocking transfer.
- void LPI2C_SlaveTransferAbort (LPI2C_Type *base, lpi2c_slave_handle_t *handle)

  Aborts the slave non-blocking transfers.

Slave IRQ handler

- void LPI2C_SlaveTransferHandleIRQ (LPI2C_Type *base, lpi2c_slave_handle_t *handle)

  Reusable routine to handle slave interrupts.

18.9 platform/drivers/lpuart/fsl_lpuart.h File Reference

Data Structures

- struct lpuart_config_t

  LPUART configuration structure.
- struct lpuart_transfer_t

  LPUART transfer structure.
- struct lpuart_handle_t

  LPUART handle structure.

Macros

- #define UART_RETRY_TIMES 0U /* Defining to zero means to keep waiting for the flag until it is assert/deassert. */

  Retry times for waiting flag.

Driver version

- #define FSL_LPUART_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))

  LPUART driver version 2.3.0.

Typedefs

- typedef void(* lpuart_transfer_callback_t) (LPUART_Type *base, lpuart_handle_t *handle, status_t status, void *userData)

  LPUART transfer callback function.

Enumerations

- enum { kStatus_LPUART_TxBusy = MAKE_STATUS(kStatusGroup_LPUART, 0), kStatus_LPUART_RxBusy = MAKE↩ _STATUS(kStatusGroup_LPUART, 1), kStatus_LPUART_TxIdle = MAKE_STATUS(kStatusGroup_LPUART, 2), kStatus_LPUART_RxIdle = MAKE_STATUS(kStatusGroup_LPUART, 3), kStatus_LPUART_TxWatermarkTooLarge = MAKE_STATUS(kStatusGroup_LPUART, 4), kStatus_LPUART_RxWatermarkTooLarg = MAKE_STATUS(kStatusGroup_LPUART, 5), kStatus_LPUART_FlagCannotClearManually = MAKE_STAT↩ US(kStatusGroup_LPUART, 6), kStatus_LPUART_Error = MAKE_STATUS(kStatusGroup_LPUART, 7), kStatus_LPUART_RxRingBufferOverrun, kStatus_LPUART_RxHardwareOverrun = MAKE_STATUS(k↩ StatusGroup_LPUART, 9), kStatus_LPUART_NoiseError = MAKE_STATUS(kStatusGroup_LPUART, 10), kStatus_LPUART_FramingError = MAKE_STATUS(kStatusGroup_LPUART, 11), kStatus_LPUART_ParityError = MAKE_STATUS(kStatusGroup_LPUART, 12), kStatus_LPUART_BaudrateNotSupport, kStatus_LPUART_IdleLineDetected = MAKE_STATUS(kStatusGroup_LPUART, 14), kStatus_LPUART_Timeout = MAKE_STATUS(kStatusGroup_LPUART, 15) }

  Error codes for the LPUART driver.
- enum lpuart_parity_mode_t { kLPUART_ParityDisabled = 0x0U, kLPUART_ParityEven = 0x2U, kLPUART_ParityOdd = 0x3U }

  LPUART parity mode.
- enum lpuart_data_bits_t { kLPUART_EightDataBits = 0x0U }

  LPUART data bits count.
- enum lpuart_stop_bit_count_t { kLPUART_OneStopBit = 0U, kLPUART_TwoStopBit = 1U }

  LPUART stop bit count.
- enum lpuart_idle_type_select_t { kLPUART_IdleTypeStartBit = 0U, kLPUART_IdleTypeStopBit = 1U }

  LPUART idle flag type defines when the receiver starts counting.
- enum lpuart_idle_config_t { kLPUART_IdleCharacter1 = 0U, kLPUART_IdleCharacter2 = 1U, kLPUART_IdleCharacter4 = 2U, kLPUART_IdleCharacter8 = 3U, kLPUART_IdleCharacter16 = 4U, kLPUART_IdleCharacter32 = 5U, kLPUART_IdleCharacter64 = 6U, kLPUART_IdleCharacter128 = 7U }

  LPUART idle detected configuration.

- enum _lpuart_interrupt_enable { kLPUART_RxActiveEdgeInterruptEnable = (LPUART_BAUD_RXEDGIE_MASK >> 8), kLPUART_TxDataRegEmptyInterruptEnab = (LPUART_CTRL_TIE_MASK), kLPUART_TransmissionCompleteInterruptEnable = (LPUART_CTRL_TCIE_↩ MASK), kLPUART_RxDataRegFullInterruptEnable = (LPUART_CTRL_RIE_MASK), kLPUART_IdleLineInterruptEnable = (LPUART_CTRL_ILIE_MASK), kLPUART_RxOverrunInterruptEnable = (LPUART_CTRL_ORIE_MASK), kLPUART_NoiseErrorInterruptEnable = (LPUART_CTRL_NEIE_MASK), kLPUART_FramingErrorInterruptEnable = (LPUART_CTRL_FEIE_MASK), kLPUART_ParityErrorInterruptEnable = (LPUART_CTRL_PEIE_MASK) }

  LPUART interrupt configuration structure, default settings all disabled.
- enum _lpuart_flags { kLPUART_TxDataRegEmptyFlag, kLPUART_TransmissionCompleteFlag, kLPUART_RxDataRegFullFlag, kLPUART_IdleLineFlag = (LPUART_STAT_IDLE_MASK), kLPUART_RxOverrunFlag = (LPUART_STAT_OR_MASK), kLPUART_NoiseErrorFlag = (LPUART_STAT_N↩ F_MASK), kLPUART_FramingErrorFlag, kLPUART_ParityErrorFlag = (LPUART_STAT_PF_MASK), kLPUART_RxActiveEdgeFlag, kLPUART_RxActiveFlag }

  LPUART status flags.

Functions

Initialization and deinitialization

- status_t LPUART_Init (LPUART_Type *base, const lpuart_config_t *config, uint32_t srcClock_Hz)

  Initializes an LPUART instance with the user configuration structure and the peripheral clock.
- void LPUART_Deinit (LPUART_Type *base)

  Deinitializes a LPUART instance.
- void LPUART_GetDefaultConfig (lpuart_config_t *config)

  Gets the default configuration structure.
- status_t LPUART_SetBaudRate (LPUART_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)

  Sets the LPUART instance baudrate.

Status

- uint32_t LPUART_GetStatusFlags (LPUART_Type *base)

  Gets LPUART status flags.
- status_t LPUART_ClearStatusFlags (LPUART_Type *base, uint32_t mask)

  Clears status flags with a provided mask.

Interrupts

- void LPUART_EnableInterrupts (LPUART_Type *base, uint32_t mask)

  Enables LPUART interrupts according to a provided mask.
- void LPUART_DisableInterrupts (LPUART_Type *base, uint32_t mask)

  Disables LPUART interrupts according to a provided mask.
- uint32_t LPUART_GetEnabledInterrupts (LPUART_Type *base)

  Gets enabled LPUART interrupts.

Bus Operations

- uint32_t LPUART_GetInstance (LPUART_Type *base)

  Get the LPUART instance from peripheral base address.
- static void LPUART_EnableTx (LPUART_Type *base, bool enable)

Enables or disables the LPUART transmitter.

- static void LPUART_EnableRx (LPUART_Type *base, bool enable)

  Enables or disables the LPUART receiver.
- static void LPUART_WriteByte (LPUART_Type *base, uint8_t data)

  Writes to the transmitter register.
- static uint8_t LPUART_ReadByte (LPUART_Type *base)

  Reads the receiver register.
- status_t LPUART_WriteBlocking (LPUART_Type *base, const uint8_t *data, size_t length)

  Writes to the transmitter register using a blocking method.
- status_t LPUART_ReadBlocking (LPUART_Type *base, uint8_t *data, size_t length)

  Reads the receiver data register using a blocking method.

Transactional

- void LPUART_TransferCreateHandle (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_callback_t callback, void *userData)

  Initializes the LPUART handle.
- status_t LPUART_TransferSendNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer)

  Transmits a buffer of data using the interrupt method.
- void LPUART_TransferStartRingBuffer (LPUART_Type *base, lpuart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)

  Sets up the RX ring buffer.
- void LPUART_TransferStopRingBuffer (LPUART_Type *base, lpuart_handle_t *handle)

  Aborts the background transfer and uninstalls the ring buffer.
- size_t LPUART_TransferGetRxRingBufferLength (LPUART_Type *base, lpuart_handle_t *handle)

  Get the length of received data in RX ring buffer.
- void LPUART_TransferAbortSend (LPUART_Type *base, lpuart_handle_t *handle)

  Aborts the interrupt-driven data transmit.
- status_t LPUART_TransferGetSendCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)

  Gets the number of bytes that have been sent out to bus.
- status_t LPUART_TransferReceiveNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer, size_t *receivedBytes)

  Receives a buffer of data using the interrupt method.
- void LPUART_TransferAbortReceive (LPUART_Type *base, lpuart_handle_t *handle)

  Aborts the interrupt-driven data receiving.
- status_t LPUART_TransferGetReceiveCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)

  Gets the number of bytes that have been received.
- void LPUART_TransferHandleIRQ (LPUART_Type *base, lpuart_handle_t *handle)

  LPUART IRQ handle function.
- void LPUART_TransferHandleErrorIRQ (LPUART_Type *base, lpuart_handle_t *handle)

  LPUART Error IRQ handle function.

18.10 platform/drivers/pmic/fsl_pmic.h File Reference

Data Structures

- struct pmic_version_t

  Structure for ID and Revision of PMIC.

Macros

- #define **i2c_error_flags**

Typedefs

- typedef uint8_t pmic_id_t

  This type is used to declare which PMIC to address.

Functions

- status_t i2c_write_sub (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function is a simple write to an i2c register on the PMIC.
- status_t i2c_write (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function writes an i2c register on the PMIC device with clock management.
- status_t i2c_read_sub (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function is a simple read of an i2c register on the PMIC.
- status_t i2c_read (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function reads an i2c register on the PMIC device with clock management.
- status_t i2c_j1850_write (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function writes an i2c register on the PMIC device with j1850 CRC appended and clock management.
- status_t i2c_j1850_read (uint8_t device_addr, uint8_t reg, void ∗data, uint32_t dataLength)

  This function reads an i2c register on the PMIC device with j1850 CRC and clock management.
- uint8_t pmic_get_device_id (uint8_t address)

  This function reads the register at address 0x0 for the Device ID.

18.11 platform/drivers/pmic/pf100/fsl_pf100.h File Reference

Macros

Defines for pf100_vol_regs_t

- #define SW1AB 0x20U

  Base register for SW1AB control.
- #define SW1C 0x2EU

  Base register for SW1C control.
- #define SW2 0x35U

  Base register for SW2 control.
- #define SW3A 0x3cU

  Base register for SW3A control.
- #define SW3B 0x43U

  Base register for SW3B control.
- #define SW4 0x4AU

  Base register for SW4 control.
- #define VGEN1 0x6CU

  Base register for VGEN1 control.
- #define VGEN2 0x6DU

Base register for VGEN2 control.

- #define VGEN3 0x6EU
  Base register for VGEN3 control.
- #define VGEN4 0x6FU
  Base register for VGEN4 control.
- #define VGEN5 0x70U
  Base register for VGEN5 control.
- #define VGEN6 0x71U
  Base register for VGEN6 control.

Defines for sw_pmic_mode_t

- #define SW_MODE_OFF_STBY_OFF 0x0U
  Normal Mode: OFF, Standby Mode: OFF
- #define SW_MODE_PWM_STBY_OFF 0x1U
  Normal Mode: PWM, Standby Mode: OFF
- #define SW_MODE_PFM_STBY_OFF 0x3U
  Normal Mode: PFM, Standby Mode: OFF
- #define SW_MODE_APS_STBY_OFF 0x4U
  Normal Mode: APS, Standby Mode: OFF
- #define SW_MODE_PWM_STBY_PWM 0x5U
  Normal Mode: PWM, Standby Mode: PWM
- #define SW_MODE_PWM_STBY_APS 0x6U
  Normal Mode: PWM, Standby Mode: APS
- #define SW_MODE_APS_STBY_APS 0x8U
  Normal Mode: APS, Standby Mode: APS
- #define SW_MODE_APS_STBY_PFM 0xCU
  Normal Mode: APS, Standby Mode: PFM
- #define SW_MODE_PWM_STBY_PFM 0xDU
  Normal Mode: PWM, Standby Mode: PFM

Defines for vgen_pmic_mode_t

- #define VGEN_MODE_OFF (0x0U << 4U)
  VGEN always OFF.
- #define VGEN_MODE_ON (0x1U << 4U)
  VGEN always ON
- #define VGEN_MODE_STBY_OFF (0x3U << 4U)
  VGEN Run: ON STBY: OFF.
- #define VGEN_MODE_LP (0x5U << 4U)
  VGEN Run: LPWR STBY: LPWR.
- #define VGEN_MODE_LP2 (0x7U << 4U)
  VGEN Run: LPWR STBY: LPWR.

Defines for sw_vmode_reg_t

- #define SW_RUN_MODE 0U
  SW run mode voltage
- #define SW_STBY_MODE 1U
  SW standby mode voltage.
- #define SW_OFF_MODE 2U
  SW off/sleep mode voltage.

Typedefs

- typedef uint8_t pf100_vol_regs_t
  This type is used to indicate which register to address.
- typedef uint8_t sw_pmic_mode_t
  This type is used to indicate a switching regulator mode.
- typedef uint8_t vgen_pmic_mode_t
  This type is used to indicate a VGEN (LDO) regulator mode.
- typedef uint8_t sw_vmode_reg_t
  This type encodes which voltage mode register to set when calling pf100_pmic_set_voltage().

Functions

- pmic_version_t pf100_get_pmic_version (pmic_id_t id)
  This function returns the device ID and revision for the PF100 PMIC.
- sc_err_t pf100_pmic_set_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t vol_mv, uint32_t mode_to_set)
  This function sets the voltage of a corresponding voltage regulator for the PF100 PMIC.
- sc_err_t pf100_pmic_get_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t *vol_mv, uint32_t mode_to_get)
  This function gets the voltage on a corresponding voltage regulator for the PF100 PMIC.
- sc_err_t pf100_pmic_set_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t mode)
  This function sets the mode of the specified regulator.
- uint32_t pf100_get_pmic_temp (pmic_id_t id)
  This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.
- uint32_t pf100_set_pmic_temp_alarm (pmic_id_t id, uint32_t temp)
  This function sets the temp alarm for the PMIC in Celsius.
- sc_err_t **pf100_pmic_register_access** (pmic_id_t id, uint32_t address, sc_bool_t read_write, uint8_t *value)
- sc_bool_t pf100_pmic_irq_service (pmic_id_t id)
  This function services the interrupt for the temp alarm.

18.12 platform/drivers/pmic/pf8100/fsl_pf8100.h File Reference

Macros

- #define **I2C_WRITE** i2c_write
- #define **I2C_READ** i2c_read

Defines for pf8100_vregs_t

- #define PF8100_CTRL1 0x37U
  CTRL1 register of PF8100/PF8200.
- #define PF8100_SW1 0x4DU
  Base register for SW1 regulator control.
- #define PF8100_SW2 0x55U
  Base register for SW2 regulator control.
- #define PF8100_SW3 0x5DU
  Base register for SW3 regulator control.
- #define PF8100_SW4 0x65U
  Base register for SW4 regulator control.
- #define PF8100_SW5 0x6DU
  Base register for SW5 regulator control.
- #define PF8100_SW6 0x75U
  Base register for SW6 regulator control.
- #define PF8100_SW7 0x7DU
  Base register for SW7 regulator control.
- #define PF8100_LDO1 0x85U
  Base register for LDO1 regulator control.
- #define PF8100_LDO2 0x8BU
  Base register for LDO2 regulator control.
- #define PF8100_LDO3 0x91U
  Base register for LDO3 regulator control.
- #define PF8100_LDO4 0x97U
  Base register for LDO4 regulator control.

Defines for sw_mode_t

- #define SW_RUN_OFF 0x0U
  Run mode: OFF.
- #define SW_RUN_PWM 0x1U
  Run mode: PWM.
- #define SW_RUN_PFM 0x2U
  Run mode: PFM.
- #define SW_RUN_ASM 0x3U
  Run mode: ASM.
- #define SW_STBY_OFF (0x0U << 2U)
  Standby mode: OFF.
- #define SW_STBY_PWM (0x1U << 2U)
  Standby mode: PWM.
- #define SW_STBY_PFM (0x2U << 2U)
  Standby mode: PFM.
- #define SW_STBY_ASM (0x3U << 2U)
  Standby mode: ASM.

Defines for ldo_mode_t

- #define RUN_OFF_STBY_OFF 0x0U
  Run mode: OFF, Standby mode: OFF.
- #define RUN_OFF_STBY_EN 0x1U
  Run mode: OFF, Standby mode: ON
- #define RUN_EN_STBY_OFF 0x2U
  Run mode: ON, Standby mode: OFF.
- #define RUN_EN_STBY_EN 0x3U
  Run mode: ON, Standby mode: ON
- #define VSELECT_EN 0x8U
  Enable VSELECT input pin for LDO 2 only.

Defines for vmode_reg_t

- #define **REG_STBY_MODE** 0U
- #define **REG_RUN_MODE** 1U

Typedefs

- typedef uint8_t pf8100_vregs_t
  This type is used to indicate which register to address.
- typedef uint8_t sw_mode_t
  This type is used to indicate a switching regulator mode.
- typedef uint8_t ldo_mode_t
  This type is used to indicate an LDO regulator mode.
- typedef uint8_t vmode_reg_t
  This type is used to indicate a Switching regulator voltage setpoint.

Functions

- pmic_version_t pf8100_get_pmic_version (pmic_id_t id)
  This function returns the device ID and revision for the PF8100 PMIC.
- sc_err_t pf8100_pmic_set_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t vol_mv, uint32_t mode_to_set)
  This function sets the voltage of a corresponding voltage regulator for the PF8100 PMIC.
- sc_err_t pf8100_pmic_get_voltage (pmic_id_t id, uint32_t pmic_reg, uint32_t *vol_mv, uint32_t mode_to_get)
  This function gets the voltage on a corresponding voltage regulator for the PF8100 PMIC.
- sc_err_t pf8100_pmic_set_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t mode)
  This function sets the mode of the specified regulator.
- sc_err_t pf8100_pmic_get_mode (pmic_id_t id, uint32_t pmic_reg, uint32_t *mode)
  This function gets the mode of the specified regulator.
- uint32_t pf8100_get_pmic_temp (pmic_id_t id)
  This function gets the current PMIC temperature as sensed by the PMIC temperature sensor.
- uint32_t pf8100_set_pmic_temp_alarm (pmic_id_t id, uint32_t temp)
  This function sets the temp alarm for the PMIC in Celsius.
- sc_err_t **pf8100_pmic_register_access** (pmic_id_t id, uint32_t address, sc_bool_t read_write, uint8_t *value)

- sc_bool_t pf8100_pmic_irq_service (pmic_id_t id)
  This function services the interrupt for the temp alarm.
- sc_err_t **pf8100_pmic_wdog_enable** (pmic_id_t id, sc_bool_t wd_en, sc_bool_t stby_en, sc_bool_t wdi_stby↩ _active)
- sc_err_t **pf8100_pmic_wdog_disable** (pmic_id_t id, sc_bool_t wd_dis, sc_bool_t stby_en, sc_bool_t wdi_stby↩ _active)
- sc_err_t **pf8100_pmic_wdog_set_timeout** (pmic_id_t id, uint32_t *timeout)
- sc_err_t **pf8100_pmic_wdog_service** (pmic_id_t id)

18.13 platform/drivers/rgpio/fsl_rgpio.h File Reference

Data Structures

- struct rgpio_pin_config_t
  The RGPIO pin configuration structure.

Macros

Driver version

- #define FSL_RGPIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 2))
  RGPIO driver version 2.0.2.

Enumerations

- enum rgpio_pin_direction_t { kRGPIO_DigitalInput = 0U, kRGPIO_DigitalOutput = 1U }
  RGPIO direction definition.

Functions

RGPIO Configuration

- void RGPIO_PinInit (RGPIO_Type *base, uint32_t pin, const rgpio_pin_config_t *config)
  Initializes a RGPIO pin used by the board.
- uint32_t RGPIO_GetInstance (RGPIO_Type *base)
  Gets the RGPIO instance according to the RGPIO base.

RGPIO Output Operations

- static void RGPIO_PinWrite (RGPIO_Type *base, uint32_t pin, uint8_t output)
  Sets the output level of the multiple RGPIO pins to the logic 1 or 0.
- static void RGPIO_WritePinOutput (RGPIO_Type *base, uint32_t pin, uint8_t output)
  Sets the output level of the multiple RGPIO pins to the logic 1 or 0.
- static void RGPIO_PortSet (RGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple RGPIO pins to the logic 1.
- static void RGPIO_SetPinsOutput (RGPIO_Type *base, uint32_t mask)

Sets the output level of the multiple RGPIO pins to the logic 1.

- static void RGPIO_PortClear (RGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple RGPIO pins to the logic 0.
- static void RGPIO_ClearPinsOutput (RGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple RGPIO pins to the logic 0.
- static void RGPIO_PortToggle (RGPIO_Type *base, uint32_t mask)
  Reverses the current output logic of the multiple RGPIO pins.
- static void RGPIO_TogglePinsOutput (RGPIO_Type *base, uint32_t mask)
  Reverses the current output logic of the multiple RGPIO pins.

RGPIO Input Operations

- static uint32_t RGPIO_PinRead (RGPIO_Type *base, uint32_t pin)
  Reads the current input value of the RGPIO port.
- static uint32_t RGPIO_ReadPinInput (RGPIO_Type *base, uint32_t pin)
  Reads the current input value of the RGPIO port.

FGPIO Configuration

- void FGPIO_PinInit (FGPIO_Type *base, uint32_t pin, const rgpio_pin_config_t *config)
  Initializes a FGPIO pin used by the board.
- uint32_t FGPIO_GetInstance (FGPIO_Type *base)
  Gets the FGPIO instance according to the RGPIO base.

FGPIO Output Operations

- static void FGPIO_PinWrite (FGPIO_Type *base, uint32_t pin, uint8_t output)
  Sets the output level of the multiple FGPIO pins to the logic 1 or 0.
- static void FGPIO_WritePinOutput (FGPIO_Type *base, uint32_t pin, uint8_t output)
  Sets the output level of the multiple FGPIO pins to the logic 1 or 0.
- static void FGPIO_PortSet (FGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple FGPIO pins to the logic 1.
- static void FGPIO_SetPinsOutput (FGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple FGPIO pins to the logic 1.
- static void FGPIO_PortClear (FGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple FGPIO pins to the logic 0.
- static void FGPIO_ClearPinsOutput (FGPIO_Type *base, uint32_t mask)
  Sets the output level of the multiple FGPIO pins to the logic 0.
- static void FGPIO_PortToggle (FGPIO_Type *base, uint32_t mask)
  Reverses the current output logic of the multiple FGPIO pins.
- static void FGPIO_TogglePinsOutput (FGPIO_Type *base, uint32_t mask)
  Reverses the current output logic of the multiple FGPIO pins.

FGPIO Input Operations

- static uint32_t FGPIO_PinRead (FGPIO_Type *base, uint32_t pin)
  Reads the current input value of the FGPIO port.
- static uint32_t FGPIO_ReadPinInput (FGPIO_Type *base, uint32_t pin)
  Reads the current input value of the FGPIO port.

18.14 platform/drivers/seco/fsl_seco.h File Reference

Macros

Defines for seco_lifecycle_t

- #define SECO_LIFECYCLE_DEFAULT BIT(0)
  Default fab mode (early_fuses_pgrm not blown)
- #define SECO_LIFECYCLE_FAB BIT(1)
  Fab mode.
- #define SECO_LIFECYCLE_NO_SECRETS BIT(2)
  No secrets.
- #define SECO_LIFECYCLE_SECRETS BIT(3)
  With Secrets.
- #define SECO_LIFECYCLE_SC_FW_CLSD BIT(4)
  SCU FW Closed.
- #define SECO_LIFECYCLE_SECO_FW_CLSD BIT(5)
  SECO FW Closed.
- #define SECO_LIFECYCLE_CLOSED BIT(6)
  Closed.
- #define SECO_LIFECYCLE_CLOSED_FW BIT(7)
  Closed with FW.
- #define SECO_LIFECYCLE_PART_RTN BIT(8,
  Partial field return.
- #define SECO_LIFECYCLE_RTN BIT(9)
  Field return.
- #define SECO_LIFECYCLE_NO_RTN BIT(10)
  No Return.

Defines for seco_snvs_id_t

- #define AHAB_SNVS_ID_INIT 0x00U
  Init SNVS.
- #define AHAB_SNVS_ID_POWER_OFF 0x01U
  Power off the system.
- #define AHAB_SNVS_ID_SRTC 0x02U
  R/W the SRTC.
- #define AHAB_SNVS_ID_SRTC_CALB 0x03U
  R/W the SRTC calibration.
- #define AHAB_SNVS_ID_SRTC_ALRM 0x04U
  R/W the SRTC alarm.
- #define AHAB_SNVS_ID_RTC 0x05U
  R/W the RTC.
- #define AHAB_SNVS_ID_RTC_CALB 0x06U
  R/W the RTC calibration.
- #define AHAB_SNVS_ID_RTC_ALRM 0x07U
  R/W the RTC alarm.
- #define AHAB_SNVS_ID_BTN_CONFIG 0x08U
  R/W the button configuration.
- #define AHAB_SNVS_ID_BTN_MASK 0x09U
  R/W the button mask.
- #define AHAB_SNVS_ID_BTN 0x0AU
  R/W the button state.

- #define AHAB_SNVS_ID_BTN_CLEAR 0x0BU
  Clear the button IRQ.
- #define AHAB_SNVS_ID_SSM_STATE 0x0CU
  Read the SSM state.
- #define AHAB_SNVS_ID_BTN_TIME 0x0DU
  R/W the button time parameters.
- #define AHAB_SNVS_ID_WAKE_UP_IT 0x0EU
  Clear the wake IRQ.

Defines for SNVS access

- #define SECO_SNVS_READ 0U
  SNVS read operation.
- #define SECO_SNVS_WRITE 1U
  SNVS write operation.

Macros for version parsing

- #define SECO_PROD_VER(X) (((X) >> 16) & 0x7FFFUL)
  Extract SECO production ver.
- #define SECO_MAJOR_VER(X) (((X) >> 4) & 0xFFFUL)
  Extract SECO major ver.
- #define SECO_MINOR_VER(X) ((X) & 0xFUL)
  Extract SECO minor ver.

Defines for V2X state

- #define V2X_STATE_AUTH_RX 0x01U
  Authentication request received.
- #define V2X_STATE_PROV_NORMAL 0x02U
  Provisioned successfully in normal mode.
- #define V2X_STATE_PROV_DEBUG 0x04U
  Provisioned successfully in debug mode.
- #define V2X_STATE_AUTH_IP 0x08U
  Authentication on going.
- #define V2X_STATE_AUTH_SUCCESS 0x10U
  Authentication success.
- #define V2X_STATE_AUTH_FAIL 0x20U
  Authentication failure.
- #define V2X_STATE_CRYPTO_DIS 0x40U
  Crypto accelerators disabled.
- #define V2X_STATE_HOLD_EN 0x80U
  V2X provisioning on hold.

Typedefs

- typedef uint16_t seco_lifecycle_t
  This type is used to return the lifecycle.
- typedef uint8_t seco_snvs_id_t
  This type is used to indicate the ID of anSNVS register to access.

Functions

Initialization Functions

- void SECO_Init (boot_phase_t phase)
  This function initializes the SECO driver.
- void SECO_CAAM_Config (uint16_t master, sc_bool_t lock, sc_rm_spa_t sa, sc_rm_did_t did, sc_rm_sid_t sid)
  This function configures the CAAM MP.
- void SECO_ClearCache (void)
  This function clears the CAAM MP cache.
- void SECO_MU_Config (uint8_t mu, sc_rm_spa_t sa, sc_rm_did_t did)
  This function configures MU ownership.
- uint16_t SECO_SetMonoCounterPartition (uint16_t she)
  This function partitions the monotonic counter.
- uint32_t SECO_SetFipsMode (uint8_t mode)
  This function configures the SECO in FIPS mode.

Power Mangement Functions

- void SECO_Power (sc_sub_t ss, uint32_t inst, sc_bool_t up)
  This function notifies SECO that a subsystem power state has changed.
- void SECO_CAAM_PowerDown (void)
  This function notifies SECO that CAAM is powering down.
- void SECO_EnterLPM (void)
  This function notifies SECO the system is entering low power mode.
- void SECO_ExitLPM (void)
  This function notifies SECO the system is has exited low power mode.

Image Functions

- void SECO_Image_Load (sc_faddr_t addr_src, sc_faddr_t addr_dst, uint32_t len, sc_bool_t fw)
  This function loads a SECO image.
- void SECO_Authenticate (sc_seco_auth_cmd_t cmd, sc_faddr_t addr, uint32_t mask1, uint32_t mask2)
  This function is used to authenticate a SECO image or command.

Lifecycle Functions

- seco_lifecycle_t SECO_Get_Lifecycle (void)
  This function is used get the lifecycle from the ADM.
- void SECO_ForwardLifecycle (uint32_t change)
  This function updates the lifecycle of the device.
- void SECO_ReturnLifecycle (sc_faddr_t addr)
  This function updates the lifecycle to one of the return lifecycles.
- void SECO_Commit (uint32_t *info)
  This function is used to commit into the fuses any new SRK revocation and FW version information that have been found in the primary and secondary containers.

Attestation Functions

- void SECO_AttestMode (uint32_t mode)
  This function is used to set the attestation mode.

- void SECO_Attest (uint64_t nonce)
  This function is used to request atestation.
- void SECO_GetAttestPublicKey (sc_faddr_t addr)
  This function is used to retrieve the attestation public key.
- void SECO_GetAttestSign (sc_faddr_t addr)
  This function is used to retrieve attestation signature and parameters.
- void SECO_AttestVerify (sc_faddr_t addr)
  This function is used to verify attestation.

Key Functions

- void SECO_GenKeyBlob (uint32_t id, sc_faddr_t load_addr, sc_faddr_t export_addr, uint16_t max_size)
  This function is used to generate a SECO key blob.
- void SECO_LoadKey (uint32_t id, sc_faddr_t addr)
  This function is used to load a SECO key.

Manufacturing Protection Functions

- void SECO_GetMPKey (sc_faddr_t dst_addr, uint16_t dst_size)
  This function is used to get the manufacturing protection public key.
- void SECO_UpdateMPMR (sc_faddr_t addr, uint8_t size, uint8_t lock)
  This function is used to update the manufacturing protection message register.
- void SECO_GetMPSign (sc_faddr_t msg_addr, uint16_t msg_size, sc_faddr_t dst_addr, uint16_t dst_size)
  This function is used to get the manufacturing protection signature.

V2X Functions

- uint8_t SECO_V2X_Forward (uint32_t *buf)
  This function is used to forward a message received from V2X.
- void SECO_V2X_Ping (void)
  This function sends a ping to V2X through SECO.
- void SECO_V2X_Hold (uint32_t hold_value)
  This function is used to set a control variable indicating whether or not the configuration of the V2X must be done as soon as possible or should be delayed and left under the control of the SCU.
- void SECO_V2X_Provision (uint32_t provision_mode)
  This function is used to provision the V2X either in "normal" mode or in "debug" mode.
- uint32_t SECO_V2X_GetState (uint32_t *req_status)
  This function returns the v2x_state (provisioned, successfully authenticated, etc.).

Debug Functions

- void SECO_Version (uint32_t *version, uint32_t *commit, sc_bool_t *dirty)
  This function is used to return the SECO FW build info.
- void SECO_ChipInfo (uint16_t *lc, uint16_t *monotonic, uint32_t *uid_l, uint32_t *uid_h)
  This function is used to return SECO chip info.
- void SECO_AttachDebug (void)
  This function notifies SECO that a JTAG connection has been made.
- void SECO_EnableDebug (sc_faddr_t addr)
  This function securely enables debug.
- uint32_t SECO_GetEvent (uint8_t idx)
  This function is used to return an event from the SECO error log.
- void SECO_DumpDebug (void)

This function dumps low-level SECO debug info to the SCU debug UART.

- uint32_t SECO_ErrNumber (void)

  This function return the internal SECO error number returned by the last SECO function call.

Miscellaneous Functions

- void SECO_Ping (void)

  This function sends a ping to SECO.
- void SECO_KickWdog (void)

  This function sends a a message to SECO to service the 24H watchdog.
- void SECO_WriteFuse (uint32_t word, uint32_t val)

  This function writes a given fuse word index.
- void SECO_SecureWriteFuse (sc_faddr_t addr)

  This function securely writes a group of fuse words.
- void SECO_ScuPatch (sc_faddr_t addr)

  This function applies a patch.
- sc_seco_rng_stat_t SECO_StartRNG (void)

  This function starts the random number generator.
- void SECO_SABSignedMesg (sc_faddr_t addr)

  This function is used to send a generic signed message to the SECO SHE/HSM components.

SNVS Functions

- void SECO_WriteSNVS (seco_snvs_id_t id, uint32_t val)

  This function write an SNVS parameter.
- uint32_t SECO_ReadSNVS (seco_snvs_id_t id)

  This function reads an SNVS parameter.
- void SECO_ManageSNVS (uint8_t id, uint8_t access, uint32_t *val, uint8_t size)

  This function is used to manage the SNVS.
- void SECO_ManageSNVS_DGO (uint8_t id, uint8_t access, uint32_t *val)

  This function is used to manage the SNVS DGO.

Variables

- sc_err_t seco_err

  SECO error return.

18.15 platform/drivers/snvs/fsl_snvs.h File Reference

Macros

Defines for snvs_btn_config_t

Used to configure which feature of the button (BTN) input signal constitutes "active".

BTN_CONFIG field in the SNVS_HP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_CONFIG_ACTIVELOW 0U

  Button signal is active low.
- #define SNVS_DRV_BTN_CONFIG_ACTIVEHIGH 1U

  Button signal is active high.

- #define SNVS_DRV_BTN_CONFIG_RISINGEDGE 2U

  Button signal is active on the rising edge.
- #define SNVS_DRV_BTN_CONFIG_FALLINGEDGE 3U

  Button signal is active on the falling edge.
- #define SNVS_DRV_BTN_CONFIG_ANYEDGE 4U

  Button signal is active on any edge.

Defines for snvs_btn_on_time_t

Used to configure the period of time after BTN is asserted before SoC power is turned on.

ON_TIME field in the SNVS_LP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_ON_50MS 0U

  500 msec off->on transition time
- #define SNVS_DRV_BTN_ON_100MS 1U

  50 msec off->on transition time
- #define SNVS_DRV_BTN_ON_500MS 2U

  100 msec off->on transition time
- #define SNVS_DRV_BTN_ON_0MS 3U

  0 msec off->on transition time

Defines for snvs_btn_debounce_t

Use to configure the amount of debounce time for the BTN input signal.

DEBOUNCE field in the SNVS_LP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_DEBOUNCE_50MS 0U

  50 msec debounce
- #define SNVS_DRV_BTN_DEBOUNCE_100MS 1U

  100 msec debounce
- #define SNVS_DRV_BTN_DEBOUNCE_500MS 2U

  500 msec debounce
- #define SNVS_DRV_BTN_DEBOUNCE_0MS 3U

  0 msec debounce

Defines for snvs_btn_press_time_t

Used to configure the button press time out values for the PMIC logic.

BTN_PRESS_TIME field in the SNVS_LP regsiter. See the SNVS section of the SRM.

- #define SNVS_DRV_BTN_PRESS_5S 0U

  5 secs
- #define SNVS_DRV_BTN_PRESS_10S 1U

  10 secs
- #define SNVS_DRV_BTN_PRESS_15S 2U

  15 secs
- #define SNVS_DRV_BTN_PRESS_OFF 3U

  Long press disabled.

Typedefs

- typedef uint8_t snvs_btn_config_t

  This type is used configure the button active state.
- typedef uint8_t snvs_btn_on_time_t

  This type is used configure the button on time.
- typedef uint8_t snvs_btn_debounce_t

  This type is used configure the button debounce time.
- typedef uint8_t snvs_btn_press_time_t

  This type is used configure the button press time.

Functions

Initialization Functions

- void SNVS_Init (boot_phase_t phase)

  Initialize SNVS driver.

SRTC Functions

- sc_err_t snvs_err

  SNVS error return.
- void SNVS_PowerOff (void)

  Power off system.
- void SNVS_SetSecureRtc (uint32_t seconds)

  Set the secure RTC.
- void SNVS_GetSecureRtc (uint32_t *seconds)

  Get the secure RTC.
- void SNVS_SetSecureRtcCalb (int8_t count)

  Set the secure RTC calibration value.
- void SNVS_GetSecureRtcCalb (int8_t *count)

  Get the secure RTC calibration value.
- void SNVS_SetSecureRtcAlarm (uint32_t seconds)

  Set secure RTC alarm.
- void SNVS_GetSecureRtcAlarm (uint32_t *seconds)

  Get secure RTC alarm.
- void SNVS_SetRtc (uint32_t seconds)

  Set the RTC.
- void SNVS_GetRtc (uint32_t *seconds)

  Get the RTC.
- void SNVS_SetRtcCalb (int8_t count)

  Set the RTC calibration value.
- void SNVS_SetRtcAlarm (uint32_t seconds)

  Set RTC alarm.
- void SNVS_GetRtcAlarm (uint32_t *seconds)

  Get RTC alarm.

- void SNVS_ConfigButton (snvs_btn_config_t config, sc_bool_t enable)

  Configure the ON/OFF button.
- void SNVS_ButtonTime (snvs_btn_on_time_t on, snvs_btn_debounce_t debounce, snvs_btn_press_time_t press)

  Configure the ON/OFF button timing parameters.
- sc_bool_t SNVS_GetButtonStatus (void)

  Get button status.
- void SNVS_ClearButtonIRQ (void)

  Clear button IRQ.
- void SNVS_EnterLPM (void)

  Enter low power mode.
- void SNVS_ExitLPM (void)

  Exit low power mode.
- uint32_t SNVS_GetState (void)

  Get the SNVS System Security Monitor State (SSM).
- void SNVS_SecurityViolation_Enable (void)

  Enable SNVS Security Violation Interrupt.
- void SNVS_SecurityViolation_IRQHandler (void)

  SNVS security violation IRQ handler.
- void SNVS_PowerOff_IRQHandler (void)

  SNVS power off IRQ handler.
- uint32_t SNVS_ReadGP (uint8_t idx)

  Read a GP register.
- void SNVS_WriteGP (uint8_t idx, uint32_t val)

  Write a GP register.
- void SNVS_SecVio (uint8_t id, uint8_t access, uint32_t *data0, uint32_t *data1, uint32_t *data2, uint32_t *data3, uint32_t *data4, uint8_t size)

  Manage security violation and tamper.
- void SNVS_SecVioDgo (uint8_t id, uint8_t access, uint32_t *data)

  Manage security violation and tamper of DGO.
- void SNVS_IncTime (uint32_t secs)

  Simulation function to increment time.

18.16 platform/drivers/wdog32/fsl_wdog32.h File Reference

Data Structures

- struct wdog32_work_mode_t

  Defines WDOG32 work mode.
- struct wdog32_config_t

  Describes WDOG32 configuration structure.

Macros

Unlock sequence

- #define WDOG_FIRST_WORD_OF_UNLOCK (WDOG_UPDATE_KEY & 0xFFFFU)
  First word of unlock sequence.
- #define WDOG_SECOND_WORD_OF_UNLOCK ((WDOG_UPDATE_KEY >> 16U) & 0xFFFFU)
  Second word of unlock sequence.

Refresh sequence

- #define WDOG_FIRST_WORD_OF_REFRESH (WDOG_REFRESH_KEY & 0xFFFFU)
  First word of refresh sequence.
- #define WDOG_SECOND_WORD_OF_REFRESH ((WDOG_REFRESH_KEY >> 16U) & 0xFFFFU)
  Second word of refresh sequence.

Driver version

- #define FSL_WDOG32_DRIVER_VERSION (MAKE_VERSION(2, 0, 3))
  WDOG32 driver version.

Enumerations

- enum wdog32_clock_source_t { kWDOG32_ClockSource0 = 0U, kWDOG32_ClockSource1 = 1U, kWDOG32_ClockSource2 = 2U, kWDOG32_ClockSource3 = 3U }
  Describes WDOG32 clock source.
- enum wdog32_clock_prescaler_t { kWDOG32_ClockPrescalerDivide1 = 0x0U, kWDOG32_ClockPrescalerDivide256 = 0x1U }
  Describes the selection of the clock prescaler.
- enum wdog32_test_mode_t { kWDOG32_TestModeDisabled = 0U, kWDOG32_UserModeEnabled = 1U, kWDOG32_LowByteTest = 2U, kWDOG32_HighByteTest = 3U }
  Describes WDOG32 test mode.
- enum _wdog32_interrupt_enable_t { kWDOG32_InterruptEnable = WDOG_CS_INT_MASK }
  WDOG32 interrupt configuration structure.
- enum _wdog32_status_flags_t { kWDOG32_RunningFlag = WDOG_CS_EN_MASK, kWDOG32_InterruptFlag = WDOG_CS_FLG_MASK }
  WDOG32 status flags.

Functions

WDOG32 Initialization and De-initialization

- void WDOG32_GetDefaultConfig (wdog32_config_t *config)
  Initializes the WDOG32 configuration structure.
- AT_QUICKACCESS_SECTION_CODE (void WDOG32_Init(WDOG_Type *base, const wdog32_config_t *config))
  Initializes the WDOG32 module.
- void WDOG32_Deinit (WDOG_Type *base)
  De-initializes the WDOG32 module.

WDOG32 functional Operation

- static void WDOG32_Enable (WDOG_Type *base)
  Enables the WDOG32 module.
- static void WDOG32_Disable (WDOG_Type *base)
  Disables the WDOG32 module.
- static void WDOG32_EnableInterrupts (WDOG_Type *base, uint32_t mask)
  Enables the WDOG32 interrupt.
- static void WDOG32_DisableInterrupts (WDOG_Type *base, uint32_t mask)
  Disables the WDOG32 interrupt.
- static uint32_t WDOG32_GetStatusFlags (WDOG_Type *base)
  Gets the WDOG32 all status flags.
- AT_QUICKACCESS_SECTION_CODE (void WDOG32_ClearStatusFlags(WDOG_Type *base, uint32_t mask))
  Clears the WDOG32 flag.
- static void WDOG32_SetTimeoutValue (WDOG_Type *base, uint16_t timeoutCount)
  Sets the WDOG32 timeout value.
- static void WDOG32_SetWindowValue (WDOG_Type *base, uint16_t windowValue)
  Sets the WDOG32 window value.
- static void WDOG32_Unlock (WDOG_Type *base)
  Unlocks the WDOG32 register written.
- static void WDOG32_Refresh (WDOG_Type *base)
  Refreshes the WDOG32 timer.
- static uint16_t WDOG32_GetCounterValue (WDOG_Type *base)
  Gets the WDOG32 counter value.

18.17 platform/main/board.h File Reference

Header file containing the board API.

Macros

- #define BOARD_PARM_RTN_NOT_USED 0U
  Feature not used.
- #define BOARD_PARM_RTN_USED 1U
  Feature used.
- #define BOARD_PARM_RTN_EXTERNAL 2U
  Return value for BOARD_PARM_PCIE_PLL.
- #define BOARD_PARM_RTN_INTERNAL 3U
  Return value for BOARD_PARM_PCIE_PLL.
- #define BOARD_PARM_RTN_INTERNAL_DPLL 4U
  Return value for BOARD_PARM_PCIE_PLL (DXL only)
- #define BOARD_PARM_RTN_DPLL_SS_0_5 0U
  0.5% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_DPLL_SS_1 1U
  1% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_DPLL_SS_1_5 2U
  1.5% spread of PCIE DPLL frequency.
- #define BOARD_PARM_RTN_DPLL_SS_2 3U

2% spread of PCIE DPLL frequency.

- #define BOARD_PARM_RTN_VDD_MEMC_NOM 0U

  MEMC Nominal.

- #define BOARD_PARM_RTN_VDD_MEMC_OD 1U

  MEMC Overdrive.

- #define BOARD_PARM_KS1_RETENTION_DISABLE 0U

  Disable retention during KS1.

- #define BOARD_PARM_KS1_RETENTION_ENABLE 1U

  Enable retention during KS1.

- #define BOARD_PARM_KS1_ONOFF_WAKE_DISABLE 0U

  Disable ONOFF wakeup during KS1.

- #define BOARD_PARM_KS1_ONOFF_WAKE_ENABLE 1U

  Enable ONOFF wakeup during KS1.

- #define BOARD_PARM_KS1_WDOG_WAKE_ENABLE 0U

  Enable SC WDOG service during KS1 (required for ON_OFF wakeup on some devices)

- #define BOARD_PARM_KS1_WDOG_WAKE_DISABLE 1U

  Disable SC WDOG service during KS1 (SC WDOG disabled during KS1)

- #define BOARD_PARM_SSC_N_0P4 4U

  Return 0.4% fspread for PLL spread spectrum.

- #define BOARD_PARM_SSC_N_1P0 10U

  Return 1.0% fspread for PLL spread spectrum.

- #define BOARD_PARM_SSC_N_1P4 14U

  Return 1.4% fspread for PLL spread spectrum.

- #define BOARD_PARM_SSC_N_2P0 20U

  Return 2.0% fspread for PLL spread spectrum.

- #define BRD_ERR(X)

  Macro for debug of board calls.

Macros for DCD processing

- #define **DATA4**(A, V) ∗((volatile uint32_t∗)(A)) = U32(V)
- #define **SET_BIT4**(A, V) ∗((volatile uint32_t∗)(A)) |= U32(V)
- #define **CLR_BIT4**(A, V) ∗((volatile uint32_t∗)(A)) &= ∼(U32(V))
- #define **CHECK_BITS_SET4**(A, M)
- #define **CHECK_BITS_CLR4**(A, M)
- #define **CHECK_ANY_BIT_SET4**(A, M)
- #define **CHECK_ANY_BIT_CLR4**(A, M)

Typedefs

- typedef uint32_t board_parm_rtn_t

  Board config parameter returns.

Enumerations

- enum board_parm_t {
  BOARD_PARM_PCIE_PLL = 0, BOARD_PARM_KS1_RESUME_USEC = 1, BOARD_PARM_KS1_RETENTION = 2, BOARD_PARM_KS1_ONOFF_WAKE = 3,
  BOARD_PARM_REBOOT_TIME = 4, BOARD_PARM_DC0_PLL0_SSC = 5, BOARD_PARM_DC0_PLL1_SSC = 6, BOARD_PARM_DC1_PLL0_SSC = 7,
  BOARD_PARM_DC1_PLL1_SSC = 8, BOARD_PARM_ISI_PIX_FREQ = 9, BOARD_PARM_VDD_MEMC = 10,
  BOARD_PARM_KS1_WDOG_WAKE = 11,
  BOARD_PARM_PCIE_DPLL_SS = 12 }

  Board config parameter types.
- enum sc_bfault_t {
  BOARD_BFAULT_COMMON = 0, BOARD_BFAULT_CPU = 1, BOARD_BFAULT_EXIT = 2, BOARD_BFAULT_DDR_RET = 3,
  BOARD_BFAULT_REBOOT = 4, BOARD_BFAULT_BAD_CONTAINER = 5, BOARD_BFAULT_BRD_FAIL = 6,
  BOARD_BFAULT_TEST_FAIL = 7,
  BOARD_BFAULT_DDR_INIT_FAIL = 8 }

  Board fault types.
- enum board_reboot_to_t { BOARD_REBOOT_TO_NONE = 0, BOARD_REBOOT_TO_FORCE = 1, BOARD_REBOOT_TO_FAULT = 2 }

  Board reboot timeout actions.
- enum board_cpu_rst_ev_t { **BOARD_CPU_RESET_SELF** = 0, **BOARD_CPU_RESET_WDOG** = 1, **BOARD_CPU_RESET_LOCKUP** = 2, **BOARD_CPU_RESET_MEM_ERR** = 3 }

  Board reset event types for CPUs.
- enum board_ddr_action_t {
  BOARD_DDR_COLD_INIT = 0, BOARD_DDR_PERIODIC = 1, BOARD_DDR_SR_DRC_ON_ENTER = 2, BOARD_DDR_SR_DRC_ON_EXIT = 3,
  BOARD_DDR_SR_DRC_OFF_ENTER = 4, BOARD_DDR_SR_DRC_OFF_EXIT = 5, BOARD_DDR_PERIODIC_HALT = 6, BOARD_DDR_PERIODIC_RESTART = 7,
  BOARD_DDR_DERATE_PERIODIC = 8, BOARD_DDR0_VREF = 9, BOARD_DDR1_VREF = 10 }

  DDR actions (power state transitions, etc.)

Functions

Initialization Functions

- void board_init (boot_phase_t phase)

  This function initalizes the board.
- LPUART_Type * board_get_debug_uart (uint8_t *inst, uint32_t *baud)

  This function returns the debug UART info.
- void board_config_debug_uart (sc_bool_t early_phase)

  This function initalizes the debug UART.
- void board_disable_debug_uart (void)

  This function powers off the debug UART.
- void board_config_sc (sc_rm_pt_t pt_sc)

  This function configures SCU resources.
- board_parm_rtn_t board_parameter (board_parm_t parm)

  This function returns board configuration info.
- sc_bool_t board_rsrc_avail (sc_rsrc_t rsrc)

  This function returns resource availability info.
- sc_err_t board_init_ddr (sc_bool_t early, sc_bool_t ddr_initialized)

  This function initalizes DDR.

- sc_err_t board_ddr_config (bool rom_caller, board_ddr_action_t action)
  This function cinfigures the DDR.
- void board_system_config (sc_bool_t early, sc_rm_pt_t pt_boot)
  This function allows the board file to do SCFW configuration.
- sc_bool_t board_early_cpu (sc_rsrc_t cpu)
  This function returns SC_TRUE for early CPUs.

Power Functions

- void board_set_power_mode (sc_sub_t ss, uint8_t pd, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
  This function transitions the power state for an external board- level supply which goes to the i.MX8.
- sc_err_t board_set_voltage (sc_sub_t ss, uint32_t new_volt, uint32_t old_volt)
  This function sets the voltage for a PMIC controlled SS.
- void board_lpm (sc_pm_power_mode_t mode)
  This function is used to set power supplies of the board when entering and exiting low power mode.
- void board_trans_resource_power (sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
  This function transitions the power state for an external board- level supply which goes to a board component.
- void board_rsrc_reset (sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, sc_rm_pt_t pt)
  This function resets a board resource.

Misc Functions

- sc_err_t board_power (sc_pm_power_mode_t mode)
  This function is used to set the board power.
- sc_err_t board_reset (sc_pm_reset_type_t type, sc_pm_reset_reason_t reason, sc_rm_pt_t pt)
  This function is used to reset the system.
- void board_cpu_reset (sc_rsrc_t resource, board_cpu_rst_ev_t reset_event, sc_rm_pt_t pt)
  This function is called when a CPU encounters a reset event.
- void board_reboot_part (sc_rm_pt_t pt, sc_pm_reset_type_t *type, sc_pm_reset_reason_t *reason, sc_pm_power_mode_t *mode, uint32_t *mask)
  This function is called when a partition reboot is requested.
- void board_reboot_part_cont (sc_rm_pt_t pt, sc_rsrc_t *boot_cpu, sc_rsrc_t *boot_mu, sc_rsrc_t *boot_dev, sc_faddr_t *boot_addr)
  This function is called when a partition reboot is has powered off the partition but has not yet powered it back on.
- board_reboot_to_t board_reboot_timeout (sc_rm_pt_t pt)
  This function is called when a partition reboot times out.
- void board_panic (sc_dsc_t dsc)
  This function is called when a SS (other than SCU) reports a panic temp alarm.
- void board_fault (sc_bool_t restarted, sc_bfault_t reason, sc_rm_pt_t pt)
  This function is called when a fault is detected or the SCFW returns from main().
- void board_security_violation (void)
  This function is called when a security violation is reported by the SECO or SNVS.
- sc_bool_t board_get_button_status (void)
  This function is used to return the current status of the ON/OFF button.
- sc_err_t board_set_control (sc_rsrc_t resource, sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, uint32_t ctrl, uint32_t val)
  This function sets a miscellaneous control value.
- sc_err_t board_get_control (sc_rsrc_t resource, sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, uint32_t ctrl, uint32_t *val)
  This function gets a miscellaneous control value.
- void board_tick (uint16_t msec)

This function is called periodically to tick the board.

- sc_err_t board_ioctl (sc_rm_pt_t caller_pt, sc_rsrc_t mu, uint32_t *parm1, uint32_t *parm2, uint32_t *parm3)

  This function is called when sc_misc_board_ioctl() is called.
- void PMIC_IRQHandler (void)

  Interrupt handler for the PMIC.
- void SNVS_Button_IRQHandler (void)

  Interrupt handler for the SNVS button.

Variables

- const sc_rm_idx_t board_num_rsrc

  External variable for accessing the number of board resources.
- const sc_rsrc_map_t board_rsrc_map [BRD_NUM_RSRC_BRD]

  External variable for accessing the board resource map.
- const uint32_t board_ddr_period_ms

  External variable for specing DDR periodic training.
- const uint32_t board_ddr_derate_period_ms

  External variable for DDR periodic derate.

18.17.1 Detailed Description

Header file containing the board API.

18.18 platform/main/ipc.h File Reference

Header file for the IPC implementation.

Functions

- sc_err_t sc_ipc_open (sc_ipc_t *ipc, sc_ipc_id_t id)

  This function opens an IPC channel.
- void sc_ipc_close (sc_ipc_t ipc)

  This function closes an IPC channel.
- void sc_ipc_read (sc_ipc_t ipc, void *data)

  This function reads a message from an IPC channel.
- void sc_ipc_write (sc_ipc_t ipc, const void *data)

  This function writes a message to an IPC channel.

18.18.1 Detailed Description

Header file for the IPC implementation.

18.18.2 Function Documentation

18.18.2.1 sc_ipc_open()

```
sc_err_t sc_ipc_open (
             sc_ipc_t * ipc,
             sc_ipc_id_t id )
```

This function opens an IPC channel.

Parameters

out	*ipc*	return pointer for ipc handle
in	*id*	id of channel to open

Returns

Returns an error code (SC_ERR_NONE = success, SC_ERR_IPC otherwise).

The *id* parameter is implementation specific. Could be an MU address, pointer to a driver path, channel index, etc.

18.18.2.2 sc_ipc_close()

```
void sc_ipc_close (
            sc_ipc_t ipc )
```

This function closes an IPC channel.

Parameters

in	*ipc*	id of channel to close

18.18.2.3 sc_ipc_read()

```
void sc_ipc_read (
            sc_ipc_t ipc,
            void * data )
```

This function reads a message from an IPC channel.

Parameters

in	*ipc*	id of channel read from
out	*data*	pointer to message buffer to read

This function will block if no message is available to be read.

18.18.2.4 sc_ipc_write()

```
void sc_ipc_write (
            sc_ipc_t ipc,
            const void * data )
```

This function writes a message to an IPC channel.

Parameters

in	*ipc*	id of channel to write to
in	*data*	pointer to message buffer to write

This function will block if the outgoing buffer is full.

18.19 platform/main/soc.h File Reference

Header file containing the SoC API.

Data Structures

- struct soc_patch_area_list_t
- struct soc_freq_volt_tbl_t
- struct soc_gpu_clks_opp_t
- struct soc_cpu_state_t

  Stores CPU power state info.
- struct soc_cluster_state_t

  Stores cluster power state info.
- struct soc_multicluster_state_t

  Stores multi-cluster power state info.
- struct soc_m4_state_t

  Stores M4 sleep state info.
- struct soc_sys_if_node_t

  Stores system interface node resource info.
- struct soc_sys_if_req_t

  Stores system interface power mode reqest info.
- struct soc_hmp_node_t

  Stores HMP node power mode info.
- struct soc_fspi_ret_info_t

  Stores HMP FSPI retention info.
- struct soc_hmp_t

  Stores HMP system power mode info.
- struct soc_ddr_ret_region_t
- struct soc_ddr_ret_info_t

  Stores DDR retention info.
- struct soc_dqs2dq_sync_info_t

  Stores DQS2DQ synchronization info.
- struct soc_msi_ring_usecount_t

  Stores MSI ring usecount.

Macros

- #define STC_RCAT_SETCAT(SS, CAT, CATMASK, CMP)

  Macro to configure an STC category.
- #define STC_RCAT_SETSTARTSTOPTDM(SS, CAT, TDM, START, STOP)

  Macro to set an STC TDM.
- #define STC_RCAT_GETHPR(SS, CAT)

  Macro to get an STC HPR.
- #define STC_RCAT_SETHPR(SS, CAT, HPR)

  Macro to set an STC HPR.
- #define STC_QOS_PANIC(SS, CAT, QOS)

  Macro to set an STC QoS panic.
- #define STC_UD_THRESHOLD1(SS, CAT, TH, QOS)

  Macro to set an STC threshold.
- #define STC_UD_THRESHOLD2(SS, CAT, TH, QOS)

  Macro to set an STC threshold 2.
- #define STC_UD_DIS(SS)

  Macro to disable an STC underrun detect.
- #define **SOC_SYS_IF_NO_SAVE** (SC_PM_PW_MODE_ON + 1U)
- #define SOC_RR 1U

  Reset reason SNVS persistant storage register.
- #define SOC_RR_CHECK(X) ((((X) >> 24U) & 0xFFUL) == 0xCCUL)

  Macro to check if reset reason is valid.
- #define SOC_RR_INFO(R, P) ((0xCCUL << 24U) | (U32(R) << 8U) | U32(P))

  Macro to set the reset reason.
- #define SOC_RR_REASON(X) (((X) >> 8U) & 0xFFUL)

  Macro to extract the reset reason.
- #define SOC_RR_PT(X) (((X) >> 0U) & 0xFFUL)

  Macro to extract the resetting partition.

Defines for patch ID

- #define **SC_PATCH_ID_NONE** 0x00U /* Non patch - end marker */
- #define **SC_PATCH_ID_SCU** 0x55U /* SCU ROM patch */
- #define **SC_PATCH_ID_SECO** 0x45U /* SECO ROM patch */
- #define **SC_PATCH_ID_V2X** 0x57U /* V2X primary ROM patch */
- #define **SC_PATCH_ID_V2X2** 0x59U /* V2X secondary ROM patch */
- #define **SC_PATCH_ID_C2XS** 0x5AU /* V2X ROM patch SHA value */
- #define **SC_PATCH_ID_CTRL** 0x5BU /* Patch control */
- #define **SC_PATCH_ID_ALL** 0xFFU /* All patch IDs */

Functions

Initialization Functions

- void soc_init_common (boot_phase_t phase)

  This function initalizes the parts of the SoC.
- void soc_init (boot_phase_t phase)

  This function initalizes the SoC specific parts of the chip.

- void soc_config_sc (sc_rm_pt_t pt_sc, sc_rm_pt_t pt_boot)
  This function configures SCU resources.
- void soc_config_seco (void)
  This function configures SECO resources.
- void soc_db_stc_config (void)
  Configure the STCs in the DB when it is powered up.
- void soc_init_fused_rsrc (void)
  This function fills in a bit array with info about disabled resources.
- void soc_ss_notavail (sc_sub_t ss)
  This function configures a subsystem as not available.
- void soc_init_refgen (void)
  This function initalizes the refgen trims from the fuses.
- void soc_analog_fuse_init (void)
  This function initalize regulator, repeater and osc trims from the fuses.

Info Functions

- void soc_set_reset_info (sc_pm_reset_reason_t reason, sc_rm_pt_t pt)
  This function saves reset info into persistant storage.
- sc_pm_reset_reason_t soc_reset_reason (void)
  Return reset reason.
- sc_rm_pt_t soc_reset_part (void)
  Return partition causing reset.
- sc_bool_t soc_rsrc_avail (sc_rsrc_t rsrc)
  This function returns if a resource is available.
- uint32_t soc_get_temp_trim (sc_dsc_t dsc)
  This function returns the trim value for a temp sensor.
- int8_t soc_get_temp_ofs (sc_dsc_t dsc)
  This function returns the offset value for a temp sensor.
- uint32_t soc_get_max_freq (sc_dsc_t dsc_id)
  This function returns the maximum frequency limited by the fuses for the GPU and AP cores.
- sc_bool_t soc_enet_get_freq_limit (sc_rsrc_t enet_rsrc)
  This function checks if the frequency is limited by fuse.
- void soc_get_max_freq_fuse (void)
  Initialize the maximum frequency of certain resources based on fuses.
- sc_bool_t soc_pd_switchable (sc_dsc_t dsc, uint32_t pd)
  This function identifies if the given pd has internal or external switches.
- sc_bool_t soc_pd_retention (sc_dsc_t dsc, uint32_t pd)
  This function checks if the given power domain of the given dsc supports retention.
- sc_bool_t soc_ss_has_bias (sc_sub_t ss)
  This function checks if the given subsystem has forward body-bias.
- dsc_ai_type_t soc_ss_ai_type (sc_sub_t ss)
  This function returns the subsystem AI type, mainly used to identify if an SS has temp sensor.
- uint32_t soc_mem_type (sc_dsc_t dsc, uint32_t pd)
  Return the type of memory used in the given PD of the DSC.
- uint8_t soc_mem_pwr_plane (sc_dsc_t dsc_id)
  This function returns the uniquely defined memory power plane for the given dsc id.
- void soc_dsc_clock_info (dsc_clk_type_t *clk_type, uint32_t *idx, sc_pm_clk_parent_t *parent)
  Return the DSCMIX clock slice index and type.
- uint32_t soc_get_clock_div (sc_dsc_t dsc, uint8_t *pll_div)
  Return the DSCMIX clock slice divider and pll-divided output connected to all the slices in the dsc.
- sc_bool_t soc_slice_is_dsc (const dsc_clk_info_t *clk_info)
  Checks if the given clock slice is the DSCMIX slice.
- uint8_t soc_get_avpll_ssc_n (sc_dsc_t dsc, uint8_t pll_index)

This function returns spread spectrum info required to setup the AVPLL.

- sc_bool_t soc_gpu_freq_hw_limited (void)
  This function checks if the GPU frequency is HW limited based on fuses.
- void soc_rompatch_checksum (uint32_t *checksum, uint16_t len)
  Calculate and return the ROM patch checksum.

Analog Functions

- void soc_setup_anamix (sc_bool_t enable)
  Enable/Disable anamix in some SS during init and low power mode.
- void soc_dsc_powerup_anamix (sc_dsc_t dsc)
  This function powers up the DSC anamix.
- void soc_dsc_powerup_phymix (sc_dsc_t dsc)
  This function powers up the DSC phymix.
- void soc_dsc_powerdown_anamix (sc_dsc_t dsc)
  This function powers down the DSC anamix.
- void soc_dsc_powerdown_phymix (sc_dsc_t dsc)
  This function powers down the DSC phymix.
- void soc_setup_hsio_repeater (board_parm_rtn_t internal_clk, sc_bool_t enable)
  Setup HSIO repeaters for internal or external PCIE clock.
- void soc_set_bias (sc_sub_t ss, uint8_t bias_mask, sc_bool_t enable, uint32_t delay)
  Setup the Forward body-bias for the given subsystem.
- uint32_t soc_dpll_dco_pc (sc_dsc_t dsc, uint8_t pll_index, uint32_t rate)
  Return the DPLL DCO-P trim value.
- void soc_dpll_populate_tbl (void)
  Populate the DPLL DCO-PC values based on fuses.

Power Functions

- sc_err_t soc_set_freq_voltage (sc_sub_t ss, uint32_t old_freq, uint32_t *new_freq, sc_bool_t pmic_change)
  Set the voltage based on the frequency for SS controlled by PMIC rail.
- void soc_trans_pd (sc_sub_t ss, uint8_t pd, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_↩ mode)
  Handle SoC and board level power transitions required to power up or down a power domain.
- sc_bool_t soc_bias_enabled (sc_sub_t ss)
  Check if the Forward body bias is enabled for the cluster, this function is only valid for the AP clusters.
- sc_bool_t soc_ss_has_vd_detect (sc_dsc_t dsc, sc_pm_clock_rate_t rate)
  Check if the new PLL rate is below the max freq vd-detect in the SS can support.
- void soc_trans_bandgap (sc_sub_t ss, sc_rsrc_t rsrc_idx, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
  Transition internal SOC level bandgap.
- void **soc_fabric_force_on** (sc_sub_t ss, sc_bool_t enb)
- void **soc_post_ss_reset** (sc_dsc_t dsc, DSC_Type *dsc_base)
- void **soc_gicr_quiesce** (uint8_t cluster_idx, uint32_t cpu_idx)
- void **soc_pause_ddr_traffic** (sc_bool_t pause)

HPM Functions

- void **soc_init_hmp** (boot_phase_t phase)
- sc_err_t **soc_set_cpu_resume** (uint8_t cluster_idx, uint8_t cpu_idx, sc_bool_t isPrimary, sc_faddr_t resume_addr)
- sc_err_t **soc_set_m4_resume** (uint8_t m4_idx, sc_faddr_t resume_addr)
- sc_err_t **soc_set_multicluster_power_mode** (sc_pm_power_mode_t mode)
- sc_err_t **soc_set_cluster_power_mode** (uint8_t cluster_idx, sc_pm_power_mode_t mode)

- sc_err_t **soc_set_cpu_power_mode** (uint8_t cluster_idx, uint8_t cpu_idx, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)
- void **soc_set_cpu_rst_mode** (uint8_t cluster_idx, uint8_t cpu_idx, sc_bool_t rst)
- void **soc_set_m4_sleep_mode** (uint8_t m4_idx, sc_bool_t dsm, uint8_t stopm, uint8_t pstopo)
- sc_bool_t **soc_get_m4_sleep_mode_active** (uint8_t m4_idx)
- void **soc_set_m4_rst_mode** (uint8_t m4_idx, sc_bool_t rst)
- sc_err_t **soc_req_sys_if_power_mode** (uint8_t hmp_idx, sc_pm_sys_if_t sys_if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)
- void **soc_trans_sys_if_hpm** (uint8_t hmp_idx)
- void **soc_trans_sys_if_lpm** (void)
- void **soc_sync_sys_if_pm** (void)
- void **soc_trans_cpu_power_mode** (uint8_t cluster_idx, uint8_t cpu_idx)
- void **soc_trans_m4_power_mode** (uint8_t m4_idx)
- void **soc_prewake_cpu** (void)
- void **soc_wake_cpu** (uint8_t cluster_idx, uint8_t cpu_idx)
- void **soc_wake_m4** (uint8_t m4_idx)
- void **soc_wake_lsio_mu** (void)
- void **soc_wake_m4_mu** (uint8_t m4_idx)
- void **soc_wake_sys_if_interconnect** (void)
- sc_pm_power_mode_t **soc_get_hmp_sys_power_mode** (void)
- void **soc_dump_hmp_power_state** (void)
- sc_bool_t **soc_can_hmp_enter_lpm** (void)

DDR Functions

- sc_err_t soc_init_ddr (sc_bool_t early)

  This function initalizes DDR.
- void soc_self_refresh_power_down_clk_disable_entry (void)

  This function places the DDR in SRPD (self-refresh power down) and disables DDR clocks.
- void soc_refresh_power_down_clk_disable_exit (void)

  This function enables DDR clocks and exits the DDR from SRPD (self-refresh power down).
- void soc_ddr_config_retention (soc_ddr_ret_info_t *ddr_ret_info)

  This function configures parameters for DDR low-power retention (SRPD with DRC powered down).
- void soc_ddr_enter_retention (void)

  This function places the DDR into low-power retention (SRPD with DRC powered down).
- void soc_ddr_exit_retention (void)

  This function exits the DDR from low-power retention (SRPD with DRC powered down).
- void soc_ddr_dqs2dq_init (void)

  This function initializes LPDDR4 DQS2DQ training.
- void soc_ddr_bit_deskew (void)

  This function does DDR bit deskew training.
- void soc_ddr_dqs2dq_periodic (void)

  This function invokes LPDDR4 DQS2DQ periodic training.
- void soc_ddr_dqs2dq_config (soc_dqs2dq_sync_info_t *dqs2dq_sync_info)

  This function configures parameters of LPDDR4 DQS2DQ periodic training.
- void soc_ddr_dqs2dq_sync (void)

  This function sychronizes LPDDR4 DQS2DQ periodic training to DDR traffic events (i.e.
- void soc_drc_lpcg_setup (void)

  This function enables DDR LPCG clock gating.

Misc Functions

- void soc_temp_sensor_tick (uint16_t msec)

  This function ticks the temp sensor processing.

- void **soc_setup_msi_slave_ring** (sc_sub_t cur_ss, sc_sub_t parent, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
- void **soc_msi_ring_workaround** (sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode, soc_msi_ring_usecount_t *msi_slv_ring, uint32_t num_msi_slaves, MSI_MSTR_Type *msi_reg, sc_sub_t cur_ss)

Debug Functions

- void soc_dsc_ai_dumpmodule (sc_dsc_t dsc, uint8_t tog, sc_ai_t ai)
  Dumps registers of single analog module.
- void soc_dsc_ai_dump (sc_dsc_t dsc)
  Dumps registers of analog modules in a subsystem.
- void soc_anamix_test_out (sc_dsc_t dsc)
  Allows for muxing out analog clocks and voltage levels.

Variables

- sc_rm_pt_t soc_reset_pt
  Global variable to hold resetting partition.
- sc_pm_reset_reason_t soc_reset_rsn
  Global variable to hold reset reason.
- uint32_t **soc_dpll_tbl_0** [ ]
- uint32_t **soc_dpll_tbl_1** [ ]
- sc_bool_t soc_clk_off_trans
  Global variable to store the state of clocks during power transition.
- soc_hmp_t soc_hmp
  Global variable to hold the SCU standalone repeater trim.
- soc_sys_if_req_t **soc_sys_if_req** [SOC_NUM_HMP_NODES][SOC_NUM_SYS_IF]
- soc_m4_state_t **soc_m4_state** [SOC_NUM_M4]
- soc_cluster_state_t **soc_cluster_state** [SOC_NUM_CLUSTER]
- soc_dqs2dq_sync_info_t * **soc_dqs2dq_sync_info**

18.19.1 Detailed Description

Header file containing the SoC API.

This abstracts SoC-specific functionality such as init, info, analog, power, HPM, and DDR.

18.20 platform/main/types.h File Reference

Header file containing types used across multiple service APIs.

Macros

- #define SC_R_NONE 0xFFF0U
  Define for ATF/Linux.
- #define SC_C_TEMP 0U

Defines for sc_ctrl_t.

- #define **SC_C_TEMP_HI** 1U
- #define **SC_C_TEMP_LOW** 2U
- #define **SC_C_PXL_LINK_MST1_ADDR** 3U
- #define **SC_C_PXL_LINK_MST2_ADDR** 4U
- #define **SC_C_PXL_LINK_MST_ENB** 5U
- #define **SC_C_PXL_LINK_MST1_ENB** 6U
- #define **SC_C_PXL_LINK_MST2_ENB** 7U
- #define **SC_C_PXL_LINK_SLV1_ADDR** 8U
- #define **SC_C_PXL_LINK_SLV2_ADDR** 9U
- #define **SC_C_PXL_LINK_MST_VLD** 10U
- #define **SC_C_PXL_LINK_MST1_VLD** 11U
- #define **SC_C_PXL_LINK_MST2_VLD** 12U
- #define **SC_C_SINGLE_MODE** 13U
- #define **SC_C_ID** 14U
- #define **SC_C_PXL_CLK_POLARITY** 15U
- #define **SC_C_LINESTATE** 16U
- #define **SC_C_PCIE_G_RST** 17U
- #define **SC_C_PCIE_BUTTON_RST** 18U
- #define **SC_C_PCIE_PERST** 19U
- #define **SC_C_PHY_RESET** 20U
- #define **SC_C_PXL_LINK_RATE_CORRECTION** 21U
- #define **SC_C_PANIC** 22U
- #define **SC_C_PRIORITY_GROUP** 23U
- #define **SC_C_TXCLK** 24U
- #define **SC_C_CLKDIV** 25U
- #define **SC_C_DISABLE_50** 26U
- #define **SC_C_DISABLE_125** 27U
- #define **SC_C_SEL_125** 28U
- #define **SC_C_MODE** 29U
- #define **SC_C_SYNC_CTRL0** 30U
- #define **SC_C_KACHUNK_CNT** 31U
- #define **SC_C_KACHUNK_SEL** 32U
- #define **SC_C_SYNC_CTRL1** 33U
- #define **SC_C_DPI_RESET** 34U
- #define **SC_C_MIPI_RESET** 35U
- #define **SC_C_DUAL_MODE** 36U
- #define **SC_C_VOLTAGE** 37U
- #define **SC_C_PXL_LINK_SEL** 38U
- #define **SC_C_OFS_SEL** 39U
- #define **SC_C_OFS_AUDIO** 40U
- #define **SC_C_OFS_PERIPH** 41U
- #define **SC_C_OFS_IRQ** 42U
- #define **SC_C_RST0** 43U
- #define **SC_C_RST1** 44U
- #define **SC_C_SEL0** 45U
- #define **SC_C_CALIB0** 46U
- #define **SC_C_CALIB1** 47U
- #define **SC_C_CALIB2** 48U
- #define **SC_C_IPG_DEBUG** 49U
- #define **SC_C_IPG_DOZE** 50U

- #define **SC_C_IPG_WAIT** 51U
- #define **SC_C_IPG_STOP** 52U
- #define **SC_C_IPG_STOP_MODE** 53U
- #define **SC_C_IPG_STOP_ACK** 54U
- #define **SC_C_SYNC_CTRL** 55U
- #define **SC_C_OFS_AUDIO_ALT** 56U
- #define **SC_C_DSP_BYP** 57U
- #define **SC_C_CLK_GEN_EN** 58U
- #define **SC_C_INTF_SEL** 59U
- #define **SC_C_RXC_DLY** 60U
- #define **SC_C_TIMER_SEL** 61U
- #define **SC_C_MISC0** 62U
- #define **SC_C_MISC1** 63U
- #define **SC_C_MISC2** 64U
- #define **SC_C_MISC3** 65U
- #define **SC_C_LAST** 66U
- #define SC_P_ALL ((sc_pad_t) UINT16_MAX)

  Define for used to specify all pads.

Defines for chip IDs

- #define CHIP_ID_QM 0x1U

  i.MX8QM
- #define CHIP_ID_QX 0x2U

  i.MX8QX
- #define CHIP_ID_DXL 0xEU

  i.MX8DXL

Defines for common frequencies

- #define SC_32KHZ 32768U

  32KHz
- #define SC_1MHZ 1000000U

  1MHz
- #define SC_10MHZ 10000000U

  10MHz
- #define SC_16MHZ 16000000U

  16MHz
- #define SC_20MHZ 20000000U

  20MHz
- #define SC_25MHZ 25000000U

  25MHz
- #define SC_27MHZ 27000000U

  27MHz
- #define SC_40MHZ 40000000U

  40MHz
- #define SC_45MHZ 45000000U

  45MHz
- #define SC_50MHZ 50000000U

  50MHz
- #define SC_60MHZ 60000000U

60MHz

- #define SC_66MHZ 66666666U

  66MHz
- #define SC_74MHZ 74250000U

  74.25MHz
- #define SC_80MHZ 80000000U

  80MHz
- #define SC_83MHZ 83333333U

  83MHz
- #define SC_84MHZ 84375000U

  84.37MHz
- #define SC_100MHZ 100000000U

  100MHz
- #define SC_114MHZ 114000000U

  114MHz
- #define SC_125MHZ 125000000U

  125MHz
- #define SC_128MHZ 128000000U

  128MHz
- #define SC_133MHZ 133333333U

  133MHz
- #define SC_135MHZ 135000000U

  135MHz
- #define SC_150MHZ 150000000U

  150MHz
- #define SC_160MHZ 160000000U

  160MHz
- #define SC_166MHZ 166666666U

  166MHz
- #define SC_175MHZ 175000000U

  175MHz
- #define SC_180MHZ 180000000U

  180MHz
- #define SC_200MHZ 200000000U

  200MHz
- #define SC_250MHZ 250000000U

  250MHz
- #define SC_266MHZ 266666666U

  266MHz
- #define SC_300MHZ 300000000U

  300MHz
- #define SC_312MHZ 312500000U

  312.5MHZ
- #define SC_320MHZ 320000000U

  320MHz
- #define SC_325MHZ 325000000U

  325MHz
- #define SC_333MHZ 333333333U

  333MHz
- #define SC_350MHZ 350000000U

  350MHz
- #define SC_372MHZ 372000000U

  372MHz
- #define SC_375MHZ 375000000U

  375MHz

- #define SC_400MHZ 400000000U
  400MHz
- #define SC_465MHZ 465000000U
  465MHz
- #define SC_500MHZ 500000000U
  500MHz
- #define SC_594MHZ 594000000U
  594MHz
- #define SC_625MHZ 625000000U
  625MHz
- #define SC_640MHZ 640000000U
  640MHz
- #define SC_648MHZ 648000000U
  648MHz
- #define SC_650MHZ 650000000U
  650MHz
- #define SC_667MHZ 666666667U
  667MHz
- #define SC_675MHZ 675000000U
  675MHz
- #define SC_700MHZ 700000000U
  700MHz
- #define SC_720MHZ 720000000U
  720MHz
- #define SC_750MHZ 750000000U
  750MHz
- #define SC_753MHZ 753000000U
  753MHz
- #define SC_793MHZ 793000000U
  793MHz
- #define SC_800MHZ 800000000U
  800MHz
- #define SC_850MHZ 850000000U
  850MHz
- #define SC_858MHZ 858000000U
  858MHz
- #define SC_900MHZ 900000000U
  900MHz
- #define SC_953MHZ 953000000U
  953MHz
- #define SC_963MHZ 963000000U
  963MHz
- #define SC_1000MHZ 1000000000U
  1GHz
- #define SC_1060MHZ 1060000000U
  1.06GHz
- #define SC_1068MHZ 1068000000U
  1.068GHz
- #define SC_1121MHZ 1121000000U
  1.121GHz
- #define SC_1173MHZ 1173000000U
  1.173GHz
- #define SC_1188MHZ 1188000000U
  1.188GHz
- #define SC_1260MHZ 1260000000U

1.26GHz
- #define SC_1278MHZ 1278000000U
  1.278GHz
- #define SC_1280MHZ 1280000000U
  1.28GHz
- #define SC_1300MHZ 1300000000U
  1.3GHz
- #define SC_1313MHZ 1313000000U
  1.313GHz
- #define SC_1345MHZ 1345000000U
  1.345GHz
- #define SC_1400MHZ 1400000000U
  1.4GHz
- #define SC_1500MHZ 1500000000U
  1.5GHz
- #define SC_1600MHZ 1600000000U
  1.6GHz
- #define SC_1800MHZ 1800000000U
  1.8GHz
- #define SC_1860MHZ 1860000000U
  1.86GHz
- #define SC_2000MHZ 2000000000U
  2.0GHz
- #define SC_2112MHZ 2112000000U
  2.12GHz

Defines for 24M related frequencies

- #define SC_8MHZ 8000000U
  8MHz
- #define SC_12MHZ 12000000U
  12MHz
- #define SC_19MHZ 19800000U
  19.8MHz
- #define SC_24MHZ 24000000U
  24MHz
- #define SC_48MHZ 48000000U
  48MHz
- #define SC_120MHZ 120000000U
  120MHz
- #define SC_132MHZ 132000000U
  132MHz
- #define SC_144MHZ 144000000U
  144MHz
- #define SC_192MHZ 192000000U
  192MHz
- #define SC_211MHZ 211200000U
  211.2MHz
- #define SC_228MHZ 228000000U
  233MHz
- #define SC_240MHZ 240000000U
  240MHz
- #define SC_264MHZ 264000000U
  264MHz

- #define SC_352MHZ 352000000U
  352MHz
- #define SC_360MHZ 360000000U
  360MHz
- #define SC_384MHZ 384000000U
  384MHz
- #define SC_396MHZ 396000000U
  396MHz
- #define SC_432MHZ 432000000U
  432MHz
- #define SC_456MHZ 456000000U
  466MHz
- #define SC_480MHZ 480000000U
  480MHz
- #define SC_600MHZ 600000000U
  600MHz
- #define SC_744MHZ 744000000U
  744MHz
- #define SC_792MHZ 792000000U
  792MHz
- #define SC_864MHZ 864000000U
  864MHz
- #define SC_912MHZ 912000000U
  912MHz
- #define SC_960MHZ 960000000U
  960MHz
- #define SC_1056MHZ 1056000000U
  1056MHz
- #define SC_1104MHZ 1104000000U
  1104MHz
- #define SC_1200MHZ 1200000000U
  1.2GHz
- #define SC_1464MHZ 1464000000U
  1.464GHz
- #define SC_2400MHZ 2400000000U
  2.4GHz

Defines for A/V related frequencies

- #define SC_62MHZ 62937500U
  62.9375MHz
- #define SC_755MHZ 755250000U
  755.25MHz

Defines for type widths

- #define SC_BOOL_W 1U
  Width of sc_bool_t.
- #define SC_ERR_W 4U
  Width of sc_err_t.
- #define SC_RSRC_W 10U
  Width of sc_rsrc_t.
- #define SC_CTRL_W 7U

Width of sc_ctrl_t.

Defines for sc_bool_t

- #define SC_FALSE ((sc_bool_t) 0U)
  False.
- #define SC_TRUE ((sc_bool_t) 1U)
  True.

Defines for sc_err_t

- #define SC_ERR_NONE 0U
  Success.
- #define SC_ERR_VERSION 1U
  Incompatible API version.
- #define SC_ERR_CONFIG 2U
  Configuration error.
- #define SC_ERR_PARM 3U
  Bad parameter.
- #define SC_ERR_NOACCESS 4U
  Permission error (no access)
- #define SC_ERR_LOCKED 5U
  Permission error (locked)
- #define SC_ERR_UNAVAILABLE 6U
  Unavailable (out of resources)
- #define SC_ERR_NOTFOUND 7U
  Not found.
- #define SC_ERR_NOPOWER 8U
  No power.
- #define SC_ERR_IPC 9U
  Generic IPC error.
- #define SC_ERR_BUSY 10U
  Resource is currently busy/active.
- #define SC_ERR_FAIL 11U
  General I/O failure.
- #define **SC_ERR_LAST** 12U

Defines for sc_rsrc_t

- #define **SC_R_A53** 0U
- #define **SC_R_A53_0** 1U
- #define **SC_R_A53_1** 2U
- #define **SC_R_A53_2** 3U
- #define **SC_R_A53_3** 4U
- #define **SC_R_A72** 5U
- #define **SC_R_A72_0** 6U
- #define **SC_R_A72_1** 7U
- #define **SC_R_A72_2** 8U
- #define **SC_R_A72_3** 9U
- #define **SC_R_CCI** 10U
- #define **SC_R_DB** 11U
- #define **SC_R_DRC_0** 12U
- #define **SC_R_DRC_1** 13U
- #define **SC_R_GIC_SMMU** 14U

- #define **SC_R_IRQSTR_M4_0** 15U
- #define **SC_R_IRQSTR_M4_1** 16U
- #define **SC_R_SMMU** 17U
- #define **SC_R_GIC** 18U
- #define **SC_R_DC_0_BLIT0** 19U
- #define **SC_R_DC_0_BLIT1** 20U
- #define **SC_R_DC_0_BLIT2** 21U
- #define **SC_R_DC_0_BLIT_OUT** 22U
- #define **SC_R_PERF** 23U
- #define **SC_R_USB_1_PHY** 24U
- #define **SC_R_DC_0_WARP** 25U
- #define **SC_R_V2X_MU_0** 26U
- #define **SC_R_V2X_MU_1** 27U
- #define **SC_R_DC_0_VIDEO0** 28U
- #define **SC_R_DC_0_VIDEO1** 29U
- #define **SC_R_DC_0_FRAC0** 30U
- #define **SC_R_V2X_MU_2** 31U
- #define **SC_R_DC_0** 32U
- #define **SC_R_GPU_2_PID0** 33U
- #define **SC_R_DC_0_PLL_0** 34U
- #define **SC_R_DC_0_PLL_1** 35U
- #define **SC_R_DC_1_BLIT0** 36U
- #define **SC_R_DC_1_BLIT1** 37U
- #define **SC_R_DC_1_BLIT2** 38U
- #define **SC_R_DC_1_BLIT_OUT** 39U
- #define **SC_R_V2X_MU_3** 40U
- #define **SC_R_V2X_MU_4** 41U
- #define **SC_R_DC_1_WARP** 42U
- #define **SC_R_UNUSED1** 43U
- #define **SC_R_SECVIO** 44U
- #define **SC_R_DC_1_VIDEO0** 45U
- #define **SC_R_DC_1_VIDEO1** 46U
- #define **SC_R_DC_1_FRAC0** 47U
- #define **SC_R_UNUSED13** 48U
- #define **SC_R_DC_1** 49U
- #define **SC_R_UNUSED14** 50U
- #define **SC_R_DC_1_PLL_0** 51U
- #define **SC_R_DC_1_PLL_1** 52U
- #define **SC_R_SPI_0** 53U
- #define **SC_R_SPI_1** 54U
- #define **SC_R_SPI_2** 55U
- #define **SC_R_SPI_3** 56U
- #define **SC_R_UART_0** 57U
- #define **SC_R_UART_1** 58U
- #define **SC_R_UART_2** 59U
- #define **SC_R_UART_3** 60U
- #define **SC_R_UART_4** 61U
- #define **SC_R_EMVSIM_0** 62U
- #define **SC_R_EMVSIM_1** 63U
- #define **SC_R_DMA_0_CH0** 64U
- #define **SC_R_DMA_0_CH1** 65U
- #define **SC_R_DMA_0_CH2** 66U
- #define **SC_R_DMA_0_CH3** 67U
- #define **SC_R_DMA_0_CH4** 68U
- #define **SC_R_DMA_0_CH5** 69U
- #define **SC_R_DMA_0_CH6** 70U
- #define **SC_R_DMA_0_CH7** 71U
- #define **SC_R_DMA_0_CH8** 72U
- #define **SC_R_DMA_0_CH9** 73U
- #define **SC_R_DMA_0_CH10** 74U

- #define **SC_R_DMA_0_CH11** 75U
- #define **SC_R_DMA_0_CH12** 76U
- #define **SC_R_DMA_0_CH13** 77U
- #define **SC_R_DMA_0_CH14** 78U
- #define **SC_R_DMA_0_CH15** 79U
- #define **SC_R_DMA_0_CH16** 80U
- #define **SC_R_DMA_0_CH17** 81U
- #define **SC_R_DMA_0_CH18** 82U
- #define **SC_R_DMA_0_CH19** 83U
- #define **SC_R_DMA_0_CH20** 84U
- #define **SC_R_DMA_0_CH21** 85U
- #define **SC_R_DMA_0_CH22** 86U
- #define **SC_R_DMA_0_CH23** 87U
- #define **SC_R_DMA_0_CH24** 88U
- #define **SC_R_DMA_0_CH25** 89U
- #define **SC_R_DMA_0_CH26** 90U
- #define **SC_R_DMA_0_CH27** 91U
- #define **SC_R_DMA_0_CH28** 92U
- #define **SC_R_DMA_0_CH29** 93U
- #define **SC_R_DMA_0_CH30** 94U
- #define **SC_R_DMA_0_CH31** 95U
- #define **SC_R_I2C_0** 96U
- #define **SC_R_I2C_1** 97U
- #define **SC_R_I2C_2** 98U
- #define **SC_R_I2C_3** 99U
- #define **SC_R_I2C_4** 100U
- #define **SC_R_ADC_0** 101U
- #define **SC_R_ADC_1** 102U
- #define **SC_R_FTM_0** 103U
- #define **SC_R_FTM_1** 104U
- #define **SC_R_CAN_0** 105U
- #define **SC_R_CAN_1** 106U
- #define **SC_R_CAN_2** 107U
- #define **SC_R_DMA_1_CH0** 108U
- #define **SC_R_DMA_1_CH1** 109U
- #define **SC_R_DMA_1_CH2** 110U
- #define **SC_R_DMA_1_CH3** 111U
- #define **SC_R_DMA_1_CH4** 112U
- #define **SC_R_DMA_1_CH5** 113U
- #define **SC_R_DMA_1_CH6** 114U
- #define **SC_R_DMA_1_CH7** 115U
- #define **SC_R_DMA_1_CH8** 116U
- #define **SC_R_DMA_1_CH9** 117U
- #define **SC_R_DMA_1_CH10** 118U
- #define **SC_R_DMA_1_CH11** 119U
- #define **SC_R_DMA_1_CH12** 120U
- #define **SC_R_DMA_1_CH13** 121U
- #define **SC_R_DMA_1_CH14** 122U
- #define **SC_R_DMA_1_CH15** 123U
- #define **SC_R_DMA_1_CH16** 124U
- #define **SC_R_DMA_1_CH17** 125U
- #define **SC_R_DMA_1_CH18** 126U
- #define **SC_R_DMA_1_CH19** 127U
- #define **SC_R_DMA_1_CH20** 128U
- #define **SC_R_DMA_1_CH21** 129U
- #define **SC_R_DMA_1_CH22** 130U
- #define **SC_R_DMA_1_CH23** 131U
- #define **SC_R_DMA_1_CH24** 132U
- #define **SC_R_DMA_1_CH25** 133U
- #define **SC_R_DMA_1_CH26** 134U

- #define **SC_R_DMA_1_CH27** 135U
- #define **SC_R_DMA_1_CH28** 136U
- #define **SC_R_DMA_1_CH29** 137U
- #define **SC_R_DMA_1_CH30** 138U
- #define **SC_R_DMA_1_CH31** 139U
- #define **SC_R_V2X_PID0** 140U
- #define **SC_R_V2X_PID1** 141U
- #define **SC_R_V2X_PID2** 142U
- #define **SC_R_V2X_PID3** 143U
- #define **SC_R_GPU_0_PID0** 144U
- #define **SC_R_GPU_0_PID1** 145U
- #define **SC_R_GPU_0_PID2** 146U
- #define **SC_R_GPU_0_PID3** 147U
- #define **SC_R_GPU_1_PID0** 148U
- #define **SC_R_GPU_1_PID1** 149U
- #define **SC_R_GPU_1_PID2** 150U
- #define **SC_R_GPU_1_PID3** 151U
- #define **SC_R_PCIE_A** 152U
- #define **SC_R_SERDES_0** 153U
- #define **SC_R_MATCH_0** 154U
- #define **SC_R_MATCH_1** 155U
- #define **SC_R_MATCH_2** 156U
- #define **SC_R_MATCH_3** 157U
- #define **SC_R_MATCH_4** 158U
- #define **SC_R_MATCH_5** 159U
- #define **SC_R_MATCH_6** 160U
- #define **SC_R_MATCH_7** 161U
- #define **SC_R_MATCH_8** 162U
- #define **SC_R_MATCH_9** 163U
- #define **SC_R_MATCH_10** 164U
- #define **SC_R_MATCH_11** 165U
- #define **SC_R_MATCH_12** 166U
- #define **SC_R_MATCH_13** 167U
- #define **SC_R_MATCH_14** 168U
- #define **SC_R_PCIE_B** 169U
- #define **SC_R_SATA_0** 170U
- #define **SC_R_SERDES_1** 171U
- #define **SC_R_HSIO_GPIO** 172U
- #define **SC_R_MATCH_15** 173U
- #define **SC_R_MATCH_16** 174U
- #define **SC_R_MATCH_17** 175U
- #define **SC_R_MATCH_18** 176U
- #define **SC_R_MATCH_19** 177U
- #define **SC_R_MATCH_20** 178U
- #define **SC_R_MATCH_21** 179U
- #define **SC_R_MATCH_22** 180U
- #define **SC_R_MATCH_23** 181U
- #define **SC_R_MATCH_24** 182U
- #define **SC_R_MATCH_25** 183U
- #define **SC_R_MATCH_26** 184U
- #define **SC_R_MATCH_27** 185U
- #define **SC_R_MATCH_28** 186U
- #define **SC_R_LCD_0** 187U
- #define **SC_R_LCD_0_PWM_0** 188U
- #define **SC_R_LCD_0_I2C_0** 189U
- #define **SC_R_LCD_0_I2C_1** 190U
- #define **SC_R_PWM_0** 191U
- #define **SC_R_PWM_1** 192U
- #define **SC_R_PWM_2** 193U
- #define **SC_R_PWM_3** 194U

- #define **SC_R_PWM_4** 195U
- #define **SC_R_PWM_5** 196U
- #define **SC_R_PWM_6** 197U
- #define **SC_R_PWM_7** 198U
- #define **SC_R_GPIO_0** 199U
- #define **SC_R_GPIO_1** 200U
- #define **SC_R_GPIO_2** 201U
- #define **SC_R_GPIO_3** 202U
- #define **SC_R_GPIO_4** 203U
- #define **SC_R_GPIO_5** 204U
- #define **SC_R_GPIO_6** 205U
- #define **SC_R_GPIO_7** 206U
- #define **SC_R_GPT_0** 207U
- #define **SC_R_GPT_1** 208U
- #define **SC_R_GPT_2** 209U
- #define **SC_R_GPT_3** 210U
- #define **SC_R_GPT_4** 211U
- #define **SC_R_KPP** 212U
- #define **SC_R_MU_0A** 213U
- #define **SC_R_MU_1A** 214U
- #define **SC_R_MU_2A** 215U
- #define **SC_R_MU_3A** 216U
- #define **SC_R_MU_4A** 217U
- #define **SC_R_MU_5A** 218U
- #define **SC_R_MU_6A** 219U
- #define **SC_R_MU_7A** 220U
- #define **SC_R_MU_8A** 221U
- #define **SC_R_MU_9A** 222U
- #define **SC_R_MU_10A** 223U
- #define **SC_R_MU_11A** 224U
- #define **SC_R_MU_12A** 225U
- #define **SC_R_MU_13A** 226U
- #define **SC_R_MU_5B** 227U
- #define **SC_R_MU_6B** 228U
- #define **SC_R_MU_7B** 229U
- #define **SC_R_MU_8B** 230U
- #define **SC_R_MU_9B** 231U
- #define **SC_R_MU_10B** 232U
- #define **SC_R_MU_11B** 233U
- #define **SC_R_MU_12B** 234U
- #define **SC_R_MU_13B** 235U
- #define **SC_R_ROM_0** 236U
- #define **SC_R_FSPI_0** 237U
- #define **SC_R_FSPI_1** 238U
- #define **SC_R_IEE** 239U
- #define **SC_R_IEE_R0** 240U
- #define **SC_R_IEE_R1** 241U
- #define **SC_R_IEE_R2** 242U
- #define **SC_R_IEE_R3** 243U
- #define **SC_R_IEE_R4** 244U
- #define **SC_R_IEE_R5** 245U
- #define **SC_R_IEE_R6** 246U
- #define **SC_R_IEE_R7** 247U
- #define **SC_R_SDHC_0** 248U
- #define **SC_R_SDHC_1** 249U
- #define **SC_R_SDHC_2** 250U
- #define **SC_R_ENET_0** 251U
- #define **SC_R_ENET_1** 252U
- #define **SC_R_MLB_0** 253U
- #define **SC_R_DMA_2_CH0** 254U

- #define **SC_R_DMA_2_CH1** 255U
- #define **SC_R_DMA_2_CH2** 256U
- #define **SC_R_DMA_2_CH3** 257U
- #define **SC_R_DMA_2_CH4** 258U
- #define **SC_R_USB_0** 259U
- #define **SC_R_USB_1** 260U
- #define **SC_R_USB_0_PHY** 261U
- #define **SC_R_USB_2** 262U
- #define **SC_R_USB_2_PHY** 263U
- #define **SC_R_DTCP** 264U
- #define **SC_R_NAND** 265U
- #define **SC_R_LVDS_0** 266U
- #define **SC_R_LVDS_0_PWM_0** 267U
- #define **SC_R_LVDS_0_I2C_0** 268U
- #define **SC_R_LVDS_0_I2C_1** 269U
- #define **SC_R_LVDS_1** 270U
- #define **SC_R_LVDS_1_PWM_0** 271U
- #define **SC_R_LVDS_1_I2C_0** 272U
- #define **SC_R_LVDS_1_I2C_1** 273U
- #define **SC_R_LVDS_2** 274U
- #define **SC_R_LVDS_2_PWM_0** 275U
- #define **SC_R_LVDS_2_I2C_0** 276U
- #define **SC_R_LVDS_2_I2C_1** 277U
- #define **SC_R_M4_0_PID0** 278U
- #define **SC_R_M4_0_PID1** 279U
- #define **SC_R_M4_0_PID2** 280U
- #define **SC_R_M4_0_PID3** 281U
- #define **SC_R_M4_0_PID4** 282U
- #define **SC_R_M4_0_RGPIO** 283U
- #define **SC_R_M4_0_SEMA42** 284U
- #define **SC_R_M4_0_TPM** 285U
- #define **SC_R_M4_0_PIT** 286U
- #define **SC_R_M4_0_UART** 287U
- #define **SC_R_M4_0_I2C** 288U
- #define **SC_R_M4_0_INTMUX** 289U
- #define **SC_R_ENET_0_A0** 290U
- #define **SC_R_ENET_0_A1** 291U
- #define **SC_R_M4_0_MU_0B** 292U
- #define **SC_R_M4_0_MU_0A0** 293U
- #define **SC_R_M4_0_MU_0A1** 294U
- #define **SC_R_M4_0_MU_0A2** 295U
- #define **SC_R_M4_0_MU_0A3** 296U
- #define **SC_R_M4_0_MU_1A** 297U
- #define **SC_R_M4_1_PID0** 298U
- #define **SC_R_M4_1_PID1** 299U
- #define **SC_R_M4_1_PID2** 300U
- #define **SC_R_M4_1_PID3** 301U
- #define **SC_R_M4_1_PID4** 302U
- #define **SC_R_M4_1_RGPIO** 303U
- #define **SC_R_M4_1_SEMA42** 304U
- #define **SC_R_M4_1_TPM** 305U
- #define **SC_R_M4_1_PIT** 306U
- #define **SC_R_M4_1_UART** 307U
- #define **SC_R_M4_1_I2C** 308U
- #define **SC_R_M4_1_INTMUX** 309U
- #define **SC_R_UNUSED17** 310U
- #define **SC_R_UNUSED18** 311U
- #define **SC_R_M4_1_MU_0B** 312U
- #define **SC_R_M4_1_MU_0A0** 313U
- #define **SC_R_M4_1_MU_0A1** 314U

- #define **SC_R_M4_1_MU_0A2** 315U
- #define **SC_R_M4_1_MU_0A3** 316U
- #define **SC_R_M4_1_MU_1A** 317U
- #define **SC_R_SAI_0** 318U
- #define **SC_R_SAI_1** 319U
- #define **SC_R_SAI_2** 320U
- #define **SC_R_IRQSTR_SCU2** 321U
- #define **SC_R_IRQSTR_DSP** 322U
- #define **SC_R_ELCDIF_PLL** 323U
- #define **SC_R_OCRAM** 324U
- #define **SC_R_AUDIO_PLL_0** 325U
- #define **SC_R_PI_0** 326U
- #define **SC_R_PI_0_PWM_0** 327U
- #define **SC_R_PI_0_PWM_1** 328U
- #define **SC_R_PI_0_I2C_0** 329U
- #define **SC_R_PI_0_PLL** 330U
- #define **SC_R_PI_1** 331U
- #define **SC_R_PI_1_PWM_0** 332U
- #define **SC_R_PI_1_PWM_1** 333U
- #define **SC_R_PI_1_I2C_0** 334U
- #define **SC_R_PI_1_PLL** 335U
- #define **SC_R_SC_PID0** 336U
- #define **SC_R_SC_PID1** 337U
- #define **SC_R_SC_PID2** 338U
- #define **SC_R_SC_PID3** 339U
- #define **SC_R_SC_PID4** 340U
- #define **SC_R_SC_SEMA42** 341U
- #define **SC_R_SC_TPM** 342U
- #define **SC_R_SC_PIT** 343U
- #define **SC_R_SC_UART** 344U
- #define **SC_R_SC_I2C** 345U
- #define **SC_R_SC_MU_0B** 346U
- #define **SC_R_SC_MU_0A0** 347U
- #define **SC_R_SC_MU_0A1** 348U
- #define **SC_R_SC_MU_0A2** 349U
- #define **SC_R_SC_MU_0A3** 350U
- #define **SC_R_SC_MU_1A** 351U
- #define **SC_R_SYSCNT_RD** 352U
- #define **SC_R_SYSCNT_CMP** 353U
- #define **SC_R_DEBUG** 354U
- #define **SC_R_SYSTEM** 355U
- #define **SC_R_SNVS** 356U
- #define **SC_R_OTP** 357U
- #define **SC_R_VPU_PID0** 358U
- #define **SC_R_VPU_PID1** 359U
- #define **SC_R_VPU_PID2** 360U
- #define **SC_R_VPU_PID3** 361U
- #define **SC_R_VPU_PID4** 362U
- #define **SC_R_VPU_PID5** 363U
- #define **SC_R_VPU_PID6** 364U
- #define **SC_R_VPU_PID7** 365U
- #define **SC_R_ENET_0_A2** 366U
- #define **SC_R_ENET_1_A0** 367U
- #define **SC_R_ENET_1_A1** 368U
- #define **SC_R_ENET_1_A2** 369U
- #define **SC_R_ENET_1_A3** 370U
- #define **SC_R_ENET_1_A4** 371U
- #define **SC_R_DMA_4_CH0** 372U
- #define **SC_R_DMA_4_CH1** 373U
- #define **SC_R_DMA_4_CH2** 374U

- #define **SC_R_DMA_4_CH3** 375U
- #define **SC_R_DMA_4_CH4** 376U
- #define **SC_R_ISI_CH0** 377U
- #define **SC_R_ISI_CH1** 378U
- #define **SC_R_ISI_CH2** 379U
- #define **SC_R_ISI_CH3** 380U
- #define **SC_R_ISI_CH4** 381U
- #define **SC_R_ISI_CH5** 382U
- #define **SC_R_ISI_CH6** 383U
- #define **SC_R_ISI_CH7** 384U
- #define **SC_R_MJPEG_DEC_S0** 385U
- #define **SC_R_MJPEG_DEC_S1** 386U
- #define **SC_R_MJPEG_DEC_S2** 387U
- #define **SC_R_MJPEG_DEC_S3** 388U
- #define **SC_R_MJPEG_ENC_S0** 389U
- #define **SC_R_MJPEG_ENC_S1** 390U
- #define **SC_R_MJPEG_ENC_S2** 391U
- #define **SC_R_MJPEG_ENC_S3** 392U
- #define **SC_R_MIPI_0** 393U
- #define **SC_R_MIPI_0_PWM_0** 394U
- #define **SC_R_MIPI_0_I2C_0** 395U
- #define **SC_R_MIPI_0_I2C_1** 396U
- #define **SC_R_MIPI_1** 397U
- #define **SC_R_MIPI_1_PWM_0** 398U
- #define **SC_R_MIPI_1_I2C_0** 399U
- #define **SC_R_MIPI_1_I2C_1** 400U
- #define **SC_R_CSI_0** 401U
- #define **SC_R_CSI_0_PWM_0** 402U
- #define **SC_R_CSI_0_I2C_0** 403U
- #define **SC_R_CSI_1** 404U
- #define **SC_R_CSI_1_PWM_0** 405U
- #define **SC_R_CSI_1_I2C_0** 406U
- #define **SC_R_HDMI** 407U
- #define **SC_R_HDMI_I2S** 408U
- #define **SC_R_HDMI_I2C_0** 409U
- #define **SC_R_HDMI_PLL_0** 410U
- #define **SC_R_HDMI_RX** 411U
- #define **SC_R_HDMI_RX_BYPASS** 412U
- #define **SC_R_HDMI_RX_I2C_0** 413U
- #define **SC_R_ASRC_0** 414U
- #define **SC_R_ESAI_0** 415U
- #define **SC_R_SPDIF_0** 416U
- #define **SC_R_SPDIF_1** 417U
- #define **SC_R_SAI_3** 418U
- #define **SC_R_SAI_4** 419U
- #define **SC_R_SAI_5** 420U
- #define **SC_R_GPT_5** 421U
- #define **SC_R_GPT_6** 422U
- #define **SC_R_GPT_7** 423U
- #define **SC_R_GPT_8** 424U
- #define **SC_R_GPT_9** 425U
- #define **SC_R_GPT_10** 426U
- #define **SC_R_DMA_2_CH5** 427U
- #define **SC_R_DMA_2_CH6** 428U
- #define **SC_R_DMA_2_CH7** 429U
- #define **SC_R_DMA_2_CH8** 430U
- #define **SC_R_DMA_2_CH9** 431U
- #define **SC_R_DMA_2_CH10** 432U
- #define **SC_R_DMA_2_CH11** 433U
- #define **SC_R_DMA_2_CH12** 434U

- #define **SC_R_DMA_2_CH13** 435U
- #define **SC_R_DMA_2_CH14** 436U
- #define **SC_R_DMA_2_CH15** 437U
- #define **SC_R_DMA_2_CH16** 438U
- #define **SC_R_DMA_2_CH17** 439U
- #define **SC_R_DMA_2_CH18** 440U
- #define **SC_R_DMA_2_CH19** 441U
- #define **SC_R_DMA_2_CH20** 442U
- #define **SC_R_DMA_2_CH21** 443U
- #define **SC_R_DMA_2_CH22** 444U
- #define **SC_R_DMA_2_CH23** 445U
- #define **SC_R_DMA_2_CH24** 446U
- #define **SC_R_DMA_2_CH25** 447U
- #define **SC_R_DMA_2_CH26** 448U
- #define **SC_R_DMA_2_CH27** 449U
- #define **SC_R_DMA_2_CH28** 450U
- #define **SC_R_DMA_2_CH29** 451U
- #define **SC_R_DMA_2_CH30** 452U
- #define **SC_R_DMA_2_CH31** 453U
- #define **SC_R_ASRC_1** 454U
- #define **SC_R_ESAI_1** 455U
- #define **SC_R_SAI_6** 456U
- #define **SC_R_SAI_7** 457U
- #define **SC_R_AMIX** 458U
- #define **SC_R_MQS_0** 459U
- #define **SC_R_DMA_3_CH0** 460U
- #define **SC_R_DMA_3_CH1** 461U
- #define **SC_R_DMA_3_CH2** 462U
- #define **SC_R_DMA_3_CH3** 463U
- #define **SC_R_DMA_3_CH4** 464U
- #define **SC_R_DMA_3_CH5** 465U
- #define **SC_R_DMA_3_CH6** 466U
- #define **SC_R_DMA_3_CH7** 467U
- #define **SC_R_DMA_3_CH8** 468U
- #define **SC_R_DMA_3_CH9** 469U
- #define **SC_R_DMA_3_CH10** 470U
- #define **SC_R_DMA_3_CH11** 471U
- #define **SC_R_DMA_3_CH12** 472U
- #define **SC_R_DMA_3_CH13** 473U
- #define **SC_R_DMA_3_CH14** 474U
- #define **SC_R_DMA_3_CH15** 475U
- #define **SC_R_DMA_3_CH16** 476U
- #define **SC_R_DMA_3_CH17** 477U
- #define **SC_R_DMA_3_CH18** 478U
- #define **SC_R_DMA_3_CH19** 479U
- #define **SC_R_DMA_3_CH20** 480U
- #define **SC_R_DMA_3_CH21** 481U
- #define **SC_R_DMA_3_CH22** 482U
- #define **SC_R_DMA_3_CH23** 483U
- #define **SC_R_DMA_3_CH24** 484U
- #define **SC_R_DMA_3_CH25** 485U
- #define **SC_R_DMA_3_CH26** 486U
- #define **SC_R_DMA_3_CH27** 487U
- #define **SC_R_DMA_3_CH28** 488U
- #define **SC_R_DMA_3_CH29** 489U
- #define **SC_R_DMA_3_CH30** 490U
- #define **SC_R_DMA_3_CH31** 491U
- #define **SC_R_AUDIO_PLL_1** 492U
- #define **SC_R_AUDIO_CLK_0** 493U
- #define **SC_R_AUDIO_CLK_1** 494U

- #define **SC_R_MCLK_OUT_0** 495U
- #define **SC_R_MCLK_OUT_1** 496U
- #define **SC_R_PMIC_0** 497U
- #define **SC_R_PMIC_1** 498U
- #define **SC_R_SECO** 499U
- #define **SC_R_CAAM_JR1** 500U
- #define **SC_R_CAAM_JR2** 501U
- #define **SC_R_CAAM_JR3** 502U
- #define **SC_R_SECO_MU_2** 503U
- #define **SC_R_SECO_MU_3** 504U
- #define **SC_R_SECO_MU_4** 505U
- #define **SC_R_HDMI_RX_PWM_0** 506U
- #define **SC_R_A35** 507U
- #define **SC_R_A35_0** 508U
- #define **SC_R_A35_1** 509U
- #define **SC_R_A35_2** 510U
- #define **SC_R_A35_3** 511U
- #define **SC_R_DSP** 512U
- #define **SC_R_DSP_RAM** 513U
- #define **SC_R_CAAM_JR1_OUT** 514U
- #define **SC_R_CAAM_JR2_OUT** 515U
- #define **SC_R_CAAM_JR3_OUT** 516U
- #define **SC_R_VPU_DEC_0** 517U
- #define **SC_R_VPU_ENC_0** 518U
- #define **SC_R_CAAM_JR0** 519U
- #define **SC_R_CAAM_JR0_OUT** 520U
- #define **SC_R_PMIC_2** 521U
- #define **SC_R_DBLOGIC** 522U
- #define **SC_R_HDMI_PLL_1** 523U
- #define **SC_R_BOARD_R0** 524U
- #define **SC_R_BOARD_R1** 525U
- #define **SC_R_BOARD_R2** 526U
- #define **SC_R_BOARD_R3** 527U
- #define **SC_R_BOARD_R4** 528U
- #define **SC_R_BOARD_R5** 529U
- #define **SC_R_BOARD_R6** 530U
- #define **SC_R_BOARD_R7** 531U
- #define **SC_R_MJPEG_DEC_MP** 532U
- #define **SC_R_MJPEG_ENC_MP** 533U
- #define **SC_R_VPU_TS_0** 534U
- #define **SC_R_VPU_MU_0** 535U
- #define **SC_R_VPU_MU_1** 536U
- #define **SC_R_VPU_MU_2** 537U
- #define **SC_R_VPU_MU_3** 538U
- #define **SC_R_VPU_ENC_1** 539U
- #define **SC_R_VPU** 540U
- #define **SC_R_DMA_5_CH0** 541U
- #define **SC_R_DMA_5_CH1** 542U
- #define **SC_R_DMA_5_CH2** 543U
- #define **SC_R_DMA_5_CH3** 544U
- #define **SC_R_ATTESTATION** 545U
- #define **SC_R_LAST** 546U
- #define SC_R_ALL ((sc_rsrc_t) UINT16_MAX)

  All resources.

Typedefs

- typedef uint8_t sc_bool_t

  This type is used to store a boolean.
- typedef uint64_t sc_faddr_t

  This type is used to store a system (full-size) address.
- typedef uint8_t sc_err_t

  This type is used to indicate error response for most functions.
- typedef uint16_t sc_rsrc_t

  This type is used to indicate a resource.
- typedef uint32_t sc_ctrl_t

  This type is used to indicate a control.
- typedef uint16_t sc_pad_t

  This type is used to indicate a pad.
- typedef __INT8_TYPE__ int8_t

  Type used to declare an 8-bit integer.
- typedef __INT16_TYPE__ int16_t

  Type used to declare a 16-bit integer.
- typedef __INT32_TYPE__ int32_t

  Type used to declare a 32-bit integer.
- typedef __INT64_TYPE__ int64_t

  Type used to declare a 64-bit integer.
- typedef __UINT8_TYPE__ uint8_t

  Type used to declare an 8-bit unsigned integer.
- typedef __UINT16_TYPE__ uint16_t

  Type used to declare a 16-bit unsigned integer.
- typedef __UINT32_TYPE__ uint32_t

  Type used to declare a 32-bit unsigned integer.
- typedef __UINT64_TYPE__ uint64_t

  Type used to declare a 64-bit unsigned integer.

18.20.1 Detailed Description

Header file containing types used across multiple service APIs.

18.20.2 Macro Definition Documentation

18.20.2.1 SC_R_NONE

```
#define SC_R_NONE 0xFFF0U
```

Define for ATF/Linux.

Not used by SCFW. Not a valid parameter for any SCFW API calls!

18.20.2.2 SC_P_ALL

```
#define SC_P_ALL ((sc_pad_t) UINT16_MAX)
```

Define for used to specify all pads.

All pads

Examples

board.c.

18.20.3 Typedef Documentation

18.20.3.1 sc_rsrc_t

```
typedef uint16_t sc_rsrc_t
```

This type is used to indicate a resource.

Resources include peripherals and bus masters (but not memory regions). Note items from list should never be changed or removed (only added to at the end of the list).

18.20.3.2 sc_pad_t

```
typedef uint16_t sc_pad_t
```

This type is used to indicate a pad.

Valid values are SoC specific.

Refer to the SoC Pad List for valid pad values.

18.21 platform/ss/inf/inf.h File Reference

Common functions for interfacing with the subsystems.

Data Structures

- struct sc_rsrc_map_t

  This type is used store static constant info to map resources to the containing subsystem.
- struct ss_rsrc_info_t

  This type is used store static constant info about resources in a subsystem.
- struct ss_ctrl_info_t

  This type is used store static constant info about controls in a subsystem.
- struct ss_pd_info_t

  This type is used to store static constant info about the power domains in the subsystem.

- struct ss_xexp_info_t

  This type is used to store static constant info about resources to keep assigned to the SCU or associated with another resource.
- struct ss_mdac_info_t

  This type is used to store static constant info about the MDACs in a subsystem.
- struct ss_msc_info_t

  This type is used to store static constant info about the MSCs in a subsystem.
- struct ss_mrc_info_t

  This type is used to store static constant info about the MRCs in a subsystem.
- struct ss_base_info_t

  This type is used to store static constant info about a subsystem.
- struct ss_clk_data_t

  This type is used to store dynamic data about the clocks/PLLs in the subsystem.
- struct ss_base_data_t

  This type is used to store dynamic data about a subsystem.

Macros

- #define SS_CLK_W 6U

  Width of ss_clock_t.
- #define SS_PLL_W 2U

  Width of ss_pll_t.
- #define SS_IO_W 4U

  Width of ss_io_type_t.
- #define SS_XEXP_W 8U

  Width of ss_xexp_idx_t.
- #define SS_FIELD_POS_W 16U

  Width of I/O field position.
- #define SS_FIELD_WID_W 6U

  Width of I/O field width.
- #define SS_CID_W 4U

  Width of CPU ID.
- #define SS_IDX_W 8U

  Width of SS index.
- #define SS_NUM_SSI_W 2U

  Width of num SSIs.
- #define SS_MAX_CLK 35U

  Max number of clocks per subsystem.
- #define SS_MAX_PLL 3U

  Max number of PLLs per subsystem.
- #define **SS_MAX_PM_CLKS** 5U
- #define NV ((uint8_t) UINT8_MAX)

  Define to indicate invalid power domains and clocks.
- #define RSRC(R, I, X)

  Define to fill in a sc_rsrc_map_t variable.
- #define **SS_I1** 0x8001U
- #define **XNFO_DL** {0U, 0U}

- #define BASE_INFO(XEXP_INFO, MDAC_INFO, PAC_INFO, MSC_INFO, MRC_INFO, CTRL_INFO)

  Define to fill in a ss_base_info_t variable (with XRDC)

- #define RNFO(PWD, C1, C2, C3, C4, C5, M, P, X, MI, PI, MATCHF, MASKF)

  Define to fill in a ss_rsrc_info_t variable (with XRDC)

- #define XNFO(S, N)

  Define to fill in a ss_xexp_info_t variable.

- #define TNFO(R, C, IO, B, W)

  Define to fill in a ss_ctrl_info_t variable.

- #define MNFO(P, ST, EN, AJ, M, I, SL, PWD, SB, C)

  Define to fill in a ss_mrc_info_t variable.

Typedefs

- typedef uint8_t ss_idx_t

  Type for a ss resource index.

- typedef sc_rm_idx_t ss_ridx_t

  Type for a resource index.

- typedef uint8_t ss_clock_t

  Type for a clock index.

- typedef uint8_t ss_pll_t

  Type for a PLL index.

- typedef uint8_t ss_xexp_idx_t

  Type for an XRDC expansion info index.

- typedef xrdc_pac_info_t ss_pac_info_t

  This type is used to store static constant info about the PACs in a subsystem.

- typedef sc_bool_t(* ss_dsc_l2irq_handler) (sc_dsc_t dsc, uint32_t irqIndex)

  Type for IRQ handler.

Enumerations

- enum ss_prepost_t { SS_PREAMBLE, SS_POSTAMBLE }

  This type is used to indicate pre- or post-amble function calls.

- enum ss_io_type_t {
  SS_IO_GPR_CTRL, SS_IO_GPR_STAT, SS_IO_CSR, SS_IO_CSR2,
  SS_IO_CSR3, SS_IO_AI_RW, SS_IO_AI_RO, SS_IO_RST_CTRL,
  SS_IO_BRD_CTRL, SS_IO_SW_CTRL }

  This type is used to indicate type of DSC I/O.

Functions

Interface Functions

- void ss_init (sc_sub_t ss, sc_bool_t api_phase)
  This function initalizes a subsystem.
- void ss_trans_power_mode (ss_ridx_t rsrc_idx, sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
  This function transitions a resource from one power mode to another.
- sc_err_t ss_rsrc_reset (ss_ridx_t rsrc_idx, sc_rm_pt_t pt, sc_bool_t pre)
  This function requests a resource be reset.
- sc_err_t ss_set_cpu_power_mode (ss_ridx_t rsrc_idx, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)
  This function requests the power power mode to be entered for some resources under certain circumstances.
- sc_err_t ss_set_cpu_resume (ss_ridx_t rsrc_idx, sc_bool_t isPrimary, sc_faddr_t addr)
  This function sets the resume address of a CPU.
- sc_err_t ss_req_sys_if_power_mode (ss_ridx_t rsrc_idx, sc_pm_sys_if_t sys_if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)
  This function requests the power mode for system-level interfaces including messaging units, interconnect, and memories.
- sc_err_t ss_set_clock_rate (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)
  This function sets a clock rate.
- sc_err_t ss_get_clock_rate (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)
  This function gets a clock rate.
- sc_err_t ss_clock_enable (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_bool_t enable, sc_bool_t autog)
  This function enables a clock.
- sc_err_t ss_force_clock_enable (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_bool_t enable)
  This function enables a clock.
- sc_err_t ss_set_clock_parent (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clk_parent_t new_parent)
  This function sets the parent of a resource's clock.
- sc_err_t ss_get_clock_parent (ss_ridx_t rsrc_idx, sc_pm_clk_t clk, sc_pm_clk_parent_t *parent)
  This function gets the parent of a resource's clock.
- sc_bool_t ss_is_rsrc_accessible (ss_ridx_t rsrc_idx)
  This function returns the functional state of a resource.
- void ss_mu_irq (ss_ridx_t rsrc_idx, uint32_t mask)
  This function triggers an interrupt on an MU.
- sc_err_t ss_cpu_start (ss_ridx_t rsrc_idx, sc_bool_t enable, sc_faddr_t addr)
  This function starts or stops a subsystem CPU.
- void ss_rdc_enable (sc_sub_t ss, sc_bool_t master)
  This function enables the subsystem hardware resource manager.
- void ss_rdc_set_master (ss_ridx_t rsrc_idx, sc_bool_t valid, sc_bool_t lock, sc_rm_spa_t sa, sc_rm_spa_t pa, sc_rm_did_t did, sc_rm_sid_t sid, uint8_t cid)
  This function configures a subsystem master.
- void ss_rdc_set_peripheral (ss_ridx_t rsrc_idx, sc_bool_t valid, sc_bool_t lock, const sc_rm_perm_t *perms, sc_bool_t no_update)
  This function configures a subsystem peripheral.
- sc_err_t ss_rdc_set_memory (sc_faddr_t start, sc_faddr_t end, sc_bool_t valid, const sc_rm_perm_t *perms, sc_rm_det_t det, sc_rm_rmsg_t rmsg, sc_faddr_t new_start, sc_faddr_t new_end)
  This function configures a memory region.
- sc_err_t ss_set_control (ss_ridx_t rsrc_idx, uint32_t ctrl, uint32_t val)
  This function sets a miscellaneous control value.
- sc_err_t ss_get_control (ss_ridx_t rsrc_idx, uint32_t ctrl, uint32_t *val)
  This function gets a miscellaneous control value.
- sc_err_t ss_irq_enable (ss_ridx_t rsrc_idx, sc_irq_group_t group, uint32_t mask, sc_bool_t enable)
  This function enables/disables interrupts.

- sc_err_t ss_irq_status (ss_ridx_t rsrc_idx, sc_irq_group_t group, uint32_t *status)
  This function returns the current interrupt status.
- void ss_irq_trigger (sc_irq_group_t group, uint32_t irq, sc_rm_pt_t pt)
  This function triggers an interrupt.
- void ss_dump (sc_sub_t ss, sc_bool_t xrdc, sc_bool_t dsc, sc_bool_t clk)
  This function dumps the state of a subsystem.

Helper Functions

- void ss_do_mem_repair (sc_sub_t ss, dsc_pdom_t pd, sc_bool_t enable)
  This function runs manual memory repair on a subsystem.
- void ss_updown (sc_sub_t ss, sc_bool_t up)
  This function is used to configure SS features after a SS is fully powered up (SSI link enabled) or before powering down.
- void ss_prepost_power_mode (sc_sub_t ss, dsc_pdom_t pd, ss_prepost_t type, sc_pm_power_mode_t from↩ _mode, sc_pm_power_mode_t to_mode, sc_bool_t rom_boot)
  This function is a pre- and post-amble for power domain power mode transitions.
- void ss_iso_disable (sc_sub_t ss, dsc_pdom_t pd, sc_bool_t enable)
  This function enables/disables the isolation in a subsystem.
- void ss_link_enable (sc_sub_t ss, dsc_pdom_t pd, sc_bool_t enable)
  This function enables/disables the interfaces in a subsystem.
- void ss_ssi_power (sc_sub_t ss, sc_bool_t enable)
  This function enables/disables a subsystems's SSI ports.
- void ss_ssi_bhole_mode (sc_sub_t ss, sc_sub_t remote, uint8_t port, sc_bool_t enable)
  This function enables/disables black hole mode of an SSI.
- void ss_ssi_pause_mode (sc_sub_t ss, sc_sub_t remote, uint8_t port, sc_bool_t enable)
  This function enables/disables pause mode of an SSI.
- void ss_ssi_wait_idle (sc_sub_t ss, sc_sub_t remote, uint8_t port)
  This function waits for an SSI to become idle.
- void ss_adb_enable (sc_sub_t ss, sc_sub_t remote, sc_bool_t enable)
  This function setups an ADB interface between two ss.
- void ss_adb_wait (sc_sub_t ss, sc_sub_t remote, sc_bool_t enable)
  This function waits for the ADB to be powered up.
- void ss_prepost_clock_mode (sc_sub_t ss, ss_clock_t clk, ss_prepost_t type, sc_pm_clk_mode_t from_mode, sc_pm_clk_mode_t to_mode)
  This function is a pre- and post-amble for clock mode transitions.
- sc_bool_t ss_rdc_is_did_vld (sc_sub_t ss, const sc_rm_perm_t *perms)
  This function checks if a subsystem generates transactions matching domains.
- sc_rsrc_t ss_get_resource (sc_sub_t ss, ss_idx_t ss_idx)
  This function returns a system-wide resource from a subsystem and subsystem relative resource index.
- sc_bool_t ss_overlap (sc_faddr_t start1, sc_faddr_t end1, sc_faddr_t start2, sc_faddr_t end2)
  This function determines if two memory regions overlap.
- sc_bool_t ss_temp_sensor (ss_ridx_t rsrc_idx)
  This function gets temp sensor availability of a subsystem.

Variables

- const sc_ss_ep_t **sc_ss_ep** [SC_SUBSYS_LAST+1U]
- ss_base_data_t **sc_ss_data** [SC_SUBSYS_LAST+1U]

18.21.1 Detailed Description

Common functions for interfacing with the subsystems.

18.22 platform/svc/misc/api.h File Reference

Header file containing the public API for the System Controller (SC) Miscellaneous (MISC) function.

Macros

- #define SC_MISC_DMA_GRP_MAX 31U
  Max DMA channel priority group.

Defines for type widths

- #define SC_MISC_DMA_GRP_W 5U
  Width of sc_misc_dma_group_t.

Defines for sc_misc_boot_status_t

- #define SC_MISC_BOOT_STATUS_SUCCESS 0U
  Success.
- #define SC_MISC_BOOT_STATUS_SECURITY 1U
  Security violation.

Defines for sc_misc_temp_t

- #define SC_MISC_TEMP 0U
  Temp sensor.
- #define SC_MISC_TEMP_HIGH 1U
  Temp high alarm.
- #define SC_MISC_TEMP_LOW 2U
  Temp low alarm.

Defines for sc_misc_bt_t

- #define SC_MISC_BT_PRIMARY 0U
  Primary boot.
- #define SC_MISC_BT_SECONDARY 1U
  Secondary boot.
- #define SC_MISC_BT_RECOVERY 2U
  Recovery boot.
- #define SC_MISC_BT_MANUFACTURE 3U
  Manufacture boot.
- #define SC_MISC_BT_SERIAL 4U
  Serial boot.

Typedefs

- typedef uint8_t sc_misc_dma_group_t

  This type is used to store a DMA channel priority group.
- typedef uint8_t sc_misc_boot_status_t

  This type is used report boot status.
- typedef uint8_t sc_misc_temp_t

  This type is used report boot status.
- typedef uint8_t sc_misc_bt_t

  This type is used report the boot type.

Functions

Control Functions

- sc_err_t sc_misc_set_control (sc_ipc_t ipc, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t val)

  This function sets a miscellaneous control value.
- sc_err_t sc_misc_get_control (sc_ipc_t ipc, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t *val)

  This function gets a miscellaneous control value.

DMA Functions

- sc_err_t sc_misc_set_max_dma_group (sc_ipc_t ipc, sc_rm_pt_t pt, sc_misc_dma_group_t max)

  This function configures the max DMA channel priority group for a partition.
- sc_err_t sc_misc_set_dma_group (sc_ipc_t ipc, sc_rsrc_t resource, sc_misc_dma_group_t group)

  This function configures the priority group for a DMA channel.

Debug Functions

- void sc_misc_debug_out (sc_ipc_t ipc, uint8_t ch)

  This function is used output a debug character from the SCU UART.
- sc_err_t sc_misc_waveform_capture (sc_ipc_t ipc, sc_bool_t enable)

  This function starts/stops emulation waveform capture.
- void sc_misc_build_info (sc_ipc_t ipc, uint32_t *build, uint32_t *commit)

  This function is used to return the SCFW build info.
- void sc_misc_api_ver (sc_ipc_t ipc, uint16_t *cl_maj, uint16_t *cl_min, uint16_t *sv_maj, uint16_t *sv_min)

  This function is used to return the SCFW API versions.
- void sc_misc_unique_id (sc_ipc_t ipc, uint32_t *id_l, uint32_t *id_h)

  This function is used to return the device's unique ID.

Other Functions

- sc_err_t sc_misc_set_ari (sc_ipc_t ipc, sc_rsrc_t resource, sc_rsrc_t resource_mst, uint16_t ari, sc_bool_t enable)

  This function configures the ARI match value for PCIe/SATA resources.
- void sc_misc_boot_status (sc_ipc_t ipc, sc_misc_boot_status_t status)

  This function reports boot status.
- sc_err_t sc_misc_boot_done (sc_ipc_t ipc, sc_rsrc_t cpu)

  This function tells the SCFW that a CPU is done booting.
- sc_err_t sc_misc_otp_fuse_read (sc_ipc_t ipc, uint32_t word, uint32_t *val)

This function reads a given fuse word index.

- sc_err_t sc_misc_otp_fuse_write (sc_ipc_t ipc, uint32_t word, uint32_t val)
  This function writes a given fuse word index.
- sc_err_t sc_misc_set_temp (sc_ipc_t ipc, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t celsius, int8_t tenths)
  This function sets a temp sensor alarm.
- sc_err_t sc_misc_get_temp (sc_ipc_t ipc, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t *celsius, int8_t *tenths)
  This function gets a temp sensor value.
- void sc_misc_get_boot_dev (sc_ipc_t ipc, sc_rsrc_t *dev)
  This function returns the boot device.
- sc_err_t sc_misc_get_boot_type (sc_ipc_t ipc, sc_misc_bt_t *type)
  This function returns the boot type.
- sc_err_t sc_misc_get_boot_container (sc_ipc_t ipc, uint8_t *idx)
  This function returns the boot container index.
- void sc_misc_get_button_status (sc_ipc_t ipc, sc_bool_t *status)
  This function returns the current status of the ON/OFF button.
- sc_err_t sc_misc_rompatch_checksum (sc_ipc_t ipc, uint32_t *checksum)
  This function returns the ROM patch checksum.
- sc_err_t sc_misc_board_ioctl (sc_ipc_t ipc, uint32_t *parm1, uint32_t *parm2, uint32_t *parm3)
  This function calls the board IOCTL function.

18.22.1 Detailed Description

Header file containing the public API for the System Controller (SC) Miscellaneous (MISC) function.

18.23 platform/svc/irq/api.h File Reference

Header file containing the public API for the System Controller (SC) Interrupt (IRQ) function.

Macros

- #define SC_IRQ_NUM_GROUP 7U
  Number of groups.

Defines for sc_irq_group_t

- #define SC_IRQ_GROUP_TEMP 0U
  Temp interrupts.
- #define SC_IRQ_GROUP_WDOG 1U
  Watchdog interrupts.
- #define SC_IRQ_GROUP_RTC 2U
  RTC interrupts.
- #define SC_IRQ_GROUP_WAKE 3U
  Wakeup interrupts.
- #define SC_IRQ_GROUP_SYSCTR 4U
  System counter interrupts.
- #define SC_IRQ_GROUP_REBOOTED 5U
  Partition reboot complete.
- #define SC_IRQ_GROUP_REBOOT 6U

Partition reboot starting.

Defines for sc_irq_temp_t

- #define SC_IRQ_TEMP_HIGH (1UL << 0U)
  Temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU0_HIGH (1UL << 1U)
  CPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU1_HIGH (1UL << 2U)
  CPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU0_HIGH (1UL << 3U)
  GPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU1_HIGH (1UL << 4U)
  GPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC0_HIGH (1UL << 5U)
  DRC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC1_HIGH (1UL << 6U)
  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_VPU_HIGH (1UL << 7U)
  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC0_HIGH (1UL << 8U)
  PMIC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC1_HIGH (1UL << 9U)
  PMIC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_LOW (1UL << 10U)
  Temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU0_LOW (1UL << 11U)
  CPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_CPU1_LOW (1UL << 12U)
  CPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU0_LOW (1UL << 13U)
  GPU0 temp alarm interrupt.
- #define SC_IRQ_TEMP_GPU1_LOW (1UL << 14U)
  GPU1 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC0_LOW (1UL << 15U)
  DRC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_DRC1_LOW (1UL << 16U)
  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_VPU_LOW (1UL << 17U)
  DRC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC0_LOW (1UL << 18U)
  PMIC0 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC1_LOW (1UL << 19U)
  PMIC1 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC2_HIGH (1UL << 20U)
  PMIC2 temp alarm interrupt.
- #define SC_IRQ_TEMP_PMIC2_LOW (1UL << 21U)
  PMIC2 temp alarm interrupt.

Defines for sc_irq_wdog_t

- #define SC_IRQ_WDOG (1U << 0U)
  Watchdog interrupt.

Defines for sc_irq_rtc_t

- #define SC_IRQ_RTC (1U << 0U)
  RTC interrupt.

Defines for sc_irq_wake_t

- #define SC_IRQ_BUTTON (1U << 0U)
  Button interrupt.
- #define SC_IRQ_PAD (1U << 1U)
  Pad wakeup.
- #define SC_IRQ_USR1 (1U << 2U)
  User defined 1.
- #define SC_IRQ_USR2 (1U << 3U)
  User defined 2.
- #define SC_IRQ_BC_PAD (1U << 4U)
  Pad wakeup (broadcast to all partitions)
- #define SC_IRQ_SW_WAKE (1U << 5U)
  Software requested wake.
- #define SC_IRQ_SECVIO (1U << 6U)
  Security violation.

Defines for sc_irq_sysctr_t

- #define SC_IRQ_SYSCTR (1U << 0U)
  SYSCTR interrupt.

Typedefs

- typedef uint8_t sc_irq_group_t
  This type is used to declare an interrupt group.
- typedef uint8_t sc_irq_temp_t
  This type is used to declare a bit mask of temp interrupts.
- typedef uint8_t sc_irq_wdog_t
  This type is used to declare a bit mask of watchdog interrupts.
- typedef uint8_t sc_irq_rtc_t
  This type is used to declare a bit mask of RTC interrupts.
- typedef uint8_t sc_irq_wake_t
  This type is used to declare a bit mask of wakeup interrupts.

Functions

- sc_err_t sc_irq_enable (sc_ipc_t ipc, sc_rsrc_t resource, sc_irq_group_t group, uint32_t mask, sc_bool_t enable)
  This function enables/disables interrupts.
- sc_err_t sc_irq_status (sc_ipc_t ipc, sc_rsrc_t resource, sc_irq_group_t group, uint32_t *status)
  This function returns the current interrupt status (regardless if masked).

18.23.1 Detailed Description

Header file containing the public API for the System Controller (SC) Interrupt (IRQ) function.

18.24 platform/svc/pad/api.h File Reference

Header file containing the public API for the System Controller (SC) Pad Control (PAD) function.

Macros

Defines for type widths

- #define SC_PAD_MUX_W 3U
  Width of mux parameter.

Defines for sc_pad_config_t

- #define SC_PAD_CONFIG_NORMAL 0U
  Normal.
- #define SC_PAD_CONFIG_OD 1U
  Open Drain.
- #define SC_PAD_CONFIG_OD_IN 2U
  Open Drain and input.
- #define SC_PAD_CONFIG_OUT_IN 3U
  Output and input.

Defines for sc_pad_iso_t

- #define SC_PAD_ISO_OFF 0U
  ISO latch is transparent.
- #define SC_PAD_ISO_EARLY 1U
  Follow EARLY_ISO.
- #define SC_PAD_ISO_LATE 2U
  Follow LATE_ISO.
- #define SC_PAD_ISO_ON 3U
  ISO latched data is held.

Defines for sc_pad_28fdsoi_dse_t

- #define SC_PAD_28FDSOI_DSE_18V_1MA 0U
  Drive strength of 1mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_2MA 1U
  Drive strength of 2mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_4MA 2U
  Drive strength of 4mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_6MA 3U
  Drive strength of 6mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_8MA 4U
  Drive strength of 8mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_10MA 5U
  Drive strength of 10mA for 1.8v.

- #define SC_PAD_28FDSOI_DSE_18V_12MA 6U
  Drive strength of 12mA for 1.8v.
- #define SC_PAD_28FDSOI_DSE_18V_HS 7U
  High-speed drive strength for 1.8v.
- #define SC_PAD_28FDSOI_DSE_33V_2MA 0U
  Drive strength of 2mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_33V_4MA 1U
  Drive strength of 4mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_33V_8MA 2U
  Drive strength of 8mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_33V_12MA 3U
  Drive strength of 12mA for 3.3v.
- #define SC_PAD_28FDSOI_DSE_DV_HIGH 0U
  High drive strength for dual volt.
- #define SC_PAD_28FDSOI_DSE_DV_LOW 1U
  Low drive strength for dual volt.

Defines for sc_pad_28fdsoi_ps_t

- #define SC_PAD_28FDSOI_PS_KEEPER 0U
  Bus-keeper (only valid for 1.8v)
- #define SC_PAD_28FDSOI_PS_PU 1U
  Pull-up.
- #define SC_PAD_28FDSOI_PS_PD 2U
  Pull-down.
- #define SC_PAD_28FDSOI_PS_NONE 3U
  No pull (disabled)

Defines for sc_pad_28fdsoi_pus_t

- #define SC_PAD_28FDSOI_PUS_30K_PD 0U
  30K pull-down
- #define SC_PAD_28FDSOI_PUS_100K_PU 1U
  100K pull-up
- #define SC_PAD_28FDSOI_PUS_3K_PU 2U
  3K pull-up
- #define SC_PAD_28FDSOI_PUS_30K_PU 3U
  30K pull-up

Defines for sc_pad_wakeup_t

- #define SC_PAD_WAKEUP_OFF 0U
  Off.
- #define SC_PAD_WAKEUP_CLEAR 1U
  Clears pending flag.
- #define SC_PAD_WAKEUP_LOW_LVL 4U
  Low level.
- #define SC_PAD_WAKEUP_FALL_EDGE 5U
  Falling edge.
- #define SC_PAD_WAKEUP_RISE_EDGE 6U
  Rising edge.
- #define SC_PAD_WAKEUP_HIGH_LVL 7U
  High-level.

Typedefs

- typedef uint8_t sc_pad_config_t

  This type is used to declare a pad config.
- typedef uint8_t sc_pad_iso_t

  This type is used to declare a pad low-power isolation config.
- typedef uint8_t sc_pad_28fdsoi_dse_t

  This type is used to declare a drive strength.
- typedef uint8_t sc_pad_28fdsoi_ps_t

  This type is used to declare a pull select.
- typedef uint8_t sc_pad_28fdsoi_pus_t

  This type is used to declare a pull-up select.
- typedef uint8_t sc_pad_wakeup_t

  This type is used to declare a wakeup mode of a pad.

Functions

Generic Functions

- sc_err_t sc_pad_set_mux (sc_ipc_t ipc, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso)

  This function configures the mux settings for a pad.
- sc_err_t sc_pad_get_mux (sc_ipc_t ipc, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso)

  This function gets the mux settings for a pad.
- sc_err_t sc_pad_set_gp (sc_ipc_t ipc, sc_pad_t pad, uint32_t ctrl)

  This function configures the general purpose pad control.
- sc_err_t sc_pad_get_gp (sc_ipc_t ipc, sc_pad_t pad, uint32_t *ctrl)

  This function gets the general purpose pad control.
- sc_err_t sc_pad_set_wakeup (sc_ipc_t ipc, sc_pad_t pad, sc_pad_wakeup_t wakeup)

  This function configures the wakeup mode of the pad.
- sc_err_t sc_pad_get_wakeup (sc_ipc_t ipc, sc_pad_t pad, sc_pad_wakeup_t *wakeup)

  This function gets the wakeup mode of a pad.
- sc_err_t sc_pad_set_all (sc_ipc_t ipc, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso, uint32_t ctrl, sc_pad_wakeup_t wakeup)

  This function configures a pad.
- sc_err_t sc_pad_get_all (sc_ipc_t ipc, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso, uint32_t *ctrl, sc_pad_wakeup_t *wakeup)

  This function gets a pad's config.

SoC Specific Functions

- sc_err_t sc_pad_set (sc_ipc_t ipc, sc_pad_t pad, uint32_t val)

  This function configures the settings for a pad.
- sc_err_t sc_pad_get (sc_ipc_t ipc, sc_pad_t pad, uint32_t *val)

  This function gets the settings for a pad.
- sc_err_t sc_pad_config (sc_ipc_t ipc, sc_pad_t pad, uint32_t val)

  This function writes a configuration register.

Technology Specific Functions

- sc_err_t sc_pad_set_gp_28fdsoi (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_pad_28fdsoi_ps_t ps)
  This function configures the pad control specific to 28FDSOI.
- sc_err_t sc_pad_get_gp_28fdsoi (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_pad_28fdsoi_ps_t *ps)
  This function gets the pad control specific to 28FDSOI.
- sc_err_t sc_pad_set_gp_28fdsoi_hsic (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_bool_t hys, sc_pad_28fdsoi_pus_t pus, sc_bool_t pke, sc_bool_t pue)
  This function configures the pad control specific to 28FDSOI.
- sc_err_t sc_pad_get_gp_28fdsoi_hsic (sc_ipc_t ipc, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_bool_t *hys, sc_pad_28fdsoi_pus_t *pus, sc_bool_t *pke, sc_bool_t *pue)
  This function gets the pad control specific to 28FDSOI.
- sc_err_t sc_pad_set_gp_28fdsoi_comp (sc_ipc_t ipc, sc_pad_t pad, uint8_t compen, sc_bool_t fastfrz, uint8_t rasrcp, uint8_t rasrcn, sc_bool_t nasrc_sel, sc_bool_t psw_ovr)
  This function configures the compensation control specific to 28FDSOI.
- sc_err_t sc_pad_get_gp_28fdsoi_comp (sc_ipc_t ipc, sc_pad_t pad, uint8_t *compen, sc_bool_t *fastfrz, uint8_t *rasrcp, uint8_t *rasrcn, sc_bool_t *nasrc_sel, sc_bool_t *compok, uint8_t *nasrc, sc_bool_t *psw↩ _ovr)
  This function gets the compensation control specific to 28FDSOI.

18.24.1 Detailed Description

Header file containing the public API for the System Controller (SC) Pad Control (PAD) function.

18.25 platform/svc/pm/api.h File Reference

Header file containing the public API for the System Controller (SC) Power Management (PM) function.

Macros

Defines for type widths

- #define SC_PM_POWER_MODE_W 2U
  Width of sc_pm_power_mode_t.
- #define SC_PM_CLOCK_MODE_W 3U
  Width of sc_pm_clock_mode_t.
- #define SC_PM_RESET_TYPE_W 2U
  Width of sc_pm_reset_type_t.
- #define SC_PM_RESET_REASON_W 4U
  Width of sc_pm_reset_reason_t.

Defines for ALL parameters

- #define SC_PM_CLK_ALL ((sc_pm_clk_t) UINT8_MAX)
  All clocks.

Defines for sc_pm_power_mode_t

- #define SC_PM_PW_MODE_OFF 0U
  Power off.

- #define SC_PM_PW_MODE_STBY 1U
  Power in standby.
- #define SC_PM_PW_MODE_LP 2U
  Power in low-power.
- #define SC_PM_PW_MODE_ON 3U
  Power on.

Defines for sc_pm_clk_t

- #define SC_PM_CLK_SLV_BUS 0U
  Slave bus clock.
- #define SC_PM_CLK_MST_BUS 1U
  Master bus clock.
- #define SC_PM_CLK_PER 2U
  Peripheral clock.
- #define SC_PM_CLK_PHY 3U
  Phy clock.
- #define SC_PM_CLK_MISC 4U
  Misc clock.
- #define SC_PM_CLK_MISC0 0U
  Misc 0 clock.
- #define SC_PM_CLK_MISC1 1U
  Misc 1 clock.
- #define SC_PM_CLK_MISC2 2U
  Misc 2 clock.
- #define SC_PM_CLK_MISC3 3U
  Misc 3 clock.
- #define SC_PM_CLK_MISC4 4U
  Misc 4 clock.
- #define SC_PM_CLK_CPU 2U
  CPU clock.
- #define SC_PM_CLK_PLL 4U
  PLL.
- #define SC_PM_CLK_BYPASS 4U
  Bypass clock.

Defines for sc_pm_clk_parent_t

- #define SC_PM_PARENT_XTAL 0U
  Parent is XTAL.
- #define SC_PM_PARENT_PLL0 1U
  Parent is PLL0.
- #define SC_PM_PARENT_PLL1 2U
  Parent is PLL1 or PLL0/2.
- #define SC_PM_PARENT_PLL2 3U
  Parent in PLL2 or PLL0/4.
- #define SC_PM_PARENT_BYPS 4U
  Parent is a bypass clock.

Defines for sc_pm_reset_type_t

- #define SC_PM_RESET_TYPE_COLD 0U
  Cold reset.

- #define SC_PM_RESET_TYPE_WARM 1U
  Warm reset.
- #define SC_PM_RESET_TYPE_BOARD 2U
  Board reset.

Defines for sc_pm_reset_reason_t

- #define SC_PM_RESET_REASON_POR 0U
  Power on reset.
- #define SC_PM_RESET_REASON_JTAG 1U
  JTAG reset.
- #define SC_PM_RESET_REASON_SW 2U
  Software reset.
- #define SC_PM_RESET_REASON_WDOG 3U
  Partition watchdog reset.
- #define SC_PM_RESET_REASON_LOCKUP 4U
  SCU lockup reset.
- #define SC_PM_RESET_REASON_SNVS 5U
  SNVS reset.
- #define SC_PM_RESET_REASON_TEMP 6U
  Temp panic reset.
- #define SC_PM_RESET_REASON_MSI 7U
  MSI reset.
- #define SC_PM_RESET_REASON_UECC 8U
  ECC reset.
- #define SC_PM_RESET_REASON_SCFW_WDOG 9U
  SCFW watchdog reset.
- #define SC_PM_RESET_REASON_ROM_WDOG 10U
  SCU ROM watchdog reset.
- #define SC_PM_RESET_REASON_SECO 11U
  SECO reset.
- #define SC_PM_RESET_REASON_SCFW_FAULT 12U
  SCFW fault reset.
- #define SC_PM_RESET_REASON_V2X_DEBUG 13U
  V2X debug switch.

Defines for sc_pm_sys_if_t

- #define SC_PM_SYS_IF_INTERCONNECT 0U
  System interconnect.
- #define SC_PM_SYS_IF_MU 1U
  AP -> SCU message units.
- #define SC_PM_SYS_IF_OCMEM 2U
  On-chip memory (ROM/OCRAM)
- #define SC_PM_SYS_IF_DDR 3U
  DDR memory.

Defines for sc_pm_wake_src_t

- #define SC_PM_WAKE_SRC_NONE 0U
  No wake source, used for self-kill.
- #define SC_PM_WAKE_SRC_SCU 1U
  Wakeup from SCU to resume CPU (IRQSTEER & GIC powered down)
- #define SC_PM_WAKE_SRC_IRQSTEER 2U
  Wakeup from IRQSTEER to resume CPU (GIC powered down)
- #define SC_PM_WAKE_SRC_IRQSTEER_GIC 3U
  Wakeup from IRQSTEER+GIC to wake CPU (GIC clock gated)
- #define SC_PM_WAKE_SRC_GIC 4U
  Wakeup from GIC to wake CPU.

Typedefs

- typedef uint8_t sc_pm_power_mode_t

  This type is used to declare a power mode.
- typedef uint8_t sc_pm_clk_t

  This type is used to declare a clock.
- typedef uint8_t sc_pm_clk_parent_t

  This type is used to declare the clock parent.
- typedef uint32_t sc_pm_clock_rate_t

  This type is used to declare clock rates.
- typedef uint8_t sc_pm_reset_type_t

  This type is used to declare a desired reset type.
- typedef uint8_t sc_pm_reset_reason_t

  This type is used to declare a reason for a reset.
- typedef uint8_t sc_pm_sys_if_t

  This type is used to specify a system-level interface to be power managed.
- typedef uint8_t sc_pm_wake_src_t

  This type is used to specify a wake source for CPU resources.

Functions

Power Functions

- sc_err_t sc_pm_set_sys_power_mode (sc_ipc_t ipc, sc_pm_power_mode_t mode)

  This function sets the system power mode.
- sc_err_t sc_pm_set_partition_power_mode (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_power_mode_t mode)

  This function sets the power mode of a partition.
- sc_err_t sc_pm_get_sys_power_mode (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_power_mode_t *mode)

  This function gets the power mode of a partition.
- sc_err_t sc_pm_partition_wake (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function sends a wake interrupt to a partition.
- sc_err_t sc_pm_set_resource_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  This function sets the power mode of a resource.
- sc_err_t sc_pm_set_resource_power_mode_all (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_power_mode_t mode, sc_rsrc_t exclude)

  This function sets the power mode for all the resources owned by a child partition.
- sc_err_t sc_pm_get_resource_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t *mode)

  This function gets the power mode of a resource.
- sc_err_t sc_pm_req_low_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  This function specifies the low power mode some of the resources can enter based on their state.
- sc_err_t sc_pm_req_cpu_low_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)

  This function requests low-power mode entry for CPU/cluster resources.
- sc_err_t sc_pm_set_cpu_resume_addr (sc_ipc_t ipc, sc_rsrc_t resource, sc_faddr_t address)

  This function is used to set the resume address of a CPU.
- sc_err_t sc_pm_set_cpu_resume (sc_ipc_t ipc, sc_rsrc_t resource, sc_bool_t isPrimary, sc_faddr_t address)

  This function is used to set parameters for CPU resume from low-power mode.
- sc_err_t sc_pm_req_sys_if_power_mode (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_sys_if_t sys_↩ if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)

  This function requests the power mode configuration for system-level interfaces including messaging units, interconnect, and memories.

Clock/PLL Functions

- sc_err_t sc_pm_set_clock_rate (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)
  This function sets the rate of a resource's clock/PLL.
- sc_err_t sc_pm_get_clock_rate (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)
  This function gets the rate of a resource's clock/PLL.
- sc_err_t sc_pm_clock_enable (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_bool_t enable, sc_bool_t autog)
  This function enables/disables a resource's clock.
- sc_err_t sc_pm_set_clock_parent (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t parent)
  This function sets the parent of a resource's clock.
- sc_err_t sc_pm_get_clock_parent (sc_ipc_t ipc, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t *parent)
  This function gets the parent of a resource's clock.

Reset Functions

- sc_err_t sc_pm_reset (sc_ipc_t ipc, sc_pm_reset_type_t type)
  This function is used to reset the system.
- sc_err_t sc_pm_reset_reason (sc_ipc_t ipc, sc_pm_reset_reason_t *reason)
  This function gets a caller's reset reason.
- sc_err_t sc_pm_get_reset_part (sc_ipc_t ipc, sc_rm_pt_t *pt)
  This function gets the partition that caused a reset.
- sc_err_t sc_pm_boot (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)
  This function is used to boot a partition.
- sc_err_t sc_pm_set_boot_parm (sc_ipc_t ipc, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)
  This function is used to change the boot parameters for a partition.
- void sc_pm_reboot (sc_ipc_t ipc, sc_pm_reset_type_t type)
  This function is used to reboot the caller's partition.
- sc_err_t sc_pm_reboot_partition (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pm_reset_type_t type)
  This function is used to reboot a partition.
- sc_err_t sc_pm_reboot_continue (sc_ipc_t ipc, sc_rm_pt_t pt)
  This function is used to continue the reboot a partition.
- sc_err_t sc_pm_cpu_start (sc_ipc_t ipc, sc_rsrc_t resource, sc_bool_t enable, sc_faddr_t address)
  This function is used to start/stop a CPU.
- void sc_pm_cpu_reset (sc_ipc_t ipc, sc_rsrc_t resource, sc_faddr_t address)
  This function is used to reset a CPU.
- sc_err_t sc_pm_resource_reset (sc_ipc_t ipc, sc_rsrc_t resource)
  This function is used to reset a peripheral.
- sc_bool_t sc_pm_is_partition_started (sc_ipc_t ipc, sc_rm_pt_t pt)
  This function returns a bool indicating if a partition was started.

18.25.1 Detailed Description

Header file containing the public API for the System Controller (SC) Power Management (PM) function.

This includes functions for power state control, clock control, reset control, and wake-up event control.

18.26 platform/svc/seco/api.h File Reference

Header file containing the public API for the System Controller (SC) Security (SECO) function.

Macros

Defines for sc_seco_auth_cmd_t

- #define SC_SECO_AUTH_CONTAINER 0U
  Authenticate container.
- #define SC_SECO_VERIFY_IMAGE 1U
  Verify image.
- #define SC_SECO_REL_CONTAINER 2U
  Release container.
- #define SC_SECO_AUTH_SECO_FW 3U
  SECO Firmware.
- #define SC_SECO_AUTH_HDMI_TX_FW 4U
  HDMI TX Firmware.
- #define SC_SECO_AUTH_HDMI_RX_FW 5U
  HDMI RX Firmware.
- #define SC_SECO_EVERIFY_IMAGE 6U
  Enhanced verify image.

Defines for seco_rng_stat_t

- #define SC_SECO_RNG_STAT_UNAVAILABLE 0U
  Unable to initialize the RNG.
- #define SC_SECO_RNG_STAT_INPROGRESS 1U
  Initialization is on-going.
- #define SC_SECO_RNG_STAT_READY 2U
  Initialized.

Typedefs

- typedef uint8_t sc_seco_auth_cmd_t
  This type is used to issue SECO authenticate commands.
- typedef uint32_t sc_seco_rng_stat_t
  This type is used to return the RNG initialization status.

Functions

Image Functions

- sc_err_t sc_seco_image_load (sc_ipc_t ipc, sc_faddr_t addr_src, sc_faddr_t addr_dst, uint32_t len, sc_bool_t fw)
  This function loads a SECO image.
- sc_err_t sc_seco_authenticate (sc_ipc_t ipc, sc_seco_auth_cmd_t cmd, sc_faddr_t addr)
  This function is used to authenticate a SECO image or command.
- sc_err_t sc_seco_enh_authenticate (sc_ipc_t ipc, sc_seco_auth_cmd_t cmd, sc_faddr_t addr, uint32_t mask1, uint32_t mask2)

This function is used to authenticate a SECO image or command.

Lifecycle Functions

- sc_err_t sc_seco_forward_lifecycle (sc_ipc_t ipc, uint32_t change)
  This function updates the lifecycle of the device.
- sc_err_t sc_seco_return_lifecycle (sc_ipc_t ipc, sc_faddr_t addr)
  This function updates the lifecycle to one of the return lifecycles.
- sc_err_t sc_seco_commit (sc_ipc_t ipc, uint32_t *info)
  This function is used to commit into the fuses any new SRK revocation and FW version information that have been found in the primary and secondary containers.

Attestation Functions

- sc_err_t sc_seco_attest_mode (sc_ipc_t ipc, uint32_t mode)
  This function is used to set the attestation mode.
- sc_err_t sc_seco_attest (sc_ipc_t ipc, uint64_t nonce)
  This function is used to request attestation.
- sc_err_t sc_seco_get_attest_pkey (sc_ipc_t ipc, sc_faddr_t addr)
  This function is used to retrieve the attestation public key.
- sc_err_t sc_seco_get_attest_sign (sc_ipc_t ipc, sc_faddr_t addr)
  This function is used to retrieve attestation signature and parameters.
- sc_err_t sc_seco_attest_verify (sc_ipc_t ipc, sc_faddr_t addr)
  This function is used to verify attestation.

Key Functions

- sc_err_t sc_seco_gen_key_blob (sc_ipc_t ipc, uint32_t id, sc_faddr_t load_addr, sc_faddr_t export_addr, uint16_t max_size)
  This function is used to generate a SECO key blob.
- sc_err_t sc_seco_load_key (sc_ipc_t ipc, uint32_t id, sc_faddr_t addr)
  This function is used to load a SECO key.

Manufacturing Protection Functions

- sc_err_t sc_seco_get_mp_key (sc_ipc_t ipc, sc_faddr_t dst_addr, uint16_t dst_size)
  This function is used to get the manufacturing protection public key.
- sc_err_t sc_seco_update_mpmr (sc_ipc_t ipc, sc_faddr_t addr, uint8_t size, uint8_t lock)
  This function is used to update the manufacturing protection message register.
- sc_err_t sc_seco_get_mp_sign (sc_ipc_t ipc, sc_faddr_t msg_addr, uint16_t msg_size, sc_faddr_t dst_addr, uint16_t dst_size)
  This function is used to get the manufacturing protection signature.

Debug Functions

- void sc_seco_build_info (sc_ipc_t ipc, uint32_t *version, uint32_t *commit)
  This function is used to return the SECO FW build info.
- sc_err_t sc_seco_chip_info (sc_ipc_t ipc, uint16_t *lc, uint16_t *monotonic, uint32_t *uid_l, uint32_t *uid_h)
  This function is used to return SECO chip info.
- sc_err_t sc_seco_enable_debug (sc_ipc_t ipc, sc_faddr_t addr)
  This function securely enables debug.
- sc_err_t sc_seco_get_event (sc_ipc_t ipc, uint8_t idx, uint32_t *event)

This function is used to return an event from the SECO error log.

Miscellaneous Functions

- sc_err_t sc_seco_fuse_write (sc_ipc_t ipc, sc_faddr_t addr)
  This function securely writes a group of fuse words.
- sc_err_t sc_seco_patch (sc_ipc_t ipc, sc_faddr_t addr)
  This function applies a patch.
- sc_err_t sc_seco_set_mono_counter_partition (sc_ipc_t ipc, uint16_t *she)
  This function partitions the monotonic counter.
- sc_err_t sc_seco_set_fips_mode (sc_ipc_t ipc, uint8_t mode, uint32_t *reason)
  This function configures the SECO in FIPS mode.
- sc_err_t sc_seco_start_rng (sc_ipc_t ipc, sc_seco_rng_stat_t *status)
  This function starts the random number generator.
- sc_err_t sc_seco_sab_msg (sc_ipc_t ipc, sc_faddr_t addr)
  This function sends a generic signed message to the SECO SHE/HSM components.
- sc_err_t sc_seco_secvio_enable (sc_ipc_t ipc)
  This function is used to enable security violation and tamper interrupts.
- sc_err_t sc_seco_secvio_config (sc_ipc_t ipc, uint8_t id, uint8_t access, uint32_t *data0, uint32_t *data1, uint32_t *data2, uint32_t *data3, uint32_t *data4, uint8_t size)
  This function is used to read/write SNVS security violation and tamper registers.
- sc_err_t sc_seco_secvio_dgo_config (sc_ipc_t ipc, uint8_t id, uint8_t access, uint32_t *data)
  This function is used to read/write SNVS security violation and tamper DGO registers.

18.26.1 Detailed Description

Header file containing the public API for the System Controller (SC) Security (SECO) function.

18.27 platform/svc/rm/api.h File Reference

Header file containing the public API for the System Controller (SC) Resource Management (RM) function.

Macros

Defines for type widths

- #define SC_RM_PARTITION_W 5U
  Width of sc_rm_pt_t.
- #define SC_RM_MEMREG_W 6U
  Width of sc_rm_mr_t.
- #define SC_RM_DID_W 4U
  Width of sc_rm_did_t.
- #define SC_RM_SID_W 6U
  Width of sc_rm_sid_t.
- #define SC_RM_SPA_W 2U
  Width of sc_rm_spa_t.
- #define SC_RM_PERM_W 3U
  Width of sc_rm_perm_t.
- #define SC_RM_DET_W 1U
  Width of sc_rm_det_t.
- #define SC_RM_RMSG_W 4U

Width of sc_rm_rmsg_t.

Defines for ALL parameters

- #define SC_RM_PT_ALL ((sc_rm_pt_t) UINT8_MAX)
  All partitions.
- #define SC_RM_MR_ALL ((sc_rm_mr_t) UINT8_MAX)
  All memory regions.

Defines for sc_rm_spa_t

- #define SC_RM_SPA_PASSTHRU 0U
  Pass through (attribute driven by master)
- #define SC_RM_SPA_PASSSID 1U
  Pass through and output on SID.
- #define SC_RM_SPA_ASSERT 2U
  Assert (force to be secure/privileged)
- #define SC_RM_SPA_NEGATE 3U
  Negate (force to be non-secure/user)

Defines for sc_rm_perm_t

- #define SC_RM_PERM_NONE 0U
  No access.
- #define SC_RM_PERM_SEC_R 1U
  Secure RO.
- #define SC_RM_PERM_SECPRIV_RW 2U
  Secure privilege R/W.
- #define SC_RM_PERM_SEC_RW 3U
  Secure R/W.
- #define SC_RM_PERM_NSPRIV_R 4U
  Secure R/W, non-secure privilege RO.
- #define SC_RM_PERM_NS_R 5U
  Secure R/W, non-secure RO.
- #define SC_RM_PERM_NSPRIV_RW 6U
  Secure R/W, non-secure privilege R/W.
- #define SC_RM_PERM_FULL 7U
  Full access.

Typedefs

- typedef uint8_t sc_rm_pt_t
  This type is used to declare a resource partition.
- typedef uint8_t sc_rm_mr_t
  This type is used to declare a memory region.
- typedef uint8_t sc_rm_did_t
  This type is used to declare a resource domain ID used by the isolation HW.
- typedef uint16_t sc_rm_sid_t
  This type is used to declare an SMMU StreamID.
- typedef uint8_t sc_rm_spa_t

This type is a used to declare master transaction attributes.

- typedef uint8_t sc_rm_perm_t

  This type is used to declare a resource/memory region access permission.

- typedef uint8_t sc_rm_det_t

  This type is used to indicate memory region transactions should detour to the IEE.

- typedef uint8_t sc_rm_rmsg_t

  This type is used to assign an RMSG value to a memory region.

Functions

Partition Functions

- sc_err_t sc_rm_partition_alloc (sc_ipc_t ipc, sc_rm_pt_t *pt, sc_bool_t secure, sc_bool_t isolated, sc_bool_t restricted, sc_bool_t grant, sc_bool_t coherent)

  This function requests that the SC create a new resource partition.

- sc_err_t sc_rm_set_confidential (sc_ipc_t ipc, sc_rm_pt_t pt, sc_bool_t retro)

  This function makes a partition confidential.

- sc_err_t sc_rm_partition_free (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function frees a partition and assigns all resources to the caller.

- sc_rm_did_t sc_rm_get_did (sc_ipc_t ipc)

  This function returns the DID of a partition.

- sc_err_t sc_rm_partition_static (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rm_did_t did)

  This function forces a partition to use a specific static DID.

- sc_err_t sc_rm_partition_lock (sc_ipc_t ipc, sc_rm_pt_t pt)

  This function locks a partition.

- sc_err_t sc_rm_get_partition (sc_ipc_t ipc, sc_rm_pt_t *pt)

  This function gets the partition handle of the caller.

- sc_err_t sc_rm_set_parent (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rm_pt_t pt_parent)

  This function sets a new parent for a partition.

- sc_err_t sc_rm_move_all (sc_ipc_t ipc, sc_rm_pt_t pt_src, sc_rm_pt_t pt_dst, sc_bool_t move_rsrc, sc_bool_t move_pads)

  This function moves all movable resources/pads owned by a source partition to a destination partition.

Resource Functions

- sc_err_t sc_rm_assign_resource (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rsrc_t resource)

  This function assigns ownership of a resource to a partition.

- sc_err_t sc_rm_set_resource_movable (sc_ipc_t ipc, sc_rsrc_t resource_fst, sc_rsrc_t resource_lst, sc_bool_t movable)

  This function flags resources as movable or not.

- sc_err_t sc_rm_set_subsys_rsrc_movable (sc_ipc_t ipc, sc_rsrc_t resource, sc_bool_t movable)

  This function flags all of a subsystem's resources as movable or not.

- sc_err_t sc_rm_set_master_attributes (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_spa_t sa, sc_rm_spa_t pa, sc_bool_t smmu_bypass)

  This function sets attributes for a resource which is a bus master (i.e.

- sc_err_t sc_rm_set_master_sid (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_sid_t sid)

  This function sets the StreamID for a resource which is a bus master (i.e.

- sc_err_t sc_rm_set_peripheral_permissions (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_pt_t pt, sc_rm_perm_t perm)

  This function sets access permissions for a peripheral resource.

- sc_bool_t sc_rm_is_resource_owned (sc_ipc_t ipc, sc_rsrc_t resource)

  This function gets ownership status of a resource.

- sc_err_t sc_rm_get_resource_owner (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_pt_t *pt)
  This function is used to get the owner of a resource.
- sc_bool_t sc_rm_is_resource_master (sc_ipc_t ipc, sc_rsrc_t resource)
  This function is used to test if a resource is a bus master.
- sc_bool_t sc_rm_is_resource_peripheral (sc_ipc_t ipc, sc_rsrc_t resource)
  This function is used to test if a resource is a peripheral.
- sc_err_t sc_rm_get_resource_info (sc_ipc_t ipc, sc_rsrc_t resource, sc_rm_sid_t *sid)
  This function is used to obtain info about a resource.

Memory Region Functions

- sc_err_t sc_rm_memreg_alloc (sc_ipc_t ipc, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_end)
  This function requests that the SC create a new memory region.
- sc_err_t sc_rm_memreg_split (sc_ipc_t ipc, sc_rm_mr_t mr, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)
  This function requests that the SC split an existing memory region.
- sc_err_t sc_rm_memreg_frag (sc_ipc_t ipc, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)
  This function requests that the SC fragment a memory region.
- sc_err_t sc_rm_memreg_free (sc_ipc_t ipc, sc_rm_mr_t mr)
  This function frees a memory region.
- sc_err_t sc_rm_find_memreg (sc_ipc_t ipc, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_end)
  Internal SC function to find a memory region.
- sc_err_t sc_rm_assign_memreg (sc_ipc_t ipc, sc_rm_pt_t pt, sc_rm_mr_t mr)
  This function assigns ownership of a memory region.
- sc_err_t sc_rm_set_memreg_permissions (sc_ipc_t ipc, sc_rm_mr_t mr, sc_rm_pt_t pt, sc_rm_perm_t perm)
  This function sets access permissions for a memory region.
- sc_err_t sc_rm_set_memreg_iee (sc_ipc_t ipc, sc_rm_mr_t mr, sc_rm_det_t det, sc_rm_rmsg_t rmsg)
  This function configures the IEE parameters for a memory region.
- sc_bool_t sc_rm_is_memreg_owned (sc_ipc_t ipc, sc_rm_mr_t mr)
  This function gets ownership status of a memory region.
- sc_err_t sc_rm_get_memreg_info (sc_ipc_t ipc, sc_rm_mr_t mr, sc_faddr_t *addr_start, sc_faddr_t *addr_↩ end)
  This function is used to obtain info about a memory region.

Pad Functions

- sc_err_t sc_rm_assign_pad (sc_ipc_t ipc, sc_rm_pt_t pt, sc_pad_t pad)
  This function assigns ownership of a pad to a partition.
- sc_err_t sc_rm_set_pad_movable (sc_ipc_t ipc, sc_pad_t pad_fst, sc_pad_t pad_lst, sc_bool_t movable)
  This function flags pads as movable or not.
- sc_bool_t sc_rm_is_pad_owned (sc_ipc_t ipc, sc_pad_t pad)
  This function gets ownership status of a pad.

Debug Functions

- void sc_rm_dump (sc_ipc_t ipc)
  This function dumps the RM state for debug.

18.27.1 Detailed Description

Header file containing the public API for the System Controller (SC) Resource Management (RM) function.

This includes functions for partitioning resources, pads, and memory regions.

18.28 platform/svc/timer/api.h File Reference

Header file containing the public API for the System Controller (SC) Timer function.

Macros

Defines for type widths

- #define SC_TIMER_ACTION_W 3U
  Width of sc_timer_wdog_action_t.

Defines for sc_timer_wdog_action_t

- #define SC_TIMER_WDOG_ACTION_PARTITION 0U
  Reset partition.
- #define SC_TIMER_WDOG_ACTION_WARM 1U
  Warm reset system.
- #define SC_TIMER_WDOG_ACTION_COLD 2U
  Cold reset system.
- #define SC_TIMER_WDOG_ACTION_BOARD 3U
  Reset board.
- #define SC_TIMER_WDOG_ACTION_IRQ 4U
  Only generate IRQs.

Typedefs

- typedef uint8_t sc_timer_wdog_action_t
  This type is used to configure the watchdog action.
- typedef uint32_t sc_timer_wdog_time_t
  This type is used to declare a watchdog time value in milliseconds.

Functions

Watchdog Functions

- sc_err_t sc_timer_set_wdog_timeout (sc_ipc_t ipc, sc_timer_wdog_time_t timeout)
  This function sets the watchdog timeout in milliseconds.
- sc_err_t sc_timer_set_wdog_pre_timeout (sc_ipc_t ipc, sc_timer_wdog_time_t pre_timeout)
  This function sets the watchdog pre-timeout in milliseconds.
- sc_err_t sc_timer_set_wdog_window (sc_ipc_t ipc, sc_timer_wdog_time_t window)
  This function sets the watchdog window in milliseconds.
- sc_err_t sc_timer_start_wdog (sc_ipc_t ipc, sc_bool_t lock)
  This function starts the watchdog.

- sc_err_t sc_timer_stop_wdog (sc_ipc_t ipc)
  This function stops the watchdog if it is not locked.
- sc_err_t sc_timer_ping_wdog (sc_ipc_t ipc)
  This function pings (services, kicks) the watchdog resetting the time before expiration back to the timeout.
- sc_err_t sc_timer_get_wdog_status (sc_ipc_t ipc, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *max_timeout, sc_timer_wdog_time_t *remaining_time)
  This function gets the status of the watchdog.
- sc_err_t sc_timer_pt_get_wdog_status (sc_ipc_t ipc, sc_rm_pt_t pt, sc_bool_t *enb, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *remaining_time)
  This function gets the status of the watchdog of a partition.
- sc_err_t sc_timer_set_wdog_action (sc_ipc_t ipc, sc_rm_pt_t pt, sc_timer_wdog_action_t action)
  This function configures the action to be taken when a watchdog expires.

Real-Time Clock (RTC) Functions

- sc_err_t sc_timer_set_rtc_time (sc_ipc_t ipc, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)
  This function sets the RTC time.
- sc_err_t sc_timer_get_rtc_time (sc_ipc_t ipc, uint16_t *year, uint8_t *mon, uint8_t *day, uint8_t *hour, uint8_t *min, uint8_t *sec)
  This function gets the RTC time.
- sc_err_t sc_timer_get_rtc_sec1970 (sc_ipc_t ipc, uint32_t *sec)
  This function gets the RTC time in seconds since 1/1/1970.
- sc_err_t sc_timer_set_rtc_alarm (sc_ipc_t ipc, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)
  This function sets the RTC alarm.
- sc_err_t sc_timer_set_rtc_periodic_alarm (sc_ipc_t ipc, uint32_t sec)
  This function sets the RTC alarm (periodic mode).
- sc_err_t sc_timer_cancel_rtc_alarm (sc_ipc_t ipc)
  This function cancels the RTC alarm.
- sc_err_t sc_timer_set_rtc_calb (sc_ipc_t ipc, int8_t count)
  This function sets the RTC calibration value.

System Counter (SYSCTR) Functions

- sc_err_t sc_timer_set_sysctr_alarm (sc_ipc_t ipc, uint64_t ticks)
  This function sets the SYSCTR alarm.
- sc_err_t sc_timer_set_sysctr_periodic_alarm (sc_ipc_t ipc, uint64_t ticks)
  This function sets the SYSCTR alarm (periodic mode).
- sc_err_t sc_timer_cancel_sysctr_alarm (sc_ipc_t ipc)
  This function cancels the SYSCTR alarm.

18.28.1 Detailed Description

Header file containing the public API for the System Controller (SC) Timer function.

18.29 platform/svc/misc/svc.h File Reference

Header file containing the API for the System Controller (SC) Miscellaneous (MISC) function.

Functions

Internal Functions

- void misc_init (sc_bool_t api_phase)
  Internal SC function to initializes the MISC service.
- sc_err_t misc_set_control (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t val)
  Internal SC function to set a miscellaneous control value.
- sc_err_t misc_get_control (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_ctrl_t ctrl, uint32_t *val)
  Internal SC function to get a miscellaneous control value.
- sc_err_t misc_set_ari (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rsrc_t resource_mst, uint16_t ari, sc_bool_t enable)
  Internal SC function to configure the ARI translation for PCIe/SATA resources.
- sc_err_t misc_set_max_dma_group (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_misc_dma_group_t max)
  Internal SC function to configure max DMA channel priority group for a partition.
- sc_err_t misc_set_dma_group (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_misc_dma_group_t group)
  Internal SC function to configure the priority group for a DMA channel.
- void misc_boot_status (sc_rm_pt_t caller_pt, sc_misc_boot_status_t status)
  Internal SC function to report boot status.
- sc_err_t misc_boot_done (sc_rm_pt_t caller_pt, sc_rsrc_t cpu)
  Internal SC function to report a CPU has finished initialization.
- sc_err_t misc_boot_done_wait (sc_rsrc_t cpu)
  Internal SC function to wait for a CPU to be done booting.
- sc_err_t misc_waveform_capture (sc_rm_pt_t caller_pt, sc_bool_t enable)
  Internal SC function to start/stop emulation waveform capture.
- void misc_debug_out (sc_rm_pt_t caller_pt, uint8_t ch)
  Internal SC function to output a debug charcter.
- sc_err_t misc_otp_fuse_read (sc_rm_pt_t caller_pt, uint32_t word, uint32_t *val)
  Internal SC function to read otp fuse word.
- sc_err_t misc_otp_fuse_write (sc_rm_pt_t caller_pt, uint32_t word, uint32_t val)
  Internal SC function to write otp fuse word.
- sc_bool_t misc_has_temp (sc_rsrc_t resource)
  This function reports if a resource has a temp sensor.
- sc_err_t misc_set_temp (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t celsius, int8_t tenths)
  Internal SC function to set a temp sensor alarm.
- sc_err_t misc_get_temp (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_misc_temp_t temp, int16_t *celsius, int8_t *tenths)
  Internal SC function to get a temp sensor value.
- void misc_build_info (sc_rm_pt_t caller_pt, uint32_t *build, uint32_t *commit)
  Internal SC function to return SCFW build info.
- void misc_unique_id (sc_rm_pt_t caller_pt, uint32_t *id_l, uint32_t *id_h)
  Internal SC function to return the device unique ID.
- void misc_get_boot_dev (sc_rm_pt_t caller_pt, sc_rsrc_t *dev)
  Internal SC function to return the boot device.
- sc_err_t misc_get_boot_type (sc_rm_pt_t caller_pt, sc_misc_bt_t *type)
  Internal SC function to return the boot type.
- sc_err_t misc_get_boot_container (sc_rm_pt_t caller_pt, uint8_t *idx)
  Internal SC function to return the boot container index.
- void misc_get_button_status (sc_rm_pt_t caller_pt, sc_bool_t *status)
  Internal SC function to return the current status of the ON/OFF button.
- sc_err_t misc_rompatch_checksum (sc_rm_pt_t caller_pt, uint32_t *checksum)
  Internal SC function to return the ROM patch checksum.
- sc_err_t misc_board_ioctl (sc_rsrc_t mu, uint32_t *parm1, uint32_t *parm2, uint32_t *parm3)
  Internal SC function to call board IOCTL.
- void misc_api_ver (sc_rm_pt_t caller_pt, uint16_t *cl_maj, uint16_t *cl_min, uint16_t *sv_maj, uint16_t *sv↩ _min)
  Internal SC function to return API version info.

18.29.1 Detailed Description

Header file containing the API for the System Controller (SC) Miscellaneous (MISC) function.

18.30 platform/svc/irq/svc.h File Reference

Header file containing the API for the System Controller (SC) Interrupt (IRQ) function.

Functions

- sc_err_t irq_enable (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_irq_group_t group, uint32_t mask, sc_bool_t enable)

  Internal SC function to enable/disable interrupts.
- sc_err_t irq_status (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_irq_group_t group, uint32_t *status)

  Internal SC function to get and clear interrupt status.

18.30.1 Detailed Description

Header file containing the API for the System Controller (SC) Interrupt (IRQ) function.

18.31 platform/svc/pad/svc.h File Reference

Header file containing the API for the System Controller (SC) Pad Control (PAD) function.

Functions

Internal Functions

- void pad_init (sc_bool_t api_phase)

  Internal SC function to initializes the PAD service.
- sc_err_t pad_set (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t val)

  Internal SC function to set the pad value.
- sc_err_t pad_set_mux (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso)

  Internal SC function to set the pad mux.
- void **pad_force_mux** (sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso)
- sc_err_t pad_set_gp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t ctrl)

  Internal SC function to set the pad control.
- sc_err_t pad_set_wakeup (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_wakeup_t wakeup)

  Internal SC function to set the pad wakeup control.
- sc_err_t pad_set_all (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t mux, sc_pad_config_t config, sc_pad_iso_t iso, uint32_t ctrl, sc_pad_wakeup_t wakeup)

  Internal SC function to configure a pad.
- sc_err_t pad_get (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t *val)

  Internal SC function to get the pad value.
- sc_err_t pad_get_mux (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso)

  Internal SC function to get the pad mux.
- sc_err_t pad_get_gp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t *ctrl)

Internal SC function to get the pad control.

- sc_err_t pad_get_wakeup (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_wakeup_t *wakeup)

  Internal SC function to get the pad wakeup control.
- sc_err_t pad_get_all (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t *mux, sc_pad_config_t *config, sc_pad_iso_t *iso, uint32_t *ctrl, sc_pad_wakeup_t *wakeup)

  Internal SC function to get a pad's configuration.
- sc_err_t pad_set_gp_28fdsoi (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_pad_28fdsoi_ps_t ps)

  Internal SC function to set the pad control specific to 28FDSOI.
- sc_err_t pad_get_gp_28fdsoi (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_pad_28fdsoi_ps_t *ps)

  Internal SC function to get the pad control specific to 28FDSOI.
- sc_err_t pad_set_gp_28fdsoi_hsic (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t dse, sc_bool_t hyp, sc_pad_28fdsoi_pus_t pus, sc_bool_t pke, sc_bool_t pue)

  Internal SC function to set the pad control specific to 28FDSOI.
- sc_err_t pad_get_gp_28fdsoi_hsic (sc_rm_pt_t caller_pt, sc_pad_t pad, sc_pad_28fdsoi_dse_t *dse, sc_bool_t *hyp, sc_pad_28fdsoi_pus_t *pus, sc_bool_t *pke, sc_bool_t *pue)

  Internal SC function to get the pad control specific to 28FDSOI.
- sc_err_t pad_set_gp_28fdsoi_comp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t compen, sc_bool_t fastfrz, uint8_t rasrcp, uint8_t rasrcn, sc_bool_t nasrc_sel, sc_bool_t psw_ovr)

  Internal SC function to set the pad compensation specific to 28FDSOI.
- sc_err_t pad_get_gp_28fdsoi_comp (sc_rm_pt_t caller_pt, sc_pad_t pad, uint8_t *compen, sc_bool_t *fastfrz, uint8_t *rasrcp, uint8_t *rasrcn, sc_bool_t *nasrc_sel, sc_bool_t *compok, uint8_t *nasrc, sc_bool_t *psw↩_ovr)

  Internal SC function to get the compensation control specific to 28FDSOI.
- sc_err_t pad_config (sc_rm_pt_t caller_pt, sc_pad_t pad, uint32_t val)

  Internal SC function to set a config value.
- sc_pad_t pad_map_irq (uint8_t irq, uint8_t idx)

  Internal function to map pad irq and index to pad resource.

18.31.1 Detailed Description

Header file containing the API for the System Controller (SC) Pad Control (PAD) function.

18.32 platform/svc/pm/svc.h File Reference

Header file containing the API for the System Controller (SC) Power Management (PM) function.

Functions

Internal Functions

- void **pm_set_booted** (sc_rm_pt_t pt, sc_bool_t booted)
- sc_bool_t **pm_get_booted** (sc_rm_pt_t pt)
- void pm_init (sc_bool_t api_phase)

  Internal SC function to initializes the PM service.
- void pm_init_part (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  This function initializes a new partition.
- sc_err_t pm_set_sys_power_mode (sc_rm_pt_t caller_pt, sc_pm_power_mode_t mode)

  Internal SC function to set the power mode of the system.
- sc_err_t pm_set_partition_power_mode (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t mode)

Internal SC function to set the power mode of a partition.

- sc_err_t pm_update_partition_power_mode (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t mode)

  Internal function to updates the power mode of a partition.
- sc_err_t pm_partition_wake (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)

  Internal SC function to send wake interrupt to a partition.
- sc_err_t pm_get_sys_power_mode (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t *mode)

  Internal SC function to get the power mode of a partition.
- void pm_update_ridx (sc_rm_idx_t idx)

  Internal SC function to update the power state of a resource.
- sc_bool_t pm_is_resource_accessible (sc_rsrc_t resource)

  Internal SC function to get the functional state of a resource.
- void pm_init_rsrc_power_mode (sc_rsrc_t rsrc, sc_pm_power_mode_t mode)

  Internal SC function to init the power mode of a resource just after ROM boot.
- sc_err_t pm_set_resource_power_mode (sc_rsrc_t mu, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to set the power mode of a resource.
- sc_err_t pm_set_resource_power_mode_all (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_power_mode_t mode, sc_rsrc_t exclude)

  Internal SC function to set power mode for all resources in a child partition.
- void pm_set_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t mode)

  This function sets the power mode of a resource index.
- void pm_update_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t mode)

  This function updates the power mode of a resource index.
- sc_err_t pm_force_resource_power_mode (sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to force the power mode of a resource.
- void pm_force_resource_power_mode_v (sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to force the power mode of a resource.
- sc_err_t pm_get_resource_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_power_mode_t *mode)

  Internal SC function to get the power mode of a resource.
- void pm_get_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t *mode)

  This function gets the power mode of a resource index.
- void pm_get_active_rsrc_power_mode (sc_rm_idx_t idx, sc_pm_power_mode_t *mode)

  This function gets the active power mode of a resource index.
- sc_err_t pm_req_low_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_power_mode_t mode)

  Internal SC function to request the power mode a resource can enter in some low power conditions.
- sc_err_t pm_req_cpu_low_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_power_mode_t mode, sc_pm_wake_src_t wake_src)

  Internal SC function to request low-power mode for a CPU.
- sc_err_t pm_set_cpu_resume_addr (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_faddr_t address)

  Internal SC function to set the resume address of a CPU.
- sc_err_t pm_set_cpu_resume (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_bool_t isPrimary, sc_faddr_t address)

  Internal SC function to set the resume parameters of a CPU.
- sc_err_t pm_req_sys_if_power_mode (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_sys_if_t sys_if, sc_pm_power_mode_t hpm, sc_pm_power_mode_t lpm)

  Internal SC function to request power mode for system-level interfaces.
- sc_err_t pm_set_clock_rate (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  Internal SC function to set the rate of a resource's clock/PLL.
- sc_err_t pm_get_clock_rate (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clock_rate_t *rate)

  Internal SC function to get the rate of a resource's clock/PLL.
- sc_err_t pm_clock_enable (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_bool_t enable, sc_bool_t autog)

Internal SC function to enable/disable a resource's clock.

- void pm_force_clock_enable (sc_rsrc_t resource, sc_pm_clk_t clk, sc_bool_t enable)
  Internal SC function to force a resource's clock to be enabled.
- sc_err_t pm_set_clock_parent (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t parent)
  Internal SC function to set a clock parent.
- sc_err_t pm_get_clock_parent (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_pm_clk_t clk, sc_pm_clk_parent_t *parent)
  Internal SC function to get a clock parent.
- sc_err_t pm_boot (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)
  Internal SC function to boot a partition.
- sc_err_t pm_set_boot_parm (sc_rm_pt_t caller_pt, sc_rsrc_t resource_cpu, sc_faddr_t boot_addr, sc_rsrc_t resource_mu, sc_rsrc_t resource_dev)
  Internal SC function to set a partition's boot parameters.
- void pm_reboot (sc_rm_pt_t caller_pt, sc_pm_reset_type_t type)
  Internal SC function to reboot the caller's partition.
- sc_err_t pm_reset_reason (sc_rm_pt_t caller_pt, sc_pm_reset_reason_t *reason)
  Internal SC function to get the reset reason.
- sc_err_t pm_get_reset_part (sc_rm_pt_t caller_pt, sc_rm_pt_t *pt)
  Internal SC function to get the partition that caused a reset.
- sc_err_t pm_cpu_start (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_bool_t enable, sc_faddr_t address)
  Internal SC function to start/stop a CPU.
- void pm_cpu_reset (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_faddr_t address)
  Internal SC function to reset a CPU.
- sc_err_t pm_resource_reset (sc_rsrc_t mu, sc_rsrc_t resource)
  Internal SC function to reset a resource.
- sc_err_t pm_reboot_partition (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_reset_type_t type)
  Internal SC function to reboot a partition.
- sc_err_t pm_reboot_continue (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)
  Internal SC function to conntinue reboot.
- void pm_reboot_continue_all (void)
  Internal SC function to force the conntinue of all reboots.
- sc_err_t pm_reset (sc_rm_pt_t caller_pt, sc_pm_reset_type_t type)
  Internal SC function to reset the system.
- sc_err_t pm_reboot_part (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pm_reset_type_t type, sc_pm_reset_reason_t reason, sc_pm_power_mode_t mode)
  Internal SC function used to reboot a partition.
- sc_bool_t pm_is_partition_started (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)
  Internal SC function to get boolean indicating that a partition was started.

18.32.1 Detailed Description

Header file containing the API for the System Controller (SC) Power Management (PM) function.

This includes functions for power state control, clock control, reset control, and wake-up event control.

18.33 platform/svc/seco/svc.h File Reference

Header file containing the API for the System Controller (SC) Security (SECO) function.

Functions

- sc_err_t seco_get_mp_key (sc_rm_pt_t caller_pt, sc_faddr_t dst_addr, uint16_t dst_size)

Internal SC function to get manufacturing protection public key.

- sc_err_t seco_update_mpmr (sc_rm_pt_t caller_pt, sc_faddr_t addr, uint8_t size, uint8_t lock)

  Internal SC function to update manufacturing protection message register.
- sc_err_t seco_get_mp_sign (sc_rm_pt_t caller_pt, sc_faddr_t msg_addr, uint16_t msg_size, sc_faddr_t dst_addr, uint16_t dst_size)

  Internal SC function to get manufacturing protection signature.
- sc_err_t seco_sab_msg (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to send a generic signed message to the SECO SHE/HSM components.
- sc_err_t seco_secvio_enable (sc_rm_pt_t caller_pt)

  Internal SC function to enable the security violation interrupt.
- sc_err_t seco_secvio_config (sc_rm_pt_t caller_pt, uint8_t id, uint8_t access, uint32_t *data0, uint32_t *data1, uint32_t *data2, uint32_t *data3, uint32_t *data4, uint8_t size)

  Internal SC function to read/write SNVS security violation and tamper registers.
- sc_err_t seco_secvio_dgo_config (sc_rm_pt_t caller_pt, uint8_t id, uint8_t access, uint32_t *data)

  Internal SC function to read/write SNVS security violation and tamper DGO registers.

Internal Functions

- sc_err_t seco_image_load (sc_rm_pt_t caller_pt, sc_faddr_t addr_src, sc_faddr_t addr_dst, uint32_t len, sc_bool_t fw)

  Internal SC function to load a SECO image.
- sc_err_t seco_authenticate (sc_rm_pt_t caller_pt, sc_seco_auth_cmd_t cmd, sc_faddr_t addr)

  Internal SC function to authenticate a SECO image or command.
- sc_err_t seco_enh_authenticate (sc_rm_pt_t caller_pt, sc_seco_auth_cmd_t cmd, sc_faddr_t addr, uint32_t mask1, uint32_t mask2)

  Internal SC function to authenticate a SECO image or command ((enhanced version).
- sc_err_t seco_load_key (sc_rm_pt_t caller_pt, uint32_t id, sc_faddr_t addr)

  Internal SC function to load a SECO key.
- sc_err_t seco_gen_key_blob (sc_rm_pt_t caller_pt, uint32_t id, sc_faddr_t load_addr, sc_faddr_t export_addr, uint16_t max_size)

  Internal SC function to generate a key blob.
- sc_err_t seco_fuse_write (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to securely write a group of fuse words.
- sc_err_t seco_patch (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to apply a patch.
- sc_err_t seco_set_mono_counter_partition (sc_rm_pt_t caller_pt, uint16_t *she)

  Internal SC function to partition the monotonic counter.
- sc_err_t seco_set_fips_mode (sc_rm_pt_t caller_pt, uint8_t mode, uint32_t *reason)

  Internal SC function to set FIPS mode.
- sc_err_t seco_start_rng (sc_rm_pt_t caller_pt, sc_seco_rng_stat_t *status)

  Internal SC function to start the RNG.
- sc_err_t seco_enable_debug (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to securely enable debug.
- sc_err_t seco_forward_lifecycle (sc_rm_pt_t caller_pt, uint32_t change)

  Internal SC function to update the lifecycle.
- sc_err_t seco_return_lifecycle (sc_rm_pt_t caller_pt, sc_faddr_t addr)

  Internal SC function to securely reverse the lifecycle.
- void seco_build_info (sc_rm_pt_t caller_pt, uint32_t *version, uint32_t *commit)

  Internal SC function to return SECO FW version info.
- sc_err_t seco_chip_info (sc_rm_pt_t caller_pt, uint16_t *lc, uint16_t *monotonic, uint32_t *uid_l, uint32_t *uid_h)

  Internal SC function to return SECO chip info.

- sc_err_t seco_get_event (sc_rm_pt_t caller_pt, uint8_t idx, uint32_t *event)
  Internal SC function to return an event from the SECO error log.
- sc_err_t seco_attest_mode (sc_rm_pt_t caller_pt, uint32_t mode)
  Internal SC function to set the attestation mode.
- sc_err_t seco_attest (sc_rm_pt_t caller_pt, uint64_t nonce)
  Internal SC function to request atestation.
- sc_err_t seco_get_attest_pkey (sc_rm_pt_t caller_pt, sc_faddr_t addr)
  Internal SC function to retrieve attestation public key.
- sc_err_t seco_get_attest_sign (sc_rm_pt_t caller_pt, sc_faddr_t addr)
  Internal SC function to retrieve attestation signature and parameters.
- sc_err_t seco_attest_verify (sc_rm_pt_t caller_pt, sc_faddr_t addr)
  Internal SC function to verify attestation.
- sc_err_t seco_commit (sc_rm_pt_t caller_pt, uint32_t *info)
  Internal SC function to commit SRK/FW changes.

18.33.1 Detailed Description

Header file containing the API for the System Controller (SC) Security (SECO) function.

18.34 platform/svc/rm/svc.h File Reference

Header file containing the API for the System Controller (SC) Resource Management (RM) function.

Macros

- #define SC_SS_IDX_W 8U
  Width of SS index.
- #define SC_PT_ALL SC_RM_NUM_PARTITION
  Define used to indicate function should apply to all partitions.

Typedefs

- typedef uint8_t sc_ss_idx_t
  Type for a ss resource index.

Functions

Internal Functions

- void rm_init (sc_bool_t api_phase)
  Internal SC function to initialize the RM service.
- sc_err_t rm_reserve_static_pt (sc_rm_pt_t num)
  Internal SC function to specify the number of static partitions.
- sc_err_t rm_reserve_static_did (sc_rm_did_t num)
  Internal SC function to specify the number of static domains.
- sc_err_t rm_partition_alloc (sc_rm_pt_t caller_pt, sc_rm_pt_t *pt, sc_bool_t secure, sc_bool_t isolated, sc_bool_t restricted, sc_bool_t grant, sc_bool_t coherent)
  Internal SC function to request that the SC create a new resource partition.

- sc_err_t rm_set_confidential (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_bool_t retro)
  Internal SC function to make a partition confidential.
- sc_err_t rm_partition_free (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)
  Internal SC function to free a partition and assigns all resources to the caller.
- sc_err_t rm_get_partition (sc_rm_pt_t caller_pt, sc_rm_pt_t *pt)
  Internal SC function to get the partition handle of the caller.
- sc_bool_t rm_is_partition_used (sc_rm_pt_t pt)
  Internal SC function to determine if a partition is enabled (used) or not.
- sc_bool_t rm_is_secure_partition (sc_rm_pt_t caller_pt)
  Internal SC function to get the security state of partition.
- sc_bool_t rm_is_partition_isolated (sc_rm_pt_t pt)
  Internal SC function to get the isolation state of partition.
- sc_bool_t rm_is_sys_access (sc_rm_pt_t pt)
  Internal SC function to return if the partition has system access.
- sc_rm_pt_t rm_get_partition_parent (sc_rm_pt_t pt)
  Internal SC function to return the parent of a partition.
- sc_rm_did_t rm_get_did (sc_rm_pt_t caller_pt)
  Internal SC function to get the DID of the caller's partition.
- sc_err_t rm_partition_static (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rm_did_t did)
  Internal SC function to force a partition to use a specific static DID.
- sc_err_t rm_partition_lock (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)
  Internal SC function to lock a partition.
- sc_err_t rm_set_parent (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rm_pt_t pt_parent)
  Internal SC function to set a new parent for a partition.
- sc_bool_t rm_is_parent (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)
  Internal SC function to check if caller is the parent of a partition.
- sc_bool_t rm_check_ancestor (sc_rm_pt_t caller_pt, sc_rm_pt_t pt_owner)
  Internal SC function to check if caller is an ancestor of owner.
- sc_err_t rm_move_all (sc_rm_pt_t caller_pt, sc_rm_pt_t pt_src, sc_rm_pt_t pt_dst, sc_bool_t move_rsrc, sc_bool_t move_pads)
  Internal SC function to move all resources/pads owned by a source partition to a destination partition.
- sc_err_t rm_assign_resource (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rsrc_t resource)
  Internal SC function to assign ownership of a resource to a partition.
- sc_err_t rm_set_resource_movable (sc_rm_pt_t caller_pt, sc_rsrc_t resource_fst, sc_rsrc_t resource_lst, sc_bool_t movable)
  Internal SC function to flag resource as movable or not.
- sc_err_t rm_set_subsys_rsrc_movable (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_bool_t movable)
  Internal SC function to flag all of a subsystem's resources as movable or not.
- sc_err_t rm_set_master_attributes (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_spa_t sa, sc_rm_spa_t pa, sc_bool_t smmu_bypass)
  Internal SC function to set attributes for a resource which is a bus master (i.e.
- sc_err_t rm_set_master_sid (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_sid_t sid)
  Internal SC function to set the StreamID for a resource which is a bus master (i.e.
- sc_err_t rm_update_master (sc_rm_idx_t idx)
  Internal SC function to update a master resource.
- sc_err_t rm_set_peripheral_permissions (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_pt_t pt, sc_rm_perm_t perm)
  Internal SC function to set access permissions for a peripheral resource.
- sc_err_t rm_update_peripheral (sc_rm_idx_t idx)
  Internal SC function to update a peripheral resource.
- void rm_update_resource (sc_rsrc_t resource)
  Internal SC function to update a resource in HW.
- void rm_get_ridx_ss_info (sc_rm_idx_t idx, sc_sub_t *ss, sc_ss_idx_t *ss_idx)
  Internal SC function to return subsystem specific info about a resource.
- sc_bool_t rm_check_map_ridx (sc_rsrc_t resource, sc_rm_idx_t *idx)

Internal SC function to check the validity of a resource and return the unified resource index.

- void rm_check_map_ridx_v (sc_rsrc_t resource, sc_rm_idx_t *idx)

  Internal SC function to check the validity of a resource and return the unified resource index.
- sc_bool_t rm_is_resource_owned (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function to get ownership status of a resource.
- sc_bool_t rm_is_ridx_owned (sc_rm_pt_t caller_pt, sc_rm_idx_t idx)

  Internal SC function to check if a resource is owned by the caller.
- sc_bool_t rm_is_resource_avail (sc_rsrc_t resource)

  Internal SC function to check if a resource is available.
- sc_bool_t rm_is_ridx_avail (sc_rm_idx_t idx)

  Internal SC function to check if a resource is available.
- sc_bool_t rm_is_resource_access_allowed (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function to get access rights of a resource.
- sc_bool_t rm_is_ridx_access_allowed (sc_rm_pt_t caller_pt, sc_rm_idx_t idx)

  Internal SC function to check if a resource is controllable by the caller.
- sc_err_t rm_get_resource_owner (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_pt_t *pt)

  Internal SC function to return the owner partition for a resource.
- void rm_get_ridx_owner (sc_rm_idx_t idx, sc_rm_pt_t *pt)

  Internal SC function to return the ownering partition for a resource.
- sc_bool_t rm_is_resource_master (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function used to test if a resource is a bus master.
- sc_bool_t rm_is_ridx_master (sc_rm_idx_t idx)

  Internal SC function to check if a resource is a master.
- sc_bool_t rm_is_resource_peripheral (sc_rm_pt_t caller_pt, sc_rsrc_t resource)

  Internal SC function used to test if a resource is a peripheral.
- sc_bool_t rm_is_ridx_peripheral (sc_rm_idx_t idx)

  Internal SC function to check if a resource is a peripheral.
- sc_err_t rm_get_resource_info (sc_rm_pt_t caller_pt, sc_rsrc_t resource, sc_rm_sid_t *sid)

  Internal SC function used to obtain info about a resource.
- sc_bool_t rm_ridx_block (sc_rm_idx_t idx, sc_bool_t block)

  Internal SC function to control if a access to a resource should be blocked via HW.
- sc_err_t rm_memreg_alloc (sc_rm_pt_t caller_pt, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_↩ end)

  Internal SC function to request that the SC create a new memory region.
- sc_err_t rm_memreg_split (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)

  Internal SC function to split a memory region.
- sc_err_t rm_memreg_frag (sc_rm_pt_t caller_pt, sc_rm_mr_t *mr_ret, sc_faddr_t addr_start, sc_faddr_t addr_end)

  Internal SC function to fragment a memory region.
- sc_err_t rm_memreg_free (sc_rm_pt_t caller_pt, sc_rm_mr_t mr)

  Internal SC function to free a memory region.
- sc_err_t rm_find_memreg (sc_rm_pt_t caller_pt, sc_rm_mr_t *mr, sc_faddr_t addr_start, sc_faddr_t addr_↩ end)

  Internal SC function to find a memory region.
- sc_err_t rm_assign_memreg (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_rm_mr_t mr)

  Internal SC function to assign ownership of a memory region.
- sc_err_t rm_set_memreg_permissions (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_rm_pt_t pt, sc_rm_perm_t perm)

  Internal SC function to set access permissions for a memory region.
- sc_err_t rm_set_memreg_iee (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_rm_det_t det, sc_rm_rmsg_t rmsg)

  Internal SC function to set configure IEE parameters for a mem region.
- sc_bool_t rm_is_memreg_owned (sc_rm_pt_t caller_pt, sc_rm_mr_t mr)

  Internal SC function to get ownership status of a memory region.

- sc_err_t rm_get_memreg_info (sc_rm_pt_t caller_pt, sc_rm_mr_t mr, sc_faddr_t *addr_start, sc_faddr_t *addr_end)
  Internal SC function used to obtain info about a memory region.
- sc_err_t rm_assign_pad (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_pad_t pad)
  Internal SC function to assign ownership of a pad to a partition.
- sc_err_t rm_set_pad_movable (sc_rm_pt_t caller_pt, sc_pad_t pad_first, sc_pad_t pad_last, sc_bool_t movable)
  Internal SC function to flag pad as movable or not.
- sc_bool_t rm_is_pad_owned (sc_rm_pt_t caller_pt, sc_pad_t pad)
  Internal SC function to get ownership status of a pad.
- sc_err_t rm_get_pad_owner (sc_pad_t pad, sc_rm_pt_t *pt)
  Internal SC function to get the owner of a pad.
- void rm_enable_blocking (void)
  Enable blocking of resources powered off.
- sc_err_t rm_init_subsys (sc_sub_t ss, sc_bool_t block_enb)
  Internal SC function to reload a subsystem's XRDC info after a power on.
- void rm_dump (sc_rm_pt_t caller_pt)
  Internal SC function to dump RM state for debug.

Debug Functions

- void rm_dump_partition (sc_rm_pt_t pt)
  Internal SC function to dump the internal partition state of the RM service.
- void rm_dump_resources (sc_rm_pt_t pt)
  Internal SC function to dump the internal resource state of the RM service.
- void rm_dump_memregs (sc_rm_pt_t pt)
  Internal SC function to dump the internal memory state of the RM service.
- void rm_dump_pads (sc_rm_pt_t pt)
  Internal SC function to dump the internal pad state of the RM service.

Variables

- uint8_t rm_max_did
  Max domain used.

18.34.1 Detailed Description

Header file containing the API for the System Controller (SC) Resource Management (RM) function.

This includes functions for partitioning resources, pads, and memory regions.

18.35 platform/svc/timer/svc.h File Reference

Header file containing the API for the System Controller (SC) Timer function.

Functions

Internal Functions

- void timer_init (sc_bool_t api_phase)
  Internal SC function to initializes the TIMER service.
- void timer_init_part (sc_rm_pt_t caller_pt, sc_rm_pt_t pt)
  This function initializes a new partition.
- sc_err_t timer_set_wdog_timeout (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t timeout)
  Internal SC function to set the watchdog timeout in milliseconds.
- sc_err_t timer_set_wdog_pre_timeout (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t pre_timeout)
  Internal SC function to set the watchdog pre-timeout in milliseconds.
- sc_err_t timer_set_wdog_window (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t window)
  Internal SC function to set the watchdog window in milliseconds.
- sc_err_t timer_start_wdog (sc_rm_pt_t caller_pt, sc_bool_t lock)
  Internal SC function to start the watchdog.
- sc_err_t timer_stop_wdog (sc_rm_pt_t caller_pt)
  Internal SC function to stop the watchdog (if not locked).
- void timer_halt_wdog (sc_rm_pt_t pt)
  Internal SC function to stop halt the wdog when the partition is deleted.
- sc_err_t timer_ping_wdog (sc_rm_pt_t caller_pt)
  Internal SC function to ping (services, kicks) the watchdog resetting the time before expiration back to the timeout.
- sc_err_t timer_get_wdog_status (sc_rm_pt_t caller_pt, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *max_timeout, sc_timer_wdog_time_t *remaining_time)
  Internal SC function to get the status of the watchdog.
- sc_err_t timer_pt_get_wdog_status (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_bool_t *enb, sc_timer_wdog_time_t *timeout, sc_timer_wdog_time_t *remaining_time)
  Internal SC function to get the status of the watchdog of a partition.
- sc_err_t timer_set_wdog_action (sc_rm_pt_t caller_pt, sc_rm_pt_t pt, sc_timer_wdog_action_t action)
  Internal SC function to configure the action to be taken when a watchdog expires.
- sc_err_t timer_take_wdog_action (sc_rm_pt_t pt)
  Internal SC function to take the wdog action specified.
- sc_err_t timer_set_rtc_time (sc_rm_pt_t caller_pt, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)
  Internal SC function to set the RTC time.
- sc_err_t timer_get_rtc_time (sc_rm_pt_t caller_pt, uint16_t *year, uint8_t *mon, uint8_t *day, uint8_t *hour, uint8_t *min, uint8_t *sec)
  Internal SC function to get the RTC time.
- sc_err_t timer_set_rtc_alarm (sc_rm_pt_t caller_pt, uint16_t year, uint8_t mon, uint8_t day, uint8_t hour, uint8_t min, uint8_t sec)
  Internal SC function to set the RTC alarm.
- sc_err_t timer_set_rtc_periodic_alarm (sc_rm_pt_t caller_pt, uint32_t sec)
  Internal SC function to set a periodic RTC alarm.
- sc_err_t timer_cancel_rtc_alarm (sc_rm_pt_t caller_pt)
  Internal SC function to cancel an RTC alarm.
- void timer_query_rtc_alarm (sc_rm_pt_t pt, uint32_t *alarm, uint32_t *period)
  Internal SC function to query an RTC alarm.
- void timer_restore_rtc_alarm (sc_rm_pt_t pt, uint32_t alarm, uint32_t period)
  Internal SC function to restore an RTC alarm.
- sc_err_t timer_get_rtc_sec1970 (sc_rm_pt_t caller_pt, uint32_t *sec)
  Internal SC function to get the RTC time in seconds since 1/1/1970.
- sc_err_t timer_set_rtc_calb (sc_rm_pt_t caller_pt, int8_t count)
  Internal SC function to set the RTC calibration.
- void timer_tick (uint16_t msec)
  Internal SC function to increment the RTC.
- sc_err_t timer_set_sysctr_alarm (sc_rm_pt_t caller_pt, uint64_t ticks)
  Internal SC function to set the sysctr alarm.
- sc_err_t timer_set_sysctr_periodic_alarm (sc_rm_pt_t caller_pt, uint64_t ticks)
  Internal SC function to set the periodic sysctr alarm.
- sc_err_t timer_cancel_sysctr_alarm (sc_rm_pt_t caller_pt)
  Internal SC function to cancel the sysctr alarm.

18.35.1 Detailed Description

Header file containing the API for the System Controller (SC) Timer function.

Chapter 19

Example Documentation

19.1 board.c

This is an example implementation for the i.MX8QM MEK board.

```
/*
** ###################################################################
**
**     Copyright (c) 2016 Freescale Semiconductor, Inc.
**     Copyright 2017-2020 NXP
**
**     Redistribution and use in source and binary forms, with or without modification,
**     are permitted provided that the following conditions are met:
**
**     o Redistributions of source code must retain the above copyright notice, this list
**       of conditions and the following disclaimer.
**
**     o Redistributions in binary form must reproduce the above copyright notice, this
**       list of conditions and the following disclaimer in the documentation and/or
**       other materials provided with the distribution.
**
**     o Neither the name of the copyright holder nor the names of its
**       contributors may be used to endorse or promote products derived from this
**       software without specific prior written permission.
**
**     THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND
**     ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED
**     WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE
**     DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE FOR
**     ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES
**     (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES;
**     LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON
**     ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
**     (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS
**     SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
**
**
** ###################################################################
*/
/*!=========================================================================*/
/*!
 * @file
 *
 * File containing the implementation of the MX8QM MEK board.
 *
 * @addtogroup MX8QM_MEK_BRD BRD: MX8QM MEK Board
 *
 * Module for MX8QM MEK board access.
 *
 * @{
 */
/*!=========================================================================*/
/* Includes */
```

```
#include "main/build_info.h"
#include "main/scfw.h"
#include "main/main.h"
#include "main/board.h"
#include "main/boot.h"
#include "main/soc.h"
#include "board/pmic.h"
#include "all_svc.h"
#include "drivers/lpi2c/fsl_lpi2c.h"
#include "drivers/pmic/fsl_pmic.h"
#include "drivers/pmic/pf8100/fsl_pf8100.h"
#include "drivers/rgpio/fsl_rgpio.h"
#include "drivers/snvs/fsl_snvs.h"
#include "drivers/wdog32/fsl_wdog32.h"
#include "drivers/lpuart/fsl_lpuart.h"
#include "drivers/drc/fsl_drc_cbt.h"
#include "drivers/drc/fsl_drc_derate.h"
#include "drivers/drc/fsl_drc_rdbi_deskew.h"
#include "drivers/drc/fsl_drc_dram_vref.h"
#include "drivers/systick/fsl_systick.h"
#include "pads.h"
#include "drivers/pad/fsl_pad.h"
#include "dcd/dcd_retention.h"
/* Local Defines */

/*!
 * @name Board Configuration
 * DO NOT CHANGE - must match object code.
 */
/*@{*/
#define BRD_NUM_RSRC            11U
#define BRD_NUM_CTRL            6U
/*@}*/

/*!
 * @name Board Resources
 * DO NOT CHANGE - must match object code.
 */
/*@{*/
#define BRD_R_BOARD_PMIC_0      0U
#define BRD_R_BOARD_PMIC_1      1U
#define BRD_R_BOARD_PMIC_2      2U
#define BRD_R_BOARD_R0          3U
#define BRD_R_BOARD_R1          4U
#define BRD_R_BOARD_R2          5U      /*! EMVSIM */
#define BRD_R_BOARD_R3          6U      /*!< USDHC2 on Base board */
#define BRD_R_BOARD_R4          7U
#define BRD_R_BOARD_R5          8U
#define BRD_R_BOARD_R6          9U
#define BRD_R_BOARD_R7          10U     /*!< Test */
/*@}*/
#if DEBUG_UART == 3
    /*! Use debugger terminal emulation */
    #define DEBUG_TERM_EMUL
#endif
#if DEBUG_UART == 2
    /*! Use alternate debug UART */
    #define ALT_DEBUG_SCU_UART
#endif
#if (defined(MONITOR) || defined(EXPORT_MONITOR) || defined(HAS_TEST) \
        || (DEBUG_UART == 1)) && !defined(DEBUG_TERM_EMUL) \
        && !defined(ALT_DEBUG_SCU_UART)
    #define ALT_DEBUG_UART
#endif

/*! Configure debug UART */
#ifdef ALT_DEBUG_SCU_UART
    #define LPUART_DEBUG        LPUART_SC
#else
    #define LPUART_DEBUG        LPUART_M4_0
#endif

/*! Configure debug UART instance */
#ifdef ALT_DEBUG_SCU_UART
    #define LPUART_DEBUG_INST   0U
#else
    #define LPUART_DEBUG_INST   2U
#endif
#ifdef EMUL
    /*! Configure debug baud rate */
    #define DEBUG_BAUD          4000000U
```

```
#else
    /*! Configure debug baud rate */
    #define DEBUG_BAUD          115200U
#endif
/* Local Types */
/* Local Functions */
static void pmic_init(void);
static sc_err_t pmic_ignore_current_limit(uint8_t address);
static sc_err_t pmic_update_timing(uint8_t address);
static sc_err_t pmic_match_otp(uint8_t address, pmic_version_t ver);
static void board_get_pmic_info(sc_sub_t ss,pmic_id_t *pmic_id,
    uint32_t *pmic_reg, uint8_t *num_regs);
/* Local Variables */
static pmic_version_t pmic_ver;
static uint32_t temp_alarm0;
static uint32_t temp_alarm1;

/*!
 * This constant contains info to map resources to the board.
 * DO NOT CHANGE - must match object code.
 */
const sc_rsrc_map_t board_rsrc_map[BRD_NUM_RSRC_BRD] =
{
    RSRC(PMIC_0,   0,  0),
    RSRC(PMIC_1,   0,  1),
    RSRC(PMIC_2,   0,  2),
    RSRC(BOARD_R0, 0,  3),
    RSRC(BOARD_R1, 0,  4),
    RSRC(BOARD_R2, 0,  5),
    RSRC(BOARD_R3, 0,  6),
    RSRC(BOARD_R4, 0,  7),
    RSRC(BOARD_R5, 0,  8),
    RSRC(BOARD_R6, 0,  9),
    RSRC(BOARD_R7, 0, 10)
};
/* Block of comments that get processed for documentation
   DO NOT CHANGE - must match object code. */
#ifdef DOX
    RNFO() /* PMIC 0 */
    RNFO() /* PMIC 1 */
    RNFO() /* PMIC 2 */
    RNFO() /* Misc. board component 0 */
    RNFO() /* Misc. board component 1 */
    RNFO() /* Misc. board component 2 */
    RNFO() /* Misc. board component 3 */
    RNFO() /* Misc. board component 4 */
    RNFO() /* Misc. board component 5 */
    RNFO() /* Misc. board component 6 */
    RNFO() /* Misc. board component 7 */
    TNFO(PMIC_0, TEMP,     RO, x, 8) /* Temperature sensor temp */
    TNFO(PMIC_0, TEMP_HI,  RW, x, 8) /* Temperature sensor high limit alarm temp */
    TNFO(PMIC_1, TEMP,     RO, x, 8) /* Temperature sensor temp */
    TNFO(PMIC_1, TEMP_HI,  RW, x, 8) /* Temperature sensor high limit alarm temp */
    TNFO(PMIC_2, TEMP,     RO, x, 8) /* Temperature sensor temp */
    TNFO(PMIC_2, TEMP_HI,  RW, x, 8) /* Temperature sensor high limit alarm temp */
#endif
/* External Variables */
const sc_rm_idx_t board_num_rsrc = BRD_NUM_RSRC_BRD;

/*!
 * External variable for specing DDR periodic training.
 */
#ifdef BD_LPDDR4_INC_DQS2DQ
const uint32_t board_ddr_period_ms = 3000U;
#else
const uint32_t board_ddr_period_ms = 0U;
#endif
const uint32_t board_ddr_derate_period_ms = 1000U;
/*------------------------------------------------------------------------*/
/* Init                                                                   */
/*------------------------------------------------------------------------*/
void board_init(boot_phase_t phase)
{
    rgpio_pin_config_t config;
    config.pinDirection = kRGPIO_DigitalOutput;
    ss_print(3, "board_init(%d)\n", phase);
    if (phase == BOOT_PHASE_HW_INIT)
    {
        #ifndef ALT_DEBUG_SCU_UART
            pad_force_mux(SC_P_SCU_GPIO0_01, 0,
                SC_PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF);
```

```
        #endif
        pad_force_mux(SC_P_SCU_GPIO0_02, 0, SC_PAD_CONFIG_NORMAL,
            SC_PAD_ISO_OFF);
        /* Toggle base board reset SC_GPIO_01, >= 30nS */
        config.outputLogic  = 0U;
        FGPIO_PinInit(FGPIOA, 1U, &config);
        SYSTICK_CycleDelay(SC_SYSTICK_NSEC_TO_TICKS(30U) + 1U);
        FGPIO_PinWrite(FGPIOA, 1U, 1U);
        /* SCU_LED on SC_GPIO_02 */
        config.outputLogic  = 1U;
        FGPIO_PinInit(FGPIOA, 2U, &config);
        SystemTimeDelay(2U);
    }
    else if (phase == BOOT_PHASE_FINAL_INIT)
    {
        /* Configure SNVS button for rising edge */
        SNVS_ConfigButton(SNVS_DRV_BTN_CONFIG_RISINGEDGE, SC_TRUE);
        /* Init PMIC if not already done */
        pmic_init();
    }
    else if (phase == BOOT_PHASE_TEST_INIT)
    {
        /* Configure board for SCFW tests - only called in a unit test
         * image. Called just before SC tests are run.
         */
        /* Configure ADMA UART pads. Needed for test_dma.
         *  NOTE:  Even though UART is ALT0, the TX output will not work
         *         until the pad mux is configured.
         */
        PAD_SetMux(IOMUXD__UART0_TX, 0U, SC_PAD_CONFIG_NORMAL,
            SC_PAD_ISO_OFF);
        PAD_SetMux(IOMUXD__UART0_RX, 0U, SC_PAD_CONFIG_NORMAL,
            SC_PAD_ISO_OFF);
    }
    else
    {
        ; /* Intentional empty else */
    }
}
/*------------------------------------------------------------------------*/
/* Return the debug UART info                                             */
/*------------------------------------------------------------------------*/
LPUART_Type *board_get_debug_uart(uint8_t *inst, uint32_t *baud)
{
    #if (defined(ALT_DEBUG_UART) || defined(ALT_DEBUG_SCU_UART)) \
            && !defined(DEBUG_TERM_EMUL)
        *inst = LPUART_DEBUG_INST;
        *baud = DEBUG_BAUD;
        return LPUART_DEBUG;
    #else
        return NULL;
    #endif
}
/*------------------------------------------------------------------------*/
/* Configure debug UART                                                   */
/*------------------------------------------------------------------------*/
void board_config_debug_uart(sc_bool_t early_phase)
{
    #if defined(ALT_DEBUG_SCU_UART) && !defined(DEBUG_TERM_EMUL) \
            && defined(DEBUG) && !defined(SIMU)
        /* Power up UART */
        pm_force_resource_power_mode_v(SC_R_SC_UART,
            SC_PM_PW_MODE_ON);
        /* Check if debug disabled */
        if (SCFW_DBG_READY == 0U)
        {
            main_config_debug_uart(LPUART_DEBUG, SC_24MHZ);
        }
    #elif defined(ALT_DEBUG_UART) && defined(DEBUG) && !defined(SIMU)
        /* Use M4 UART if ALT_DEBUG_UART defined */
        /* Return if debug already enabled */
        if ((SCFW_DBG_READY == 0U) && (early_phase == SC_FALSE))
        {
            sc_pm_clock_rate_t rate = SC_24MHZ;
            static sc_bool_t banner = SC_FALSE;
            /* Configure pads */
            pad_force_mux(SC_P_M40_I2C0_SDA, 1,
                SC_PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF);
            pad_force_mux(SC_P_M40_I2C0_SCL, 1,
                SC_PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF);
            /* Power and enable clock */
```

```
            pm_force_resource_power_mode_v(SC_R_SC_PID0,
                SC_PM_PW_MODE_ON);
            pm_force_resource_power_mode_v(SC_R_DBLOGIC,
                SC_PM_PW_MODE_ON);
            pm_force_resource_power_mode_v(SC_R_DB, SC_PM_PW_MODE_ON);
            pm_force_resource_power_mode_v(SC_R_M4_0_UART,
                SC_PM_PW_MODE_ON);
            (void) pm_set_clock_rate(SC_PT, SC_R_M4_0_UART, SC_PM_CLK_PER,
                &rate);
            (void) pm_clock_enable(SC_PT, SC_R_M4_0_UART, SC_PM_CLK_PER,
                SC_TRUE, SC_FALSE);
            /* Configure UART */
            main_config_debug_uart(LPUART_DEBUG, rate);
            if (banner == SC_FALSE)
            {
                debug_print(1,
                    "\nHello from SCU (Build %u, Commit %08x, %s %s)\n\n",
                    SCFW_BUILD, SCFW_COMMIT, SCFW_DATE, SCFW_TIME);
                banner = SC_TRUE;
            }
        }
    #elif defined(DEBUG_TERM_EMUL) && defined(DEBUG) && !defined(SIMU)
        *SCFW_DBG_TX_PTR = 0U;
        *SCFW_DBG_RX_PTR = 0U;
        /* Set to 2 for JTAG emulation */
        SCFW_DBG_READY = 2U;
    #endif
}
/*--------------------------------------------------------------------------*/
/* Disable debug UART                                                       */
/*--------------------------------------------------------------------------*/
void board_disable_debug_uart(void)
{
    /* Use M4 UART if ALT_DEBUG_UART defined */
    #if defined(ALT_DEBUG_UART) && defined(DEBUG) && !defined(SIMU)
        /* Return if debug already disabled */
        if (SCFW_DBG_READY != 0U)
        {
            /* Disable use of UART */
            SCFW_DBG_READY = 0U;
            // UART deinit to flush TX buffers
            LPUART_Deinit(LPUART_DEBUG);
            /* Turn off UART */
            pm_force_resource_power_mode_v(SC_R_M4_0_UART,
                SC_PM_PW_MODE_OFF);
        }
    #endif
}
/*--------------------------------------------------------------------------*/
/* Configure SCFW resource/pins                                             */
/*--------------------------------------------------------------------------*/
void board_config_sc(sc_rm_pt_t pt_sc)
{
    /* By default, the SCFW keeps most of the resources found in the SCU
     * subsystem. It also keeps the SCU/PMIC pads required for the main
     * code to function. Any additional resources or pads required for
     * the board code to run should be kept here. This is done by marking
     * them as not movable.
     */
    #ifdef ALT_DEBUG_UART
        (void) rm_set_resource_movable(SC_PT, SC_R_M4_0_UART, SC_R_M4_0_UART,
            SC_FALSE);
        (void) rm_set_pad_movable(SC_PT, SC_P_M40_I2C0_SCL, SC_P_M40_I2C0_SDA,
            SC_FALSE);
    #endif
    (void) rm_set_resource_movable(pt_sc, SC_R_SC_I2C, SC_R_SC_I2C,
        SC_FALSE);
    (void) rm_set_pad_movable(pt_sc, SC_P_PMIC_I2C_SDA, SC_P_PMIC_I2C_SCL,
        SC_FALSE);
    #ifdef ALT_DEBUG_SCU_UART
        (void) rm_set_pad_movable(pt_sc, SC_P_SCU_GPIO0_00,
            SC_P_SCU_GPIO0_02, SC_FALSE);
    #else
        (void) rm_set_pad_movable(pt_sc, SC_P_SCU_GPIO0_01,
            SC_P_SCU_GPIO0_02, SC_FALSE);
    #endif
}
/*--------------------------------------------------------------------------*/
/* Get board parameter                                                      */
/*--------------------------------------------------------------------------*/
board_parm_rtn_t board_parameter(board_parm_t parm)
```

```
{
    board_parm_rtn_t rtn = BOARD_PARM_RTN_NOT_USED;
    /* Note return values are usually static. Can be made dynamic by storing
       return in a global variable and setting using board_set_control() */
    switch (parm)
    {
        /* Used whenever HSIO SS powered up. Valid return values are
           BOARD_PARM_RTN_EXTERNAL or BOARD_PARM_RTN_INTERNAL */
        case BOARD_PARM_PCIE_PLL :
            rtn = BOARD_PARM_RTN_EXTERNAL;
            break;
        case BOARD_PARM_KS1_RESUME_USEC:
            rtn = BOARD_KS1_RESUME_USEC;
            break;
        case BOARD_PARM_KS1_RETENTION:
            rtn = BOARD_KS1_RETENTION;
            break;
        case BOARD_PARM_KS1_ONOFF_WAKE:
            rtn = BOARD_KS1_ONOFF_WAKE;
            break;
        case BOARD_PARM_DC0_PLL0_SSC:
            rtn = BOARD_PARM_RTN_NOT_USED;
            break;
        case BOARD_PARM_DC0_PLL1_SSC:
            rtn = BOARD_PARM_RTN_NOT_USED;
            break;
        case BOARD_PARM_DC1_PLL0_SSC:
            rtn = BOARD_PARM_RTN_NOT_USED;
            break;
        case BOARD_PARM_DC1_PLL1_SSC:
            rtn = BOARD_PARM_RTN_NOT_USED;
            break;
        case BOARD_PARM_KS1_WDOG_WAKE:
            rtn = BOARD_PARM_KS1_WDOG_WAKE_ENABLE;
            break;
        default :
            ; /* Intentional empty default */
            break;
    }
    return rtn;
}
/*------------------------------------------------------------------------*/
/* Get resource avaiability info                                          */
/*------------------------------------------------------------------------*/
sc_bool_t board_rsrc_avail(sc_rsrc_t rsrc)
{
    sc_bool_t rtn = SC_TRUE;
    /* Return SC_FALSE here if a resource isn't available due to board
       connections (typically lack of power). Examples incluse DRC_0/1
       and ADC. */
    /* The value here may be overridden by SoC fuses or emulation config */

    /* Note return values are usually static. Can be made dynamic by storing
       return in a global variable and setting using board_set_control() */
    #if defined(BD_DDR_RET_NUM_DRC) && (BD_DDR_RET_NUM_DRC == 1U)
        if(rsrc == SC_R_DRC_1)
        {
            rtn = SC_FALSE;
        }
    #endif
    if(rsrc == SC_R_PMIC_2)
    {
        rtn = SC_FALSE;
    }
    return rtn;
}
/*------------------------------------------------------------------------*/
/* Init DDR                                                               */
/*------------------------------------------------------------------------*/
sc_err_t board_init_ddr(sc_bool_t early, sc_bool_t ddr_initialized)
{
    /*
     * Variables for DDR retention
     */
    #if defined(BD_DDR_RET) & !defined(SKIP_DDR)
        /* Storage for DRC registers */
        static ddrc board_ddr_ret_drc_inst[BD_DDR_RET_NUM_DRC];
        /* Storage for DRC PHY registers */
        static ddr_phy board_ddr_ret_drc_phy_inst[BD_DDR_RET_NUM_DRC];
        /* Storage for DDR regions */
        static uint32_t board_ddr_ret_buf1[BD_DDR_RET_REGION1_SIZE];
```

```
    #ifdef BD_DDR_RET_REGION2_SIZE
    static uint32_t board_ddr_ret_buf2[BD_DDR_RET_REGION2_SIZE];
    #endif
    #ifdef BD_DDR_RET_REGION3_SIZE
    static uint32_t board_ddr_ret_buf3[BD_DDR_RET_REGION3_SIZE];
    #endif
    #ifdef BD_DDR_RET_REGION4_SIZE
    static uint32_t board_ddr_ret_buf4[BD_DDR_RET_REGION4_SIZE];
    #endif
    #ifdef BD_DDR_RET_REGION5_SIZE
    static uint32_t board_ddr_ret_buf5[BD_DDR_RET_REGION5_SIZE];
    #endif
    #ifdef BD_DDR_RET_REGION6_SIZE
    static uint32_t board_ddr_ret_buf6[BD_DDR_RET_REGION6_SIZE];
    #endif
    /* DDR region descriptors */
    static const soc_ddr_ret_region_t board_ddr_ret_region[BD_DDR_RET_NUM_REGION] =
    {
        { BD_DDR_RET_REGION1_ADDR, BD_DDR_RET_REGION1_SIZE, board_ddr_ret_buf1 },
    #ifdef BD_DDR_RET_REGION2_SIZE
        { BD_DDR_RET_REGION2_ADDR, BD_DDR_RET_REGION2_SIZE, board_ddr_ret_buf2 },
    #endif
    #ifdef BD_DDR_RET_REGION3_SIZE
        { BD_DDR_RET_REGION3_ADDR, BD_DDR_RET_REGION3_SIZE, board_ddr_ret_buf3 },
    #endif
    #ifdef BD_DDR_RET_REGION4_SIZE
        { BD_DDR_RET_REGION4_ADDR, BD_DDR_RET_REGION4_SIZE, board_ddr_ret_buf4 },
    #endif
    #ifdef BD_DDR_RET_REGION5_SIZE
        { BD_DDR_RET_REGION5_ADDR, BD_DDR_RET_REGION5_SIZE, board_ddr_ret_buf5 },
    #endif
    #ifdef BD_DDR_RET_REGION6_SIZE
        { BD_DDR_RET_REGION6_ADDR, BD_DDR_RET_REGION6_SIZE, board_ddr_ret_buf6 }
    #endif
    };
    /* DDR retention descriptor passed to SCFW */
    static soc_ddr_ret_info_t board_ddr_ret_info =
    {
      BD_DDR_RET_NUM_DRC, board_ddr_ret_drc_inst, board_ddr_ret_drc_phy_inst,
      BD_DDR_RET_NUM_REGION, board_ddr_ret_region
    };
#endif
#if defined(BD_LPDDR4_INC_DQS2DQ) && defined(BOARD_DQS2DQ_SYNC)
    static soc_dqs2dq_sync_info_t board_dqs2dq_sync_info =
    {
        BOARD_DQS2DQ_ISI_RSRC, BOARD_DQS2DQ_ISI_REG, BOARD_DQS2DQ_SYNC_TIME
    };
#endif
board_print(3, "board_init_ddr(%d)\n", early);
#ifdef SKIP_DDR
    return SC_ERR_UNAVAILABLE;
#else
    sc_err_t err = SC_ERR_NONE;
    /* Don't power up DDR for M4s */
    ASRT_ERR(early == SC_FALSE, SC_ERR_UNAVAILABLE);
    if ((err == SC_ERR_NONE) && (ddr_initialized == SC_FALSE))
    {
        board_print(1, "SCFW: ");
        err = board_ddr_config(SC_FALSE, BOARD_DDR_COLD_INIT);
        #ifdef LP4_MANUAL_DERATE_WORKAROUND
            ddrc_lpddr4_derate_init(BD_DDR_RET_NUM_DRC);
        #endif
    }
    #ifdef DEBUG_BOARD
        uint32_t rate = 0U;
        sc_err_t rate_err = SC_ERR_FAIL;
        if (rm_is_resource_avail(SC_R_DRC_0))
        {
            rate_err = pm_get_clock_rate(SC_PT, SC_R_DRC_0,
                SC_PM_CLK_SLV_BUS, &rate);
        }
        else if (rm_is_resource_avail(SC_R_DRC_1))
        {
            rate_err = pm_get_clock_rate(SC_PT, SC_R_DRC_1,
                SC_PM_CLK_SLV_BUS, &rate);
        }
        else
        {
            ; /* Intentional empty else */
        }
        if (rate_err == SC_ERR_NONE)
```

```
            {
                board_print(1, "DDR frequency = %u\n", rate * 2U);
            }
        #endif
        if (err == SC_ERR_NONE)
        {
            #ifdef BD_DDR_RET
                soc_ddr_config_retention(&board_ddr_ret_info);
            #endif
            #ifdef BD_LPDDR4_INC_DQS2DQ
            #ifdef BOARD_DQS2DQ_SYNC
                soc_ddr_dqs2dq_config(&board_dqs2dq_sync_info);
            #endif
                if (board_ddr_period_ms != 0U)
                {
                    soc_ddr_dqs2dq_init();
                }
            #endif
        }
        #ifdef LP4_MANUAL_DERATE_WORKAROUND
            board_ddr_derate_periodic_enable(SC_TRUE);
        #endif
        return err;
    #endif
}
/*------------------------------------------------------------------------*/
/* Take action on DDR                                                     */
/*------------------------------------------------------------------------*/
sc_err_t  board_ddr_config(bool rom_caller, board_ddr_action_t action)
{
    /* Note this is called by the ROM before the SCFW is initialized.
     * Do NOT make any unqualified calls to any other APIs.
     */
    sc_err_t err = SC_ERR_NONE;
#ifdef LP4_MANUAL_DERATE_WORKAROUND
    sc_bool_t polling = SC_FALSE;
#endif
    switch(action)
    {
        case BOARD_DDR_PERIODIC:
    #ifdef BD_LPDDR4_INC_DQS2DQ
            soc_ddr_dqs2dq_periodic();
    #endif
            break;
        case BOARD_DDR_SR_DRC_OFF_ENTER:
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
            board_ddr_derate_periodic_enable(SC_FALSE);
    #endif
            board_ddr_periodic_enable(SC_FALSE);
    #ifdef BD_DDR_RET
            soc_ddr_enter_retention();
    #endif
            break;
        case BOARD_DDR_SR_DRC_OFF_EXIT:
    #ifdef BD_DDR_RET
            soc_ddr_exit_retention();
    #endif
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
            ddrc_lpddr4_derate_init(BD_DDR_RET_NUM_DRC);
            board_ddr_derate_periodic_enable(SC_TRUE);
    #endif
    #ifdef BD_LPDDR4_INC_DQS2DQ
            soc_ddr_dqs2dq_init();
    #endif
            board_ddr_periodic_enable(SC_TRUE);
            break;
        case BOARD_DDR_SR_DRC_ON_ENTER:
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
            board_ddr_derate_periodic_enable(SC_FALSE);
    #endif
            board_ddr_periodic_enable(SC_FALSE);
            soc_self_refresh_power_down_clk_disable_entry();
            break;
        case BOARD_DDR_SR_DRC_ON_EXIT:
            soc_refresh_power_down_clk_disable_exit();
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
            ddrc_lpddr4_derate_init(BD_DDR_RET_NUM_DRC);
            board_ddr_derate_periodic_enable(SC_TRUE);
    #endif
    #ifdef BD_LPDDR4_INC_DQS2DQ
            soc_ddr_dqs2dq_periodic();
```

```
    #endif
            board_ddr_periodic_enable(SC_TRUE);
            break;
        case BOARD_DDR_PERIODIC_HALT:
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
            board_ddr_derate_periodic_enable(SC_FALSE);
    #endif
            board_ddr_periodic_enable(SC_FALSE);
            break;
        case BOARD_DDR_PERIODIC_RESTART:
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
            ddrc_lpddr4_derate_init(BD_DDR_RET_NUM_DRC);
            board_ddr_derate_periodic_enable(SC_TRUE);
    #endif
    #ifdef BD_LPDDR4_INC_DQS2DQ
            soc_ddr_dqs2dq_periodic();
    #endif
            board_ddr_periodic_enable(SC_TRUE);
            break;
    #ifdef LP4_MANUAL_DERATE_WORKAROUND
        case BOARD_DDR_DERATE_PERIODIC:
            polling = ddrc_lpddr4_derate_periodic(BD_DDR_RET_NUM_DRC);
            if (polling != SC_TRUE)
            {
                board_ddr_derate_periodic_enable(SC_FALSE);
            }
            break;
    #endif
        case BOARD_DDR0_VREF:
            #if defined(MONITOR) || defined(EXPORT_MONITOR)
                // Launch VREF training
                DRAM_VREF_training_hw(0);
            #else
                // Run vref training
                DRAM_VREF_training_sw(0);
            #endif
            break;
        case BOARD_DDR1_VREF:
            #if defined(MONITOR) || defined(EXPORT_MONITOR)
                // Launch VREF training
                DRAM_VREF_training_hw(1);
            #else
                // Run vref training
                DRAM_VREF_training_sw(1);
            #endif
            break;
        default:
            #include "dcd/dcd.h"
            break;
    }
    return err;
}
/*--------------------------------------------------------------------------*/
/* Configure the system (inc. additional resource partitions)               */
/*--------------------------------------------------------------------------*/
void board_system_config(sc_bool_t early, sc_rm_pt_t pt_boot)
{
    sc_err_t err = SC_ERR_NONE;
    /* This function configures the system. It usually partitions
       resources according to the system design. It must be modified by
       customers. Partitions should then be specified using the mkimage
       -p option. */
    /* Note the configuration here is for NXP test purposes */
    sc_bool_t alt_config = SC_FALSE;
    sc_bool_t no_ap = SC_FALSE;
    /* Get boot parameters. See the Boot Flags section for defintition
       of these flags.*/
    boot_get_data(NULL, NULL, NULL, NULL, NULL, NULL, &alt_config,
        NULL, NULL, &no_ap);
    board_print(3, "board_system_config(%d, %d)\n", early, alt_config);
#ifndef EMUL
    sc_rm_mr_t mr_temp;
    /* Board has 6GB memory so fragment upper region and retain 4GB */
    BRD_ERR(rm_memreg_frag(pt_boot, &mr_temp, 0x980000000ULL,
        0xFFFFFFFFULL));
    BRD_ERR(rm_memreg_free(pt_boot, mr_temp));
#endif
    /* Configure initial resource allocation (note additional allocation
       and assignments can be made by the SCFW clients at run-time */
    if ((alt_config != SC_FALSE)
        && (rm_is_resource_avail(SC_R_M4_0_PID0) != SC_FALSE))
```

```
{
    sc_rm_pt_t pt_m4_0;
    sc_rm_pt_t pt_m4_1;
    sc_rm_mr_t mr_m4_0, mr_m4_1;
    sc_rm_pt_t pt_sh;
    sc_rm_mr_t mr_sh;
    #ifdef BOARD_RM_DUMP
        rm_dump(pt_boot);
    #endif
    /* Mark all resources as not movable */
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_ALL, SC_R_ALL,
        SC_FALSE));
    BRD_ERR(rm_set_pad_movable(pt_boot, SC_P_ALL, SC_P_ALL,
        SC_FALSE));
    /* Allocate M4_0 partition */
    BRD_ERR(rm_partition_alloc(pt_boot, &pt_m4_0, SC_FALSE, SC_TRUE,
        SC_FALSE, SC_TRUE, SC_FALSE));
    /* Mark all M4_0 subsystem resources as movable */
    BRD_ERR(rm_set_subsys_rsrc_movable(pt_boot, SC_R_M4_0_PID0,
        SC_TRUE));
    BRD_ERR(rm_set_pad_movable(pt_boot, SC_P_M40_I2C0_SCL,
        SC_P_M40_GPIO0_01, SC_TRUE));
    /* Move some resources not in the M4_0 subsystem */
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_SYSTEM,
        SC_R_SYSTEM, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_IRQSTR_M4_0,
        SC_R_IRQSTR_M4_0, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_MU_5B,
        SC_R_MU_5B, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_MU_7A,
        SC_R_MU_7A, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_MU_8B,
        SC_R_MU_8B, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_GPT_4,
        SC_R_GPT_4, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_SECO_MU_4,
        SC_R_SECO_MU_4, SC_TRUE));
    /* Move everything flagged as movable */
    BRD_ERR(rm_move_all(pt_boot, pt_boot, pt_m4_0, SC_TRUE, SC_TRUE));
    /* Allow all to access the SEMA42 */
    BRD_ERR(rm_set_peripheral_permissions(pt_m4_0, SC_R_M4_0_SEMA42,
        SC_RM_PT_ALL, SC_RM_PERM_FULL));
    /* Move M4 0 TCM */
    BRD_ERR(rm_find_memreg(pt_boot, &mr_m4_0, 0x034FE0000ULL,
        0x034FE0000ULL));
    BRD_ERR(rm_assign_memreg(pt_boot, pt_m4_0, mr_m4_0));
    /* Reserve DDR for M4_0 */
    BRD_ERR(rm_memreg_frag(pt_boot, &mr_m4_0, 0x088000000ULL,
        0x0887FFFFFULL));
    BRD_ERR(rm_assign_memreg(pt_boot, pt_m4_0, mr_m4_0));
    /* Reserve FlexSPI for M4_0 */
    BRD_ERR(rm_memreg_frag(pt_boot, &mr_m4_0, 0x08081000ULL,
        0x08180FFFULL));
    BRD_ERR(rm_assign_memreg(pt_boot, pt_m4_0, mr_m4_0));
    /* Allocate M4_1 partition */
    BRD_ERR(rm_partition_alloc(pt_boot, &pt_m4_1, SC_FALSE, SC_TRUE,
        SC_FALSE, SC_TRUE, SC_FALSE));
    /* Mark all M4_1 subsystem resources as movable */
    BRD_ERR(rm_set_subsys_rsrc_movable(pt_boot, SC_R_M4_1_PID0,
        SC_TRUE));
    BRD_ERR(rm_set_pad_movable(pt_boot, SC_P_M41_I2C0_SCL,
        SC_P_M41_GPIO0_01, SC_TRUE));
    /* Move some resources not in the M4_1 subsystem */
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_IRQSTR_M4_1,
        SC_R_IRQSTR_M4_1, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_UART_2,
        SC_R_UART_2, SC_TRUE));
    BRD_ERR(rm_set_pad_movable(pt_boot, SC_P_UART0_CTS_B,
        SC_P_UART0_RTS_B, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_MU_6B,
        SC_R_MU_6B, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_MU_7B,
        SC_R_MU_7B, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_MU_9B,
        SC_R_MU_9B, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_GPT_3,
        SC_R_GPT_3, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_CAN_0,
        SC_R_CAN_2, SC_TRUE));
    BRD_ERR(rm_set_resource_movable(pt_boot, SC_R_FSPI_0,
        SC_R_FSPI_0, SC_TRUE));
```

```
        /* Move some pads not in the M4_1 subsystem */
        BRD_ERR(rm_set_pad_movable(pt_boot, SC_P_FLEXCAN0_RX,
            SC_P_FLEXCAN2_TX, SC_TRUE));
        BRD_ERR(rm_set_pad_movable(pt_boot, SC_P_QSPI0A_DATA0,
            SC_P_COMP_CTL_GPIO_1V8_3V3_QSPI0, SC_TRUE));
        /* Move everything flagged as movable */
        BRD_ERR(rm_move_all(pt_boot, pt_boot, pt_m4_1, SC_TRUE, SC_TRUE));
        /* Allow all to access the SEMA42 */
        BRD_ERR(rm_set_peripheral_permissions(pt_m4_1, SC_R_M4_1_SEMA42,
            SC_RM_PT_ALL, SC_RM_PERM_FULL));
        /* Move M4 1 TCM */
        BRD_ERR(rm_find_memreg(pt_boot, &mr_m4_1, 0x038FE0000ULL,
            0x038FE0000ULL));
        BRD_ERR(rm_assign_memreg(pt_boot, pt_m4_1, mr_m4_1));
        /* Reserve DDR for M4_1 */
        BRD_ERR(rm_memreg_frag(pt_boot, &mr_m4_1, 0x088800000ULL,
            0x08FFFFFFFULL));
        BRD_ERR(rm_assign_memreg(pt_boot, pt_m4_1, mr_m4_1));
        /* Reserve FlexSPI for M4_1 */
        BRD_ERR(rm_memreg_frag(pt_boot, &mr_m4_1, 0x08181000ULL,
            0x08280FFFULL));
        BRD_ERR(rm_assign_memreg(pt_boot, pt_m4_1, mr_m4_1));
        /* Allow AP and M4_1 to use SYSTEM */
        BRD_ERR(rm_set_peripheral_permissions(pt_m4_0, SC_R_SYSTEM,
            pt_boot, SC_RM_PERM_SEC_RW));
        BRD_ERR(rm_set_peripheral_permissions(pt_m4_0, SC_R_SYSTEM,
            pt_m4_1, SC_RM_PERM_SEC_RW));
        /* Move partition to be owned by SC */
        BRD_ERR(rm_set_parent(pt_boot, pt_m4_0, SC_PT));
        BRD_ERR(rm_set_parent(pt_boot, pt_m4_1, SC_PT));
        /* Move boot to be owned by M4 0 */
        if (no_ap != SC_FALSE)
        {
            BRD_ERR(rm_set_parent(SC_PT, pt_boot, pt_m4_0));
        }
        /* Allocate shared partition */
        BRD_ERR(rm_partition_alloc(SC_PT, &pt_sh, SC_FALSE, SC_TRUE,
            SC_FALSE, SC_FALSE, SC_FALSE));
        /* Create shared memory space */
        BRD_ERR(rm_memreg_frag(pt_boot, &mr_sh,
            0x090000000ULL, 0x091FFFFFFULL));
        BRD_ERR(rm_assign_memreg(pt_boot, pt_sh, mr_sh));
        BRD_ERR(rm_set_memreg_permissions(pt_sh, mr_sh, pt_boot,
            SC_RM_PERM_FULL));
        BRD_ERR(rm_set_memreg_permissions(pt_sh, mr_sh, pt_m4_0,
            SC_RM_PERM_FULL));
        BRD_ERR(rm_set_memreg_permissions(pt_sh, mr_sh, pt_m4_1,
            SC_RM_PERM_FULL));
        /* Protect some resources */
        /* M4 PID1-4 can be used to allow M4 to map to other SID */
        BRD_ERR(rm_assign_resource(pt_m4_0, pt_sh, SC_R_M4_0_PID1));
        BRD_ERR(rm_assign_resource(pt_m4_0, pt_sh, SC_R_M4_0_PID2));
        BRD_ERR(rm_assign_resource(pt_m4_0, pt_sh, SC_R_M4_0_PID3));
        BRD_ERR(rm_assign_resource(pt_m4_0, pt_sh, SC_R_M4_0_PID4));
        BRD_ERR(rm_assign_resource(pt_m4_1, pt_sh, SC_R_M4_1_PID1));
        BRD_ERR(rm_assign_resource(pt_m4_1, pt_sh, SC_R_M4_1_PID2));
        BRD_ERR(rm_assign_resource(pt_m4_1, pt_sh, SC_R_M4_1_PID3));
        BRD_ERR(rm_assign_resource(pt_m4_1, pt_sh, SC_R_M4_1_PID4));
        #ifdef BOARD_RM_DUMP
            rm_dump(pt_boot);
        #endif
    }
}
/*------------------------------------------------------------------------*/
/* Early CPU query                                                        */
/*------------------------------------------------------------------------*/
sc_bool_t board_early_cpu(sc_rsrc_t cpu)
{
    sc_bool_t rtn = SC_FALSE;
    if ((cpu == SC_R_M4_0_PID0) || (cpu == SC_R_M4_1_PID0))
    {
        rtn = SC_TRUE;
    }
    return rtn;
}
/*------------------------------------------------------------------------*/
/* Transition external board-level SoC power domain                       */
/*------------------------------------------------------------------------*/
void board_set_power_mode(sc_sub_t ss, uint8_t pd,
    sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
{
```

```
    pmic_id_t pmic_id[2] = {0U, 0U};
    uint32_t pmic_reg[2] = {0U, 0U};
    uint8_t num_regs = 0U;
    board_print(3, "board_set_power_mode(%s, %d, %d, %d)\n", snames[ss],
        pd, from_mode, to_mode);
    board_get_pmic_info(ss, pmic_id, pmic_reg, &num_regs);
    /* Check for PMIC */
    if (pmic_ver.device_id != 0U)
    {
        sc_err_t err = SC_ERR_NONE;
        /* Flip switch */
        if (to_mode > SC_PM_PW_MODE_OFF)
        {
            uint8_t idx = 0U;
            while (idx < num_regs)
            {
                BRD_ERR(PMIC_SET_MODE(pmic_id[idx], pmic_reg[idx],
                    SW_RUN_PWM | SW_STBY_PWM));
                idx++;
            }
            SystemTimeDelay(PMIC_MAX_RAMP);
        }
        else
        {
            uint8_t idx = 0U;
            while (idx < num_regs)
            {
                BRD_ERR(PMIC_SET_MODE(pmic_id[idx], pmic_reg[idx],
                    SW_RUN_OFF));
                idx++;
            }
        }
    }
}
/*--------------------------------------------------------------------------*/
/* Set the voltage for the given SS.                                        */
/*--------------------------------------------------------------------------*/
sc_err_t board_set_voltage(sc_sub_t ss, uint32_t new_volt, uint32_t old_volt)
{
    sc_err_t err = SC_ERR_NONE;
    pmic_id_t pmic_id[2] = {0U, 0U};
    uint32_t pmic_reg[2] = {0U, 0U};
    uint8_t num_regs = 0U;
    board_print(3, "board_set_voltage(%s, %u, %u)\n", snames[ss], new_volt,
        old_volt);
    board_get_pmic_info(ss, pmic_id, pmic_reg, &num_regs);
    /* Check for PMIC */
    if (pmic_ver.device_id == 0U)
    {
        err = SC_ERR_NOTFOUND;
    }
    else
    {
        uint8_t idx = 0U;
        while (idx < num_regs)
        {
            BRD_ERR(PMIC_SET_VOLTAGE(pmic_id[idx], pmic_reg[idx], new_volt,
                REG_RUN_MODE));
            idx++;
        }
        if ((old_volt != 0U) && (new_volt > old_volt))
        {
            /* PMIC_MAX_RAMP_RATE is in nano Volts. */
            uint32_t ramp_time = ((new_volt - old_volt) * 1000U)
                / PMIC_MAX_RAMP_RATE;
            SystemTimeDelay(ramp_time + 1U);
        }
    }
    return err;
}
/*--------------------------------------------------------------------------*/
/* Set board power supplies when enter/exit low-power mode                  */
/*--------------------------------------------------------------------------*/
void board_lpm(sc_pm_power_mode_t mode)
{
    static uint32_t vdd_memc_mode = 0U;
    if (mode == SC_PM_PW_MODE_STBY)
    {
        /*
         * System standby (KS1) entry allows VDD_MEMC to be gated off.
         * Save current mode and switch off supply.
```

```
         */
        if (PMIC_GET_MODE(PMIC_1_ADDR, PF8100_SW5, &vdd_memc_mode)
            == SC_ERR_NONE)
        {
            (void) PMIC_SET_MODE(PMIC_1_ADDR, PF8100_SW5, SW_STBY_OFF
                | SW_RUN_OFF);
        }
    }
    else if (mode == SC_PM_PW_MODE_ON)
    {
        /*
         * System standby (KS1) exit should switch on VDD_MEMC.  Restore
         * previous mode saved during KS1 entry.
         */
        if (vdd_memc_mode != 0U)
        {
            (void) PMIC_SET_MODE(PMIC_1_ADDR, PF8100_SW5, vdd_memc_mode);
        }
    }
    else
    {
        ; /* Intentional empty else */
    }
}
/*------------------------------------------------------------------------*/
/* Reset a board resource                                                 */
/*------------------------------------------------------------------------*/
void board_rsrc_reset(sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx, sc_rm_pt_t pt)
{
}
/*------------------------------------------------------------------------*/
/* Transition external board-level supply for board component             */
/*------------------------------------------------------------------------*/
void board_trans_resource_power(sc_rm_idx_t idx, sc_rm_idx_t rsrc_idx,
    sc_pm_power_mode_t from_mode, sc_pm_power_mode_t to_mode)
{
    board_print(3, "board_trans_resource_power(%d, %s, %u, %u)\n", idx,
        rnames[rsrc_idx], from_mode, to_mode);
    /* Init PMIC */
    pmic_init();
    /* Process resource */
    if (pmic_ver.device_id != 0U)
    {
        sc_err_t err = SC_ERR_NONE;
        switch (idx)
        {
            case BRD_R_BOARD_R2 : /* EMVSIM */
                if (to_mode > SC_PM_PW_MODE_OFF)
                {
                    BRD_ERR(PMIC_SET_VOLTAGE(PMIC_1_ADDR, PF8100_LDO1,
                        3000, REG_RUN_MODE));
                    BRD_ERR(PMIC_SET_MODE(PMIC_1_ADDR, PF8100_LDO1,
                        RUN_EN_STBY_EN));
                }
                else
                {
                    BRD_ERR(PMIC_SET_MODE(PMIC_1_ADDR, PF8100_LDO1,
                        RUN_OFF_STBY_OFF));
                }
                break;
            case BRD_R_BOARD_R3 : /* USDHC2 on Base Board */
                if (to_mode > SC_PM_PW_MODE_OFF)
                {
                    BRD_ERR(PMIC_SET_MODE(PMIC_1_ADDR, PF8100_LDO2,
                        RUN_EN_STBY_EN | VSELECT_EN));
                }
                else
                {
                    BRD_ERR(PMIC_SET_MODE(PMIC_1_ADDR, PF8100_LDO2,
                        RUN_OFF_STBY_OFF));
                }
                break;
            case BRD_R_BOARD_R7 :
                /* Example for testing (use SC_R_BOARD_R7) */
                board_print(3, "SC_R_BOARD_R7 from %u to %u\n",
                    from_mode, to_mode);
                break;
            default :
                ; /* Intentional empty default */
                break;
        }
```

```
    }
}
/*-------------------------------------------------------------------------*/
/* Set board power mode                                                    */
/*-------------------------------------------------------------------------*/
sc_err_t board_power(sc_pm_power_mode_t mode)
{
    sc_err_t err = SC_ERR_NONE;
    if (mode == SC_PM_PW_MODE_OFF)
    {
        /* Request power off */
        SNVS_PowerOff();
        err = snvs_err;
        /* Loop forever */
        while(err == SC_ERR_NONE)
        {
            ; /* Intentional empty while */
        }
    }
    else
    {
        err = SC_ERR_PARM;
    }
    return err;
}
/*-------------------------------------------------------------------------*/
/* Reset board                                                             */
/*-------------------------------------------------------------------------*/
sc_err_t board_reset(sc_pm_reset_type_t type, sc_pm_reset_reason_t reason,
    sc_rm_pt_t pt)
{
    if (type == SC_PM_RESET_TYPE_BOARD)
    {
        /* Request PMIC do a board reset */
    }
    else if (type == SC_PM_RESET_TYPE_COLD)
    {
        /* Request PMIC do a cold reset */
    }
    else
    {
        ; /* Intentional empty else */
    }
    #ifdef DEBUG
        /* Dump out caller of reset request */
        always_print("Board reset (%u, caller = 0x%08X)\n", reason,
            __builtin_return_address(0));
    #endif
    #ifdef ALT_DEBUG_UART
        /* Invoke LPUART deinit to drain TX buffers if a warm reset follows */
        LPUART_Deinit(LPUART_DEBUG);
    #endif
    /* Request a warm reset */
    soc_set_reset_info(reason, pt);
    NVIC_SystemReset();
    return SC_ERR_UNAVAILABLE;
}
/*-------------------------------------------------------------------------*/
/* Handle CPU reset event                                                  */
/*-------------------------------------------------------------------------*/
void board_cpu_reset(sc_rsrc_t resource, board_cpu_rst_ev_t reset_event,
    sc_rm_pt_t pt)
{
    /* Note:  Production code should decide the response for each type
     *        of reset event.  Options include allowing the SCFW to
     *        reset the CPU or forcing a full system reset.  Additionally,
     *        the number of reset attempts can be tracked to determine the
     *        reset response.
     */
    /* Check for M4 reset event */
    if ((resource == SC_R_M4_0_PID0) || (resource == SC_R_M4_1_PID0))
    {
        always_print("CM4 reset event (rsrc = %d, event = %d)\n", resource,
            reset_event);
        /* Treat lockups or parity/ECC reset events as board faults */
        if ((reset_event == BOARD_CPU_RESET_LOCKUP) ||
            (reset_event == BOARD_CPU_RESET_MEM_ERR))
        {
            board_fault(SC_FALSE, BOARD_BFAULT_CPU, pt);
        }
    }
```

```
    /* Returning from this function will result in an attempt reset the
       partition or board depending on the event and wdog action. */
}
/*------------------------------------------------------------------------*/
/* Trap partition reboot                                                  */
/*------------------------------------------------------------------------*/
void board_reboot_part(sc_rm_pt_t pt, sc_pm_reset_type_t *type,
    sc_pm_reset_reason_t *reason, sc_pm_power_mode_t *mode,
    uint32_t *mask)
{
    /* Code can modify or log the parameters. Can also take another action like
     * reset the board. After return from this function, the partition will be
     * rebooted.
     */
    *mask = 0UL;
}
/*------------------------------------------------------------------------*/
/* Trap partition reboot continue                                         */
/*------------------------------------------------------------------------*/
void board_reboot_part_cont(sc_rm_pt_t pt, sc_rsrc_t *boot_cpu,
    sc_rsrc_t *boot_mu, sc_rsrc_t *boot_dev, sc_faddr_t *boot_addr)
{
    /* Code can modify boot parameters on a reboot. Called after partition
     * is powered off but before it is powered back on and started.
     */
}
/*------------------------------------------------------------------------*/
/* Return partition reboot timeout action                                 */
/*------------------------------------------------------------------------*/
board_reboot_to_t board_reboot_timeout(sc_rm_pt_t pt)
{
    /* Return the action to take if a partition reboot requires continue
     * ack for others and does not happen before timeout */
    return BOARD_REBOOT_TO_FORCE;
}
/*------------------------------------------------------------------------*/
/* Handle panic temp alarm                                                */
/*------------------------------------------------------------------------*/
void board_panic(sc_dsc_t dsc)
{
    /* See Porting Guide for more info on panic alarms */
    #ifdef DEBUG
        error_print("Panic temp (dsc=%d)\n", dsc);
    #endif
    (void) board_reset(SC_PM_RESET_TYPE_BOARD, SC_PM_RESET_REASON_TEMP,
        SC_PT);
}
/*------------------------------------------------------------------------*/
/* Handle fault or return from main()                                     */
/*------------------------------------------------------------------------*/
void board_fault(sc_bool_t restarted, sc_bfault_t reason,
    sc_rm_pt_t pt)
{
    /* Note, delete the DEBUG case if fault behavior should be like
       typical production build even if DEBUG defined */
    #ifdef DEBUG
        /* Disable the WDOG */
        WDOG32_Unlock(WDOG_SC);
        WDOG32_SetTimeoutValue(WDOG_SC, 0xFFFF);
        WDOG32_Disable(WDOG_SC);
        board_print(1, "board fault(%u, %u, %u)\n", restarted, reason, pt);
        /* Stop so developer can see WDOG occurred */
        HALT;
    #else
        /* Was this called to report a previous WDOG restart? */
        if (restarted == SC_FALSE)
        {
            /* Fault just occurred, need to reset */
            (void) board_reset(SC_PM_RESET_TYPE_BOARD,
                SC_PM_RESET_REASON_SCFW_FAULT, pt);
            /* Wait for reset */
            HALT;
        }
        /* Issue was before restart so just return */
    #endif
}
/*------------------------------------------------------------------------*/
/* Handle SECO/SNVS security violation                                    */
/*------------------------------------------------------------------------*/
void board_security_violation(void)
{
```

```
    always_print("SNVS security violation\n");
}
/*-------------------------------------------------------------------------*/
/* Get the status of the ON/OFF button                                     */
/*-------------------------------------------------------------------------*/
sc_bool_t board_get_button_status(void)
{
    return SNVS_GetButtonStatus();
}
/*-------------------------------------------------------------------------*/
/* Set control value                                                       */
/*-------------------------------------------------------------------------*/
sc_err_t board_set_control(sc_rsrc_t resource, sc_rm_idx_t idx,
    sc_rm_idx_t rsrc_idx, uint32_t ctrl, uint32_t val)
{
    sc_err_t err = SC_ERR_NONE;
    board_print(3,
        "board_set_control(%s, %u, %u)\n", rnames[rsrc_idx], ctrl, val);
    /* Init PMIC */
    pmic_init();
    /* Check if PMIC available */
    ASRT_ERR(pmic_ver.device_id != 0U, SC_ERR_NOTFOUND);
    if (err == SC_ERR_NONE)
    {
        /* Process control */
        switch (resource)
        {
            case SC_R_PMIC_0 :
                if (ctrl == SC_C_TEMP_HI)
                {
                    temp_alarm0 =
                        SET_PMIC_TEMP_ALARM(PMIC_0_ADDR, val);
                }
                else
                {
                    err = SC_ERR_PARM;
                }
                break;
            case SC_R_PMIC_1 :
                if (ctrl == SC_C_TEMP_HI)
                {
                    temp_alarm1 =
                        SET_PMIC_TEMP_ALARM(PMIC_1_ADDR, val);
                }
                else
                {
                    err = SC_ERR_PARM;
                }
                break;
            case SC_R_BOARD_R7 :
                if (ctrl == SC_C_VOLTAGE)
                {
                    /* Example (used for testing) */
                    board_print(3, "SC_R_BOARD_R7 voltage set to %u\n",
                        val);
                }
                else
                {
                    err = SC_ERR_PARM;
                }
                break;
            default :
                err = SC_ERR_PARM;
                break;
        }
    }
    return err;
}
/*-------------------------------------------------------------------------*/
/* Get control value                                                       */
/*-------------------------------------------------------------------------*/
sc_err_t board_get_control(sc_rsrc_t resource, sc_rm_idx_t idx,
    sc_rm_idx_t rsrc_idx, uint32_t ctrl, uint32_t *val)
{
    sc_err_t err = SC_ERR_NONE;
    board_print(3,
        "board_get_control(%s, %u)\n", rnames[rsrc_idx], ctrl);
    /* Init PMIC */
    pmic_init();
    /* Check if PMIC available */
    ASRT_ERR(pmic_ver.device_id != 0U, SC_ERR_NOTFOUND);
```

```
    if (err == SC_ERR_NONE)
    {
        /* Process control */
        switch (resource)
        {
            case SC_R_PMIC_0 :
                if (ctrl == SC_C_TEMP)
                {
                    *val = GET_PMIC_TEMP(PMIC_0_ADDR);
                }
                else if (ctrl == SC_C_TEMP_HI)
                {
                    *val = temp_alarm0;
                }
                else if (ctrl == SC_C_ID)
                {
                    pmic_version_t v = GET_PMIC_VERSION(PMIC_0_ADDR);
                    *val = (U32(v.device_id) « 8U) | U32(v.si_rev);
                }
                else
                {
                    err = SC_ERR_PARM;
                }
                break;
            case SC_R_PMIC_1 :
                if (ctrl == SC_C_TEMP)
                {
                    *val = GET_PMIC_TEMP(PMIC_1_ADDR);
                }
                else if (ctrl == SC_C_TEMP_HI)
                {
                    *val = temp_alarm1;
                }
                else if (ctrl == SC_C_ID)
                {
                    pmic_version_t v = GET_PMIC_VERSION(PMIC_1_ADDR);
                    *val = (U32(v.device_id) « 8U) | U32(v.si_rev);
                }
                else
                {
                    err = SC_ERR_PARM;
                }
                break;
            case SC_R_BOARD_R7 :
                if (ctrl == SC_C_VOLTAGE)
                {
                    /* Example (used for testing) */
                    board_print(3, "SC_R_BOARD_R7 voltage get\n");
                }
                else
                {
                    err = SC_ERR_PARM;
                }
                break;
            default :
                err = SC_ERR_PARM;
                break;
        }
    }
    return err;
}
/*--------------------------------------------------------------------------*/
/* PMIC Interrupt (INTB) handler                                            */
/*--------------------------------------------------------------------------*/
void PMIC_IRQHandler(void)
{
    if (PMIC_IRQ_SERVICE(PMIC_1_ADDR) != SC_FALSE)
    {
        ss_irq_trigger(SC_IRQ_GROUP_TEMP, SC_IRQ_TEMP_PMIC1_HIGH,
            SC_PT_ALL);
    }
    if (PMIC_IRQ_SERVICE(PMIC_0_ADDR) != SC_FALSE)
    {
        ss_irq_trigger(SC_IRQ_GROUP_TEMP, SC_IRQ_TEMP_PMIC0_HIGH,
            SC_PT_ALL);
    }
    NVIC_ClearPendingIRQ(PMIC_INT_IRQn);
}
/*--------------------------------------------------------------------------*/
/* Button Handler                                                           */
/*--------------------------------------------------------------------------*/
```

```
void SNVS_Button_IRQHandler(void)
{
    SNVS_ClearButtonIRQ();
    ss_irq_trigger(SC_IRQ_GROUP_WAKE, SC_IRQ_BUTTON,
        SC_PT_ALL);
}
/*============================================================================*/
/*----------------------------------------------------------------------------*/
/* Init the PMIC interface                                                    */
/*----------------------------------------------------------------------------*/
static void pmic_init(void)
{
    #ifndef EMUL
        static sc_bool_t pmic_checked = SC_FALSE;
        static lpi2c_master_config_t lpi2c_masterConfig;
        sc_pm_clock_rate_t rate = SC_24MHZ;
        /* See if we already checked for the PMIC */
        if (pmic_checked == SC_FALSE)
        {
            sc_err_t err = SC_ERR_NONE;
            pmic_checked = SC_TRUE;
            /* Initialize the PMIC */
            board_print(3, "Start PMIC init\n");
            /* Power up the I2C and configure clocks */
            pm_force_resource_power_mode_v(SC_R_SC_I2C,
                SC_PM_PW_MODE_ON);
            (void) pm_set_clock_rate(SC_PT, SC_R_SC_I2C,
                SC_PM_CLK_PER, &rate);
            pm_force_clock_enable(SC_R_SC_I2C, SC_PM_CLK_PER,
                SC_TRUE);
            /* Initialize the pads used to communicate with the PMIC */
            pad_force_mux(SC_P_PMIC_I2C_SDA, 0,
                SC_PAD_CONFIG_OD_IN, SC_PAD_ISO_OFF);
            (void) pad_set_gp_28fdsoi(SC_PT, SC_P_PMIC_I2C_SDA,
                SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
            pad_force_mux(SC_P_PMIC_I2C_SCL, 0,
                SC_PAD_CONFIG_OD_IN, SC_PAD_ISO_OFF);
            (void) pad_set_gp_28fdsoi(SC_PT, SC_P_PMIC_I2C_SCL,
                SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
            /* Initialize the PMIC interrupt pad */
            pad_force_mux(SC_P_PMIC_INT_B, 0,
                SC_PAD_CONFIG_NORMAL, SC_PAD_ISO_OFF);
            (void) pad_set_gp_28fdsoi(SC_PT, SC_P_PMIC_INT_B,
                SC_PAD_28FDSOI_DSE_18V_1MA, SC_PAD_28FDSOI_PS_PU);
            /* Initialize the I2C used to communicate with the PMIC */
            LPI2C_MasterGetDefaultConfig(&lpi2c_masterConfig);
            /* MEK board spec is for 1M baud for PMIC I2C bus */
            lpi2c_masterConfig.baudRate_Hz = 1000000U;
            lpi2c_masterConfig.sdaGlitchFilterWidth_ns = 100U;
            lpi2c_masterConfig.sclGlitchFilterWidth_ns = 100U;
            LPI2C_MasterInit(LPI2C_PMIC, &lpi2c_masterConfig, SC_24MHZ);
            /* Delay to allow I2C to settle */
            SystemTimeDelay(2U);
            pmic_ver = GET_PMIC_VERSION(PMIC_0_ADDR);
            temp_alarm0 = SET_PMIC_TEMP_ALARM(PMIC_0_ADDR, PMIC_TEMP_MAX);
            temp_alarm1 = SET_PMIC_TEMP_ALARM(PMIC_1_ADDR, PMIC_TEMP_MAX);
            err |= pmic_ignore_current_limit(PMIC_0_ADDR);
            err |= pmic_ignore_current_limit(PMIC_1_ADDR);
            /* Adjust startup timing */
            err |= pmic_update_timing(PMIC_0_ADDR);
            err |= pmic_update_timing(PMIC_1_ADDR);
            err |= pmic_match_otp(PMIC_0_ADDR, pmic_ver);
            err |= pmic_match_otp(PMIC_1_ADDR, pmic_ver);
            /* Enable WDI detection in Standby */
            err |= pf8100_pmic_wdog_enable(PMIC_0_ADDR, SC_FALSE, SC_FALSE, SC_TRUE);
            err |= pf8100_pmic_wdog_enable(PMIC_1_ADDR, SC_FALSE, SC_FALSE, SC_TRUE);
            if (err != SC_ERR_NONE)
            {
                /* Loop so WDOG will expire */
                HALT;
            }
            BRD_ERR(PMIC_SET_MODE(PMIC_0_ADDR, PF8100_SW1, SW_RUN_PWM
                | SW_STBY_PWM));
            BRD_ERR(PMIC_SET_MODE(PMIC_0_ADDR, PF8100_SW2, SW_RUN_PWM
                | SW_STBY_PWM));
            BRD_ERR(PMIC_SET_MODE(PMIC_0_ADDR, PF8100_SW7, SW_RUN_PWM
                | SW_STBY_PWM));
            /* Configure STBY voltage for SW1 (VDD_MAIN) */
            if (board_parameter(BOARD_PARM_KS1_RETENTION)
                == BOARD_PARM_KS1_RETENTION_ENABLE)
            {
```

```
                BRD_ERR(PMIC_SET_VOLTAGE(PMIC_0_ADDR, PF8100_SW1, 800,
                    REG_STBY_MODE));
            }
            /* Enable PMIC IRQ at NVIC level */
            NVIC_EnableIRQ(PMIC_INT_IRQn);
            board_print(3, "Finished  PMIC init\n\n");
        }
    #endif
}
/*------------------------------------------------------------------------*/
/* Bypass current limit for PF8100                                        */
/*------------------------------------------------------------------------*/
static sc_err_t pmic_ignore_current_limit(uint8_t address)
{
    sc_err_t err = SC_ERR_NONE;
    uint8_t idx;
    uint8_t val = 0U;
    static const pf8100_vregs_t switchers[11] =
    {
        PF8100_SW1,
        PF8100_SW2,
        PF8100_SW3,
        PF8100_SW4,
        PF8100_SW5,
        PF8100_SW6,
        PF8100_SW7,
        PF8100_LDO1,
        PF8100_LDO2,
        PF8100_LDO3,
        PF8100_LDO4
    };
    for (idx = 0U; idx < 11U; idx++)
    {
        /* Read the config register first */
        err = PMIC_REGISTER_ACCESS(address, switchers[idx], SC_FALSE,
            &val);
        if (err == SC_ERR_NONE)
        {
            val |= 0x20U; /* set xx_ILIM_BYPASS */
            /*
             * Enable the UV_BYPASS and OV_BYPASS for all LDOs.
             * The SDHC LDO2 constantly switches between 3.3V and 1.8V and
             * the counters are incorrectly triggered.
             * Also any other LDOs (like LDO1 on the board) that is
             * enabled/disabled during suspend/resume can trigger the counters.
             */
             if ((switchers[idx] == PF8100_LDO1) ||
                 (switchers[idx] == PF8100_LDO2) ||
                 (switchers[idx] == PF8100_LDO3) ||
                 (switchers[idx] == PF8100_LDO4))
            {
                val |= 0xC0U;
            }
            err = PMIC_REGISTER_ACCESS(address, switchers[idx], SC_TRUE,
                &val);
        }
        if (err != SC_ERR_NONE)
        {
            break;
        }
    }
    return err;
}
/*------------------------------------------------------------------------*/
/* Update power timing for PF8100                                         */
/*------------------------------------------------------------------------*/
static sc_err_t pmic_update_timing(uint8_t address)
{
    sc_err_t err = SC_ERR_NONE;
    uint8_t val = 0xED;
    /*
     * Add 60ms stable time for power down for:
     *   PMIC 1 : LDO2, SW6, SW7
     *   PMIC 2 : LDO2, SW5, SW6, SW7
     * on i.mx8QM-mek
     * board, otherwise system may reboot fail by mmc not power off
     * clean
     */
    if (address == PMIC_0_ADDR)
    {
        err |= PMIC_REGISTER_ACCESS(address, 0x8D, SC_TRUE, &val);
```

```
        err |= PMIC_REGISTER_ACCESS(address, 0x77, SC_TRUE, &val);
        err |= PMIC_REGISTER_ACCESS(address, 0x7F, SC_TRUE, &val);
        val = 0x29;
        err |= PMIC_REGISTER_ACCESS(address, 0x3C, SC_TRUE, &val);
    }
    else if (address == PMIC_1_ADDR)
    {
        err |= PMIC_REGISTER_ACCESS(address, 0x8D, SC_TRUE, &val);
        err |= PMIC_REGISTER_ACCESS(address, 0x6F, SC_TRUE, &val);
        err |= PMIC_REGISTER_ACCESS(address, 0x77, SC_TRUE, &val);
        err |= PMIC_REGISTER_ACCESS(address, 0x7F, SC_TRUE, &val);
        val = 0x29;
        err |= PMIC_REGISTER_ACCESS(address, 0x3C, SC_TRUE, &val);
    }
    else
    {
        err = SC_ERR_PARM;
    }
    return err;
}
/*------------------------------------------------------------------------*/
/* Check correct version of OTP for PF8100                                */
/*------------------------------------------------------------------------*/
static sc_err_t pmic_match_otp(uint8_t address, pmic_version_t ver)
{
    uint8_t reg_value = 0U;
    uint16_t prog_id, match;
    sc_err_t err = SC_ERR_NONE;
    if (address == PMIC_0_ADDR)
    {
        match = EP_PROG_ID;
    }
    else
    {
        match = EQ_PROG_ID;
    }
    /* Read Prog ID */
    err |= PMIC_REGISTER_ACCESS(address, 0x2, SC_FALSE, &reg_value);
    prog_id = (((uint16_t)reg_value « 4U) & 0x0F00U);
    err |= PMIC_REGISTER_ACCESS(address, 0x3, SC_FALSE, &reg_value);
    prog_id |= reg_value;
    /* test against calibration fusing */
    if (OTP_PROG_FUSE_VERSION_1_7V_CAL != 0U)
    {
        if (ver.si_rev >= PF8100_C1_SI_REV)
        {
            /* if C1 PMIC test for correct OTP */
            if(prog_id != match){/* allow only 1.7v OTP */
                error_print("PMIC INVALID!\n");
            }
        }
        else
        {
            error_print("PMIC INVALID!\n");
        }
    }
    else
    {
        if (ver.si_rev >= PF8100_C1_SI_REV)
        {
            if(prog_id == match){/* prohibit only 1.7V OTP */
                error_print("PMIC INVALID!\n");
            }
        }
    }
    return err;
}
/*------------------------------------------------------------------------*/
/* Get the pmic ids and switchers connected to SS.                        */
/*------------------------------------------------------------------------*/
static void board_get_pmic_info(sc_sub_t ss,pmic_id_t *pmic_id,
    uint32_t *pmic_reg, uint8_t *num_regs)
{
    /* Map SS/PD to PMIC switch */
    switch (ss)
    {
        case SC_SUBSYS_A53 :
            pmic_init();
            {/* PF8100_dual Card */
                pmic_id[0] = PMIC_0_ADDR;
                pmic_reg[0] = PF8100_SW5;
```

```
                *num_regs = 1U;
            }
            break;
        case SC_SUBSYS_A72 :
            pmic_init();
            {/* PF8100_dual Card */
                pmic_id[0] = PMIC_0_ADDR;
                pmic_reg[0] = PF8100_SW3;
                pmic_id[1] = PMIC_0_ADDR;
                pmic_reg[1] = PF8100_SW4;
                *num_regs = 2U;
            }
            break;
        case SC_SUBSYS_GPU_0 :
            pmic_init();
            {/* PF8100_dual Card */
                pmic_id[0] = PMIC_1_ADDR;
                pmic_reg[0] = PF8100_SW1;
                pmic_id[1] = PMIC_1_ADDR;
                pmic_reg[1] = PF8100_SW2;
                *num_regs = 2U;
            }
            break;
        case SC_SUBSYS_GPU_1 :
            pmic_init();
            {/* PF8100_dual Card */
                pmic_id[0] = PMIC_1_ADDR;
                pmic_reg[0] = PF8100_SW3;
                pmic_id[1] = PMIC_1_ADDR;
                pmic_reg[1] = PF8100_SW4;
                *num_regs = 2U;
            }
            break;
        default :
            ; /* Intentional empty default */
            break;
    }
}
/*------------------------------------------------------------------------*/
/* Board tick                                                             */
/*------------------------------------------------------------------------*/
void board_tick(uint16_t msec)
{
}
/*------------------------------------------------------------------------*/
/* Board IOCTL function                                                   */
/*------------------------------------------------------------------------*/
sc_err_t board_ioctl(sc_rm_pt_t caller_pt, sc_rsrc_t mu, uint32_t *parm1,
    uint32_t *parm2, uint32_t *parm3)
{
    sc_err_t err = SC_ERR_NONE;
    /* For test_misc */
    if (*parm1 == 0xFFFFFFFEU)
    {
        *parm1 = *parm2 + *parm3;
        *parm2 = mu;
        *parm3 = caller_pt;
    }
    else
    {
        err = SC_ERR_PARM;
    }
    return err;
}

/**@}*/
```

Index