System Controller Firmware Release Notes

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Chapter 1

Introduction

This document contains release notes for the i.MX8 System Controller Firmware (SCFW). This includes:

- Highlights
- Changes from the previous release
- Known issues
- Additional info

The table below lists the release information:

Release Info	
Release name	imx_scfw_2020q2_p1
Previous release	imx_scfw_2020q2
Branch	imx_scfw_2020q2
Build number	4612
Commit ID	732e719a
Build date	Jun 19 2020
API Version	1.21
Supported devices	i.MX8QM (B0), i.MX8QXP (B0), i.MX8QXP (C0), i.MX8DXL (A0), and phantoms

1.1 Highlights

- Various enhancements for DXL (DB/fabric auto clock gating, PCIe spread spectrum support, etc.)
- Support for fine tuning the audio PLL rate
- Many bug fixes

Note SECO firmware version 3.6.2+ is **REQUIRED** for correct operation! For DXL, the required version is 0.6.3.

This release **breaks RPC backwards compatibility** for the sc_rm_is_pad_owned() function. The call may not return an error even though the pad width has been corrected to 16-bits and using an older SCFW client API may result in the 8-bit pad being used as the upper nibble of the new 16-bit pad. The client-side SCFW API **must** be updated to match this change.

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Chapter 2

Change List

2.1 SCFW 2020Q2 Patch 1 Change List

Below is a list of changes between the previous release (imx_scfw_2020q2) and this release (imx_scfw_2020q2_p1).

2.1.1 Bug

Key	Summary	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-628	Add control to enable MLB bandgap reference [detail]	Y			
SCF-633	Deleting a memory region can result in a temporary invalid access control configuration	Y	Y	Y	Y
SCF-636	Board resource availability check mapped incorrectly	Y	Y	Y	Y
SCF-637	Fix out-of-bound memory access in iMX8QM GPU code.	Y			
SCF-638	Fix rsrc_clks monitor command	Y	Y	Y	Y
SCF-639	sc_misc_get_control() incorrectly returns error for some connectivity resources	Y			

2.2 Prior SCFW 2020Q2 Change List

Below is a list of changes between the previous release (imx_scfw_2020q1) and this release (imx_scfw_2020q2).

2.2.1 New Feature

Key	Summary	Patch	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-511	Add debug monitor command to dump clock config options [detail]		Y	Y	Y	Y
SCF-560	Add spread spectrum support for PCIe [detail]					Y
SCF-585	Add DXL DDR3L DCD					Y
SCF-602	Add API to configure memory region IEE parameters [detail]		Y	Y	Y	Y
SCF-604	Add test for measuring the OSC 24MHz locking time [detail]		Y	Y	Y	Y
SCF-611	Support temperature grade fusing	p1		Y	Y	
SCF-617	Add support for fine tuning the audio PLL rate [detail]		Y	Y	Y	Y
SCF-620	Support SECO FW version 0.6.3 for i.MX8DXL					Y

2.2.2 Improvement

Key	Summary	Patch	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-554	Improve MSI reset workaround		Y	Y	Y	
SCF-581	Support V2X disable by fuse					Y
SCF-603	Enable DB auto clock gating on i.MX8DXL					Y
SCF-610	Update to latest MCU SDK		Y	Y	Y	Y
SCF-616	Refactor i.MX8QM GPU clock code		Y			
SCF-622	Remove redundant code that re-enables LPDDR4 CA_ODT in ddr_exit_retention()		Y	Y	Y	Y

2.2.3 Bug

Key	Summary	Patch	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-579	Ensure second M4 instance follows the CORE to IPG clock ratio	p1	Y			
SCF-580	Several CPU PM related functions not bound to only the CPU (M4 related) resource [detail]	p1	Y	Y	Y	Y
SCF-582	Initialize VDD_MEMC usage count for SCFW unit test [detail]	p1				Y
SCF-583	Add missing i.MX8DXL LPDDR4 ECC defines	p1				Y
SCF-584	i.MX8DXL EVK board bus expander reset controls incorrect [detail]	p1				Y
SCF-586	Out-of-bounds memory access when calling functions with invalid clock	p1	Y	Y	Y	Y
SCF-599	FIPS fuse not correctly used	p1	Y	Y	Y	Y

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Key	Summary	Patch	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-600	RTC alarm wakeup from KS0 is not reliable	p1			Y	Y
SCF-601	Duplicate fabric and V2X init when DB transitions from/to OFF mode	p1				Y
SCF-608	Move FLEXCAN0 and 1 signals to AP as used for SAI [detail]	p1				Y
SCF-609	Debug attach with firmware-only image (flash_scfw) fails	p1	Y	Y	Y	Y
SCF-613	Initialize bypass clock rates correctly		Y	Y	Y	Y
SCF-614	Out-of-bounds array access on ROM SS state check in debug build	p1	Y	Y	Y	Y
SCF-618	Fix DDR DQ mapping issue for 8QXP/DX 17x17 LPDDR4 validation board	p2		Y	Y	
SCF-621	Incorrect pad width in sc_rm_is_pad_owned() RPC implementation [detail]		Y	Y	Y	Y
SCF-623	Enable MLB PLL regulator on i.MX8QX	p2		Y	Y	
SCF-626	Ensure M4 clock rate is equal to or below requested rate	p2	Y	Y	Y	Y

2.2.4 Silicon Workaround

These are a mix of silicon errata workarounds and recommended usage changes.

Key	Summary	Patch	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-607	Support SECO FW version 3.6.2	p1	Y	Y	Y	

2.2.5 Documentation

Key	Summary	Patch	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-89	Add documentation of definition of power modes		Y	Y	Y	Y

2.3 Details

This section provides details for select changes.

2.3.1 SCF-511: Add debug monitor command to dump clock config options

New debug monitor dump command:

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dump rsrc_clks [resource id]

will dump the following clock related information of the given resource:

- Clock rate
- Clock is enabled/disabled
- Maximum clock divider
- Current parent_rate
- Current parent (for some clocks)
- Possible parent options (for some clocks)

2.3.2 SCF-560: Add spread spectrum support for PCIe

If BOARD_PARM_RTN_INTERNAL_DPLL is selected as the clock source for PCIe (BOARD_PARM_PCIE_PLL), spread spectrum can be enabled for the PCIe clock via board parameter BOARD_PARM_PCIE_DPLL_SS.

The following values are valid for BOARD_PARM_PCIE_DPLL_SS, DPLL frequency is fixed at 720MHz :

- BOARD_PARM_RTN_DPLL_SS_0_5 => 0.5% spread of PCIE DPLL frequency
- BOARD_PARM_RTN_DPLL_SS_1 => 1% spread of PCIE DPLL frequency
- BOARD_PARM_RTN_DPLL_SS_1_5 => 1.5% spread of PCIE DPLL frequency
- BOARD_PARM_RTN_DPLL_SS_2 => 2% spread of PCIE DPLL frequency

2.3.3 SCF-580: Several CPU PM related functions not bound to only the CPU (M4 related) resource

This change fixes an issue with API calling parameters (parameter bounding). Three PM functions that expect a CPU resource could also be called with non-CPU resources.

- sc_pm_req_sys_if_power_mode()
- sc_pm_set_cpu_resume_addr()
- sc_pm_set_cpu_resume()

This issue is limited to resources in the M4 subsystem. So an owner of a non-CPU resource in an M4 subsystem can call and it will affect the associated M4 CPU resource, even if these resources have different owning partitions. After this change, only CPU resources can be used as originally intended.

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2.3.4 SCF-582: Initialize VDD_MEMC usage count for SCFW unit test

This issue only affects SCFW unit test execution.

2.3.5 SCF-584: i.MX8DXL EVK board bus expander reset controls incorrect

This issue only affects the board.c implementation for the NXP EVK board.

2.3.6 SCF-602: Add API to configure memory region IEE parameters

Added RM service function:

- sc_rm_set_memreg_iee()

This allows configuration of the det and rmsg signals that are driven to the IEE for a specific memory region.

SCFW API version increased to 1.20.

2.3.7 SCF-604: Add test for measuring the OSC 24MHz locking time

This test helps measure the 24MHz XTAL lock time on boards. It can help understand the effect of CL_TUNE parameter on XTAL locking time. Default CL_TUNE is 20pF. Build it as a standalone test T=osc24trim.

2.3.8 SCF-608: Move FLEXCAN0 and 1 signals to AP as used for SAI

This issue only affects the board.c implementation for the NXP EVK board.

2.3.9 SCF-617: Add support for fine tuning the audio PLL rate

Add support for on-the-fly fine tuning of user defined Audio PLLs (SC_R_AUDIO_PLL_0 and SC_R_AUDIO_PLL_1). The fine-tuning range is +/-250KHz.

2.3.10 SCF-621: Incorrect pad width in sc_rm_is_pad_owned() RPC implementation

Fixing this issue requires a change in the width of the pad field in the RPC protocol. This means this change breaks backwards compatibility! Updating to this SCFW requires the SCFW client API also be updated.

SCFW API version updated to 1.21.

2.3.11 SCF-628: Add control to enable MLB bandgap reference

MLB bandgap reference voltage needs to be enabled for 6-pin mode. A new SCFW control (SC_C_VOLTAGE) has been added to the MLB_0 resource which can be used to enable/disable the bandgap.

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Chapter 3

Known Issues

Below is a list of known outstanding issues in this release (imx_scfw_2020q2).

3.1 New Feature

Key	Summary	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-543	Add V2X power management				Y
SCF-619	Support i.MX8DXL A1				

3.2 Improvement

Key	Summary	QM (B0)	QXP (B0)	QXP (C0)	DXL (A0)
SCF-624	Refactor OSC 24MHz test to make more reusable	Y	Y	Y	Y
SCF-625	V2X incorrectly powers off when running SCFW unit tests				Y
SCF-629	Support memory probing and utilize during MM and MD monitor commands	Y	Y	Y	Y
SCF-632	Avoid unnecessary M4 landing zone configuration	Y	Y	Y	Y

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Chapter 4

Additional Notes

This section details any additional notes about the original release. These do not cover changes in patch releases.

4.1 General

When the SCFW is compiled for release into production devices, it is critical that this is done without debug (default is debug enabled, D=1) and without the debug monitor (default is no monitor, M=0). For example:

```
make qm R=B0 D=0 M=0
```

Turning off debug will eliminate the linking of the standard C library. See the porting guide for more information.

The porting kit contains separate tar files for each SoC/version combination. These can be combined using the following command:

```
find scfw_export_mx8*.gz -exec tar --strip-components 1 --one-top-level=scfw_export_mx8 -xzvf {} \;
```

Note i.MX8QXP B0 and C0 use the same code so the only source tarball is for B0. Also, binaries created for i.MX8QXP are run-time compatible to both silicon versions so always build with R=B0.

The tool chain used with this SCFW is 9-2019-q4-major obtained from here.

4.2 SCFW API Changes

The client API is backwards compatible at the compile-time API level. It is **NOT** compatible at the RPC/IPC level. The sc_rm_is_pad_owned() function had an incorrect pad width and that has been corrected. The call will not fail but the pad width has been changed to 16-bits and using an older SCFW client API may result in the 8-bit pad being used as the upper nibble of the new 16-bit pad.

4.2.1 Interrupt (IRQ) Service

None

4.2.2 Miscellaneous (MISC) Service Changes

None

4.2.3 Pad Service Changes

None

4.2.4 Power Management (PM) Service

Some functions have increased error checking:

- sc_pm_req_sys_if_power_mode()
- sc_pm_set_cpu_resume_addr()
- sc_pm_set_cpu_resume()

4.2.5 Resource Management (RM) Service

This release breaks backwards compatibility for the sc_rm_is_pad_owned() function. The call will not fail but the pad width has been corrected to 16-bits and using an older SCFW client API may result in the 8-bit pad being used as the upper nibble of the new 16-bit pad.

New function added:

- sc_rm_set_memreg_iee()

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4.2.6 SECO Service Changes

None

4.2.7 Timer Service Changes

None

4.3 Resource Changes

None

4.4 Clock Changes

None

4.5 Control Changes

None

4.6 Board Interface Changes

Added board parameter for PCIe PLL SS support:

- BOARD_PARM_PCIE_DPLL_SS

which can return:

- BOARD_PARM_RTN_DPLL_SS_0_5
- BOARD_PARM_RTN_DPLL_SS_1
- BOARD_PARM_RTN_DPLL_SS_1_5
- BOARD_PARM_RTN_DPLL_SS_2

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Chapter 5

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