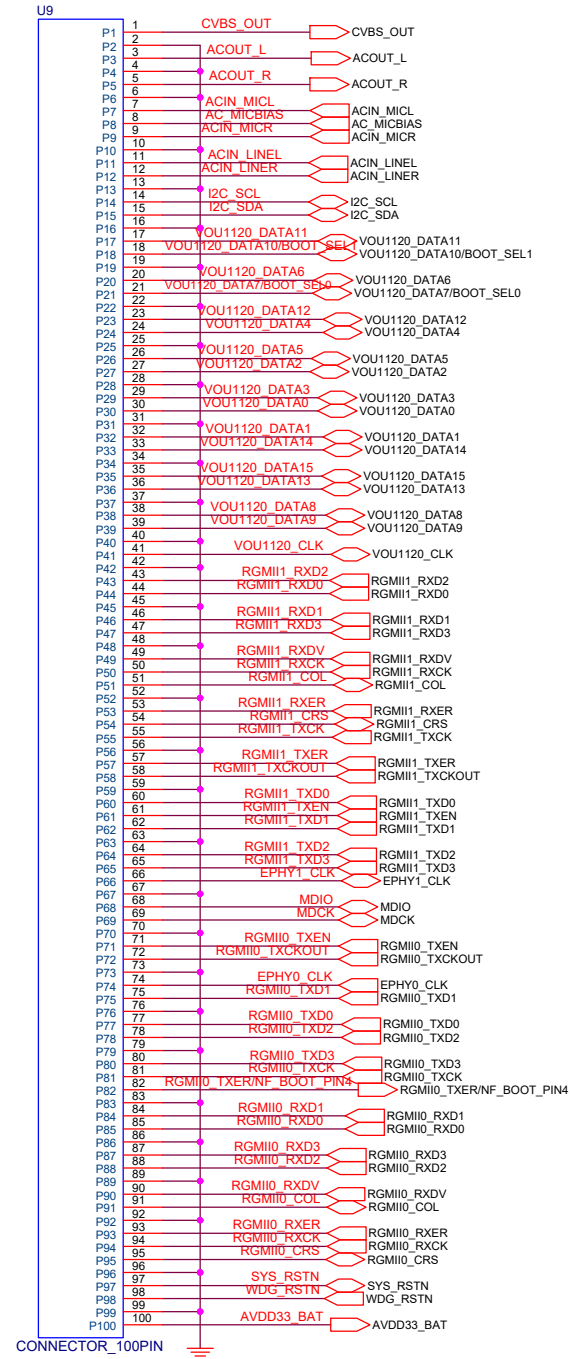
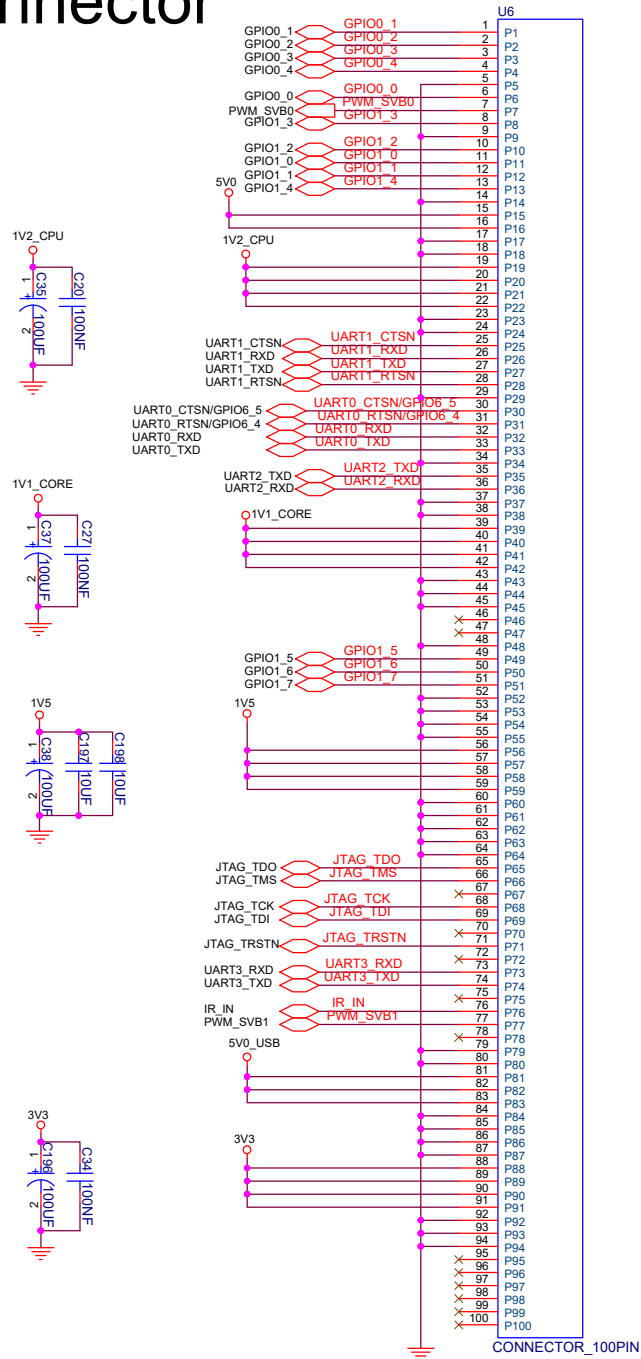
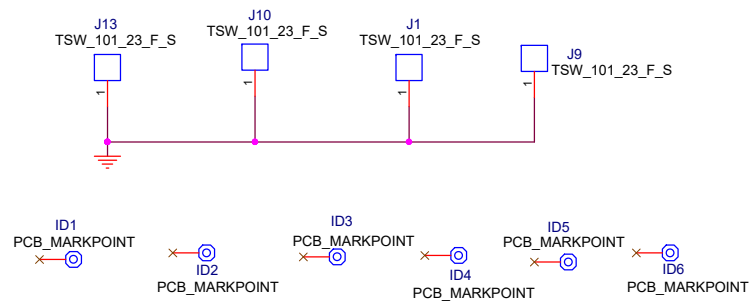
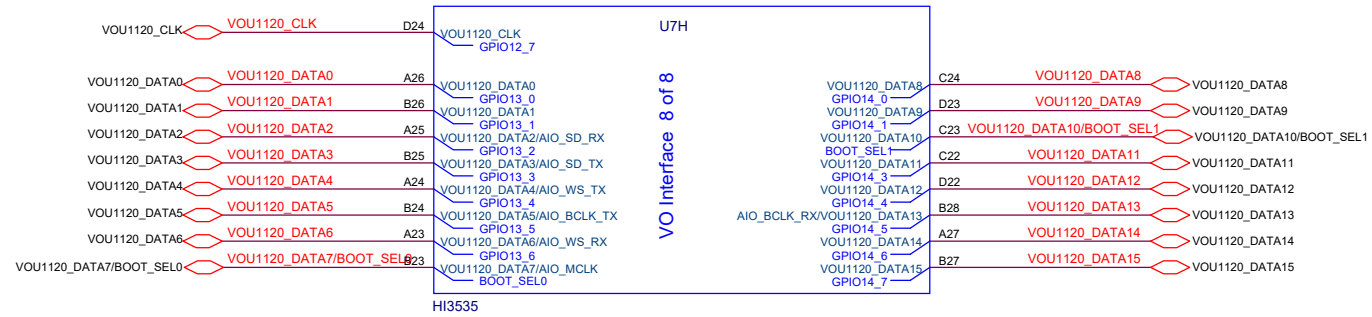


Connector

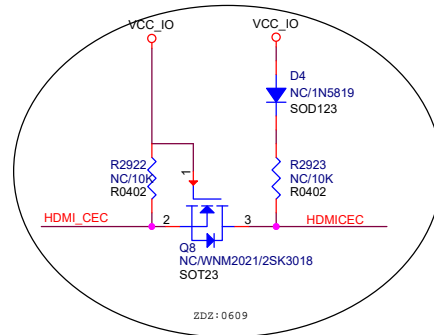
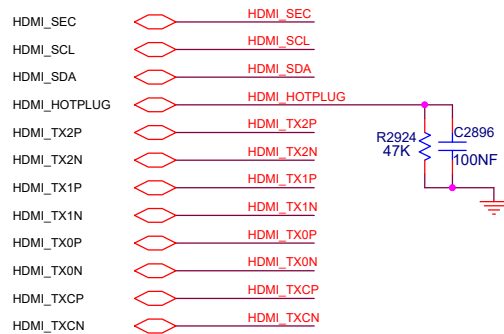


VO

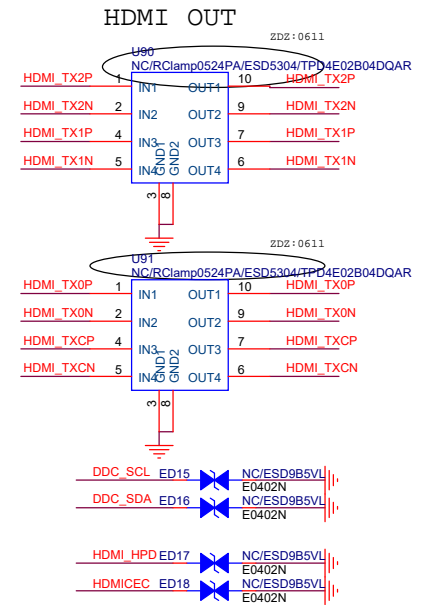
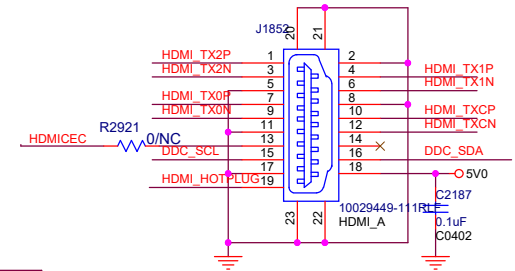
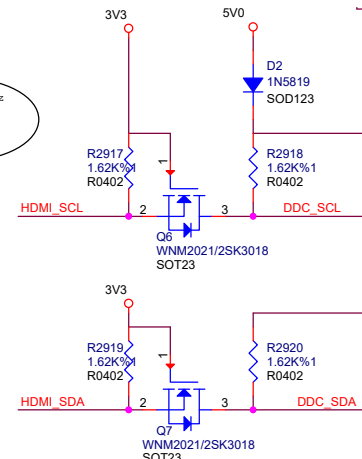


HDMI

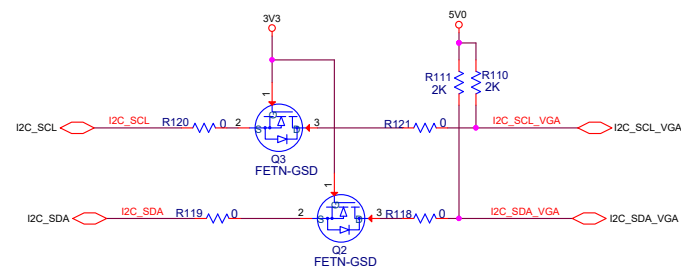
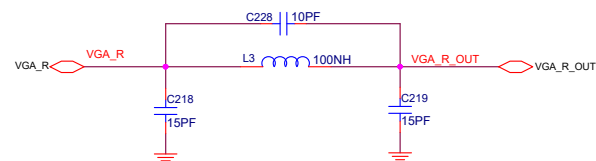
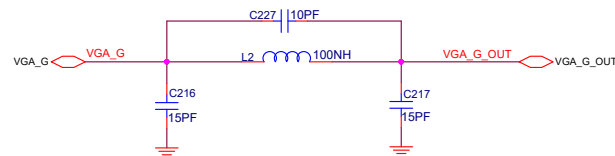
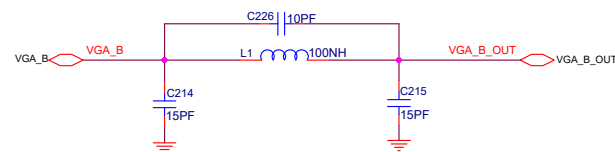
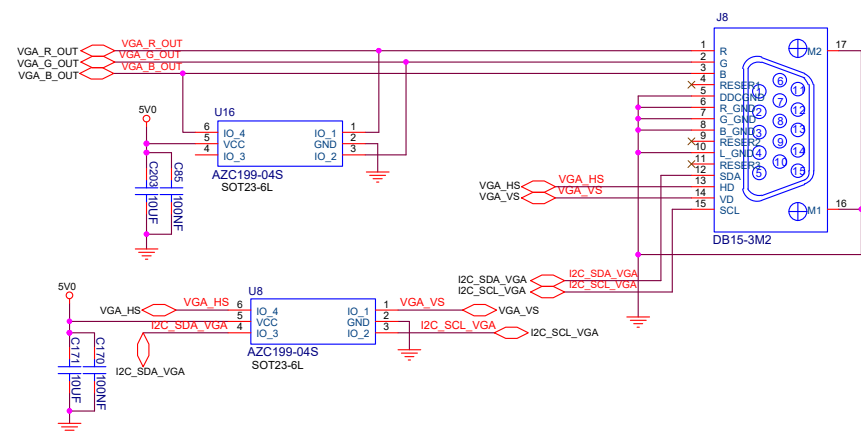
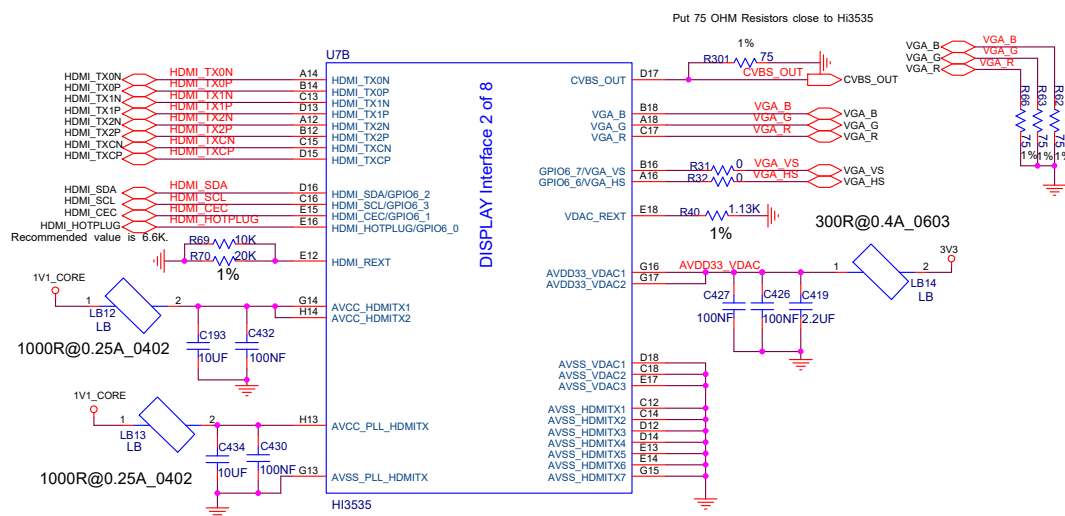
The HDMI differential trace impedance is 100 OHM.
The HDMI trace length is less than 5 inch.



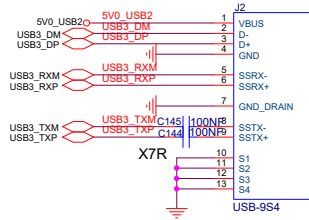
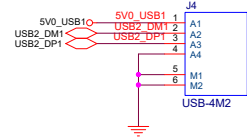
04.22 zdz



DISPLAY

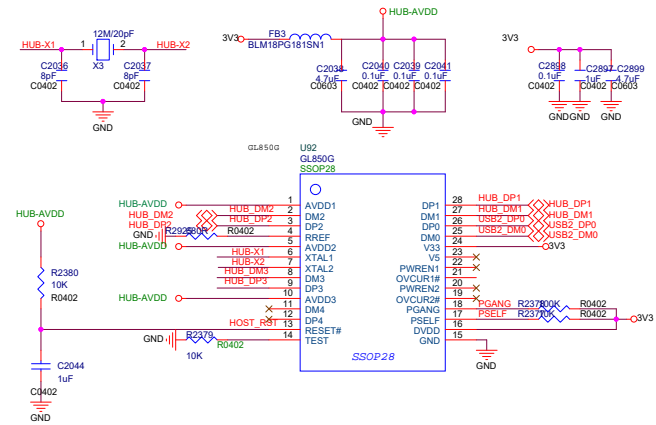


The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

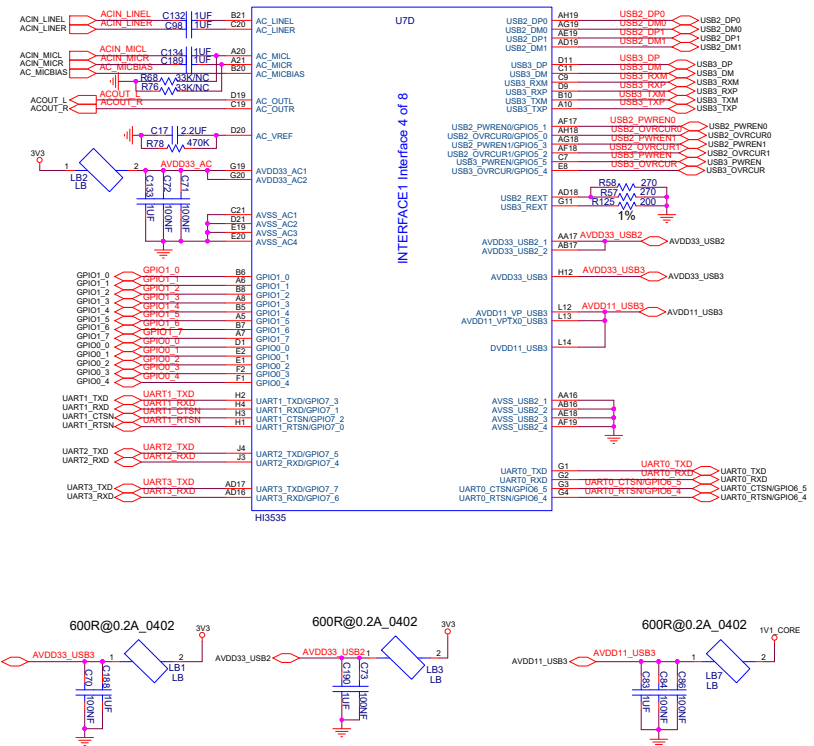
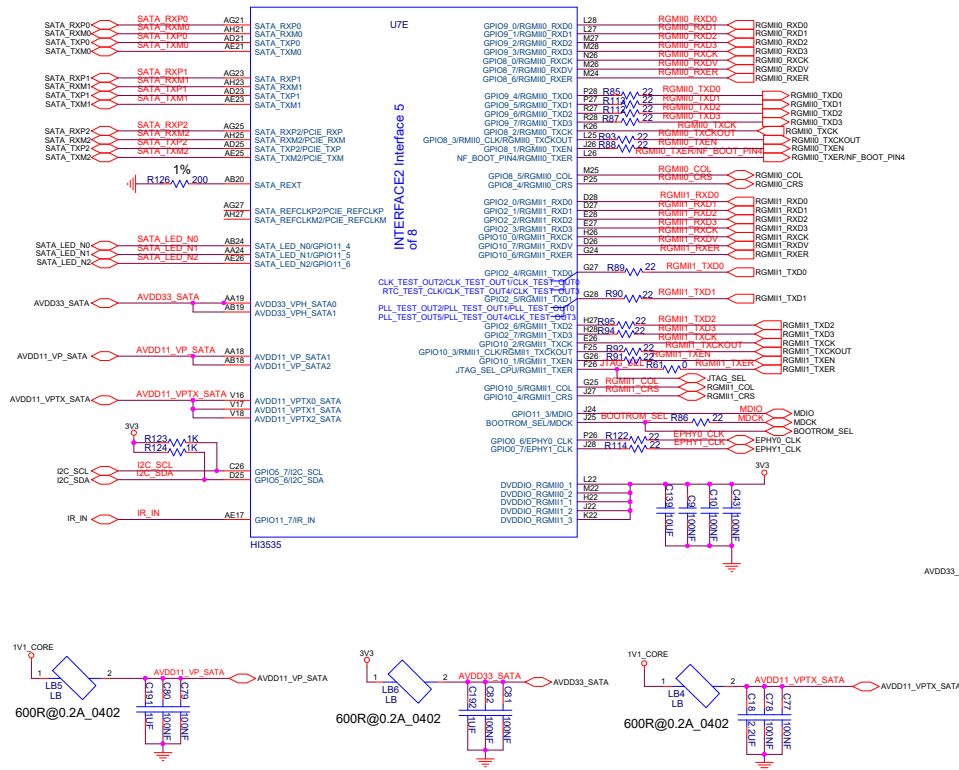


SATA3.0 Port0

USB HUB



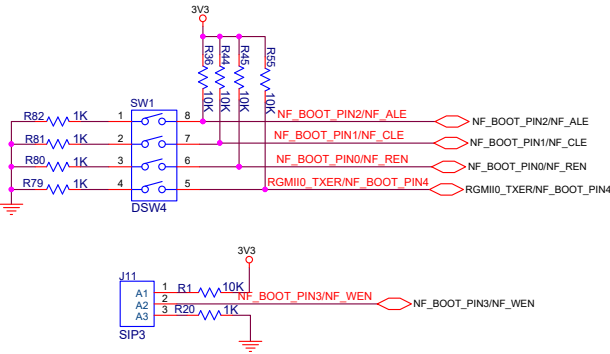
Interface



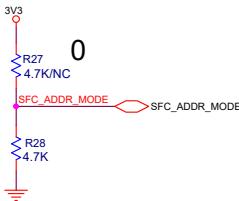
Power on setting pins

NF_BOOT_PIN[4:0]

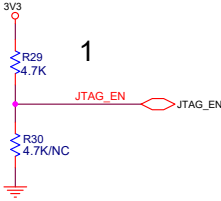
- 00011 2k page size,4bit ecc,64page/block,5addr
- 00100 4k page size,24bit ecc,256page/block,5addr
- 00101 2k page size,24bit ecc,64page/block,5addr
- 00111 8k page size,24bit ecc,256page/block,5addr
- 01000 4k page size,4bit ecc,128page/block,5addr
- 01001 4k page size,4bit ecc,64page/block,5addr
- 01010 2k page size,4bit ecc,64page/block,4addr
- 01011 4k page size,24bit ecc,128page/block,5addr
- 01101 8k page size,24bit ecc,128page/block,5addr
- 10000 8k page size,24bit ecc,64page/block,5addr
- 10001 4k page size,24bit ecc,64page/block,5addr
- 10101 2k page size,4bit ecc,128page/block,5addr
- 10110 2k page size,8bit ecc,128page/block,5addr
- 11001 2k page size,24bit ecc,128page/block,5addr
- 11010 2k page size,8bit ecc,64page/block,5addr
- 11110 4k page size,8bit ecc,64page/block,5addr
- 11111 4k page size,8bit ecc,128page/block,5addr



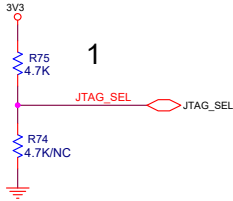
SFC_ADDR_MODE	
0	3 Byte mode
1	4 Byte mode



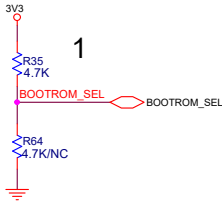
JTAG_EN	
0	Disable JTAG
1	Enable JTAG



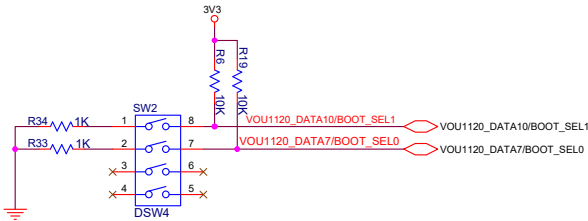
JTAG_SEL	
0	Other
1	CPU



BOOTROM_SEL	
0	Boot from BOOT_SEL
1	Boot from Bootrom

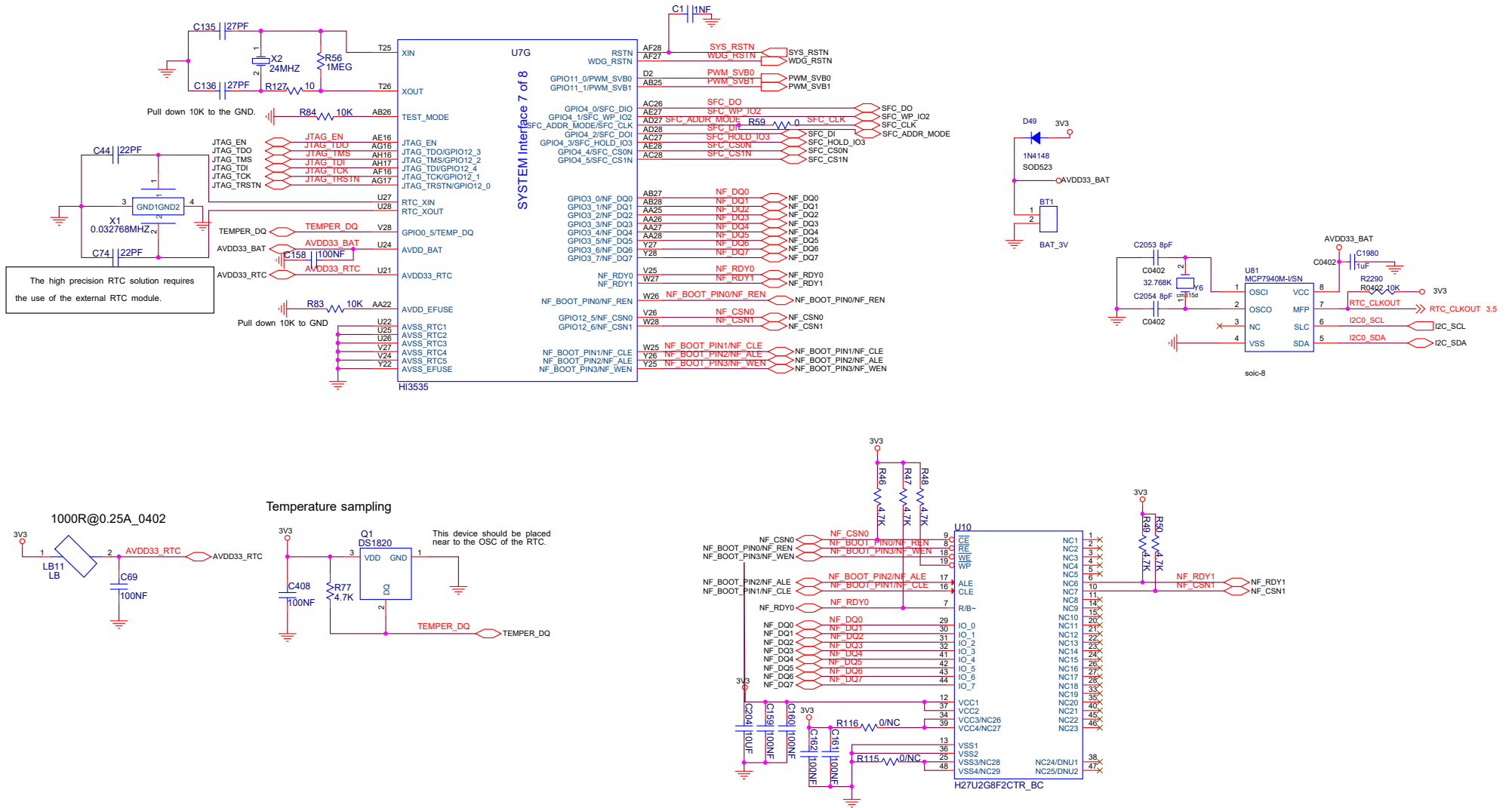


BOOT_SEL[1:0]	
00	SPI FLASH
01	DDR
10	NAND FLASH
11	Reserve



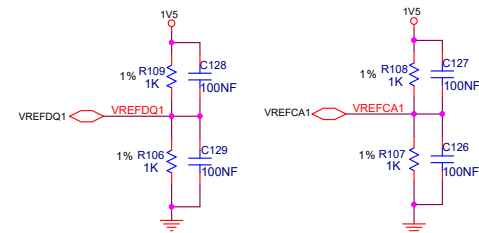
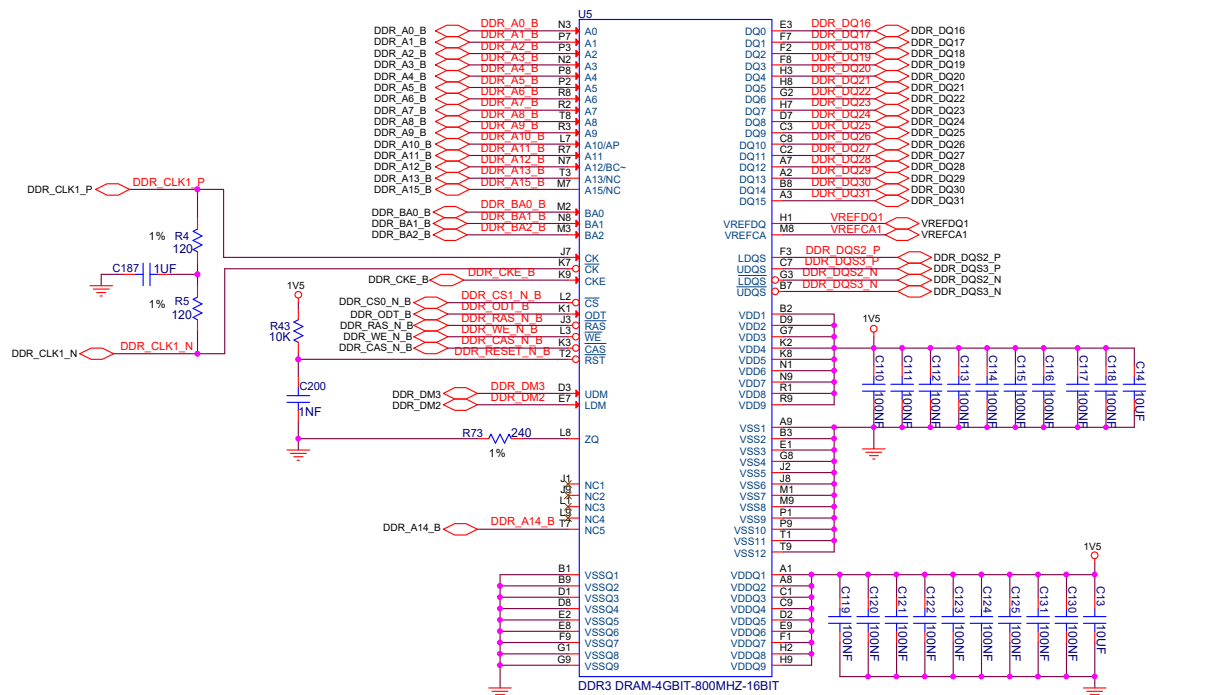
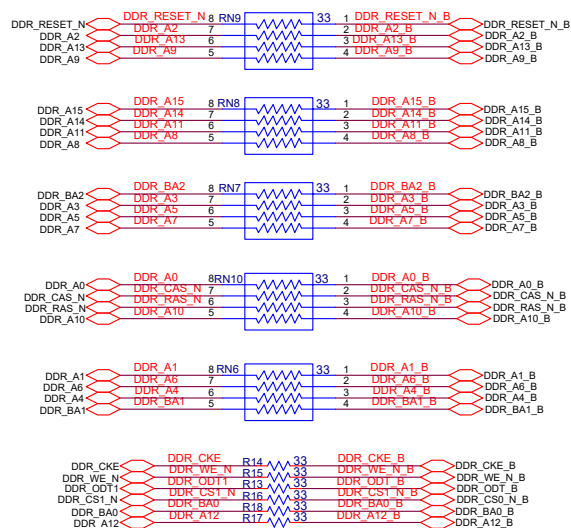
SYSTEM & FLASH

Put this cap close to the Hi3535.



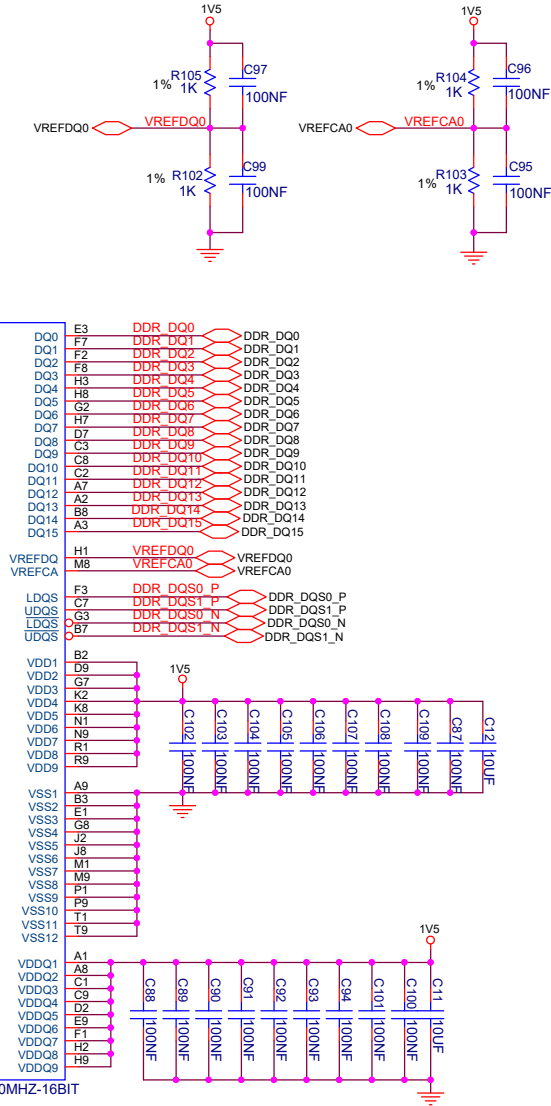
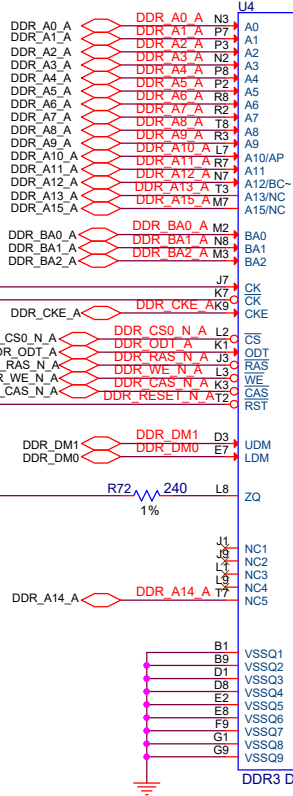
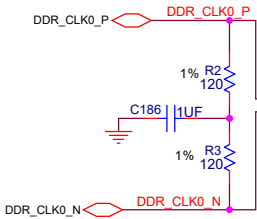
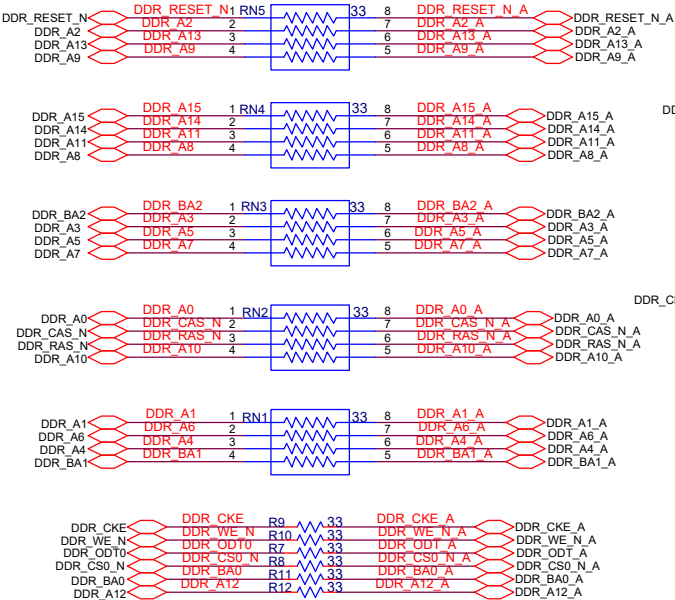
DDR3 B

The routing design of the DDR must be the same as that for the Hi3535 demo board.

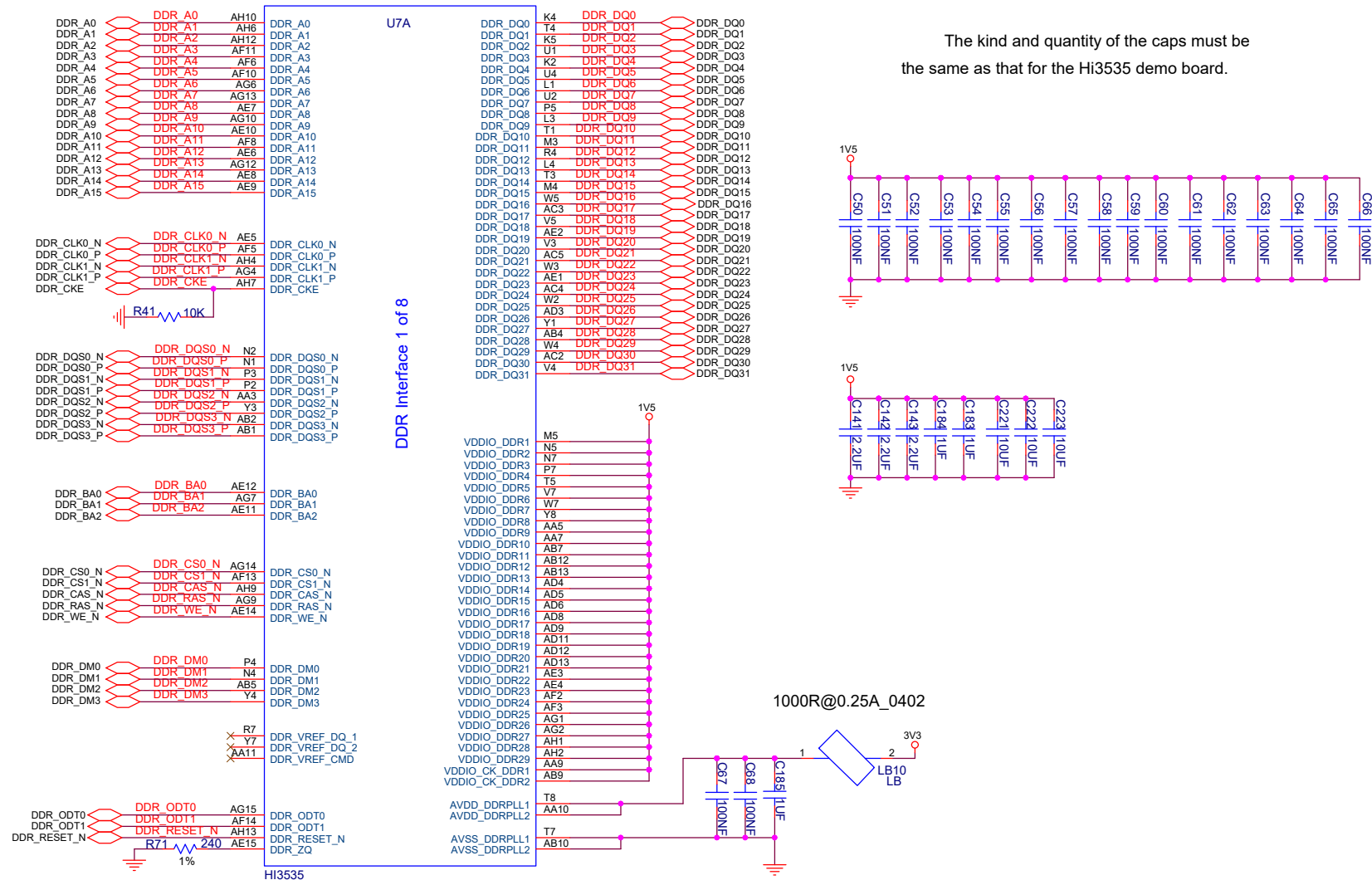


DDR3_A

The routing design of the DDR must be the same as that for the Hi3535 demo board.

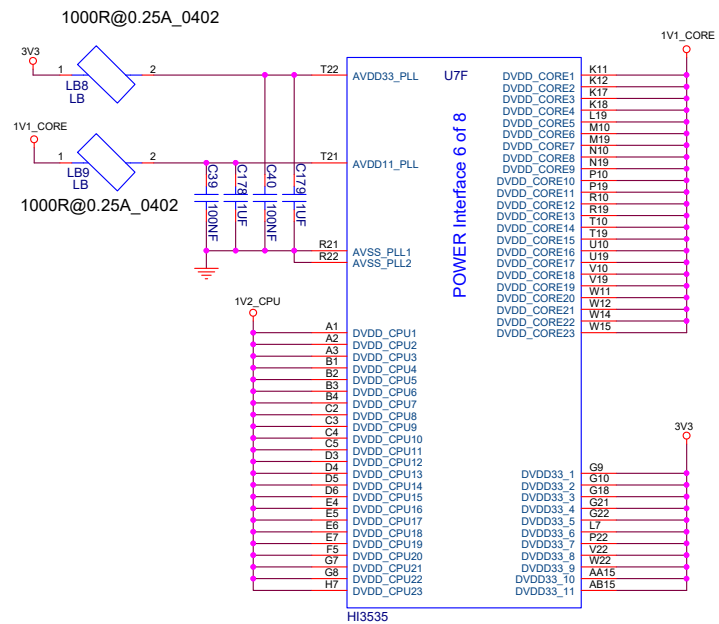


HI3535 DDR3

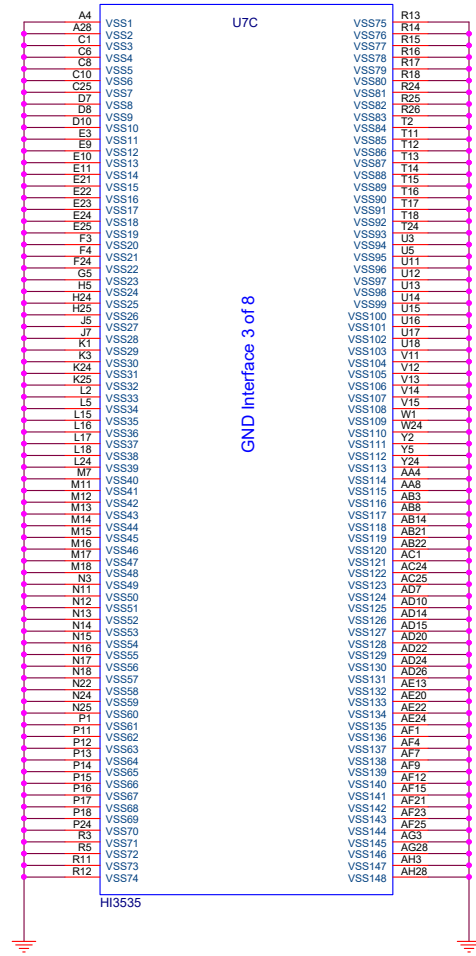
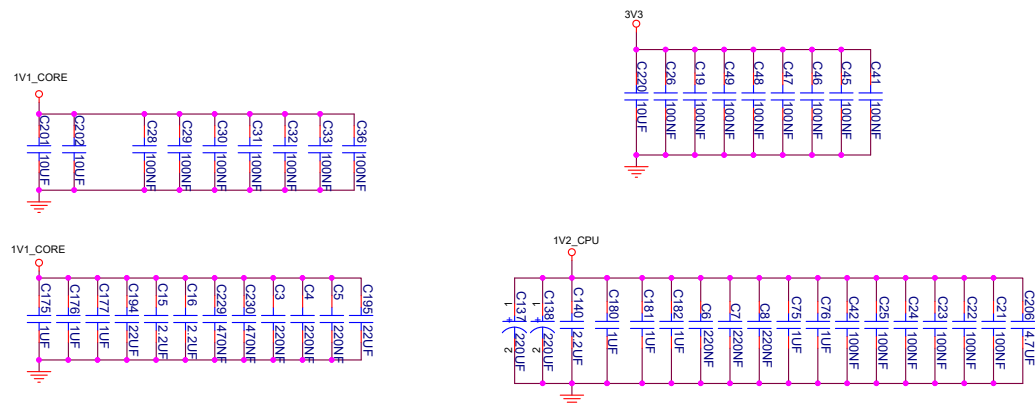


The kind and quantity of the caps must be the same as that for the Hi3535 demo board.

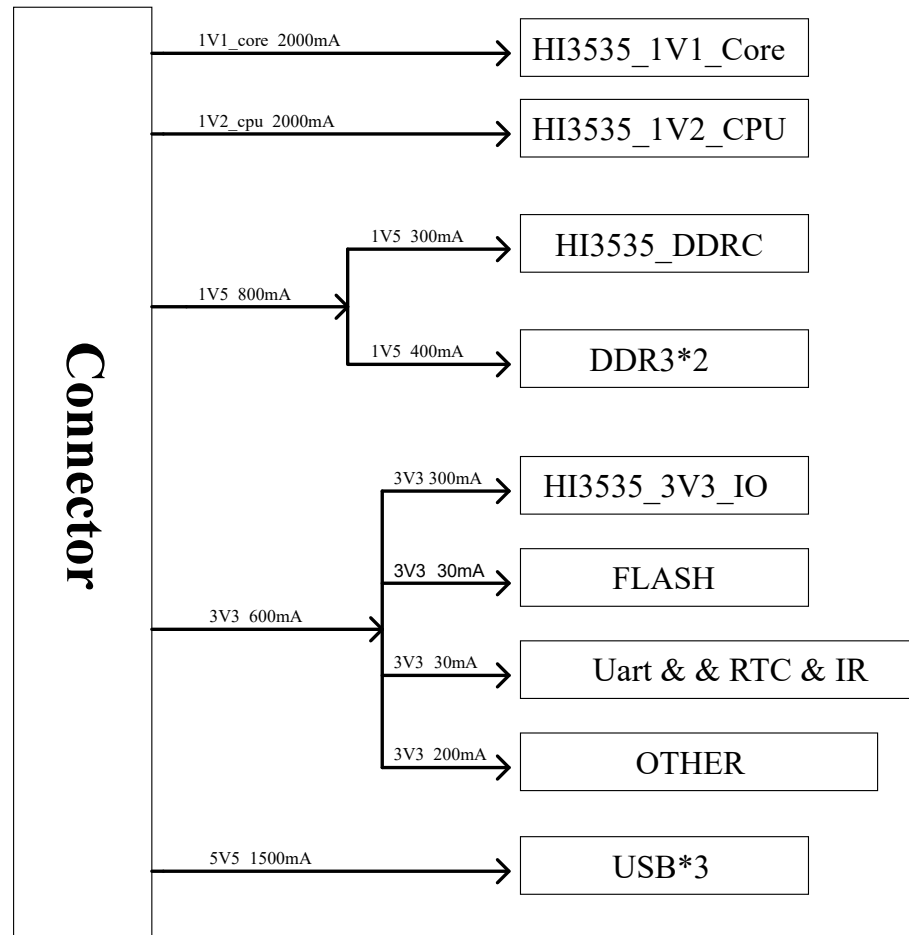
POWER & VSS



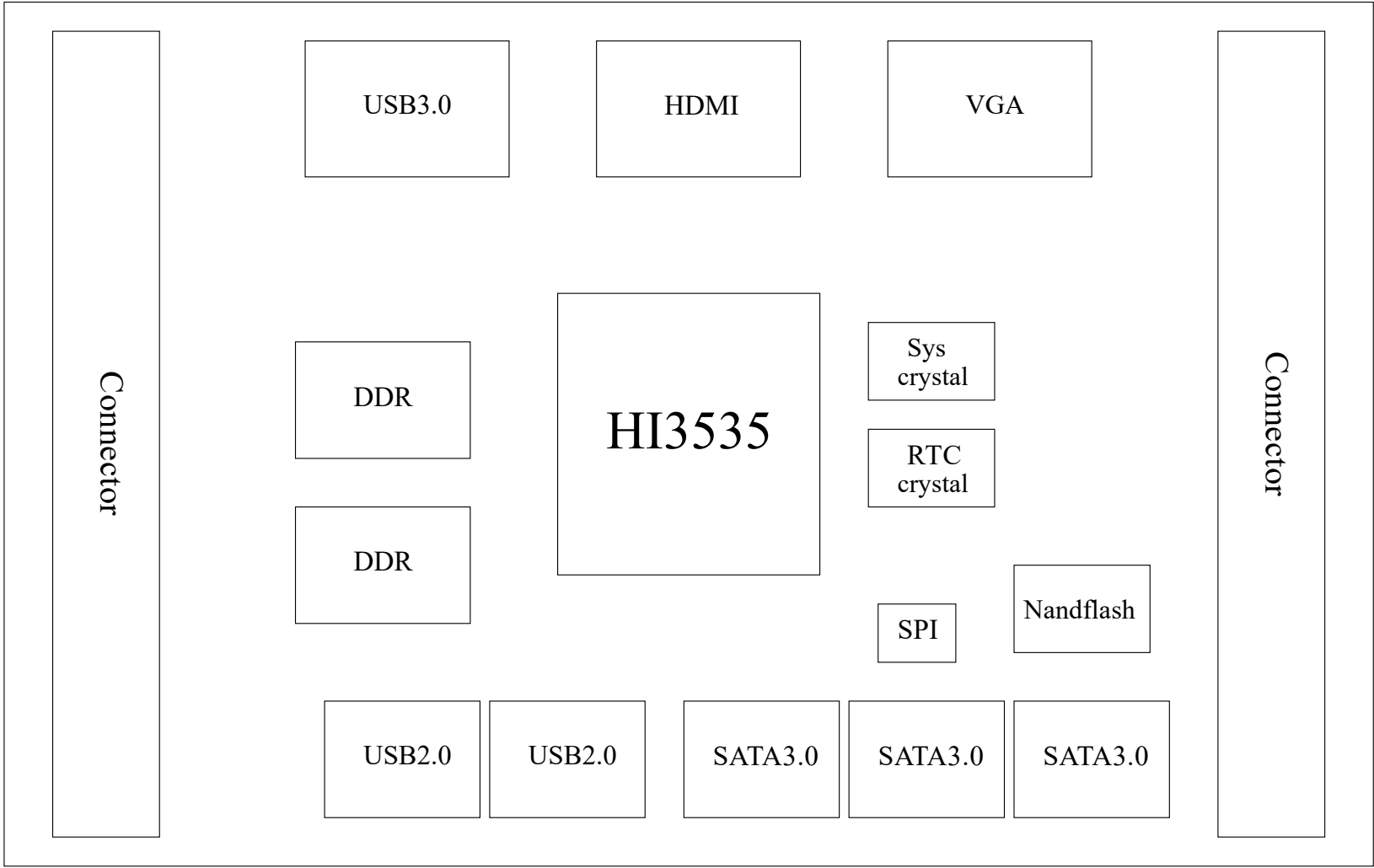
The kind and quantity of the caps must be the same as that for the Hi3535 demo board.



POWER TREE



BLOCK DIAGRAM



CHANGE LIST

2013.07.10 Ver.A schematic

2013.09.27 Change C144 C145 form 10nF to 100nF

01.Hi3535DMEB VER.A

02.CHANGE LIST

03.BLOCK DIAGRAM

04.POWER TREE

05.POWER & VSS

06.Hi3535 DDR3

07.DDR3_A

08.DDR3_B

09.SYSTEM & FLASH

10.POWER ON SETTING PINS

11.INTERFACE

12.USB & SATA

13.DISPLAY

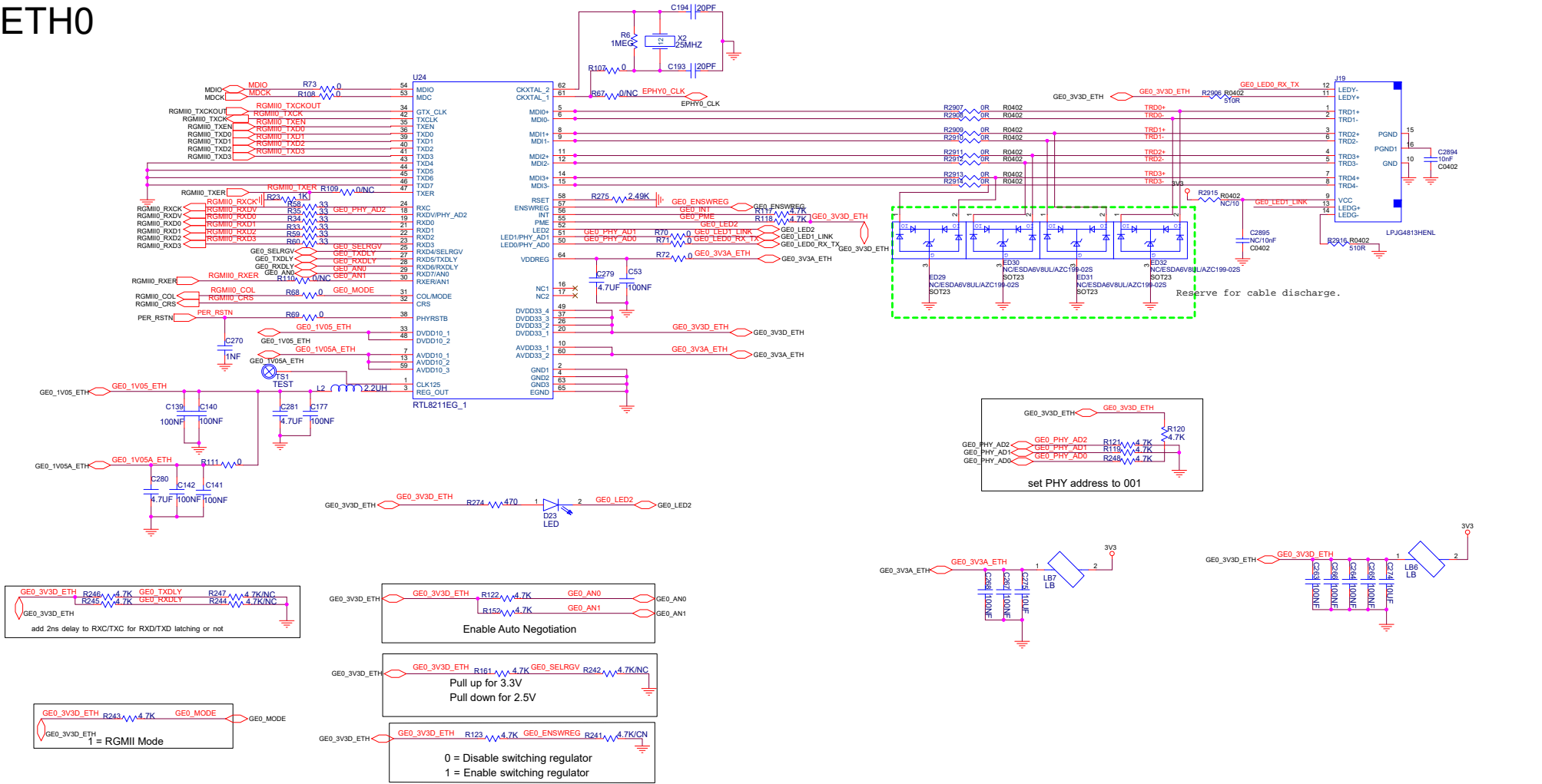
14.HDMI

15.VO

16.Connector

Hi3535DMEB VER.A

ETH0



ETH1

