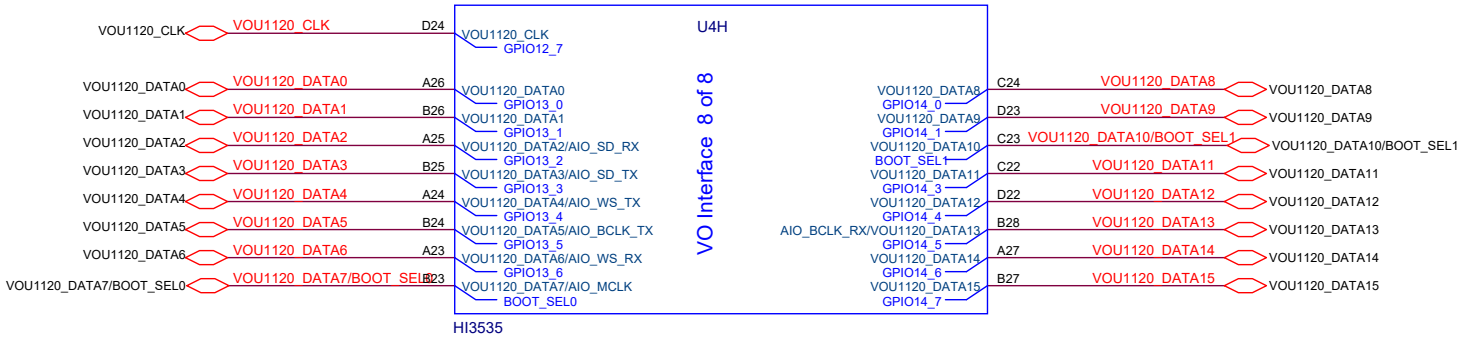
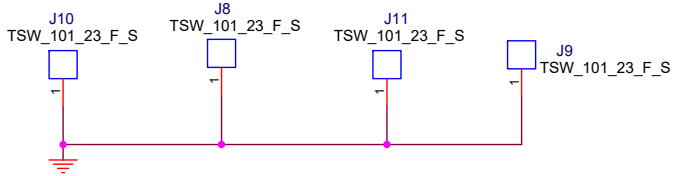
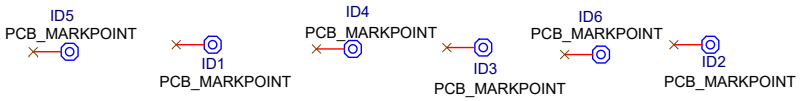
VO


VOU1120_CLK
VOU1120_CLK
D24
VOU1120_CLK
GPIO12_7
U4H
VOU1120_DATA0
VOU1120_DATA0
A26
VOU1120_DATA0
GPIO13_0
VOU1120_DATA1
VOU1120_DATA1
B26
VOU1120_DATA1
GPIO13_1
VOU1120_DATA2
VOU1120_DATA2
A25
VOU1120_DATA2/AIO_SD_RX
GPIO13_2
VOU1120_DATA3
VOU1120_DATA3
B25
VOU1120_DATA3/AIO_SD_TX
GPIO13_3
VOU1120_DATA4
VOU1120_DATA4
A24
VOU1120_DATA4/AIO_WS_TX
GPIO13_4
VOU1120_DATA5
VOU1120_DATA5
B24
VOU1120_DATA5/AIO_BCLK_TX
GPIO13_5
VOU1120_DATA6
VOU1120_DATA6
A23
VOU1120_DATA6/AIO_WS_RX
GPIO13_6
VOU1120_DATA7/BOOT_SEL0
VOU1120_DATA7/BOOT_SEL0
B23
VOU1120_DATA7/AIO_MCLK
BOOT_SEL0
VO Interface 8 of 8
VOU1120_DATA8
GPIO14_0
C24
VOU1120_DATA8
VOU1120_DATA8
VOU1120_DATA9
GPIO14_1
D23
VOU1120_DATA9
VOU1120_DATA9
VOU1120_DATA10
BOOT_SEL1
C23
VOU1120_DATA10/BOOT_SEL1
VOU1120_DATA10/BOOT_SEL1
VOU1120_DATA11
GPIO14_3
C22
VOU1120_DATA11
VOU1120_DATA11
VOU1120_DATA12
GPIO14_4
D22
VOU1120_DATA12
VOU1120_DATA12
AIO_BCLK_RX/VOU1120_DATA13
GPIO14_5
B28
VOU1120_DATA13
VOU1120_DATA13
VOU1120_DATA14
GPIO14_6
A27
VOU1120_DATA14
VOU1120_DATA14
VOU1120_DATA15
GPIO14_7
B27
VOU1120_DATA15
VOU1120_DATA15
HI3535

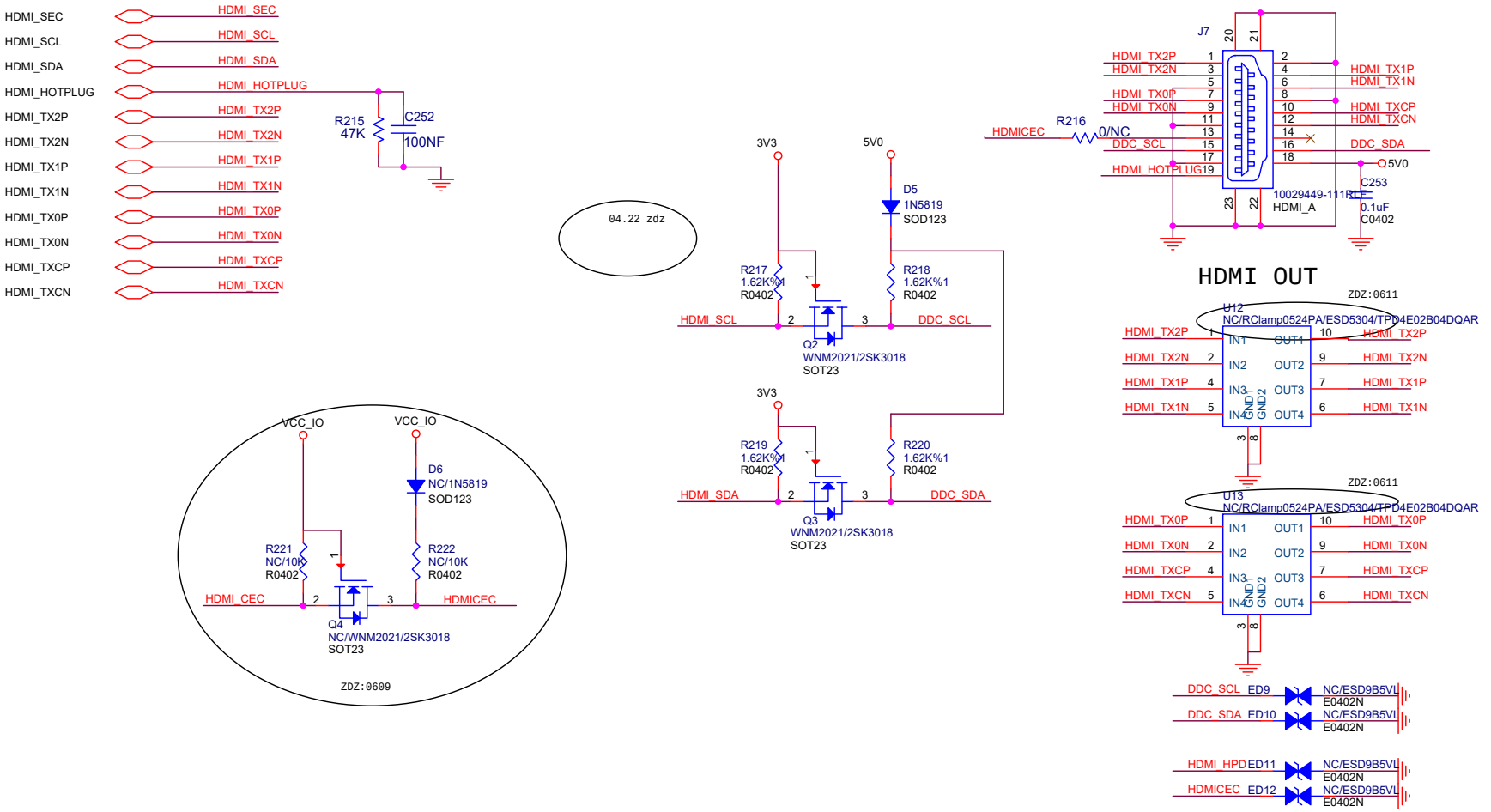

J10
TSW_101_23_F_S
J8
TSW_101_23_F_S
J11
TSW_101_23_F_S
J9
TSW_101_23_F_S
1
1
1
1


ID5
PCB_MARKPOINT
ID1
PCB_MARKPOINT
ID4
PCB_MARKPOINT
ID3
PCB_MARKPOINT
ID6
PCB_MARKPOINT
ID2
PCB_MARKPOINT

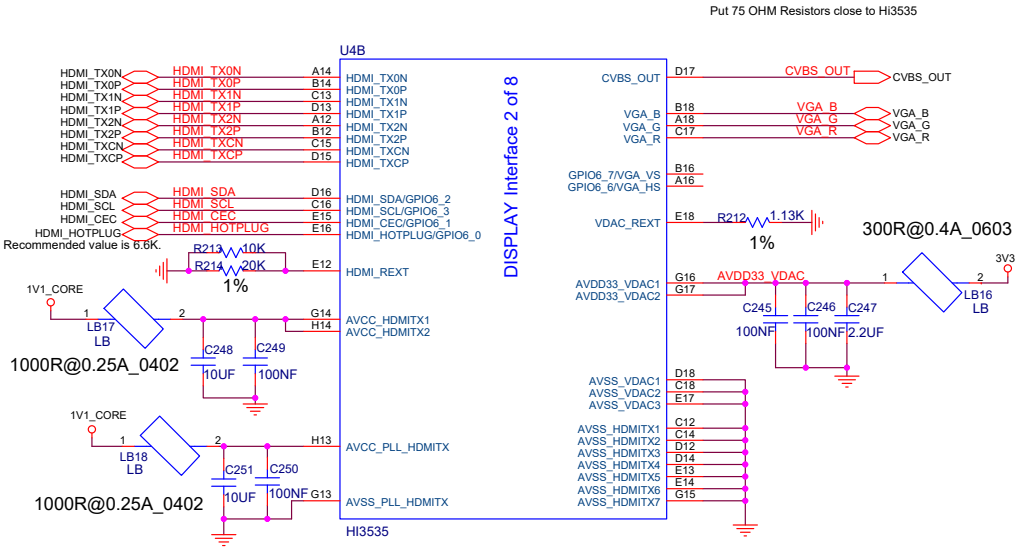
HDMI

The HDMI differential trace impedance is 100 OHM.

The HDMI trace length is less than 5 inch.



DISPLAY


Put 75 OHM Resistors close to Hi3535
U4B
DISPLAY Interface 2 of 8
HI3535
HDMI_TX0N
HDMI_TX0P
HDMI_TX1N
HDMI_TX1P
HDMI_TX2N
HDMI_TX2P
HDMI_TXCN
HDMI_TXCP
HDMI_SDA
HDMI_SCL
HDMI_CEC
HDMI_HOTPLUG
Recommended value is 6.6K.
R213 10K
R214 20K
1%
HDMI_REXT
1V1_CORE
LB17
LB
1000R@0.25A_0402
C248 10UF
C249 100NF
AVCC_HDMITX1
AVCC_HDMITX2
LB18
C251 10UF
C250 100NF
AVCC_PLL_HDMITX
AVSS_PLL_HDMITX
CVBS_OUT
VGA_B
VGA_G
VGA_R
GPIO6_7/VGA_VS
GPIO6_6/VGA_HS
VDAC_REXT
R212 1.13K
1%
300R@0.4A_0603
AVDD33_VDAC1
AVDD33_VDAC2
C245 100NF
C246 100NF
C247 2.2UF
LB16
3V3
AVSS_VDAC1
AVSS_VDAC2
AVSS_VDAC3
AVSS_HDMITX1
AVSS_HDMITX2
AVSS_HDMITX3
AVSS_HDMITX4
AVSS_HDMITX5
AVSS_HDMITX6
AVSS_HDMITX7

USB & SATA

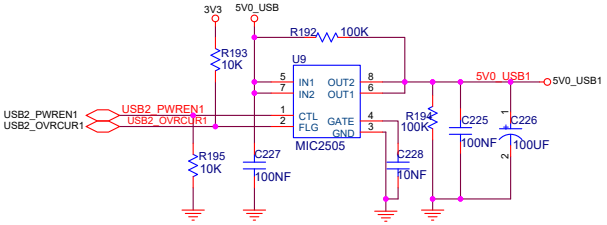
The USB differential trace impedance is 90 OHM.

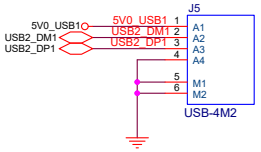
The USB trace length is less than 5 inch.

The SATA differential trace impedance is 100 OHM.

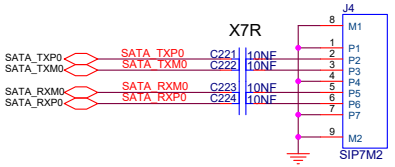
The SATA trace length is less than 5 inch.

USB2.0 Port1

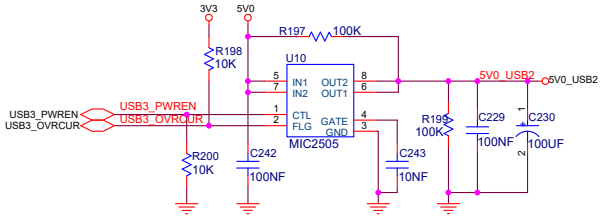


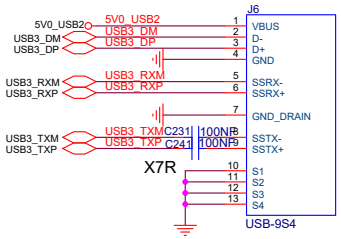


SATA3.0 Port0

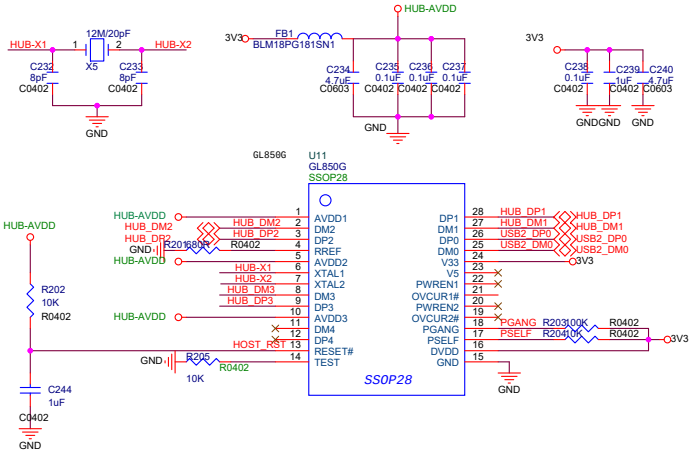


USB3.0

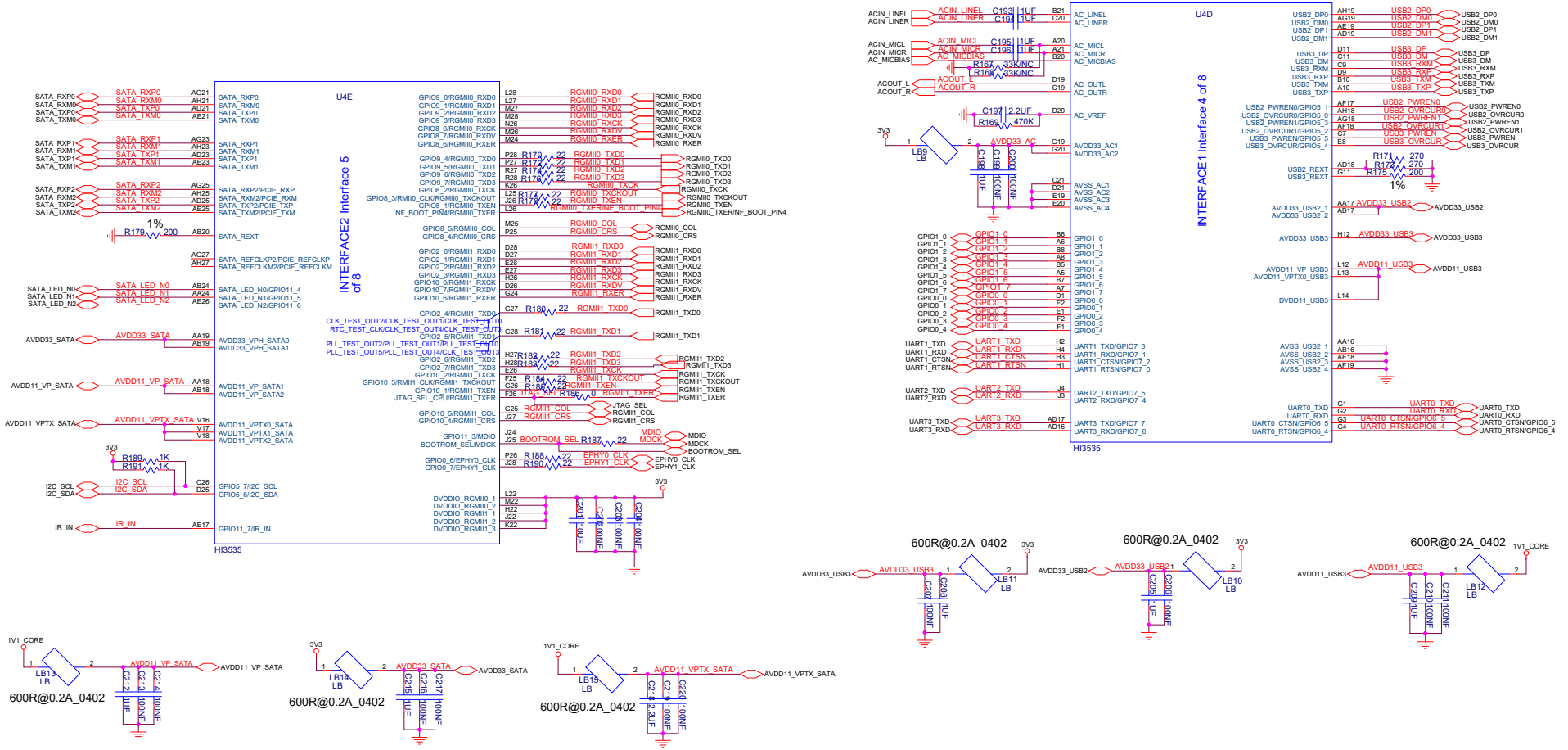




USB HUB



Interface


U4E
INTERFACE2 Interface 5 of 8
HI3535
U4D
INTERFACE1 Interface 4 of 8
HI3535
600R@0.2A_0402
600R@0.2A_0402
600R@0.2A_0402
600R@0.2A_0402

Power on setting pins

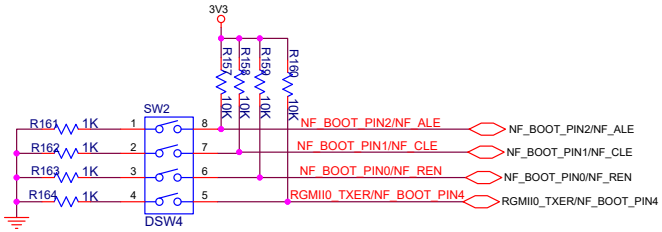
NF_BOOT_PIN[4:0]

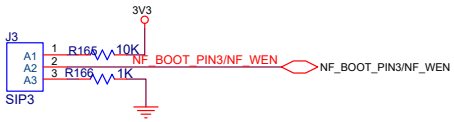
00011 2k page size,4bit ecc,64page/block,5addr

00100 4k page size,24bit ecc,256page/block,5addr
00101 2k page size,24bit ecc,64page/block,5addr
00111 8k page size,24bit ecc,256page/block,5addr

01000 4k page size,4bit ecc,128page/block,5addr
01001 4k page size,4bit ecc,64page/block,5addr
01010 2k page size,4bit ecc,64page/block,4addr
01011 4k page size,24bit ecc,128page/block,5addr
01101 8k page size,24bit ecc,128page/block,5addr

10000 8k page size,24bit ecc,64page/block,5addr
10001 4k page size,24bit ecc,64page/block,5addr
10101 2k page size,4bit ecc,128page/block,5addr
10110 2k page size,8bit ecc,128page/block,5addr
11001 2k page size,24bit ecc,128page/block,5addr
11010 2k page size,8bit ecc,64page/block,5addr
11110 4k page size,8bit ecc,64page/block,5addr
11111 4k page size,8bit ecc,128page/block,5addr

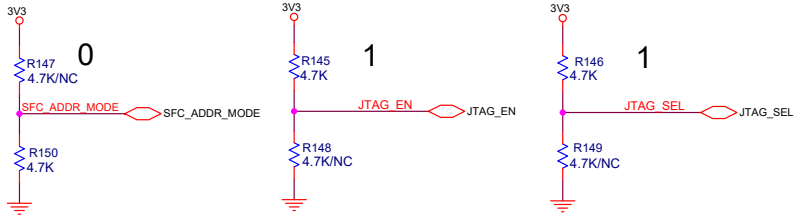




	SFC_ADDR_MODE
0	3 Byte mode
1	4 Byte mode

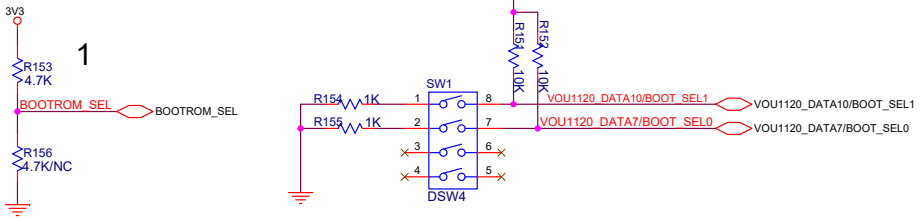
	JTAG_EN
0	Disable JTAG
1	Enable JTAG

	JTAG_SEL
0	Other
1	CPU

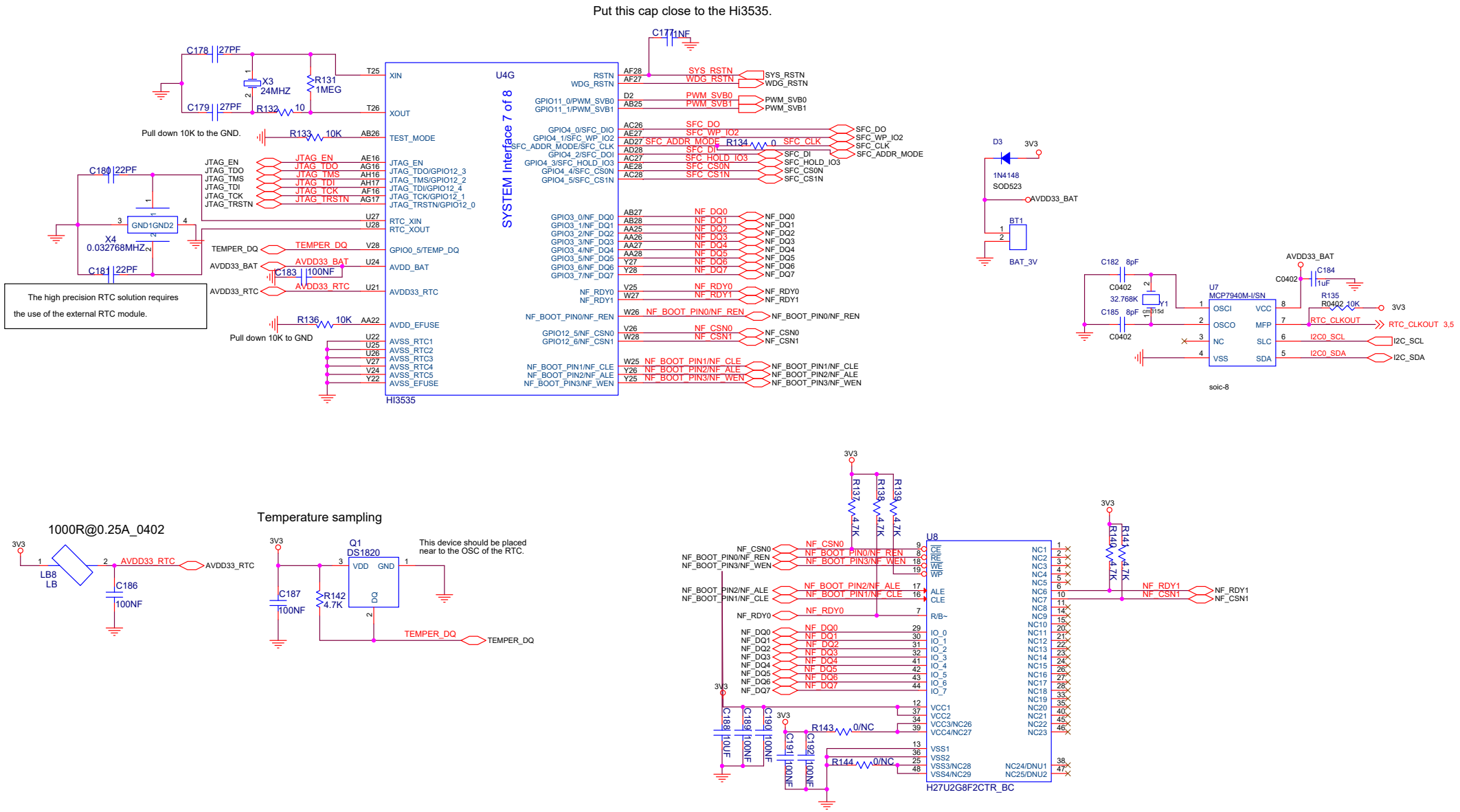


	BOOTROM_SEL
0	Boot from BOOT_SEL
1	Boot from Bootrom

	BOOT_SEL[1:0]
00	SPI FLASH
01	DDR
10	NAND FLASH
11	Reserve

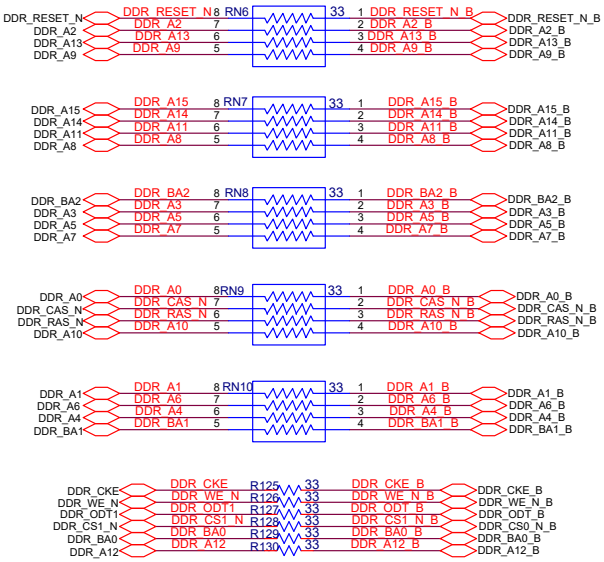


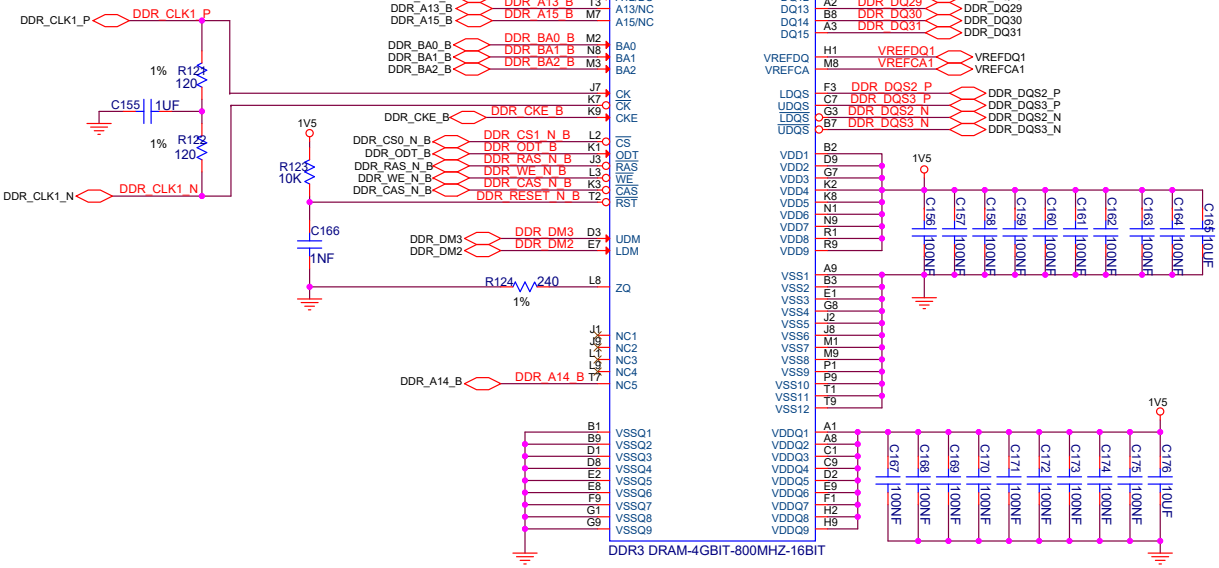
SYSTEM & FLASH

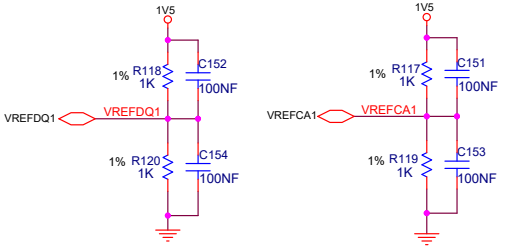


DDR3_B

The routing design of the DDR must be
the same as that for the Hi3535 demo board.

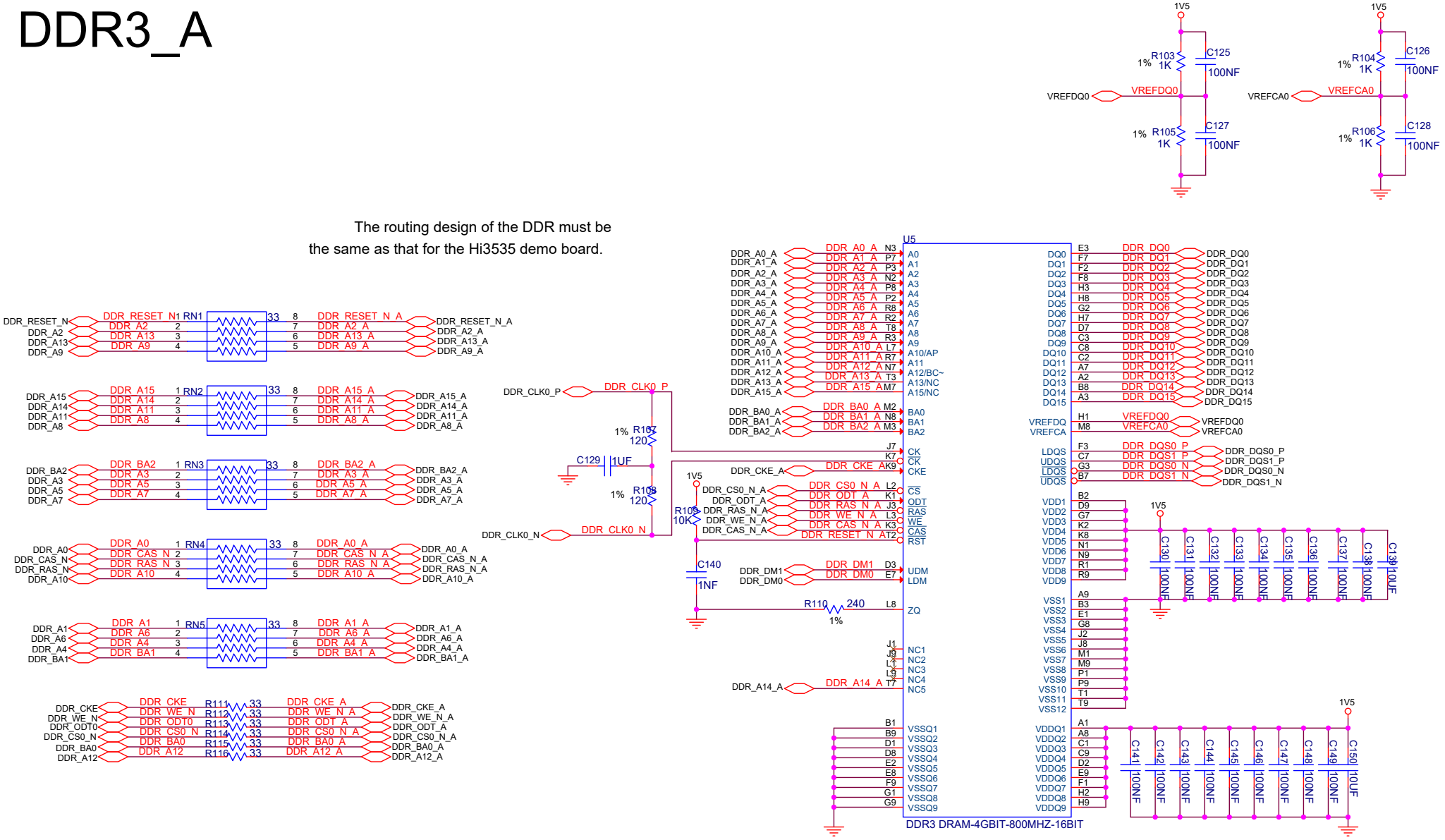




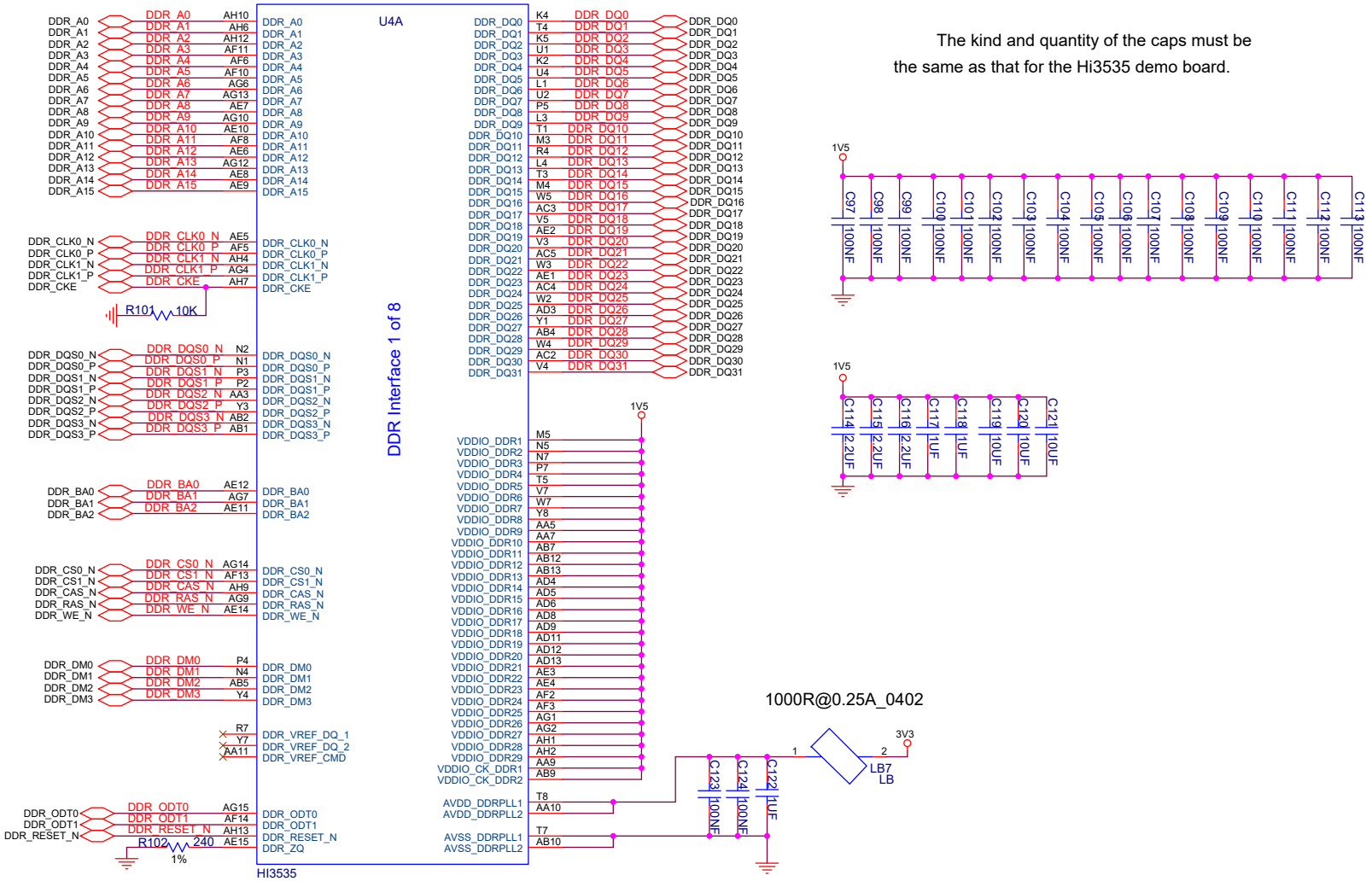


DDR3_A

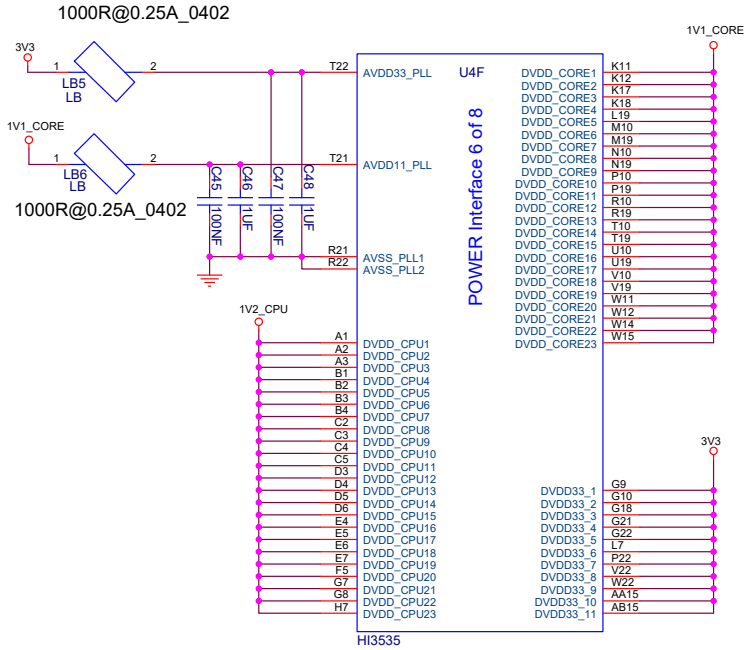
The routing design of the DDR must be the same as that for the Hi3535 demo board.

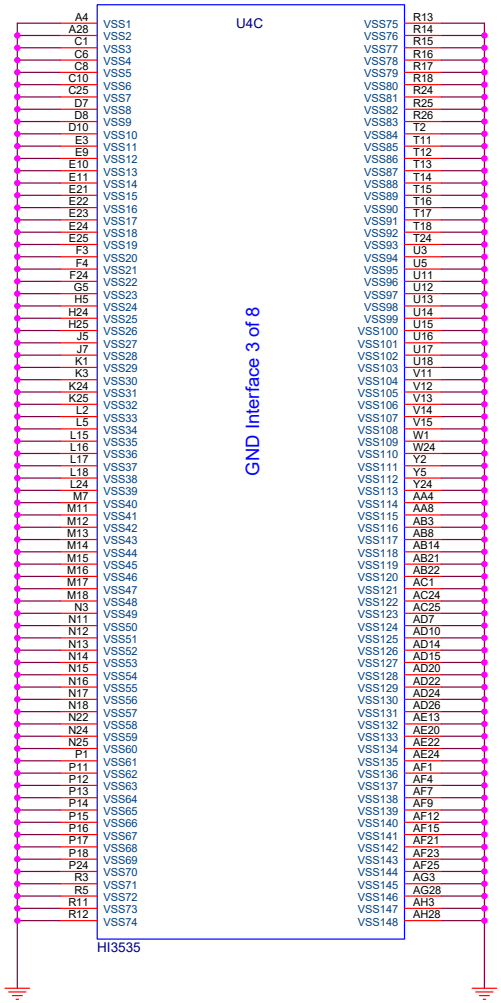


HI3535 DDR3

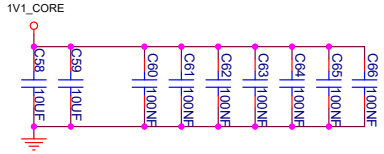

U4A
DDR Interface 1 of 8
HI3535
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14
DDR_A15
DDR_CLK0_N
DDR_CLK0_P
DDR_CLK1_N
DDR_CLK1_P
DDR_CKE
R101
10K
DDR_DQS0_N
DDR_DQS0_P
DDR_DQS1_N
DDR_DQS1_P
DDR_DQS2_N
DDR_DQS2_P
DDR_DQS3_N
DDR_DQS3_P
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CS0_N
DDR_CS1_N
DDR_CAS_N
DDR_RAS_N
DDR_WE_N
DDR_DM0
DDR_DM1
DDR_DM2
DDR_DM3
DDR_VREF_DQ_1
DDR_VREF_DQ_2
DDR_VREF_CMD
DDR_ODT0
DDR_ODT1
DDR_RESET_N
R102
240
1%
DDR_ZQ
DDR_DQ0
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQ8
DDR_DQ9
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQ16
DDR_DQ17
DDR_DQ18
DDR_DQ19
DDR_DQ20
DDR_DQ21
DDR_DQ22
DDR_DQ23
DDR_DQ24
DDR_DQ25
DDR_DQ26
DDR_DQ27
DDR_DQ28
DDR_DQ29
DDR_DQ30
DDR_DQ31
1V5
VDDIO_DDR1
VDDIO_DDR2
VDDIO_DDR3
VDDIO_DDR4
VDDIO_DDR5
VDDIO_DDR6
VDDIO_DDR7
VDDIO_DDR8
VDDIO_DDR9
VDDIO_DDR10
VDDIO_DDR11
VDDIO_DDR12
VDDIO_DDR13
VDDIO_DDR14
VDDIO_DDR15
VDDIO_DDR16
VDDIO_DDR17
VDDIO_DDR18
VDDIO_DDR19
VDDIO_DDR20
VDDIO_DDR21
VDDIO_DDR22
VDDIO_DDR23
VDDIO_DDR24
VDDIO_DDR25
VDDIO_DDR26
VDDIO_DDR27
VDDIO_DDR28
VDDIO_DDR29
VDDIO_CK_DDR1
VDDIO_CK_DDR2
AVDD_DDRPLL1
AVDD_DDRPLL2
AVSS_DDRPLL1
AVSS_DDRPLL2
C123
C124
C122
100NF
1UF
1000R@0.25A_0402
3V3
LB7
LB
The kind and quantity of the caps must be
the same as that for the Hi3535 demo board.
C97
C98
C99
C100
C101
C102
C103
C104
C105
C106
C107
C108
C109
C110
C111
C112
C113
C114
C115
C116
C117
C118
C119
C120
C121
2.2UF
10UF

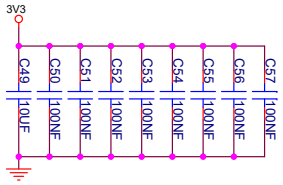
POWER & VSS

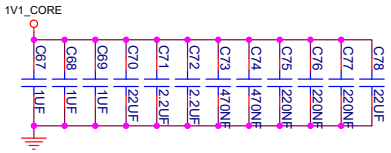


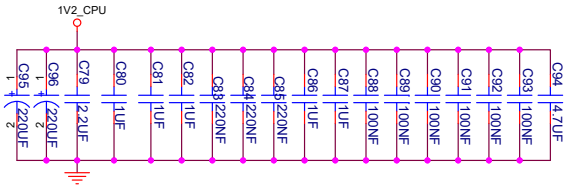


The kind and quantity of the caps must be the same as that for the Hi3535 demo board.

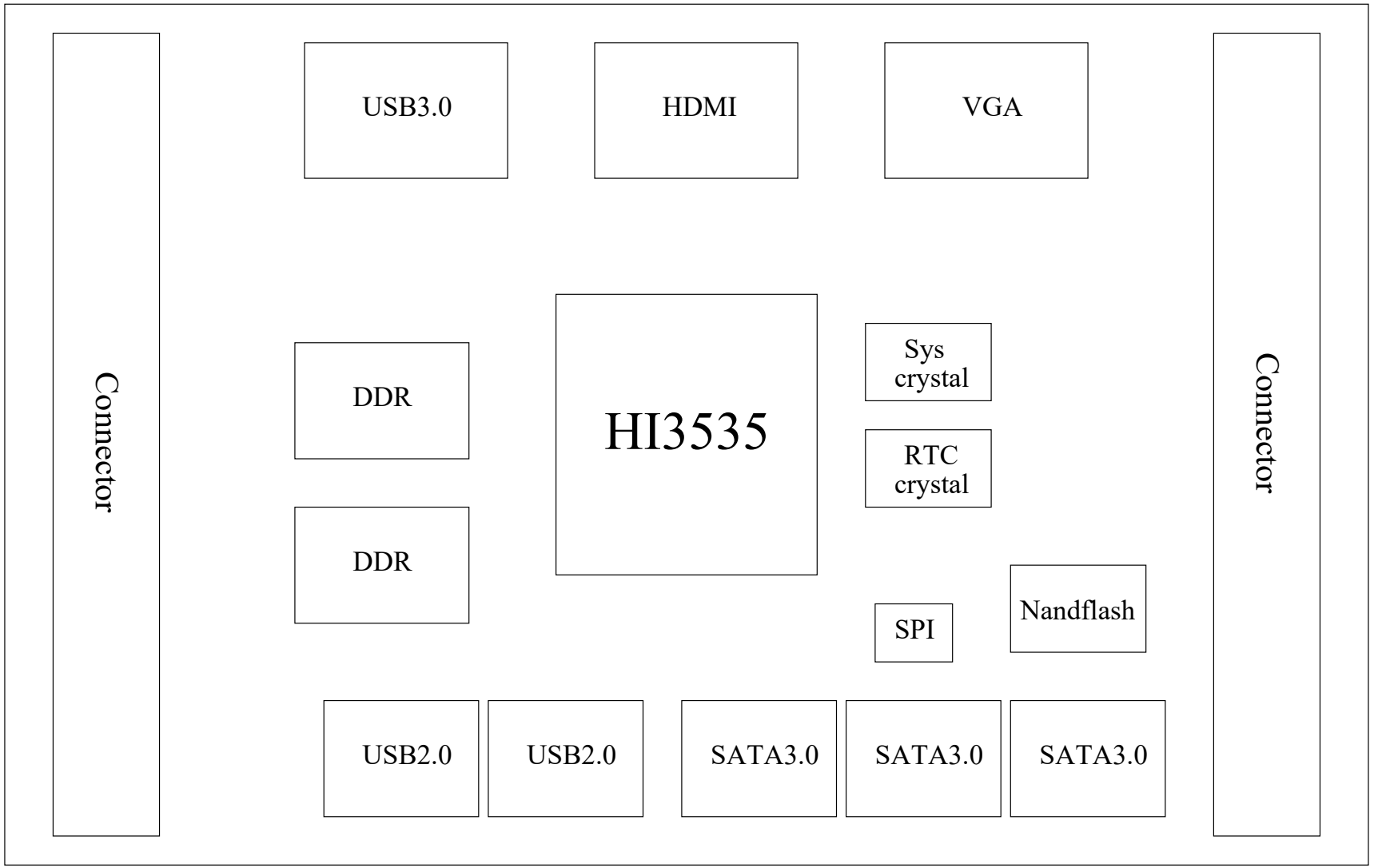








BLOCK DIAGRAM



CHANGE LIST

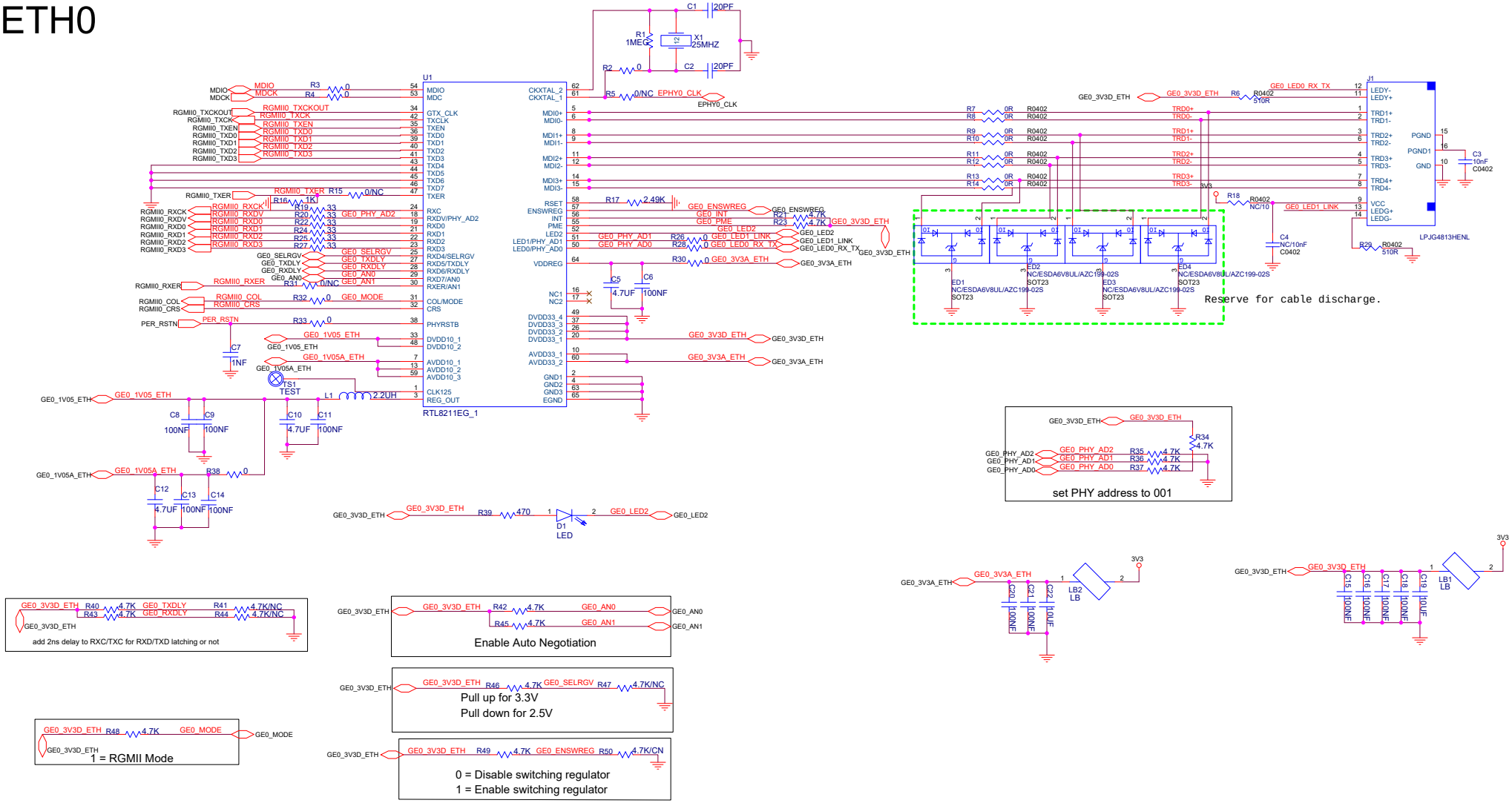
2013.07.10 Ver.A schematic

2013.09.27 Change C144 C145 form 10nF to 100nF

01.Hi3535DMEB VER.A
02.CHANGE LIST
03.BLOCK DIAGRAM
04.POWER TREE
05.POWER & VSS
06.Hi3535 DDR3
07.DDR3_A
08.DDR3_B
09.SYSTEM & FLASH
10.POWER ON SETTING PINS
11.INTERFACE
12.USB & SATA
13.DISPLAY
14.HDMI
15.VO
16.Connector

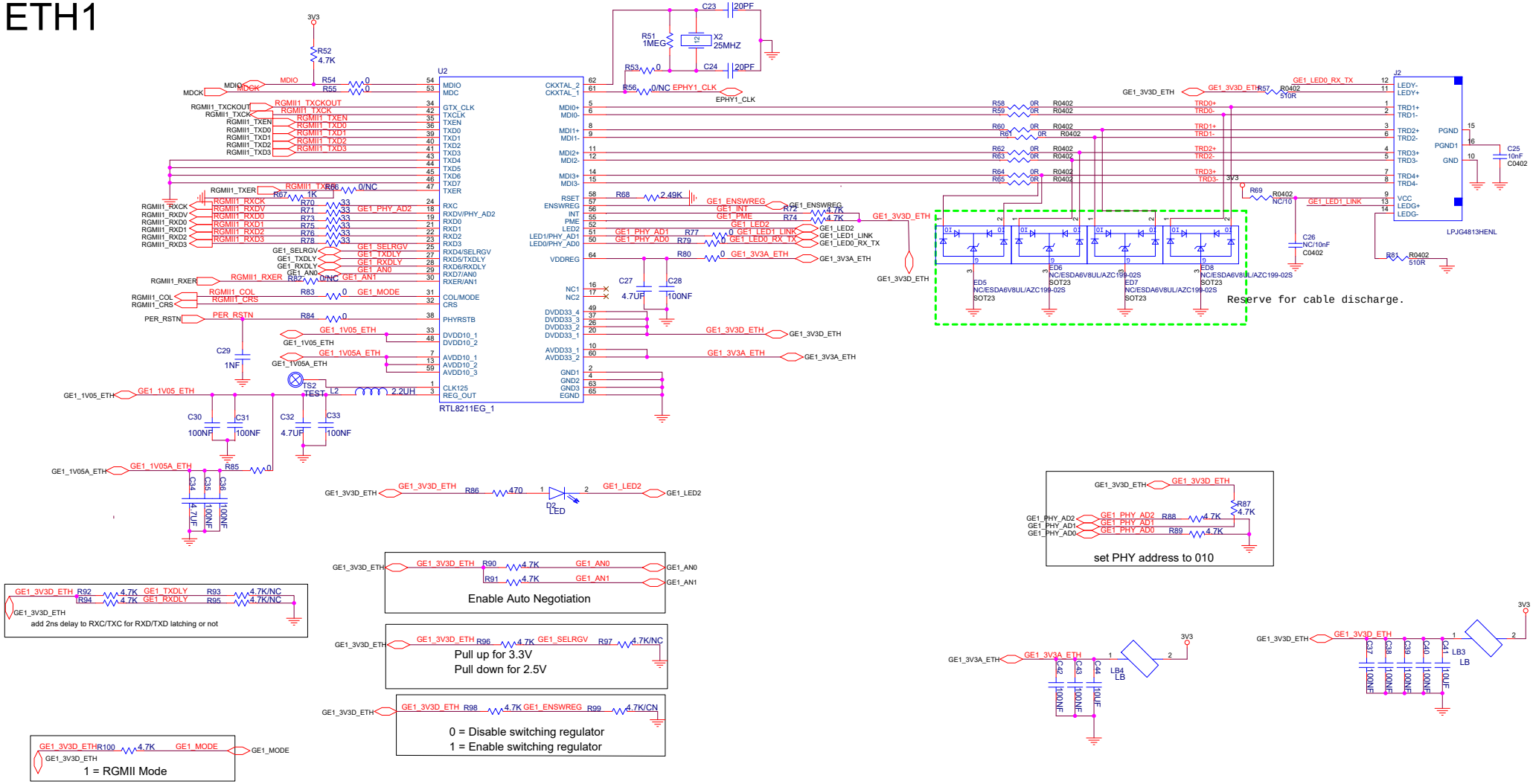
Hi3535DMEB VER.A

ETH0



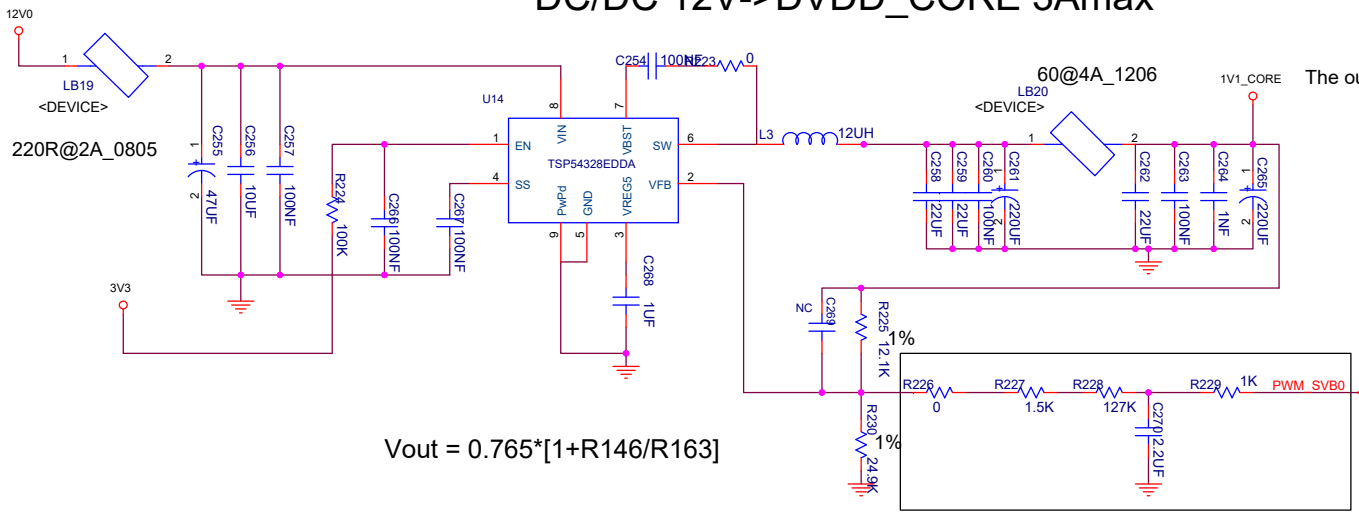
U1
RTL8211EG_1
J1
LPJG4813HENL
Reserve for cable discharge.
set PHY address to 001
Enable Auto Negotiation
add 2ns delay to RXC/TXC for RXD/TXD latching or not
Pull up for 3.3V
Pull down for 2.5V
1 = RGMII Mode
0 = Disable switching regulator
1 = Enable switching regulator

ETH1


U2
RTL8211EG_1
LPJG4813HENL
Reserve for cable discharge.
set PHY address to 010
Enable Auto Negotiation
Pull up for 3.3V
Pull down for 2.5V
0 = Disable switching regulator
1 = Enable switching regulator
1 = RGMII Mode
add 2ns delay to RXC/TXC for RXD/TXD latching or not

Power Supply

DC/DC 12V->DVDD_CORE 3Amax



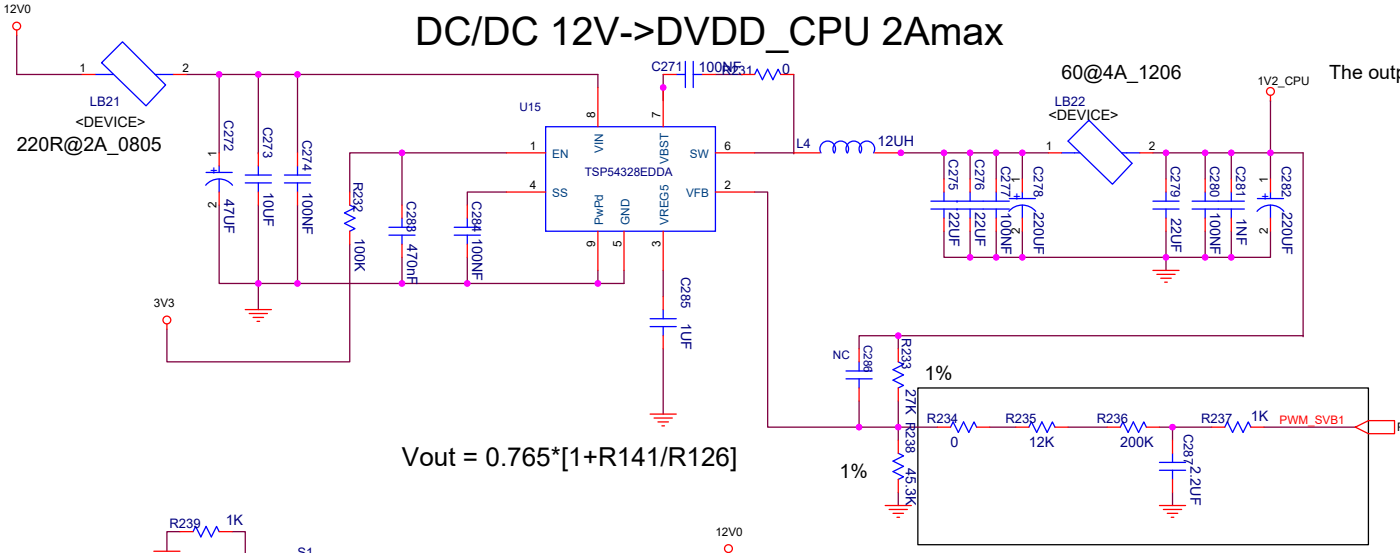
Vout = 0.765*[1+R146/R163]

The output Voltage is controlled by the SVB circuit.

This circuit should be palced near to the DC-DC.

This circuit is left for the SVB.

DC/DC 12V->DVDD_CPU 2Amax

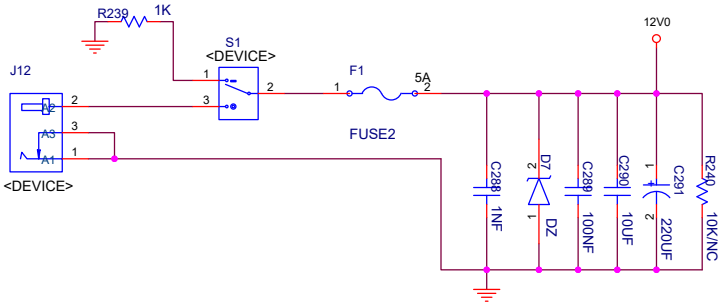


Vout = 0.765*[1+R141/R126]

The output Voltage is controlled by the SVB circuit.

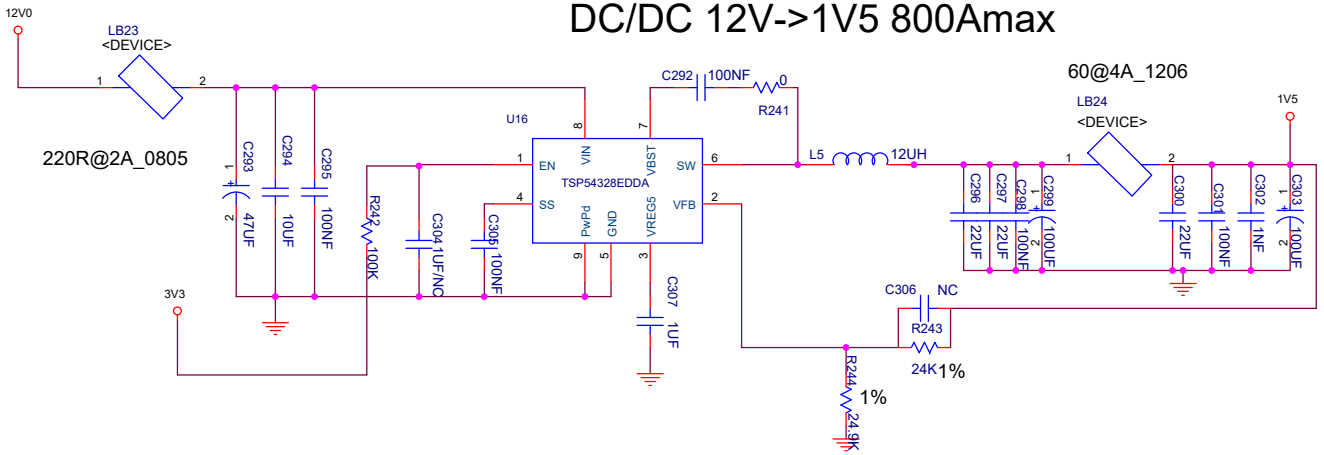
This circuit should be palced near to the DC-DC.

This circuit is left for the SVB.



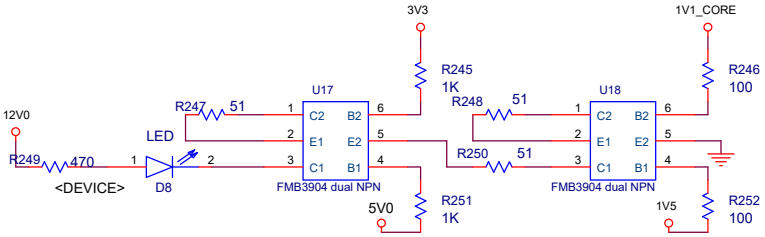
Power Supply

DC/DC 12V->1V5 800Amax



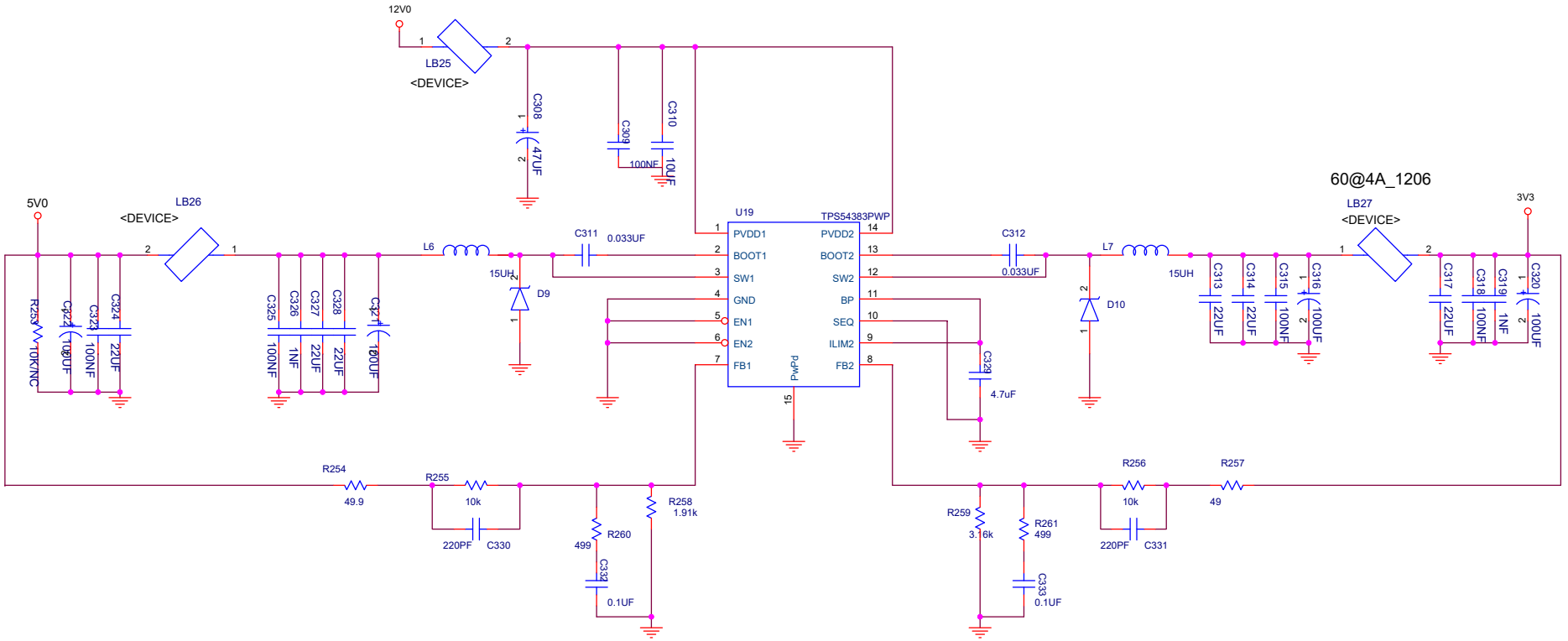
Vout = 0.765*[1+R240/R147]

Power Indicator LED

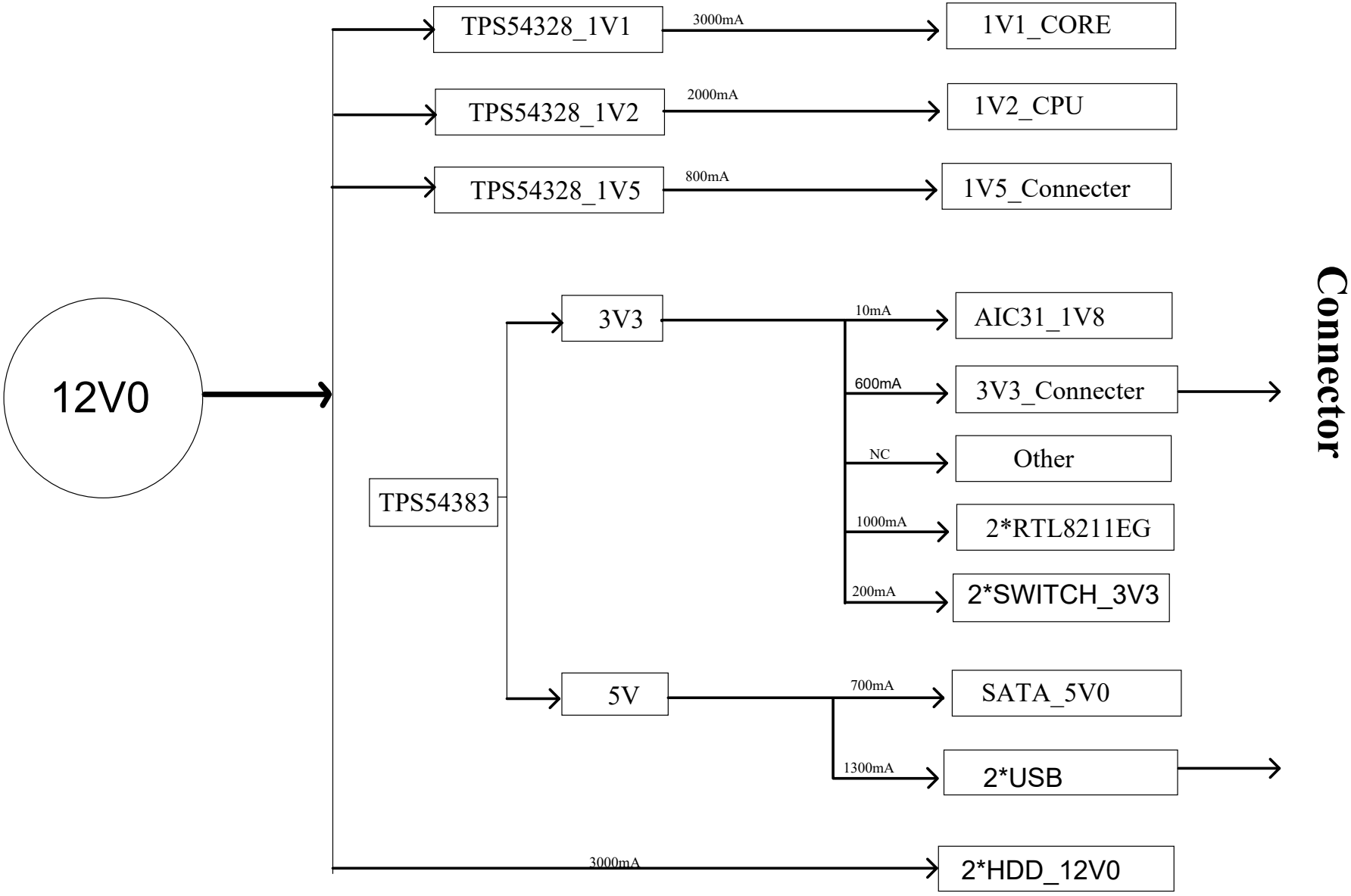


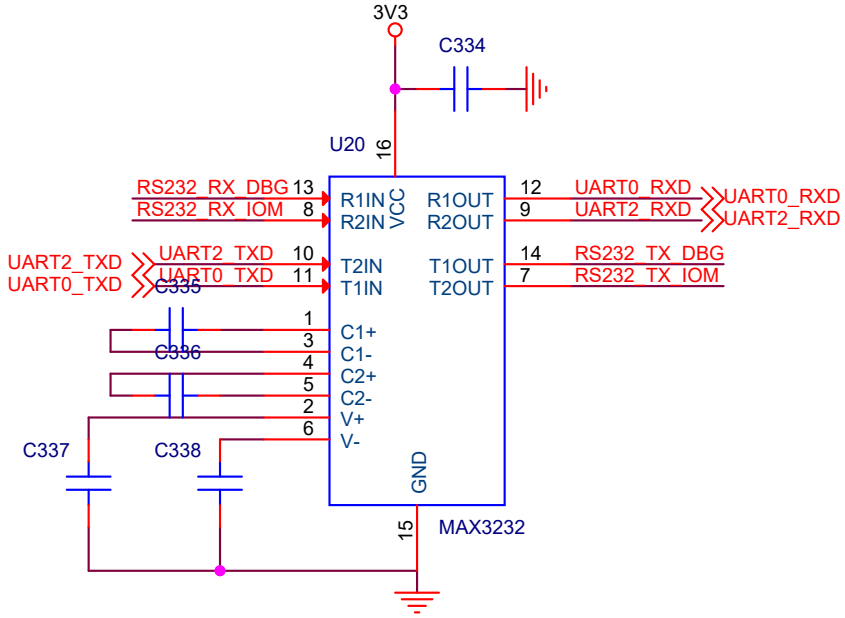
Power Supply

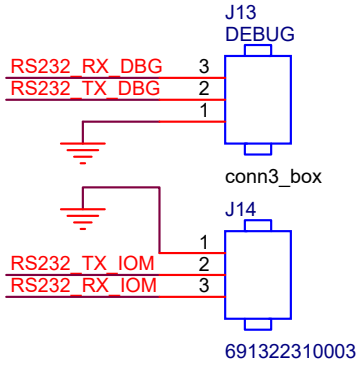
12V -> 5V - 2A and 3.3V - 2A



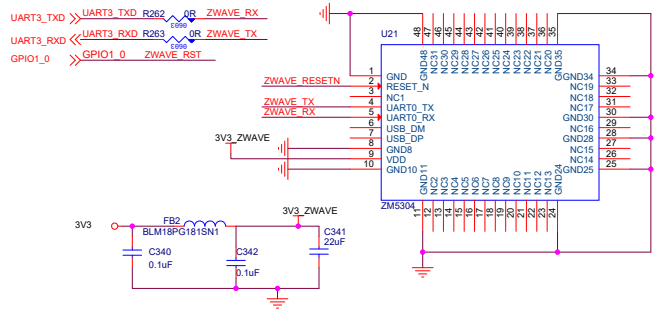
POWER TREE

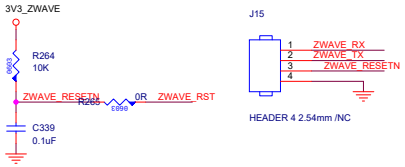

12V0
TPS54328_1V1
3000mA
1V1_CORE
TPS54328_1V2
2000mA
1V2_CPU
TPS54328_1V5
800mA
1V5_Connecter
TPS54383
3V3
10mA
AIC31_1V8
600mA
3V3_Connecter
NC
Other
1000mA
2*RTL8211EG
200mA
2*SWITCH_3V3
5V
700mA
SATA_5V0
1300mA
2*USB
3000mA
2*HDD_12V0
Connector


3V3
C334
U20
16
RS232_RX_DBG
RS232_RX_IOM
13
8
R1IN
R2IN
VCC
R1OUT
R2OUT
12
9
UART0_RXD
UART2_RXD
UART0_RXD
UART2_RXD
UART2_TXD
UART0_TXD
UART2_TXD
UART0_TXD
10
11
T2IN
T1IN
T1OUT
T2OUT
14
7
RS232_TX_DBG
RS232_TX_IOM
C335
C336
1
3
4
5
2
6
C1+
C1-
C2+
C2-
V+
V-
C337
C338
GND
15
MAX3232

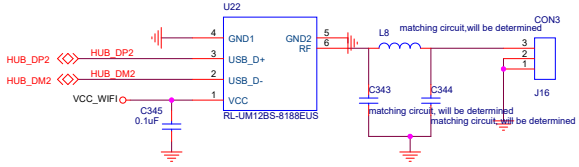

J13
DEBUG
RS232_RX_DBG
RS232_TX_DBG
3
2
1
conn3_box
J14
1
RS232_TX_IOM
RS232_RX_IOM
2
3
691322310003

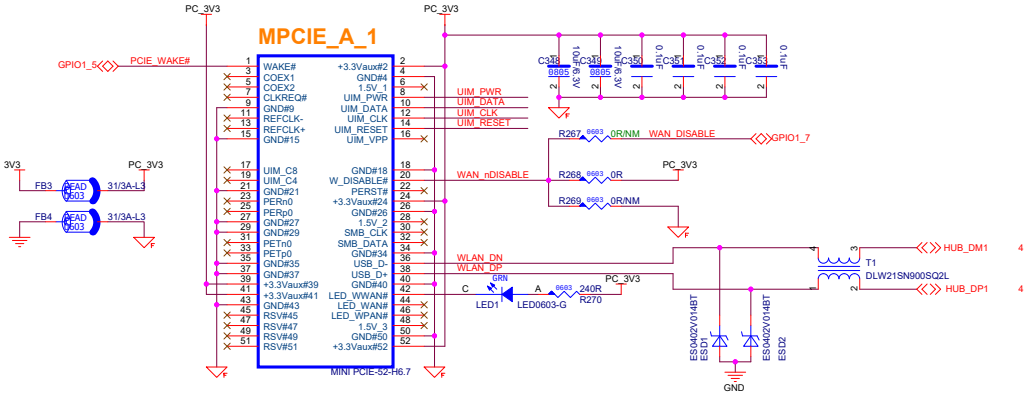
WWAN-3G

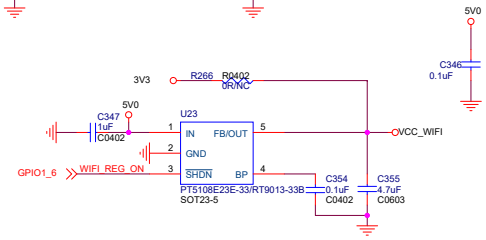

UART3_TXD
UART3_RXD
GPIO1_0
R262 0R ZWAVE_RX
R263 0R ZWAVE_TX
GPIO1_0 ZWAVE_RST
U21
ZWAVE_RESETN
ZWAVE_TX
ZWAVE_RX
3V3_ZWAVE
ZM5304
3V3
FB2
BLM18PG181SN1
C340 0.1uF
C342 0.1uF
C341 22uF

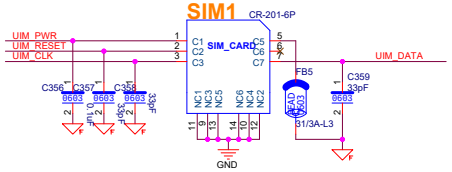

3V3_ZWAVE
R264 10K
ZWAVE_RESETN
R265 0R ZWAVE_RST
C339 0.1uF

J15
1 ZWAVE_RX
2 ZWAVE_TX
3 ZWAVE_RESETN
4
HEADER 4 2.54mm /NC


U22
HUB_DP2
HUB_DM2
VCC_WIFI
GND1
USB_D+
USB_D-
VCC
GND2
RF
RL-UM12BS-8188EUS
L8
matching circuit,will be determined
CON3
J16
C343
C344
C345 0.1uF
matching circuit, will be determined


MPCIE_A_1
PC_3V3
GPIO1_5
PCIE_WAKE#
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
WAN_nDISABLE
R267 0R/NM WAN_DISABLE
GPIO1_7
R268 0R
R269 0R/NM
WLAN_DN
WLAN_DP
LED1
LED0603-G
R270 240R
T1
DLW21SN900SQ2L
HUB_DM1
HUB_DP1
ESD1
ESD2
GND
FB3
FB4
MINI PCIE-52-H6.7


5V0
C346 0.1uF
3V3
R266 R0402 0R/NC
C347 1uF C0402
U23
IN
GND
SHDN
FB/OUT
BP
VCC_WIFI
GPIO1_6
WIFI_REG_ON
PT5108E23E-33/RT9013-33B
SOT23-5
C354 0.1uF C0402
C355 4.7uF C0603


SIM1
CR-201-6P
SIM_CARD
UIM_PWR
UIM_RESET
UIM_CLK
UIM_DATA
C356
C357
C358
C359 33pF
FB5
GND