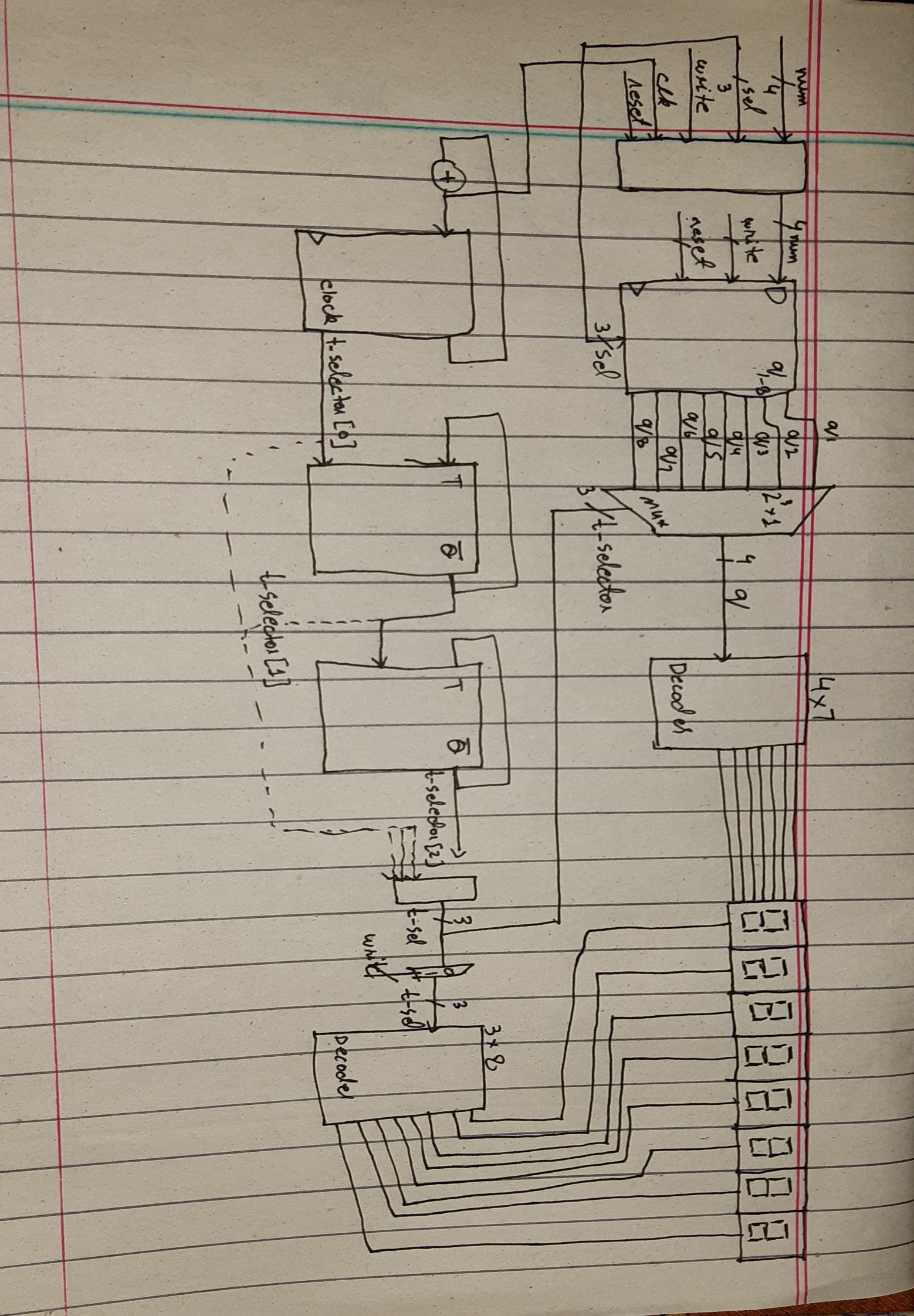
|  |  |
| --- | --- |
| Name**: M Usama** | EE-272L Digital Systems Design |
| Reg. No.: **2022-EE-116** | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

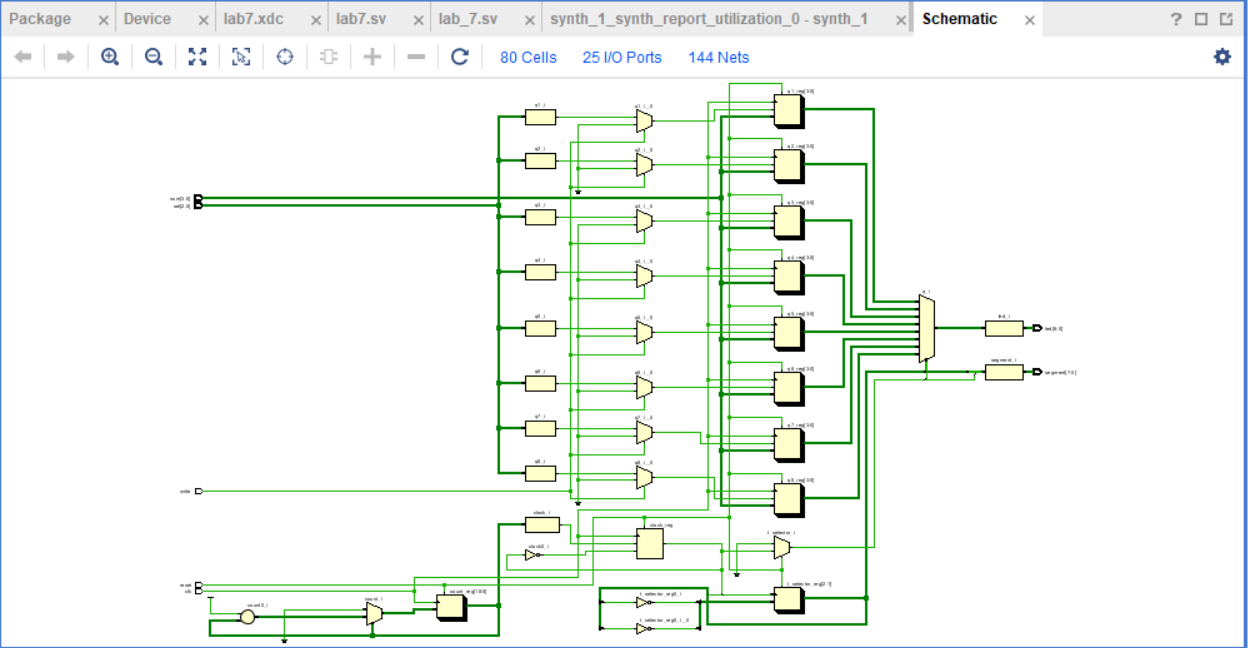
**Lab Manual**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

**Hand sketched diagram**

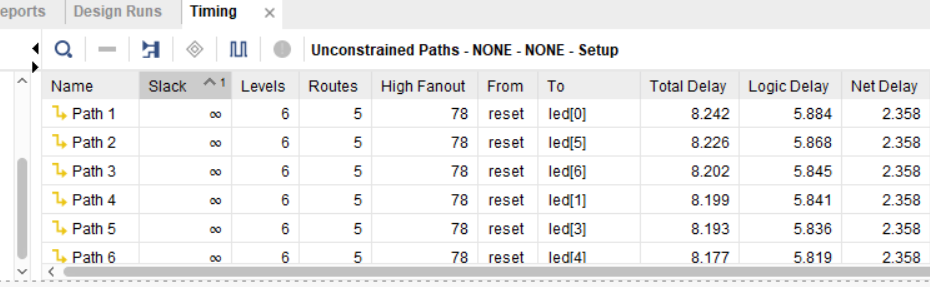
****

**Schematic diagram**

**–––––––**

**Combinational delay**

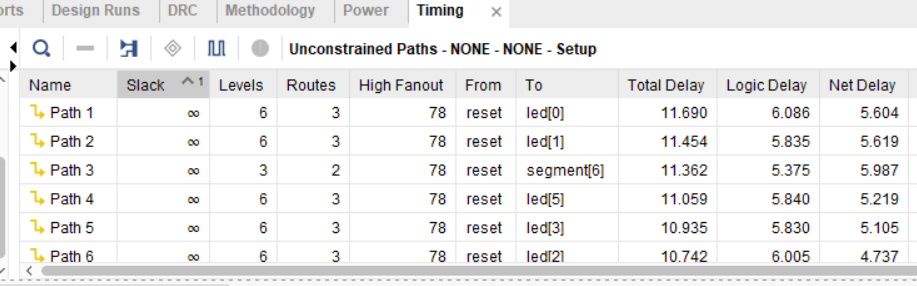
**Synthesis maximum combinational delay:**

****

Synthesis combinational delay is maximum from reset to led[0],

and it is 8.242 nano seconds.

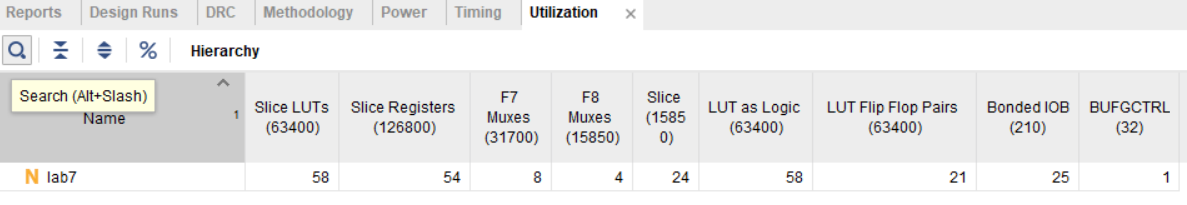
**Implementation maximum combinational delay:**

****

Implementation combinational delay is maximum from reset to led[0],

and it is 11.690 nano seconds.

**Utilization summary**

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1. Slice Logic

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+-------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-------------------------+------+-------+-----------+-------+

| Slice LUTs\* | 58 | 0 | 63400 | 0.09 |

| LUT as Logic | 58 | 0 | 63400 | 0.09 |

| LUT as Memory | 0 | 0 | 19000 | 0.00 |

| Slice Registers | 54 | 0 | 126800 | 0.04 |

| Register as Flip Flop | 54 | 0 | 126800 | 0.04 |

| Register as Latch | 0 | 0 | 126800 | 0.00 |

| F7 Muxes | 8 | 0 | 31700 | 0.03 |

| F8 Muxes | 4 | 0 | 15850 | 0.03 |

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4. IO and GT Specific

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+-----------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-----------------------------+------+-------+-----------+-------+

| Bonded IOB | 25 | 0 | 210 | 11.90 |

7. Primitives

+----------+------+---------------------+

| Ref Name | Used | Functional Category |

+----------+------+---------------------+

| LUT4 | 43 | LUT |

| LUT6 | 19 | LUT |

| OBUF | 15 | IO |

| IBUF | 10 | IO |

| LUT1 | 3 | LUT |

| LUT3 | 1 | LUT |

| BUFG | 1 | Clock |

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