

3DQ5 Lab 4 Exercise Report: Exercise 1

Exercise 1

In this exercise, we were required to modify some code from experiment 3. This exercise involved invoking the DP-Rams to perform a series of arithmetic within the W and X 8-bit signed integer arrays. The first thing we did was set all the write enables to low due to them being active high. We started with the write enables to be off in the read state. We asserted them so that on transition to the write state they would be high making this operation readily available within this state. Within the write state we updated the read addresses and put all the write enables low and transitioned back to the read state. This process was repeated to handle the logic for the rest of the equations. The RAMS were true Dual Port so we could read/write simultaneously for faster operations than what a Single Port RAM would provide us with functionality of only being able to do these operations one at a time. On the last write state we reset the Read address and flip the state back to IDLE.