
[AI System Design – Term Project]

Optimizations of

AI Accelerator Networks

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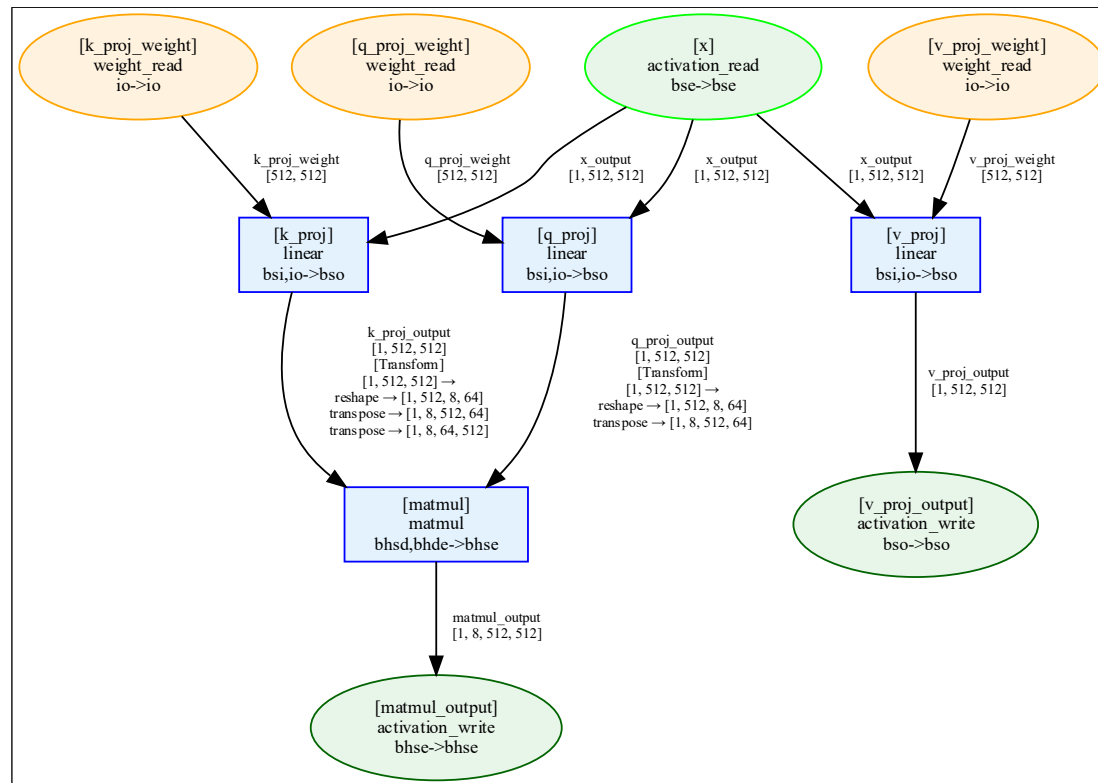
Outline

- ❑ Introduction
 - Target workload
 - NetTLMSim
- ❑ Problem to solve
- ❑ Reference codes
- ❑ Evaluation
- ❑ Submission

Target Workload

□ BERT-medium *Layer group A*

- Layer group 0 + matmul (QK^T)



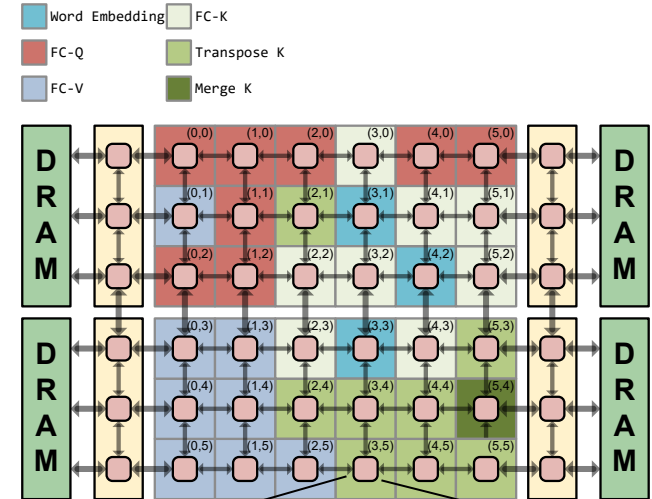
NetTLMSim

Virtual prototype

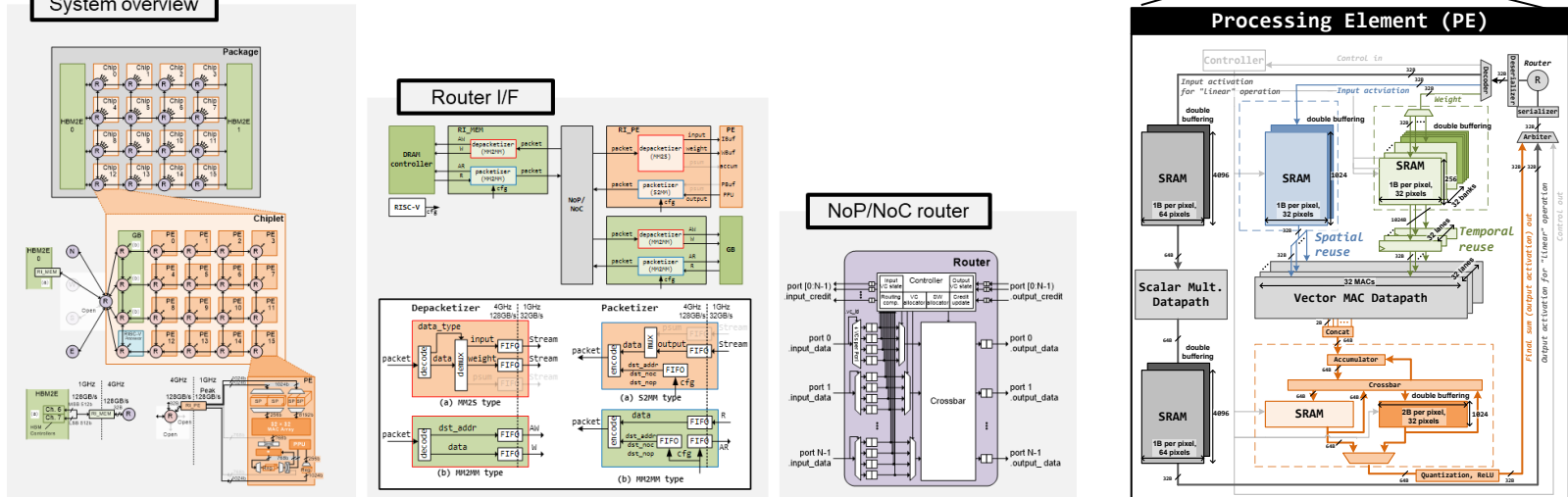
Assumed design parameters

Space-Time Mapping	Target Hardware	16 chiplets per package [1], 16 PEs per chiplet [1, 2], 1024 MACs per PE [1, 3] Total 512 TOPS at 1 GHz freq.	Memory Architecture	DRAM Type	HBM2E, 2 devices Total 1024 GB/s
	PE Style	NVDLA-like vector MAC array		SRAM Type	Dual port [3]
	Loop Order	OS-LWS [4]		Global Buf. Size, Bandwidth	640 KB activation storage [4], 128 GB/s per NoC router
Network Architecture	Topology	Mesh [2]		Local Buf. Size, Bandwidth	36 KB x2 (double buffered) [4], 128 GB/s at 1 GHz freq.
	Routing	DOR YX [2]		Precision	8 bits (24 bits for partial sums) [4]
	Flow Ctrl	Cut-through [2]			
	Packet Len	1 head flit, 16 body flits [2]			

[1] Cai et al. 2024 [3] Keller et al. 2023
[2] Zimmer et al. 2020 [4] Venkatesan et al. 2019



System overview

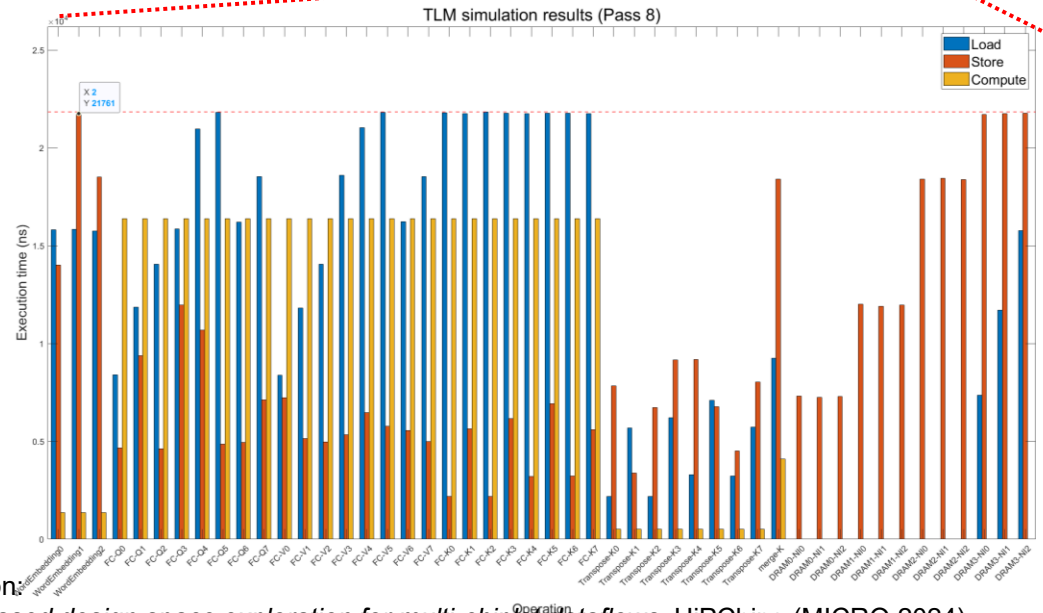
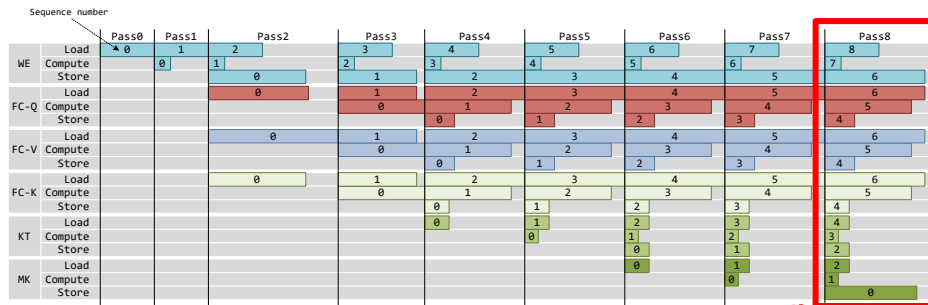
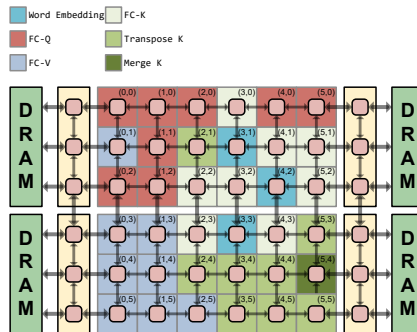


For more details, check the following presentation:

F. S. Park and C. S. Park, *Pre-RTL simulation based design space exploration for multi-chiplet dataflows*, HiPChips (MICRO 2024).

NetTLMSim

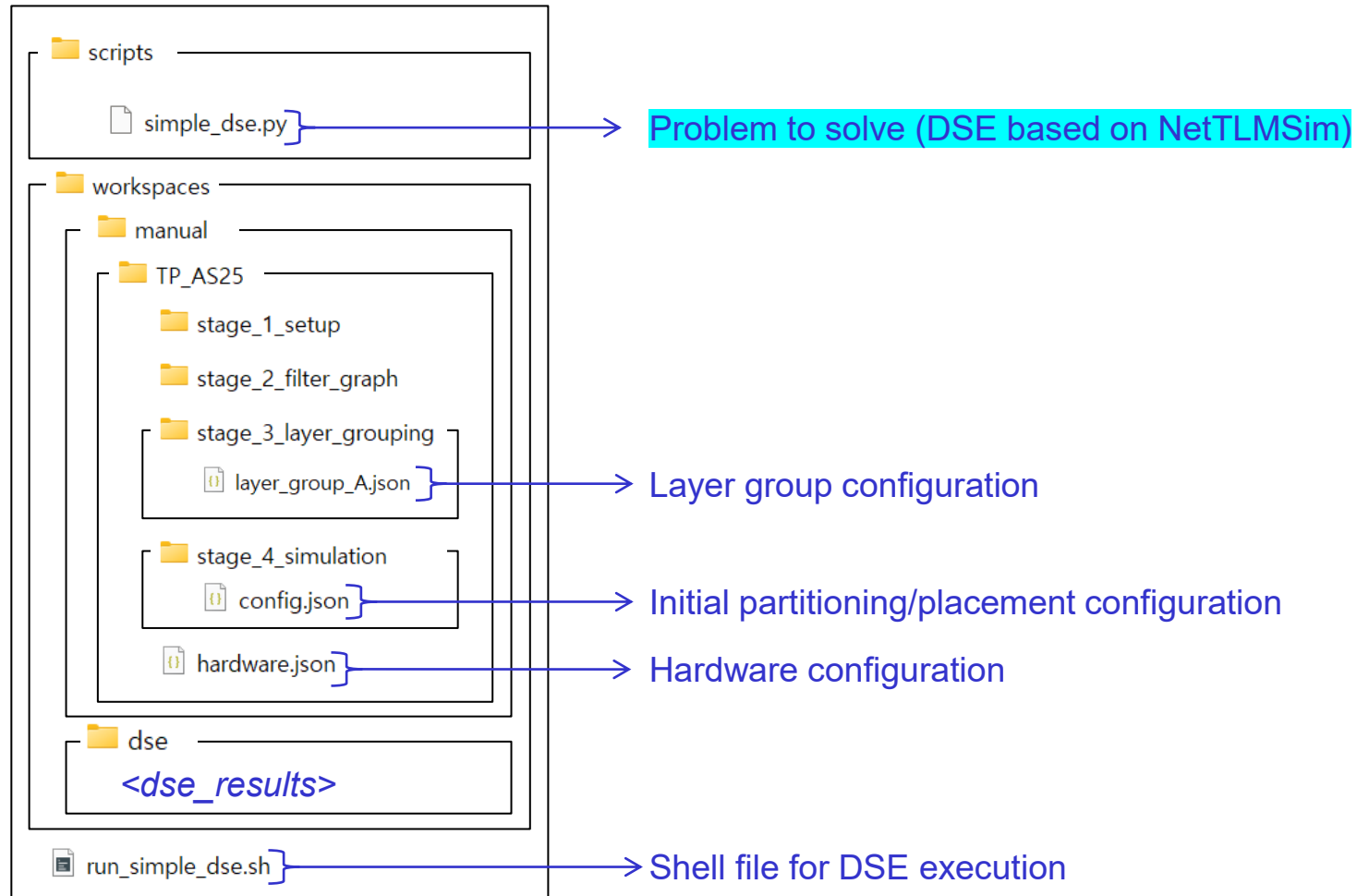
Virtual prototype (cont'd)



For more details, check the following presentation:
F. S. Park and C. S. Park, *Pre-RTL simulation based design space exploration for multi-chiplet dataflows*, HiPChips (MICRO 2024).

Reference Project

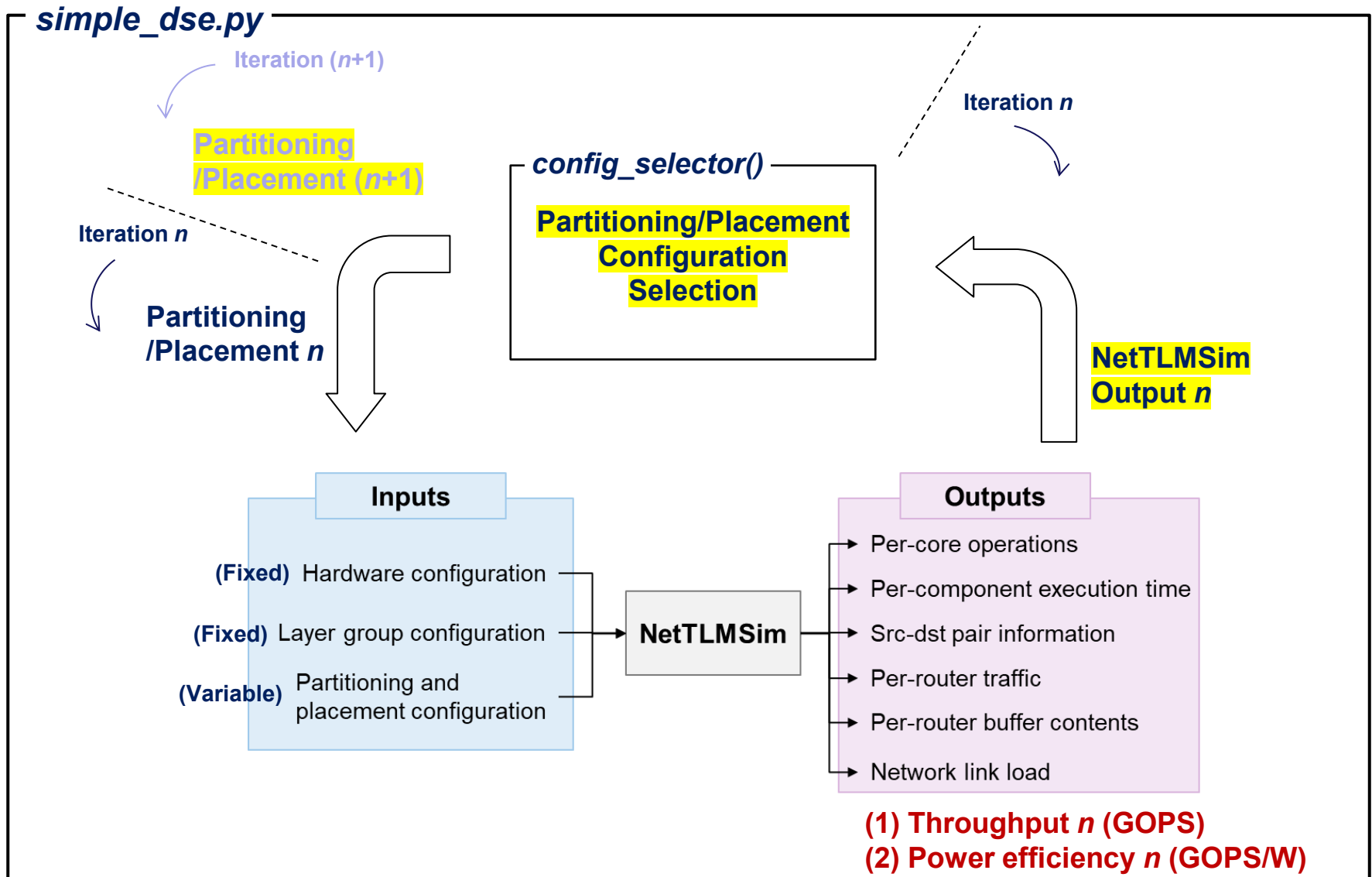
- ❑ Build project and run simulation (See *Appendix A*)



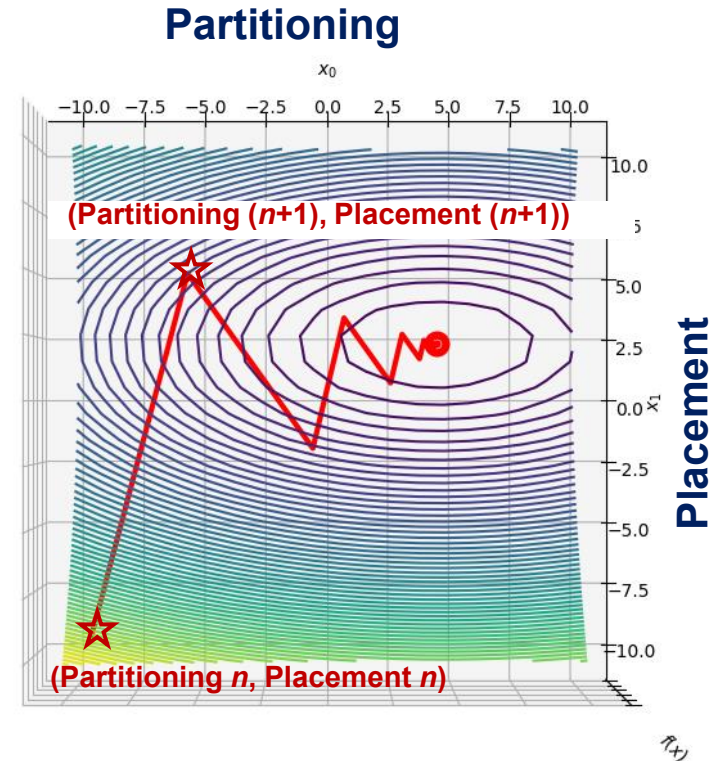
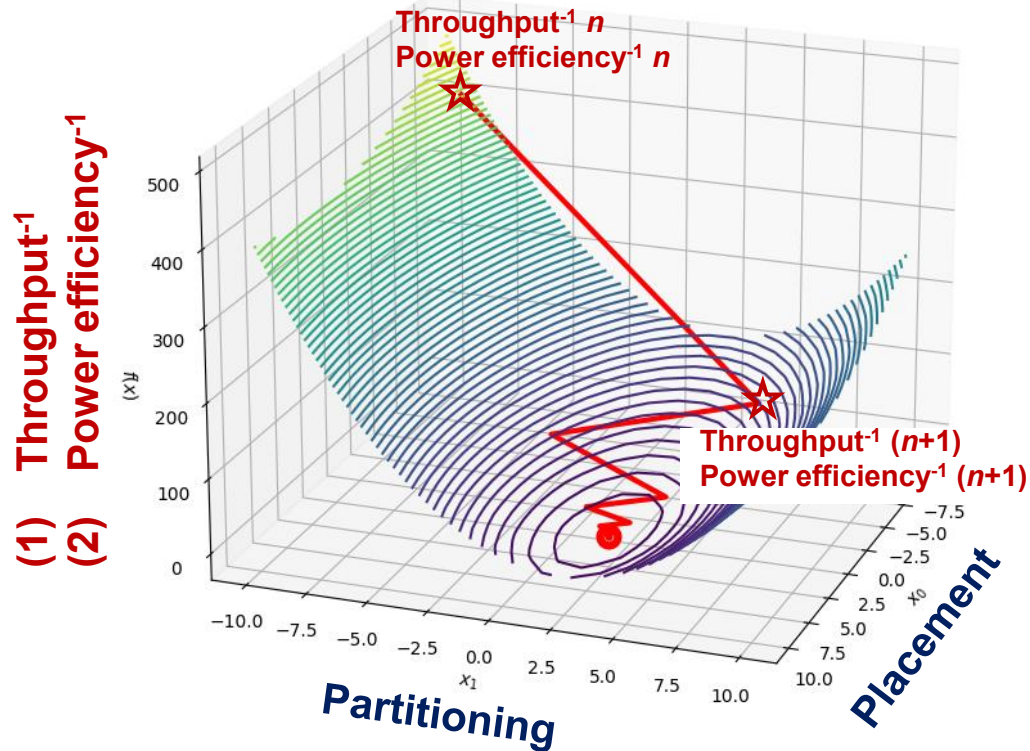
Problem to Solve

- ❑ Partitioning/placement configuration selection
 - Input: **NetTLMSim output** for the n -th iteration
 - Output: **NetTLMSim input** for the $(n+1)$ -th iteration
 - ✓ Only partitioning/placement configuration *varied*
 - ✓ Hardware/layer group configuration *kept fixed*

Problem to Solve



Problem to Solve

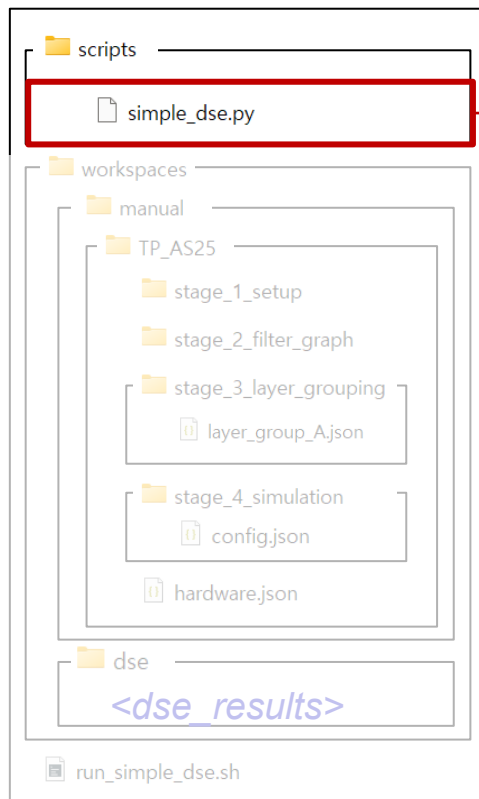


Design Constraints

- ❑ Optimize with respect to partition and placement only
 - You are ***not*** allowed to modify any other settings, e.g., hardware, layer group configurations etc.
 - ✓ Otherwise, it won't be considered for evaluation
- ❑ Run *no* additional simulations (e.g., those using NetTLMSim) *inside* the partitioning/placement configuration selection
 - Only a single simulation run is allowed per iteration.

Design Constraints

- ❑ Modify **only** (a part of) the body of *simple_dse.py*
 - You are allowed to change **only** the paragraphs between “*Edit code below*” and “*Edit code above*”



```
37 def config_selector(  
38     config: Dict[str, Any],  
39     iteration: int,  
40     allowed_groups: Optional[List[str]] = None,  
41     last_iter_dir: Optional[Path] = None,  
42 ) -> Dict[str, Any]:  
43     partitions = config.get("partitions")  
44     if not isinstance(partitions, dict):  
45         return config  
46     # Load last iteration logs  
47     if last_iter_dir.exists() & (iteration != 1):  
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```

```
47 if last_iter_dir.exists() & (iteration != 1):  
48     log_dir_path = last_iter_dir / "logs/layer_group_A"  
49     sim_result_path = last_iter_dir / "simulation_result.json"  
50     log_alloc_path = log_dir_path / "allocation.csv"  
51     log_exec_time_path = log_dir_path / "execution_time.csv"  
52     log_flowID_path = log_dir_path / "flowID.csv"  
53     log_link_load_path = log_dir_path / "link_load.csv"  
54     log_routers_path = list(log_dir_path.glob("router*.csv"))  
55     log_router_path = [f for f in log_routers_path if re.match(r"router_{d}\.csv$", f.name)]  
56     log_router_buf_path = [f for f in log_routers_path if re.match(r"router_{d}_buf\.csv$", f.name)]  
57     log_d2d_buf_path = list(log_dir_path.glob("d2d_{t}_buf.csv"))  
58  
59     with open(sim_result_path, "rb") as f:  
60         sim_result = orjson.loads(f.read())  
61         throughput = sim_result["data"]["summary"]["total_throughput_ops"]  
62         power_eff = sim_result["data"]["summary"]["power_efficiency_ops_per_w"]  
63         alloc = pd.read_csv(log_alloc_path)  
64         exec_time = pd.read_csv(log_exec_time_path)  
65         flowID = pd.read_csv(log_flowID_path)  
66         link_load = pd.read_csv(log_link_load_path)  
67         routers = [pd.read_csv(file, skipinitialspace=True) for file in log_router_path]  
68         router_bufs = [pd.read_csv(file, dtype=str, skipinitialspace=True) for file in log_router_buf_path]  
69         d2d_bufs = [pd.read_csv(file, dtype=str, skipinitialspace=True) for file in log_d2d_buf_path]
```

Using these variables to utilize the results from the previous iteration

Evaluation

- ❑ Submission completeness (10pt)
 - Reproducibility
- ❑ Optimality (40pt)
 - Final throughput and power efficiency
- ❑ DSE efficacy (30pt)
 - Sampling efficiency
 - General applicability
- ❑ Documentation (20pt)
 - Covering all those mentioned in the above

Submission Completeness

- ❑ Make sure that your submission is **complete**
 - In other words, it should be possible to **reproduce** your design together with the claimed throughput and power efficiency using **only** the files that you submitted by the submission deadline

Optimality

- ❑ Evaluated both **absolutely** and **relatively**
 - In other word, the quantity as well as the ranking matters
- ❑ Evaluate **separately** for throughput and power efficiency

DSE Efficacy

❑ Sampling efficiency

- Defined as the final quantity **divided by** the total number of iterations
 - ✓ Evaluates *how many simulation runs are required to reach the final throughput and power efficiency*
- Considered for **both** *training* (fine-tuning) and *inference* in the case of AI/ML (and separately, if necessary)
- The fewer iterations, the better sampling efficiency

❑ General applicability

- Evaluates whether the proposed idea is generally applicable
 - ✓ For example, different **layer group configurations** (including layer groups 0~2)
- May be further verified by extra hardware/layer group configurations

Submission

☐ Deadline

- **Dec. 12 (Fri), 10:00** GMT+9

☐ **Only one zip file** submission **per team** including the following files:

- Source code (**all** those needed to reproduce your results)
 - ✓ Except all those provided by TA (e.g., reference project)
- Documentation (PPT)
 - ✓ Including the explanation of the above source code

☐ Upload the zip file to the Ecampus

- Plus, send to chesterku2013@gmail.com as a *backup*

☐ You can post questions in the Ecampus (Q&A)

☐ Delayed submission will result in penalty!

Appendix A: Running a DSE

Runing a DSE

□ Start the DSE

- Open the terminal with '**Ctrl** + **`**'
- Type the following command and press '**Enter**'
 - ✓ `./run_simple_dse.sh TP_AS25 --layer-groups A --iterations N`
 - ✓ Set iteration count to **N**

