
[Microprocessor Applications – Term Project] FFT Accelerator with RISC-V

Chester Sungchung Park (박성정)
SoC Design Lab, Konkuk University
Webpage: <http://soclab.konkuk.ac.kr>

Outline

❑ Introduction

- Accelerator dataflow
- Transformer accelerator

❑ TP1: FFT accelerator w/ a single core

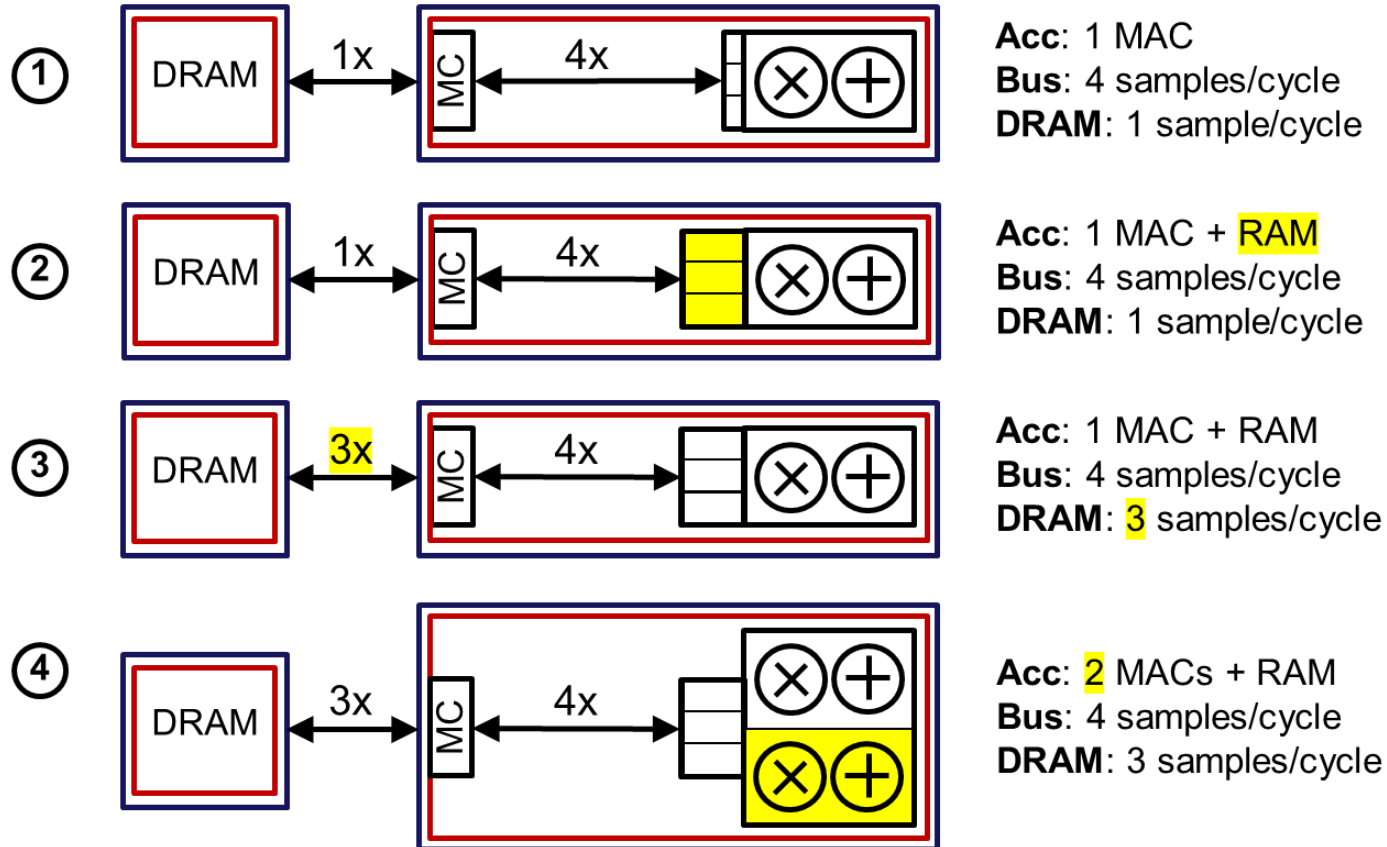
- Target system
- Reference project
- Design constraints
- Evaluation
- Submission

❑ TP2: FFT accelerator w/ multiple cores

- Target system
- Reference project
- Design constraints
- Evaluation
- Submission

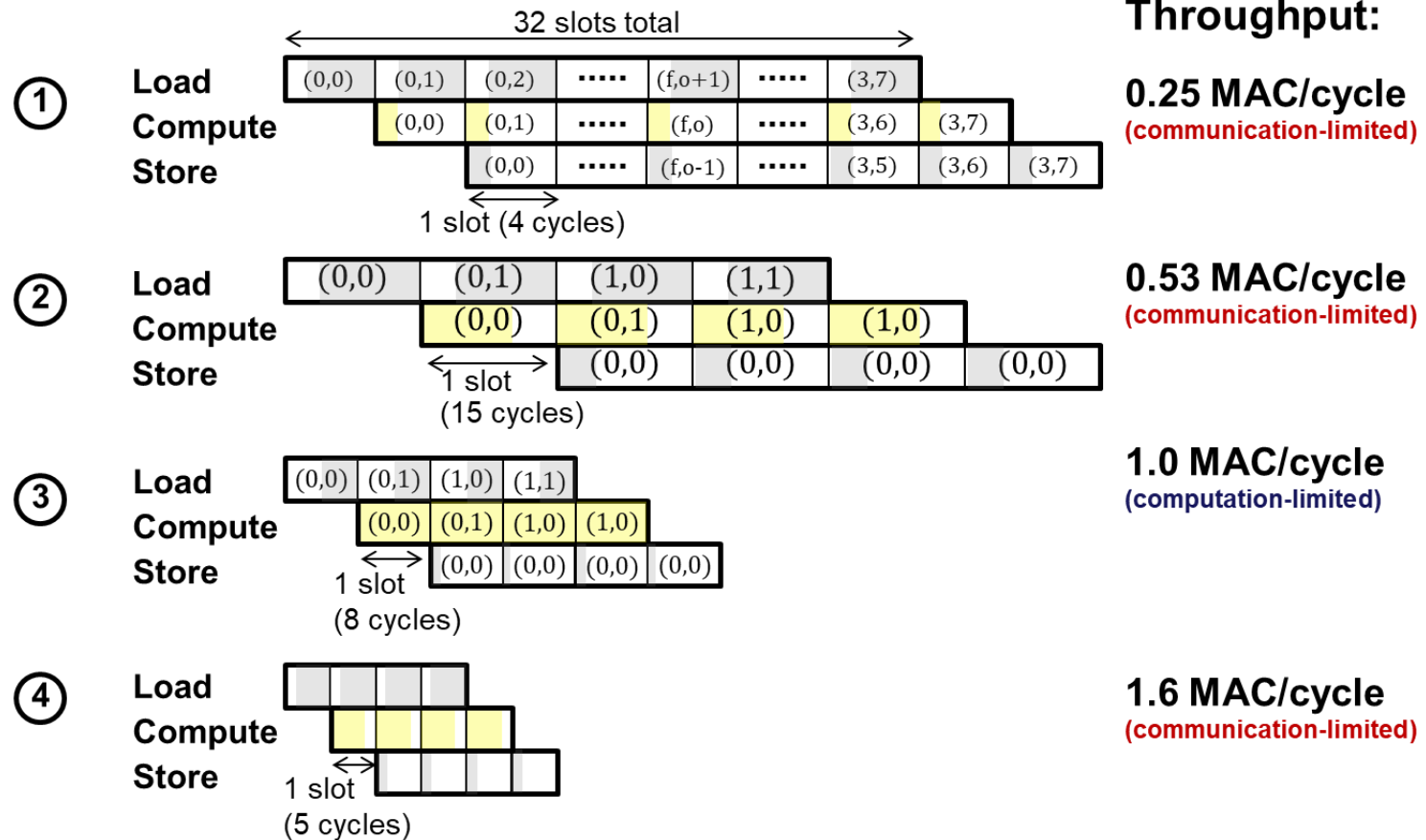
Accelerator Dataflow

□ Toy example



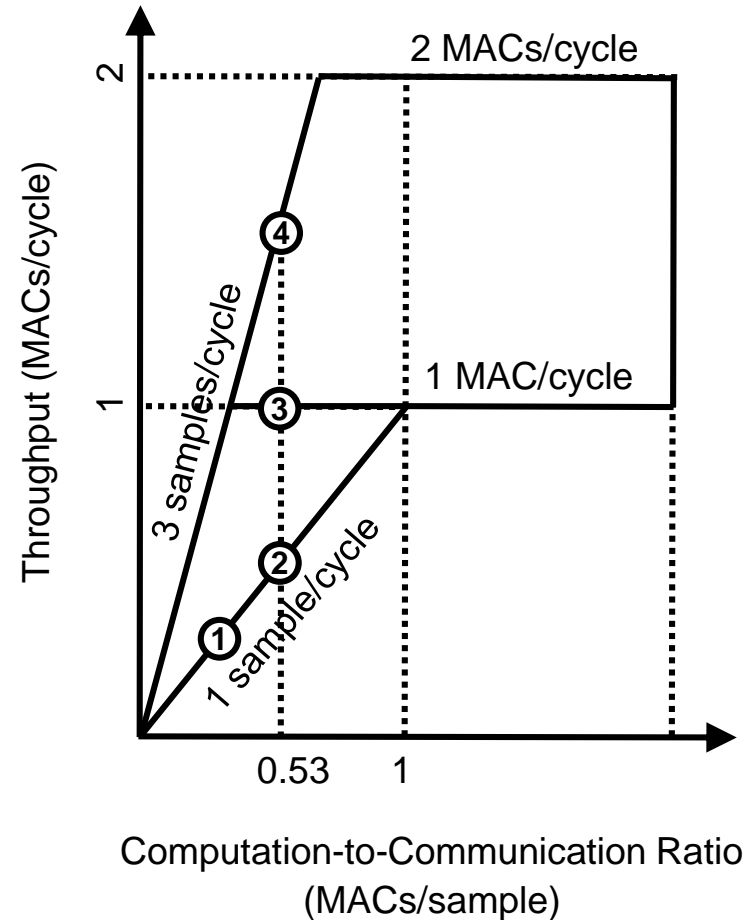
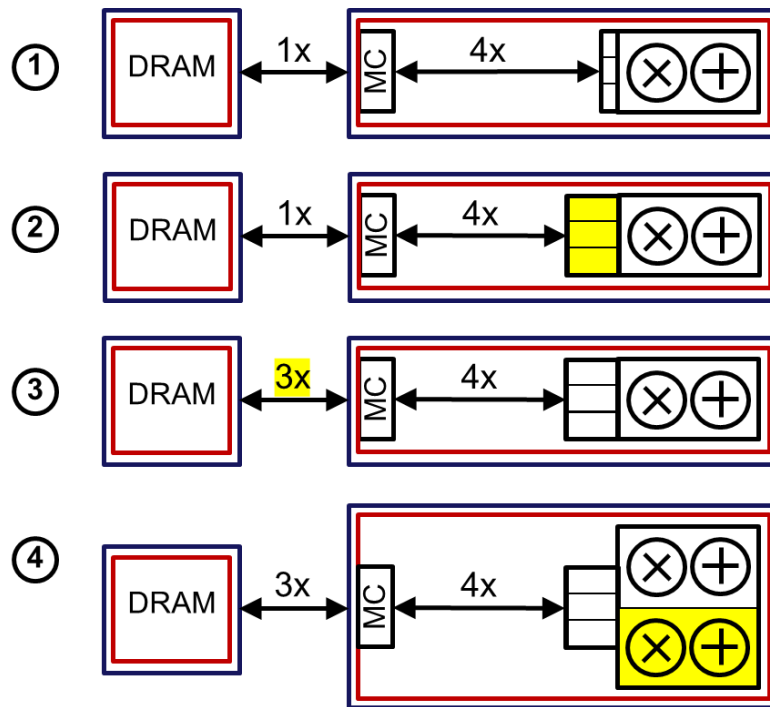
Accelerator Dataflow

❑ 3-stage pipeline (load-compute-store)



Accelerator Dataflow

Roofline model



For more details, check the following presentation:

C. S. Park, *Accelerator dataflow simulations and interconnect optimizations*, HSN 2024

Transformer Accelerator

□ GEMM-centric workload

GEMM

$$I \begin{matrix} K \\ A_{in} \end{matrix} \times K \begin{matrix} J \\ B_{in} \end{matrix} = I \begin{matrix} J \\ C_{out} \end{matrix}$$

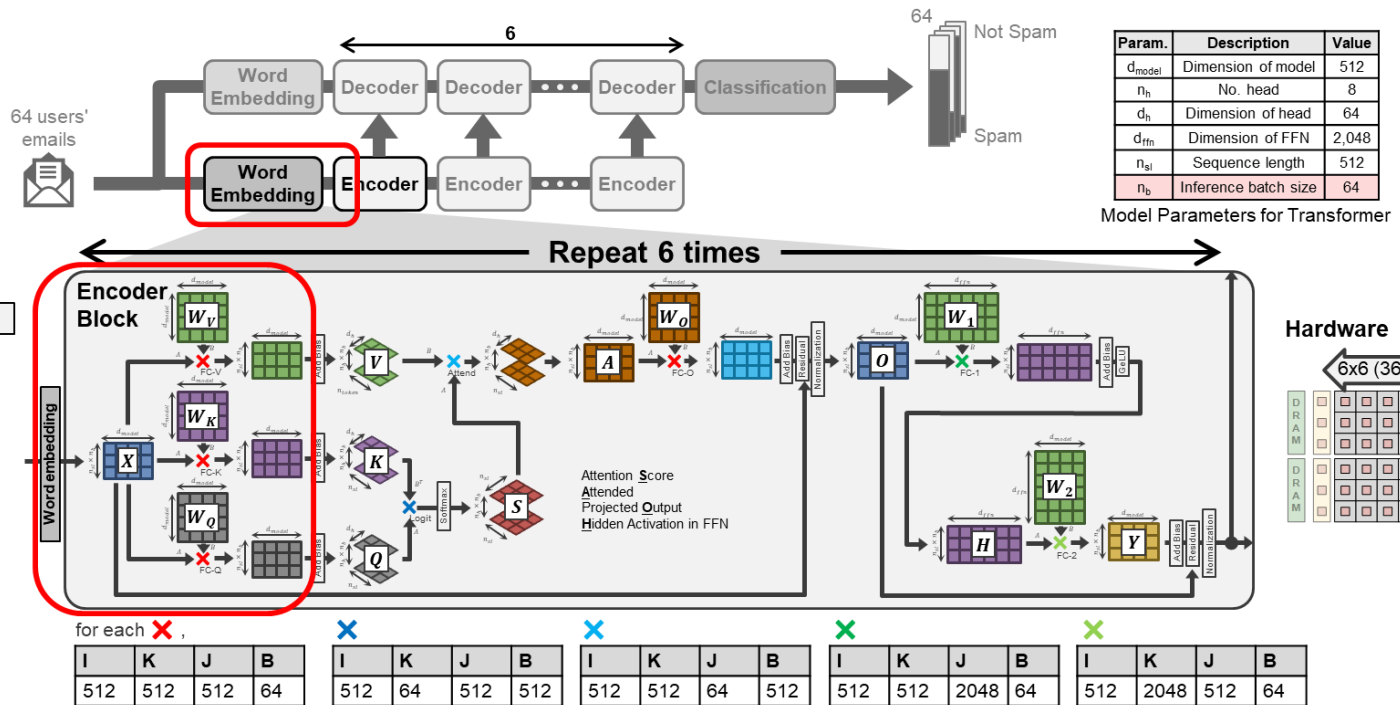
GEMM with batch
(\times \times \times)

$$B \begin{matrix} K \\ A_{in} \end{matrix} \times K \begin{matrix} J \\ B_{in} \end{matrix} = I \begin{matrix} J \\ C_{out} \end{matrix}$$

B-GEMM with batch
(\times \times)

$$B \begin{matrix} K \\ A_{in} \end{matrix} \times K \begin{matrix} J \\ B_{in} \end{matrix} = I \begin{matrix} J \\ C_{out} \end{matrix}$$

Input B reuse due to batch



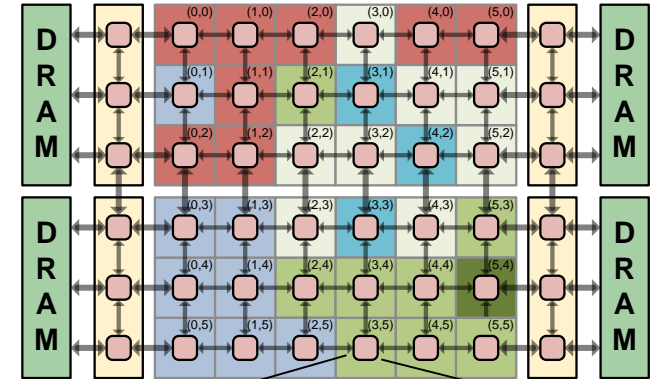
Transformer Accelerator

NetTLMSim

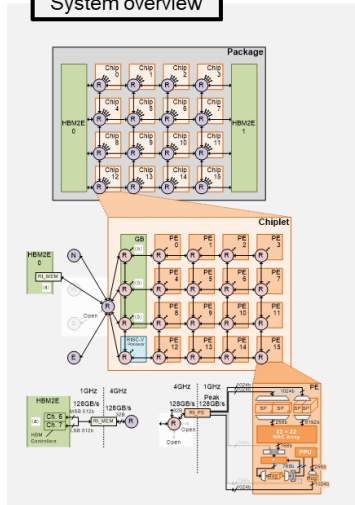
Assumed design parameters

Space-Time Mapping	Target Hardware	16 chiplets per package [1], 16 PEs per chiplet [1, 2], 1024 MACs per PE [1, 3] Total 512 TOPS at 1 GHz freq.	Memory Architecture	DRAM Type	HBM2E, 2 devices Total 1024 GB/s
	PE Style	NVDLA-like vector MAC array		SRAM Type	Dual port [3]
	Loop Order	OS-LWS [4]		Global Buf. Size, Bandwidth	640 KB activation storage [4], 128 GB/s per NoC router
Network Architecture	Topology	Mesh [2]		Local Buf. Size, Bandwidth	36 KB x2 (double buffered) [4], 128 GB/s at 1 GHz freq.
	Routing	DOR YX [2]		Precision	8 bits (24 bits for partial sums) [4]
	Flow Ctrl	Cut-through [2]			
	Packet Len	1 head flit, 16 body flits [2]			

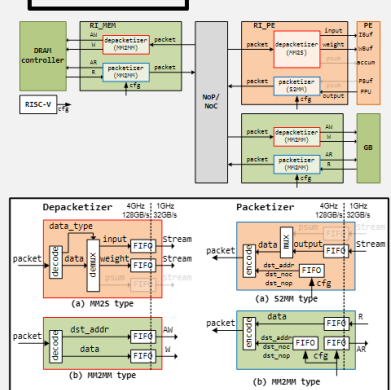
[1] Cai et al. 2024 [3] Keller et al. 2023
[2] Zimmer et al. 2020 [4] Venkatesan et al. 2019



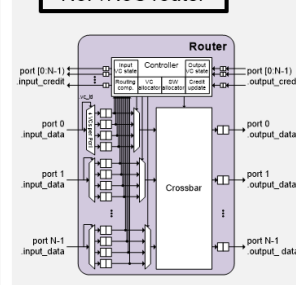
System overview



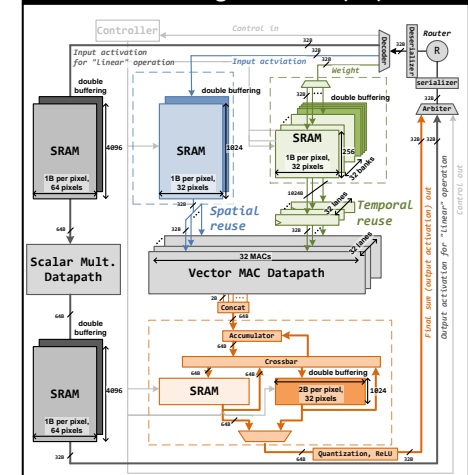
Router I/F



NoP/NoC router



Processing Element (PE)

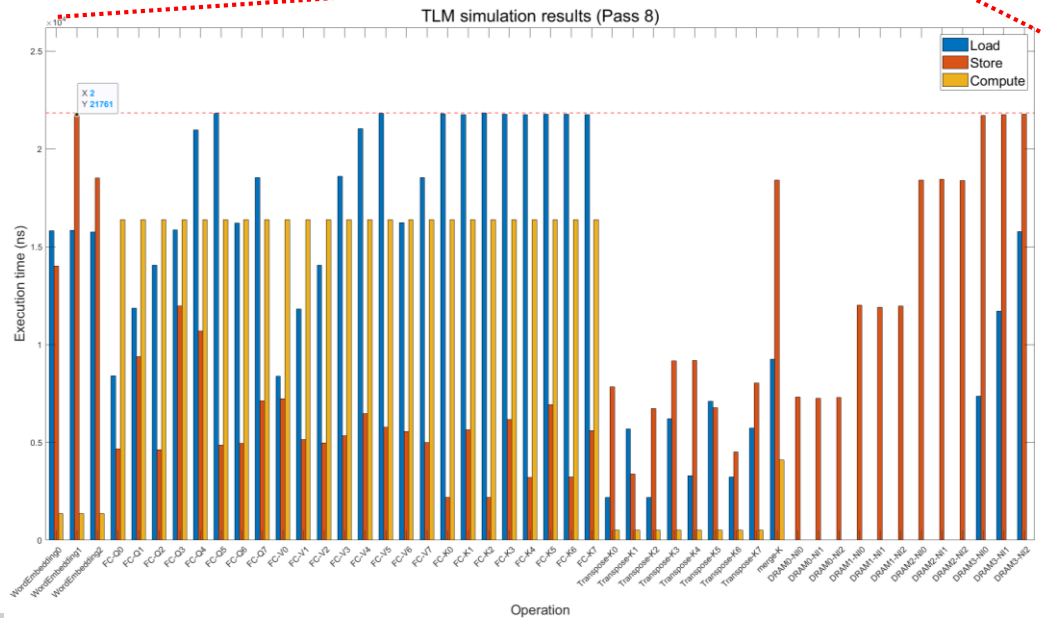
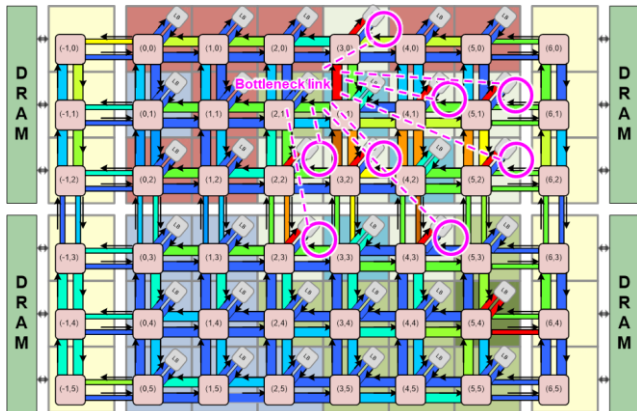
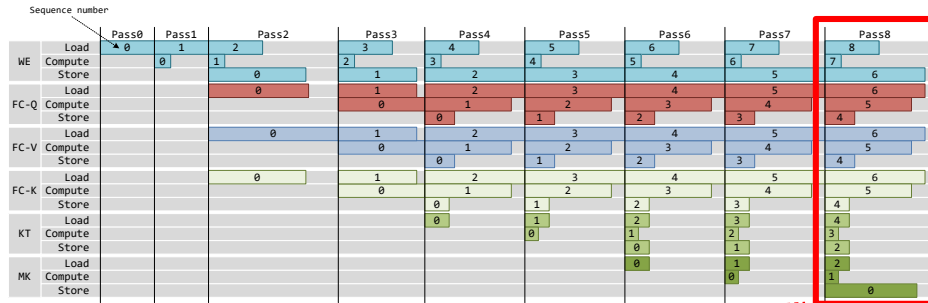
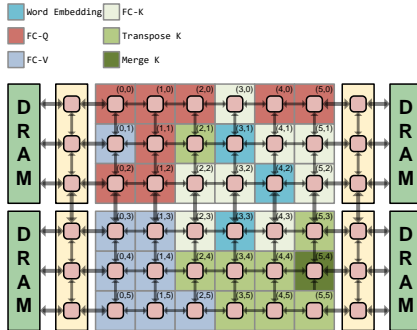


For more details, check the following presentation:

F. S. Park and C. S. Park, *Pre-RTL simulation based design space exploration for multi-chiplet dataflows*, HiPChips (MICRO 2024).

Transformer Accelerator

❑ NetTLMSim (cont'd)

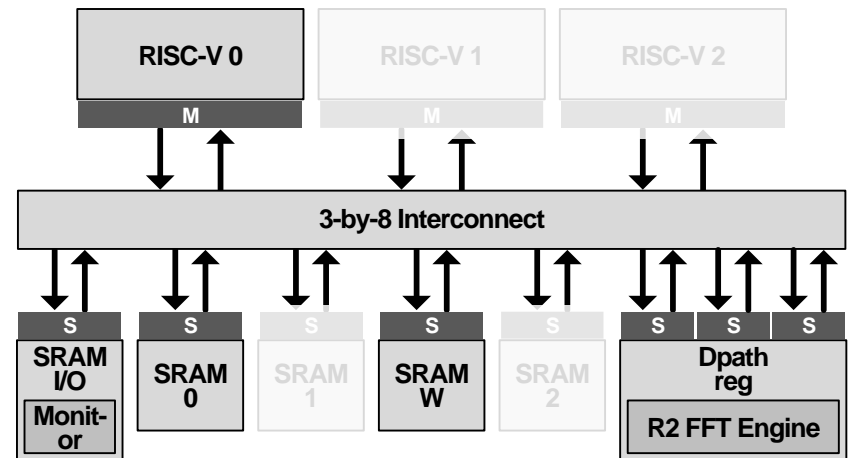


TP1: FFT Accelerator with a Single Core

Target System

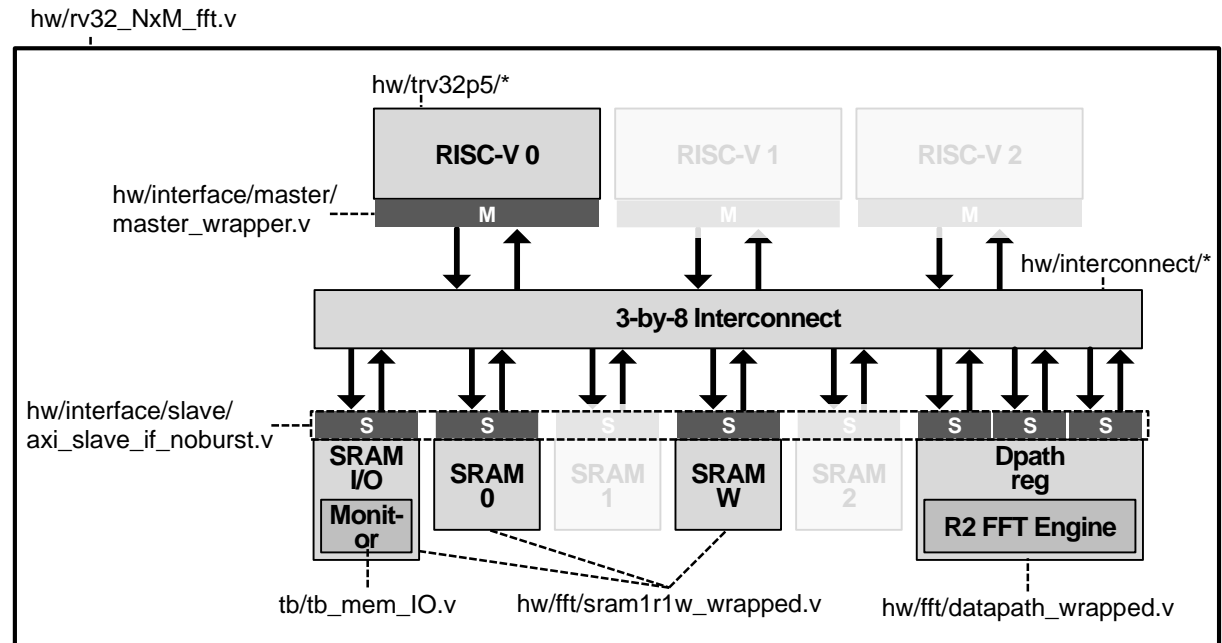
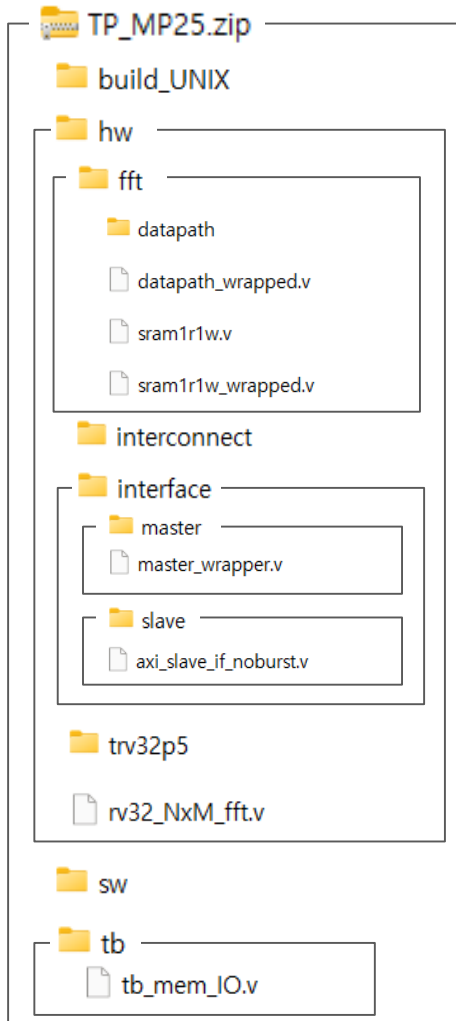
□ Overview

- 1 RISC-V core (RISC-V 0)
 - ✓ **Not** used for twiddle-factor multiplications & bufferflies
- 3-by-8 AXI interconnect
- SRAM
 - ✓ 1R1W
 - ✓ 3 banks (SRAM 0, I/O, W)
 - ✓ 16,384 lines/bank, 4 bytes/line
- R2 FFT engine
 - ✓ 5 32-bit I/O registers
 - ✓ Twiddle-factor multiplications & bufferflies (done only here!)
- Monitor
 - ✓ Counts No. output sets (3)



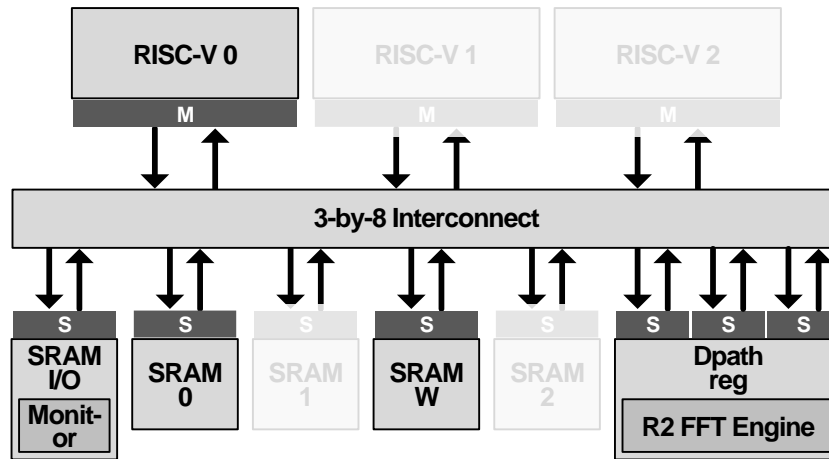
Target System

File Tree



Target System

□ Address map



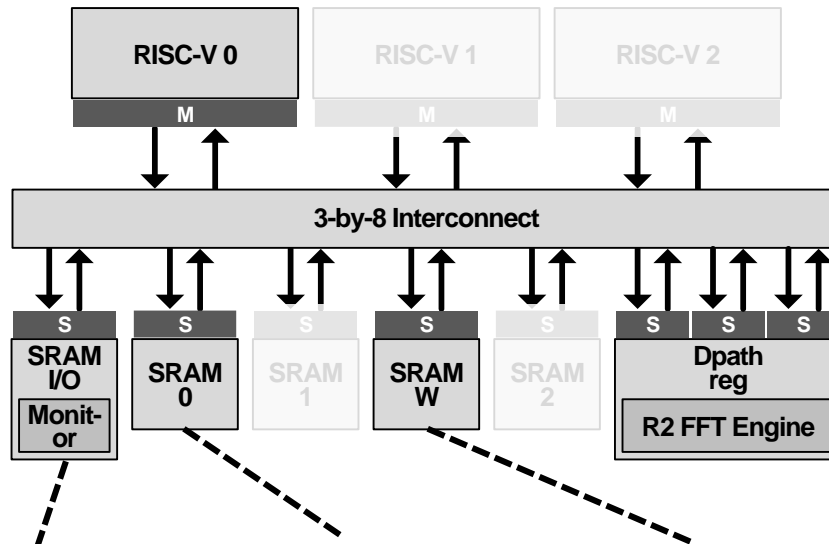
Name	31	Description	0	Address	Note
Input a	real number		imaginary number		0x0500_0000 write only
Output x	real number		imaginary number		0x0500_0004 read only
Input b	real number		imaginary number		0x0600_0000 write only
Output y	real number		imaginary number		0x0600_0004 read only
Input w	real number		imaginary number		0x0700_0000 write only

Address	Name
0xFFFF_FFFF	RESERVED
0x0700_0004	Dpath reg (port 2)
0x0700_0003	
0x0700_0000	RESERVED
0x06FF_FFFF	
0x0600_0008	Dpath reg (port 1)
0x0600_0007	
0x0600_0000	RESERVED
0x05FF_FFFF	
0x0500_0008	Dpath reg (port 0)
0x0500_0007	
0x0500_0000	RESERVED
0x04FF_FFFF	
0x0401_0000	SRAM 2
0x0400_FFFF	
0x0400_0000	RESERVED
0x03FF_FFFF	
0x0301_0000	SRAM W
0x0300_FFFF	
0x0300_0000	RESERVED
0x02FF_FFFF	
0x0201_0000	SRAM 1
0x0200_FFFF	
0x0200_0000	RESERVED
0x01FF_FFFF	
0x0101_0000	SRAM 0
0x0100_FFFF	
0x0100_0000	RESERVED
0x00FF_FFFF	
0x0001_0000	SRAM I/O
0x0000_FFFF	
0x0000_0000	

Target System

□ Data layout

- Initial condition



Address	Values in SRAM I/O
0x0000_FFFF	Zeros
0x0000_0B00	Golden Output
0x0000_0AFF	
0x0000_0800	Zeros
0x0000_07FF	
0x0000_0700	Output
0x0000_06FF	
0x0000_0400	Zeros
0x0000_03FF	
0x0000_0300	Input
0x0000_02FF	
0x0000_0000	

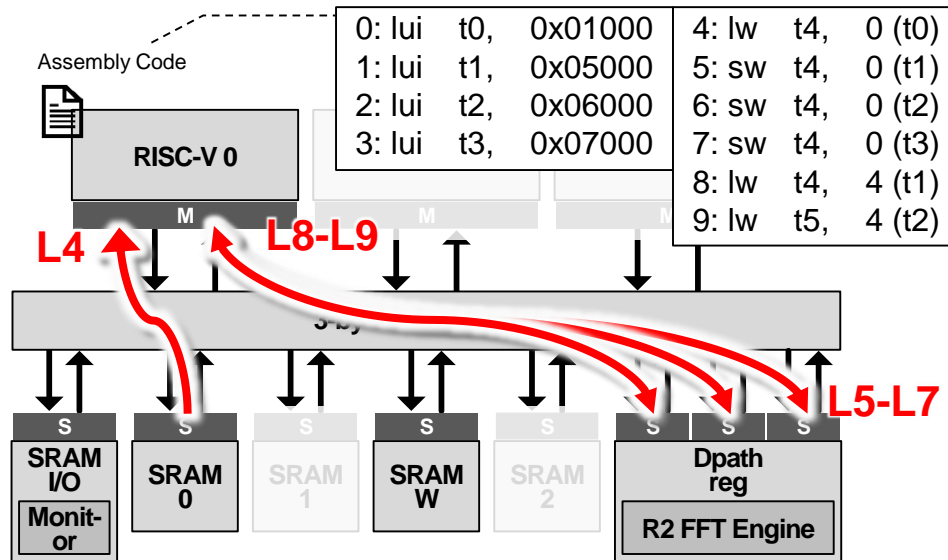
Address	Values in SRAM 0
0x01FF_FFFF	Zeros
0x0100_0080	

Address	Values in SRAM W
0x03FF_FFFF	Zeros
0x0300_0080	
0x0300_007F	Twiddle Factor
0x0300_0000	

Address	Name
0xFFFF_FFFF	RESERVED
0x0700_0004	
0x0700_0003	Dpath reg (port 2)
0x0700_0000	
0x06FF_FFFF	RESERVED
0x0600_0008	
0x0600_0007	Dpath reg (port 1)
0x0600_0000	
0x05FF_FFFF	RESERVED
0x0500_0008	
0x0500_0007	Dpath reg (port 0)
0x0500_0000	
0x04FF_FFFF	RESERVED
0x0401_0000	
0x0400_FFFF	SRAM 2
0x0400_0000	
0x03FF_FFFF	RESERVED
0x0301_0000	
0x0300_FFFF	SRAM W
0x0300_0000	
0x02FF_FFFF	RESERVED
0x0201_0000	
0x0200_FFFF	SRAM 1
0x0200_0000	
0x01FF_FFFF	RESERVED
0x0101_0000	
0x0100_FFFF	SRAM 0
0x0100_0000	
0x00FF_FFFF	RESERVED
0x0001_0000	
0x0000_FFFF	SRAM I/O
0x0000_0000	

Target System

□ Dataflow (example)



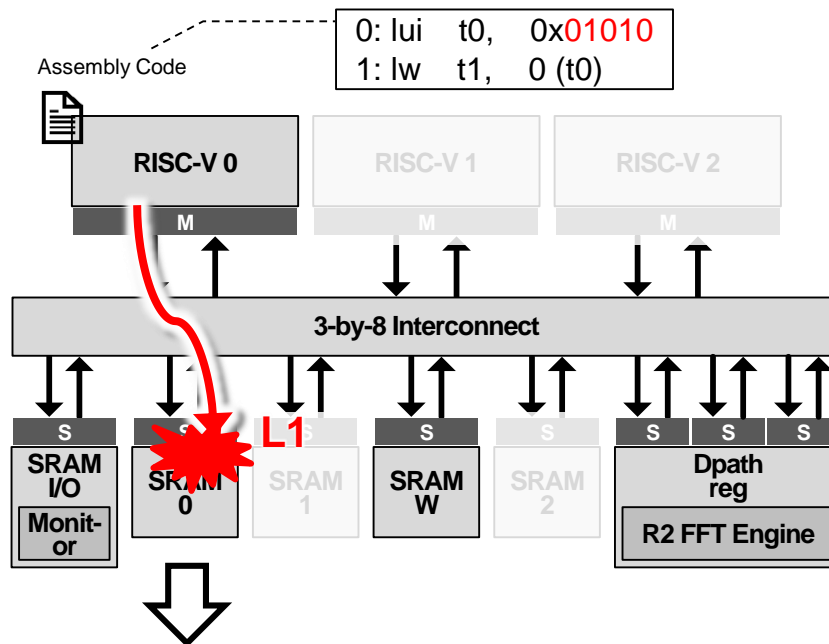
Name	31	Description	0	Address	Note
Input a	real number		imaginary number	0x0500_0000	write only
Output x	real number		imaginary number	0x0500_0004	read only
Input b	real number		imaginary number	0x0600_0000	write only
Output y	real number		imaginary number	0x0600_0004	read only
Input w	real number		imaginary number	0x0700_0000	write only

Address	Name
0xFFFF_FFFF	RESERVED
0x0700_0004	Dpath reg (port 2)
0x0700_0003	
0x0700_0000	RESERVED
0x06FF_FFFF	
0x0600_0008	Dpath reg (port 1)
0x0600_0007	
0x0600_0000	RESERVED
0x05FF_FFFF	
0x0500_0008	Dpath reg (port 0)
0x0500_0007	
0x0500_0000	RESERVED
0x04FF_FFFF	
0x0401_0000	SRAM 2
0x0400_FFFF	
0x0400_0000	RESERVED
0x03FF_FFFF	
0x0301_0000	SRAM W
0x0300_FFFF	
0x0300_0000	RESERVED
0x02FF_FFFF	
0x0201_0000	SRAM 1
0x0200_FFFF	
0x0200_0000	RESERVED
0x01FF_FFFF	
0x0101_0000	SRAM 0
0x0100_FFFF	
0x0100_0000	RESERVED
0x00FF_FFFF	
0x0001_0000	SRAM I/O
0x0000_FFFF	
0x0000_0000	

Target System

□ Dataflow (example) (cont'd)

- Warning messages for the *RESERVED* region (not mapped to SRAM/Dpath)



33 WARNING05: Invalid read address from master 1 to slave 2, got 0x01010000

Address	Name
0xFFFF_FFFF	RESERVED
0x0700_0004	Dpath reg (port 2)
0x0700_0003	
0x0700_0000	RESERVED
0x06FF_FFFF	
0x0600_0008	Dpath reg (port 1)
0x0600_0007	
0x0600_0000	RESERVED
0x05FF_FFFF	
0x0500_0008	Dpath reg (port 0)
0x0500_0007	
0x0500_0000	RESERVED
0x04FF_FFFF	
0x0401_0000	SRAM 2
0x0400_FFFF	
0x0400_0000	RESERVED
0x03FF_FFFF	
0x0301_0000	SRAM W
0x0300_FFFF	
0x0300_0000	RESERVED
0x02FF_FFFF	
0x0201_0000	SRAM 1
0x0200_FFFF	
0x0200_0000	RESERVED
0x01FF_FFFF	
0x0101_0000	SRAM 0
0x0100_FFFF	
0x0100_0000	RESERVED
0x00FF_FFFF	
0x0001_0000	SRAM I/O
0x0000_FFFF	
0x0000_0000	

Target System

□ Scenario

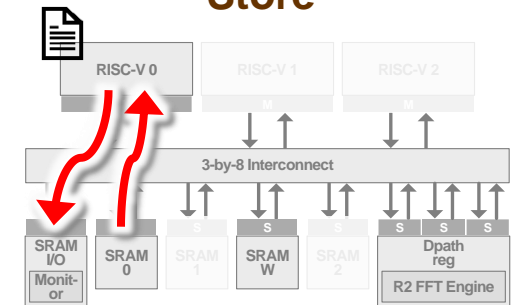
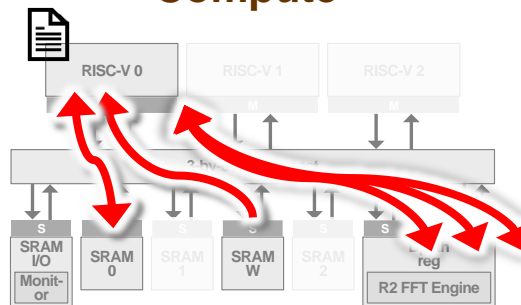
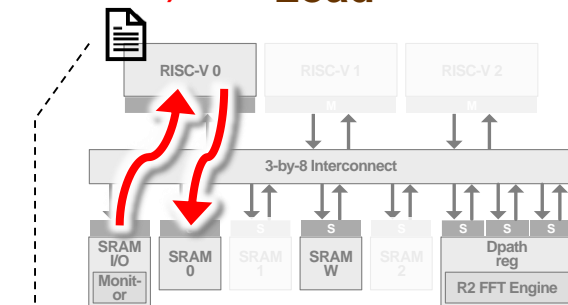
- 3-stage pipeline (load-compute-store)
- A total of 3 input/output sets

Program (ASM) (Handwritten)

Load

Compute

Store



Reference Code ('L_MP_9.pdf')

```

95 // load_input
96 for (j = 0; j < L_FFT; j++)
97 {
98     int rev = 0;
99     for (b = 0; b < N_STAGE; b++)
100     {
101         rev |= ((j >> b) & 1) << (N_STAGE - 1 - b);
102     }
103     SRAM0[rev] = input_region_of_SRAM10[set + L_FFT + j];
104 }
105 //

```

```

106 // compute_fft
107 n = 1 << N_STAGE;
108 l = 1;
109 k = N_STAGE - 1;
110 while (l < n)
111 {
112     istep = l << 1;
113     for (m = 0; m < l; ++m)
114     {
115         j = m << k;
116         twiddle = SRAM10[j];
117         for (i = m; i < n; i += istep)
118         {
119             j = i + l;
120             dpath_reg_0 = SRAM0[i];
121             dpath_reg_1 = SRAM0[j];
122             dpath_reg_2 = twiddle;
123             R2_FFT_Engine();
124             SRAM0[i] = dpath_reg_0;
125             SRAM0[j] = dpath_reg_1;
126         }
127     }
128     l = istep;
129 }
130
131 #ifdef DEBUG
132     //비활성 전처리기 블록
133 #endif
134 //

```

```

145 // store_output
146 for (j = 0; j < L_FFT; j++)
147     output_region_of_SRAM10[set + L_FFT + j] = SRAM0[j];
148 //

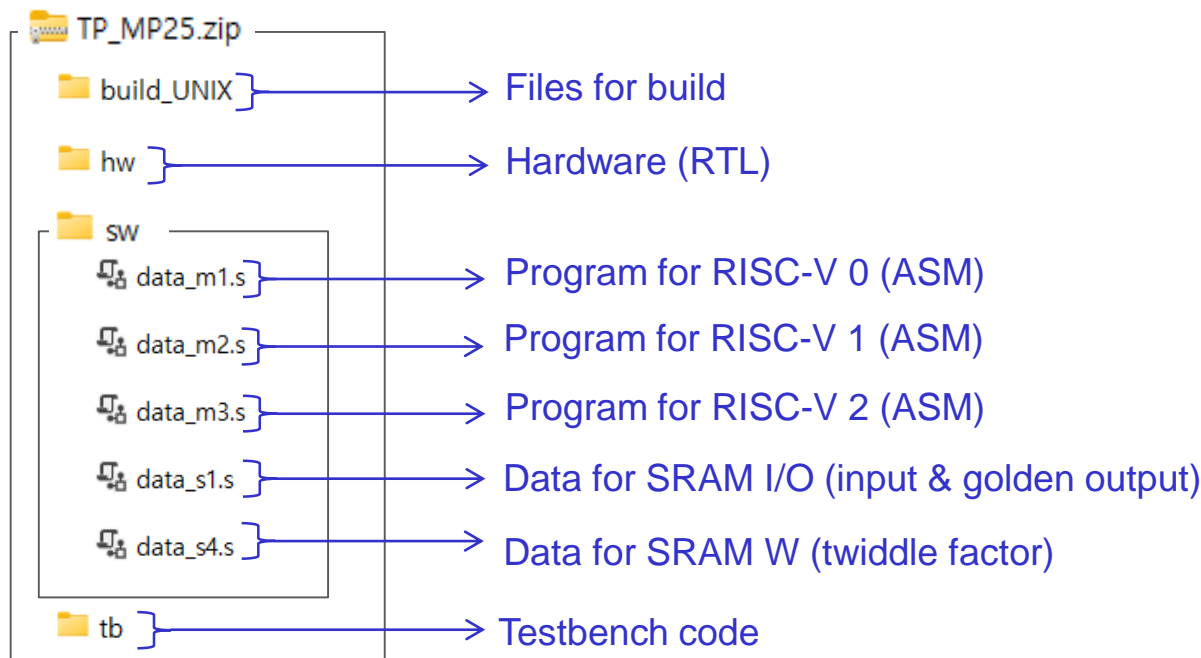
```


Reference Project

❑ Unzip '**TP_MP25.zip**'

- The input, golden output and twiddle factor values in '**data_s1.s**' and '**data_s4.s**' are set to be identical to those of the reference code (See '**L_MP_9.pdf**')

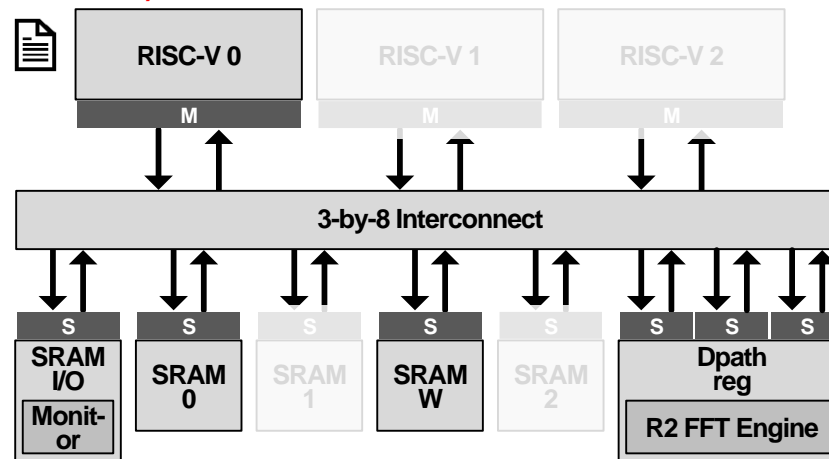
❑ Build project and run simulation (See **Appendix B**)



Design Constraints

- ❑ Design only the **software** part (ASM program)
 - You are **not** allowed to modify any other parts, e.g., the hardware part (RTL) of the target system
 - ✓ Otherwise, it won't be considered for evaluation

Program (ASM)
(Handwritten)

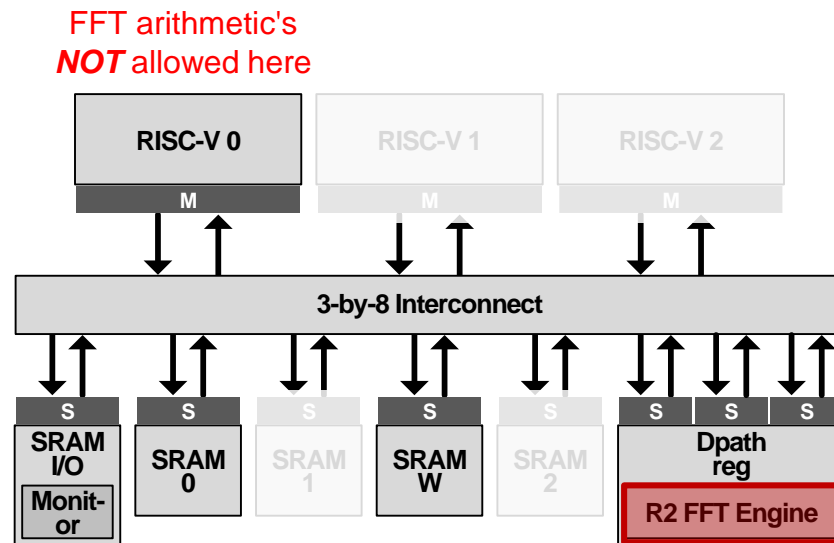


Design Constraints

❑ FFT arithmetic's **only** in datapath

- FFT arithmetic's defined as butterfly (additions/subtractions) and twiddle factor multiplications
- You are **not** allowed to use any other parts, e.g., the ALU inside RISC-V cores

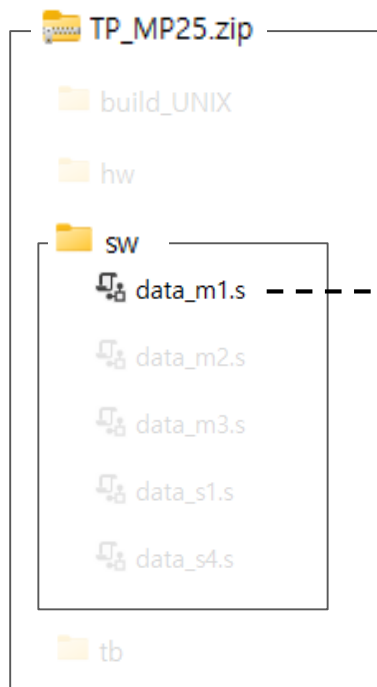
✓ Otherwise, it won't be considered for evaluation



FFT arithmetic's' allowed here

Design Constraints

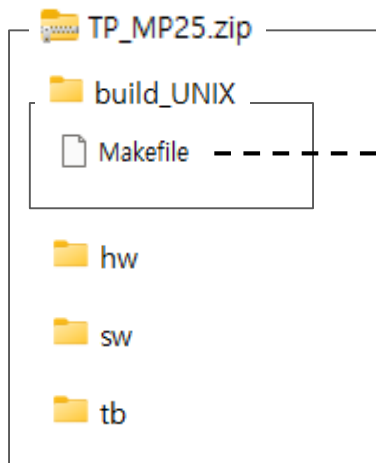
- ❑ Modify only (a part of) the body of ***data_m1.s***
 - You are allowed to change **only** the paragraphs between “***Edit code below***” and “***Edit code above***”



```
28 start_fft:
29
30 /* Edit Code Below */
31
32     mv      s11,  x0
33 input_loop:
34     bge     s11,  x0,    exit_input_loop
35 exit_input_loop:
36
37     mv      s11,  x0
38 dummy_loop:
39     bge     s11,  s7,    exit_dummy_loop
40     sw      x0,    0      (s4)
41     sw      x0,    0      (s5)
42     sw      x0,    0      (s6)
43     lw      t0,    4      (s4)
44     lw      t1,    4      (s5)
45     slli    s11,  s11,  2
46     add     s9,  s2,    s11
47     srli    s11,  s11,  2
48     sw      t0,    0      (s9)
49     addi    s11,  s11,  1
50     jal     s11,  dummy_loop
51 exit_dummy_loop:
52
53 /* Edit Code Above */
54
55     mv      s11,  x0
56 store_output:
```

Design Constraints

- ❑ Modify only (a part of) the body of ***data_m1.s*** (cont'd)
 - You should keep any other lines unchanged, for example, ***Makefile*** (that sets the instruction set to RV32I)
 - ✓ Otherwise, it won't be considered for evaluation



```
35 THISDIR = $(shell dirname $(realpath $(lastword $(MAKEFILE_LIST))))
36 VPATH = $(THISDIR)/../hw
37 APPDIR = $(THISDIR)/../sw
38 SIMDIR = $(THISDIR)/sim
39
40 AS      := /tools/binutils/riscv/riscv64-unknown-elf/bin/as
41 ASFLAGS := -march=rv32i -mabi=ilp32
42 OBJCOPY := /tools/binutils/riscv/riscv64-unknown-elf/bin/objcopy
43 PMFLAGS := -O verilog --verilog-data-width=1 -j .text
44 DMFLAGS := -O verilog --verilog-data-width=4 -j .data
45 APP = data
46
47 SRCS    := $(wildcard $(APPDIR)/*.s)
48 OBJS    := $(SRCS:.s=.o)
49 PMS     := $(SRCS:.s=.Pmb)
50 DMS     := $(SRCS:.s=.eDM)
51
52 SIMFLAGS := +fft_size=64 +num_sets=3
53
```

Evaluation

❑ Submission completeness

- Reproducibility (20pt)

❑ Accuracy

- Functionality (40pt)
 - ✓ In comparison to the golden output (provided in the reference project)

❑ Performance

- Execution time (20pt)
 - ✓ **Won't** be considered for evaluation, if functionality fails

❑ Documentation

- Explanation of the handwritten ASM code (20pt)

Reproducibility

- ❑ Make sure that your submission is **complete**
 - In other words, it should be possible to **reproduce** your design together with the claimed accuracy and performance using **only** the files that you submitted by the submission deadline

Functionality

❑ Run the simulation to check functionality (see **Appendix B**)

- For the 3 output sets, **all** the 192 output samples must **exactly match** those in the golden output.

```

Type: [All] Severity: [All] Code: [All]
- Mismatch @ output[0x00ad]: expected 0x098efed2, got 0x00000000
- Mismatch @ output[0x00ae]: expected 0xfe8cf90d, got 0x00000000
- Mismatch @ output[0x00af]: expected 0x0073f8e6, got 0x00000000
- Mismatch @ output[0x00b0]: expected 0x0535f8e6, got 0x00000000
- Mismatch @ output[0x00b1]: expected 0xff7df8e3, got 0x00000000
- Mismatch @ output[0x00b2]: expected 0xfc380302, got 0x00000000
- Mismatch @ output[0x00b3]: expected 0xfcfb03c4, got 0x00000000
- Mismatch @ output[0x00b4]: expected 0x01a2042e, got 0x00000000
- Mismatch @ output[0x00b5]: expected 0x03ba023e, got 0x00000000
- Mismatch @ output[0x00b6]: expected 0xffbefe9c, got 0x00000000
- Mismatch @ output[0x00b7]: expected 0x0356029d, got 0x00000000
- Mismatch @ output[0x00b8]: expected 0xfaf0ff0b, got 0x00000000
- Mismatch @ output[0x00b9]: expected 0xfdd5fd2a, got 0x00000000
- Mismatch @ output[0x00ba]: expected 0x06040101, got 0x00000000
- Mismatch @ output[0x00bb]: expected 0xffda0489, got 0x00000000
- Mismatch @ output[0x00bc]: expected 0x0172ff69, got 0x00000000
- Mismatch @ output[0x00bd]: expected 0x0058fc94, got 0x00000000
- Mismatch @ output[0x00be]: expected 0xfba8fc7d, got 0x00000000
- Mismatch @ output[0x00bf]: expected 0x068101c8, got 0x00000000
- Total mismatches: 192 / 192
Checking SRAM occupancy...
Test failed. Ending simulation.
#finish called from file ".../tb/tb_mem_10.v", line 132.
#finish at simulation time 4776000
Simulation complete, time is 4776000 ps.
Log /History /Search Files /Search Identifiers /Open...
dve>
  
```

Result of the code in the reference project

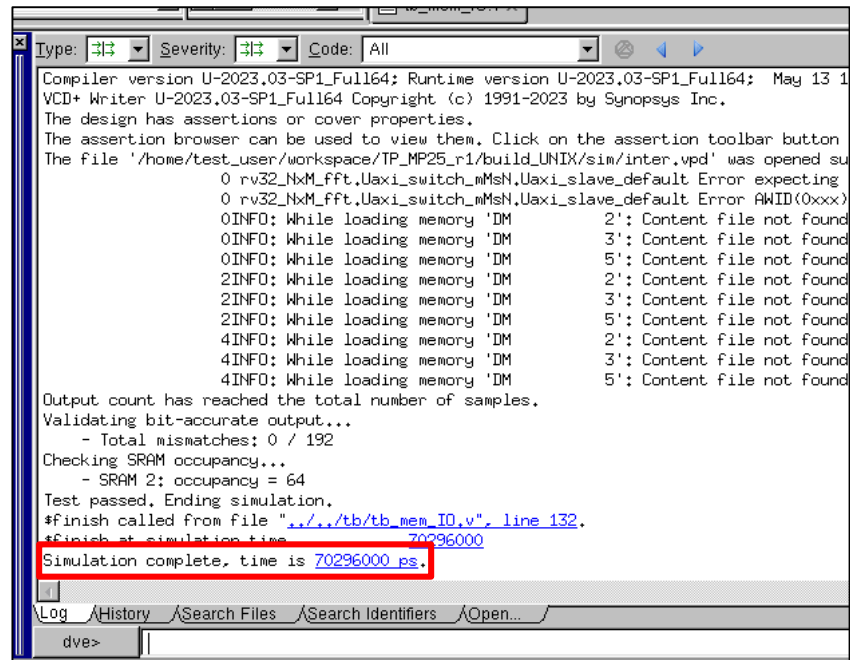
```

Type: [All] Severity: [All] Code: [All]
Compiler version U-2023.03-SP1_Full164; Runtime version U-2023.03-SP1_Full164; May 13 1
VCD+ Writer U-2023.03-SP1_Full164 Copyright (c) 1991-2023 by Synopsys Inc.
The design has assertions or cover properties.
The assertion browser can be used to view them. Click on the assertion toolbar button
The file '/home/test_user/workspace/TP_MP25_r1/build_UNIX/sim/inter.vpd' was opened su
0 rv32_NxM_fft.Uaxi_switch_mMsh.Uaxi_slave_default Error expecting
0 rv32_NxM_fft.Uaxi_switch_mMsh.Uaxi_slave_default Error AWID(0xxx)
0INFO: While loading memory 'DM' 2': Content file not found
0INFO: While loading memory 'DM' 3': Content file not found
0INFO: While loading memory 'DM' 5': Content file not found
2INFO: While loading memory 'DM' 2': Content file not found
2INFO: While loading memory 'DM' 3': Content file not found
2INFO: While loading memory 'DM' 5': Content file not found
4INFO: While loading memory 'DM' 2': Content file not found
4INFO: While loading memory 'DM' 3': Content file not found
4INFO: While loading memory 'DM' 5': Content file not found
Output count has reached the total number of samples.
Validating bit-accurate output
- Total mismatches: 0 / 192
Checking SRAM occupancy...
- SRAM 2: occupancy = 64
Test passed. Ending simulation.
#finish called from file ".../tb/tb_mem_10.v", line 132.
#finish at simulation time 70296000
Simulation complete, time is 70296000 ps.
Log /History /Search Files /Search Identifiers /Open...
dve>
  
```

Result of the **corrected** code

Execution Time

- ❑ Run the target system to measure the execution time (see **Appendix A**)



The screenshot shows a simulation log window with a toolbar at the top containing filters for Type, Severity, and Code. The log text includes compiler and runtime versions, a copyright notice for Synopsys Inc., and a series of INFO messages about loading memory. The final line of the log, "Simulation complete, time is 70296000 ps.", is highlighted with a red rectangle. Below the log window, there is a toolbar with buttons for Log, History, Search Files, Search Identifiers, and Open...

```
Type: [Filter] Severity: [Filter] Code: All
Compiler version U-2023.03-SP1_Full164; Runtime version U-2023.03-SP1_Full164; May 13 1
VCD+ Writer U-2023.03-SP1_Full164 Copyright (c) 1991-2023 by Synopsys Inc.
The design has assertions or cover properties.
The assertion browser can be used to view them. Click on the assertion toolbar button
The file '/home/test_user/workspace/TP_MP25_r1/build_UNIX/sim/inter.vpd' was opened su
0 rv32_NxM_fft,Uaxi_switch_mMsN,Uaxi_slave_default Error expecting
0 rv32_NxM_fft,Uaxi_switch_mMsN,Uaxi_slave_default Error AWID(0xxx)
0INFO: While loading memory 'DM      2': Content file not found
0INFO: While loading memory 'DM      3': Content file not found
0INFO: While loading memory 'DM      5': Content file not found
2INFO: While loading memory 'DM      2': Content file not found
2INFO: While loading memory 'DM      3': Content file not found
2INFO: While loading memory 'DM      5': Content file not found
4INFO: While loading memory 'DM      2': Content file not found
4INFO: While loading memory 'DM      3': Content file not found
4INFO: While loading memory 'DM      5': Content file not found
Output count has reached the total number of samples.
Validating bit-accurate output...
- Total mismatches: 0 / 192
Checking SRAM occupancy...
- SRAM 2: occupancy = 64
Test passed. Ending simulation.
#finish called from file ".../tb/tb_mem_ID.v", line 132.
#finish at simulation time 70296000
Simulation complete, time is 70296000 ps.
```

Documentation

- ❑ Explain your handwritten ASM code
 - Only the paragraphs that you modified, i.e., those between ***“Edit code below”*** and ***“Edit code above”***
 - Plus, if you provide as much code detail as possible

Submission

☐ Deadline

- **May 30 (Fri), 15:00** GMT+9

☐ **Only one zip file** submission **per team** including the following files:

- **ASM code (*data_m1.s*)** (needed to reproduce your design)
- **Slideset file** (PPT) (explaining the handwritten ASM code)

☐ Upload the zip file to the Ecampus

- Send to chesterku2013@gmail.com as a *backup*

☐ You can post questions in the Ecampus (Q&A)

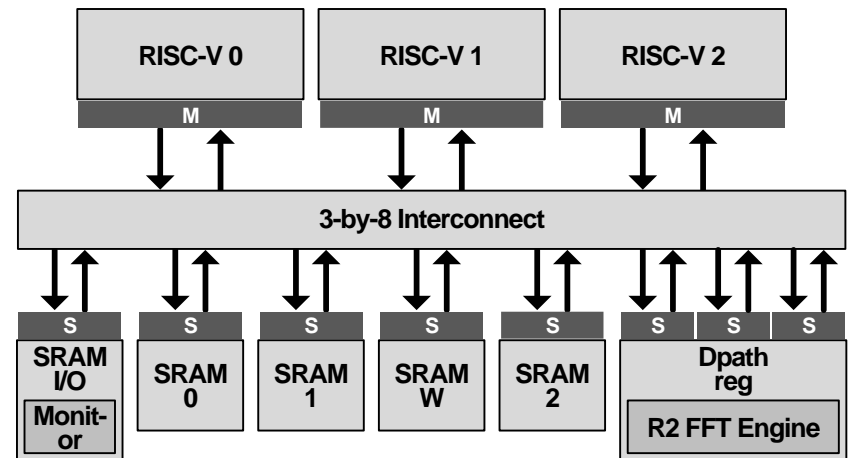
☐ Delayed submission will result in penalty!

TP2: FFT Accelerator with Multiple Cores

Target System

□ Overview

- **3 RISC-V cores** (RISC-V 0, 1, 2)
 - ✓ **Not** used for twiddle-factor multiplications & bufferflies
- 3-by-8 AXI interconnect
- SRAM
 - ✓ 1R1W
 - ✓ **5 banks** (SRAM 0, 1, 2, I/O, W)
 - ✓ 16,384 lines/bank, 4 bytes/line
- R2 FFT engine
 - ✓ 5 32-bit I/O registers
 - ✓ Twiddle-factor multiplications & bufferflies (**done only here!**)
- Monitor
 - ✓ Counts No. output sets (3)



Target System

☐ File Tree

- The same as for **TP1**

☐ Address map

- The same as for **TP1**

☐ Data layout

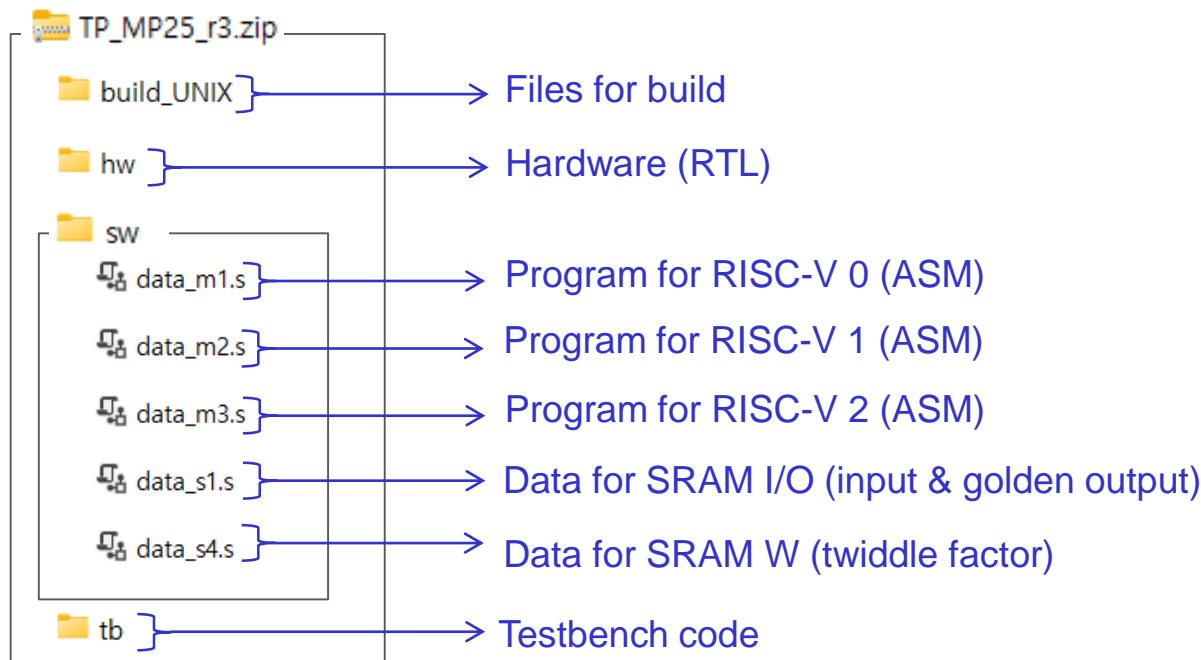
- The same as for **TP1**

Reference Project

❑ Unzip '***TP_MP25_r3.zip***'

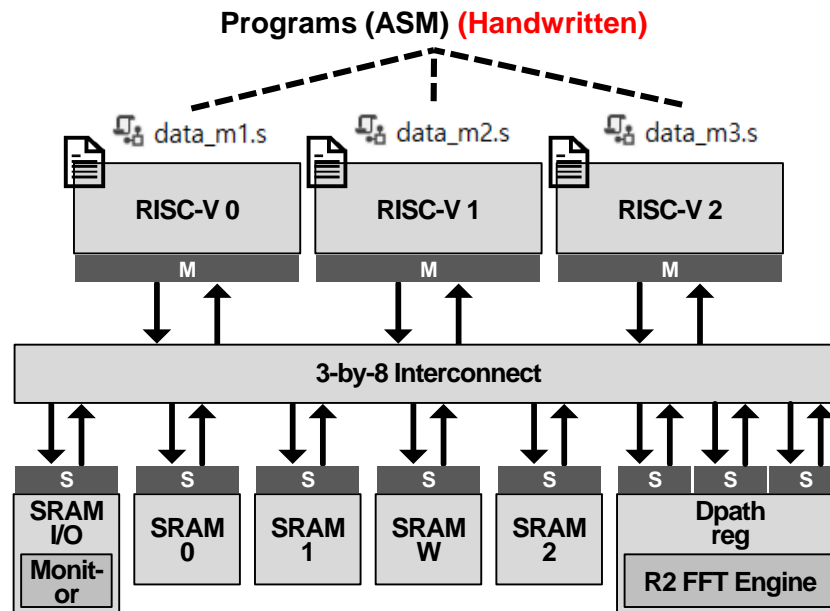
- The input, golden output and twiddle factor values in '***data_s1.s***' and '***data_s4.s***' are set to be identical to those of the reference code (See '***L_MP_9.pdf***')

❑ Build project and run simulation (See ***Appendix B***)



Design Constraints

- ❑ Design only the **software** parts (ASM programs)
 - You are **not** allowed to modify any other parts, e.g., the hardware part (RTL) of the target system
 - ✓ Otherwise, it won't be considered for evaluation

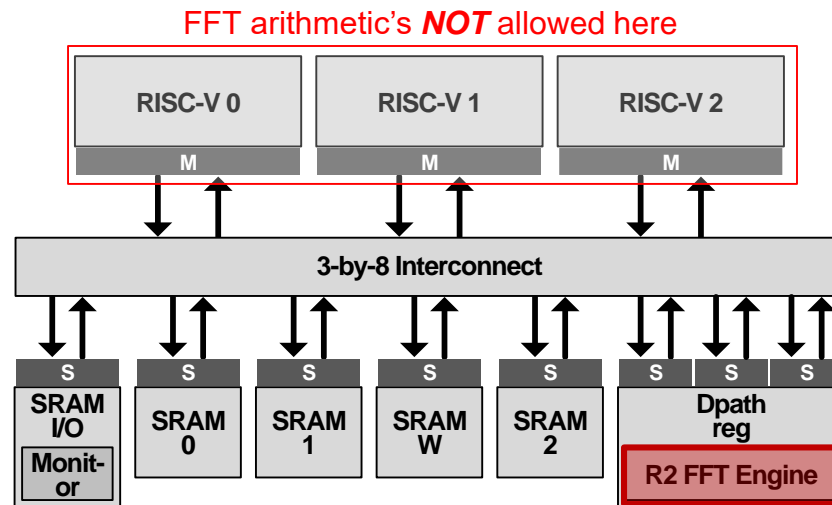


Design Constraints

❑ FFT arithmetic's **only** in datapath

- FFT arithmetic's defined as butterfly (additions/subtractions) and twiddle factor multiplications
- You are **not** allowed to use any other parts, e.g., the ALU inside RISC-V cores

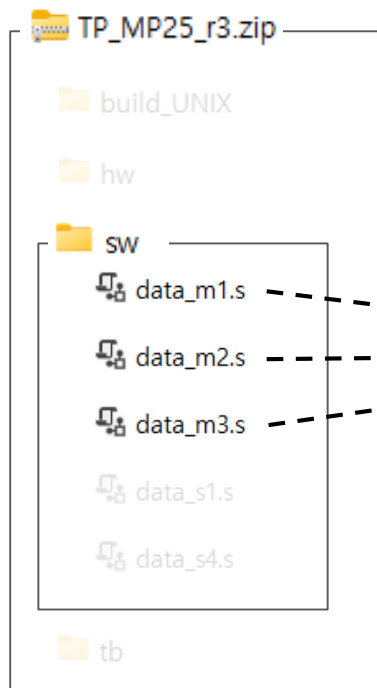
✓ Otherwise, it won't be considered for evaluation



FFT arithmetic's allowed here

Design Constraints

- ❑ Modify only (a part of) the body of ***data_m1.s***, ***data_m2.s***, and ***data_m3.s***
 - You are allowed to change **only** the paragraphs between “***Edit code below***” and “***Edit code above***”



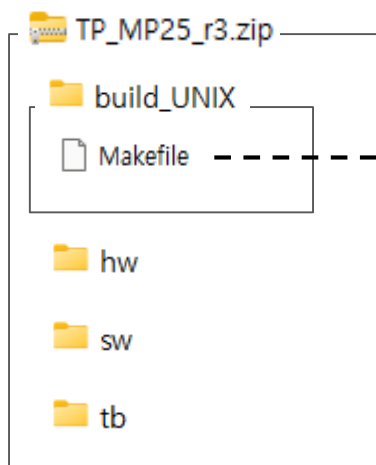
```

16  _main_init:
17
18  /* Edit Code Below */
19
20      lui    s2,    0x00000
21      lui    s4,    0x05000
22      lui    s5,    0x06000
23      lui    s6,    0x07000
24      li     s7,    64
25
26      mv     s11,   x0
27  dummy_loop:
28      bge    s11,   s7,    exit_dummy_loop
29      sw     x0,    0      (s4)
30      sw     x0,    0      (s5)
31      sw     x0,    0      (s6)
32      lw     t0,    4      (s4)
33      lw     t1,    4      (s5)
34      slli   s11,   s11,   2
35      add    s9,    s2,    s11
36      srli   s11,   s11,   2
37      sw     t0,    0      (s9)
38      addi   s11,   s11,   1
39      jal    x0,    dummy_loop
40  exit_dummy_loop:
41
42  /* Edit Code Above */

```

Design Constraints

- ❑ Modify only (a part of) the body of ***data_m1.s***, ***data_m2.s***, and ***data_m3.s*** (cont'd)
 - You should keep any other lines unchanged, for example, ***Makefile*** (that sets the instruction set to RV32I)
 - ✓ Otherwise, it won't be considered for evaluation



```
35 THISDIR = $(shell dirname $(realpath $(lastword $(MAKEFILE_LIST))))
36 VPATH = $(THISDIR)/../hw
37 APPDIR = $(THISDIR)/../sw
38 SIMDIR = $(THISDIR)/sim
39
40 AS      := /tools/binutils/riscv/riscv64-unknown-elf/bin/as
41 ASFLAGS := -march=rv32i -mabi=ilp32
42 OBJCOPY := /tools/binutils/riscv/riscv64-unknown-elf/bin/objcopy
43 PMFLAGS := -O verilog --verilog-data-width=1 -j .text
44 DMFLAGS := -O verilog --verilog-data-width=4 -j .data
45 APP = data
46
47 SRCS    := $(wildcard $(APPDIR)/*.s)
48 OBJS    := $(SRCS:.s=.o)
49 PMS     := $(SRCS:.s=.Pmb)
50 DMS     := $(SRCS:.s=.eDM)
51
52 SIMFLAGS := +fft_size=64 +num_sets=3
53
```

Design Constraints

- ❑ Do not skip the communication part
 - For each input/output set, load from/store to SRAM I/O
 - Compute on SRAM 0/1/2/W, **not** directly on SRAM I/O

Evaluation

❑ Submission completeness

- Reproducibility (20pt)

❑ Accuracy

- Functionality (20pt)
 - ✓ In comparison to the golden output (provided in the reference project)
 - ✓ Accompanied by code review (Q&A), if necessary

❑ Performance

- Execution time (20pt)
 - ✓ **Won't** be considered for evaluation, if functionality fails
 - ✓ Accompanied by code review (Q&A), if necessary

❑ Cost

- Effective memory capacity for SRAM 0~2 (20pt)
 - ✓ Defined as the **minimum** address region required for 3 input/output sets (see **Appendix D**)
 - ✓ The less capacity you propose, the better score you will get

❑ Documentation

- Explanation of the handwritten ASM codes (20pt)

Reproducibility

- ❑ Make sure that your submission is **complete**
 - In other words, it should be possible to **reproduce** your design together with the claimed accuracy and performance using **only** the files that you submitted by the submission deadline

Functionality

❑ Run the simulation to check functionality (see **Appendix B**)

- For the 3 output sets, **all** the 192 output samples must **exactly match** those in the golden output.

```

Type: [All] Severity: [All] Code: [All]
- Mismatch @ output[0x00ad]: expected 0x098efed2, got 0x00000000
- Mismatch @ output[0x00ae]: expected 0xfe8cf90d, got 0x00000000
- Mismatch @ output[0x00af]: expected 0x0073f8e6, got 0x00000000
- Mismatch @ output[0x00b0]: expected 0x0535f8e6, got 0x00000000
- Mismatch @ output[0x00b1]: expected 0xff7df8e3, got 0x00000000
- Mismatch @ output[0x00b2]: expected 0xfc380302, got 0x00000000
- Mismatch @ output[0x00b3]: expected 0xfcfb03c4, got 0x00000000
- Mismatch @ output[0x00b4]: expected 0x01a2042e, got 0x00000000
- Mismatch @ output[0x00b5]: expected 0x03ba023e, got 0x00000000
- Mismatch @ output[0x00b6]: expected 0xffbefe9c, got 0x00000000
- Mismatch @ output[0x00b7]: expected 0x0356029d, got 0x00000000
- Mismatch @ output[0x00b8]: expected 0xfaf0ff0b, got 0x00000000
- Mismatch @ output[0x00b9]: expected 0xfdd5fd2a, got 0x00000000
- Mismatch @ output[0x00ba]: expected 0x06040101, got 0x00000000
- Mismatch @ output[0x00bb]: expected 0xffda0489, got 0x00000000
- Mismatch @ output[0x00bc]: expected 0x0172ff69, got 0x00000000
- Mismatch @ output[0x00bd]: expected 0x0058fc94, got 0x00000000
- Mismatch @ output[0x00be]: expected 0xfba8fc7d, got 0x00000000
- Mismatch @ output[0x00bf]: expected 0x068101c8, got 0x00000000
- Total mismatches: 192 / 192
Checking SRAM occupancy...
Test failed. Ending simulation.
#finish called from file ".../tb/tb_mem_10.v", line 132.
#finish at simulation time 4776000
Simulation complete, time is 4776000 ps.
Log /History /Search Files /Search Identifiers /Open...
dve>

```

Result of the code in the reference project

```

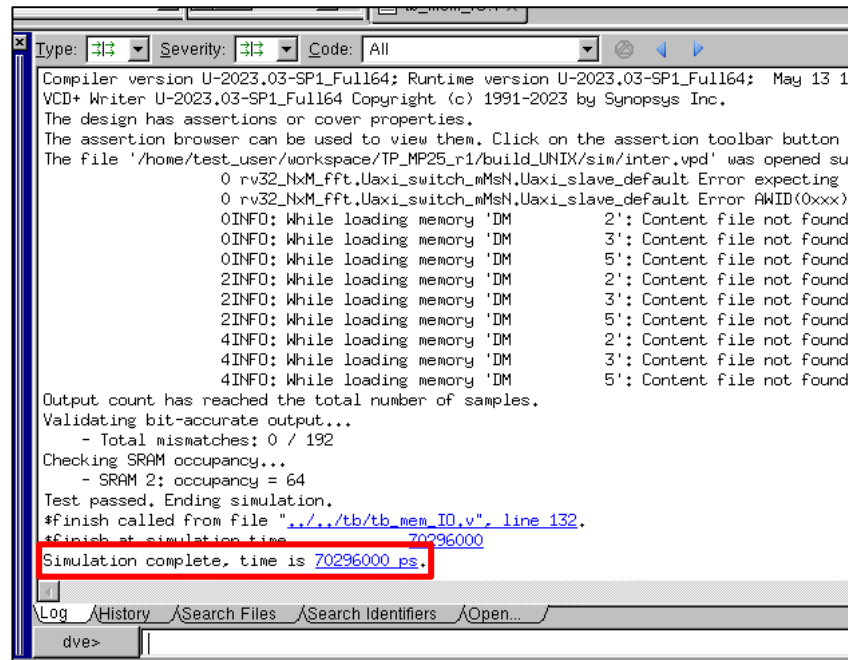
Type: [All] Severity: [All] Code: [All]
Compiler version U-2023.03-SP1_Full164; Runtime version U-2023.03-SP1_Full164; May 13 1
VCD+ Writer U-2023.03-SP1_Full164 Copyright (c) 1991-2023 by Synopsys Inc.
The design has assertions or cover properties.
The assertion browser can be used to view them. Click on the assertion toolbar button
The file '/home/test_user/workspace/TP_MP25_r1/build_UNIX/sim/inter.vpd' was opened su
0 rv32_NxM_fft.Uaxi_switch_mMsh.Uaxi_slave_default Error expecting
0 rv32_NxM_fft.Uaxi_switch_mMsh.Uaxi_slave_default Error AWID(0xxx)
0INFO: While loading memory 'DM' 2': Content file not found
0INFO: While loading memory 'DM' 3': Content file not found
0INFO: While loading memory 'DM' 5': Content file not found
2INFO: While loading memory 'DM' 2': Content file not found
2INFO: While loading memory 'DM' 3': Content file not found
2INFO: While loading memory 'DM' 5': Content file not found
4INFO: While loading memory 'DM' 2': Content file not found
4INFO: While loading memory 'DM' 3': Content file not found
4INFO: While loading memory 'DM' 5': Content file not found
Output count has reached the total number of samples.
Validating bit-accurate output
- Total mismatches: 0 / 192
Checking SRAM occupancy...
- SRAM 2: occupancy = 64
Test passed. Ending simulation.
#finish called from file ".../tb/tb_mem_10.v", line 132.
#finish at simulation time 70296000
Simulation complete, time is 70296000 ps.
Log /History /Search Files /Search Identifiers /Open...
dve>

```

Result of the **corrected** code

Execution Time

- ❑ Run the target system to measure the execution time (see **Appendix A**)



```
Type: [Error] Severity: [Error] Code: All
Compiler version U-2023.03-SP1_Full164; Runtime version U-2023.03-SP1_Full164; May 13 1
VCD+ Writer U-2023.03-SP1_Full164 Copyright (c) 1991-2023 by Synopsys Inc.
The design has assertions or cover properties.
The assertion browser can be used to view them. Click on the assertion toolbar button
The file '/home/test_user/workspace/TP_MP25_r1/build_UNIX/sim/inter.vpd' was opened su
0 rv32_NxM_fft,Uaxi_switch_mMsN,Uaxi_slave_default Error expecting
0 rv32_NxM_fft,Uaxi_switch_mMsN,Uaxi_slave_default Error AWID(0xxx)
0INFO: While loading memory 'DM' 2': Content file not found
0INFO: While loading memory 'DM' 3': Content file not found
0INFO: While loading memory 'DM' 5': Content file not found
2INFO: While loading memory 'DM' 2': Content file not found
2INFO: While loading memory 'DM' 3': Content file not found
2INFO: While loading memory 'DM' 5': Content file not found
4INFO: While loading memory 'DM' 2': Content file not found
4INFO: While loading memory 'DM' 3': Content file not found
4INFO: While loading memory 'DM' 5': Content file not found
Output count has reached the total number of samples.
Validating bit-accurate output...
- Total mismatches: 0 / 192
Checking SRAM occupancy...
- SRAM 2: occupancy = 64
Test passed. Ending simulation.
#finish called from file ".../tb/tb_mem_ID.v", line 132.
#finish at simulation time 70296000
Simulation complete, time is 70296000 ps.
```


Documentation

❑ **Screen capture** of the simulation results

- Show (1) the functionality (p. 39) and (2) the execution time (p. 40)
- Plus, if the relevant **roofline model** is correctly provide
 - ✓ Samuel Williams, Andrew Waterman, and David Patterson. 2009. Roofline: an insightful visual performance model for multicore architectures. Commun. ACM 52, 4 (April 2009)

Documentation

- ❑ Clear explanation your handwritten ASM codes
 - Only the paragraphs that you modified, i.e., those between ***“Edit code below”*** and ***“Edit code above”***

- ❑ Plus, if the relevant **ablation study** is well-documented
 - See ***Appendix C***

Submission

☐ Deadline

- **June 12 (Thu), 15:00** GMT+9

☐ **Only one zip file** submission **per team** including the following files:

- **ASM codes** (***data_m1.s***, ***data_m2.s***, and ***data_m3.s***)
(needed to reproduce your design)
- **Slideset file** (PPT) (explaining the handwritten ASM code)

☐ Upload the zip file to the Ecampus

- Send to chesterku2013@gmail.com as a *backup*

☐ You can post questions in the Ecampus (Q&A)

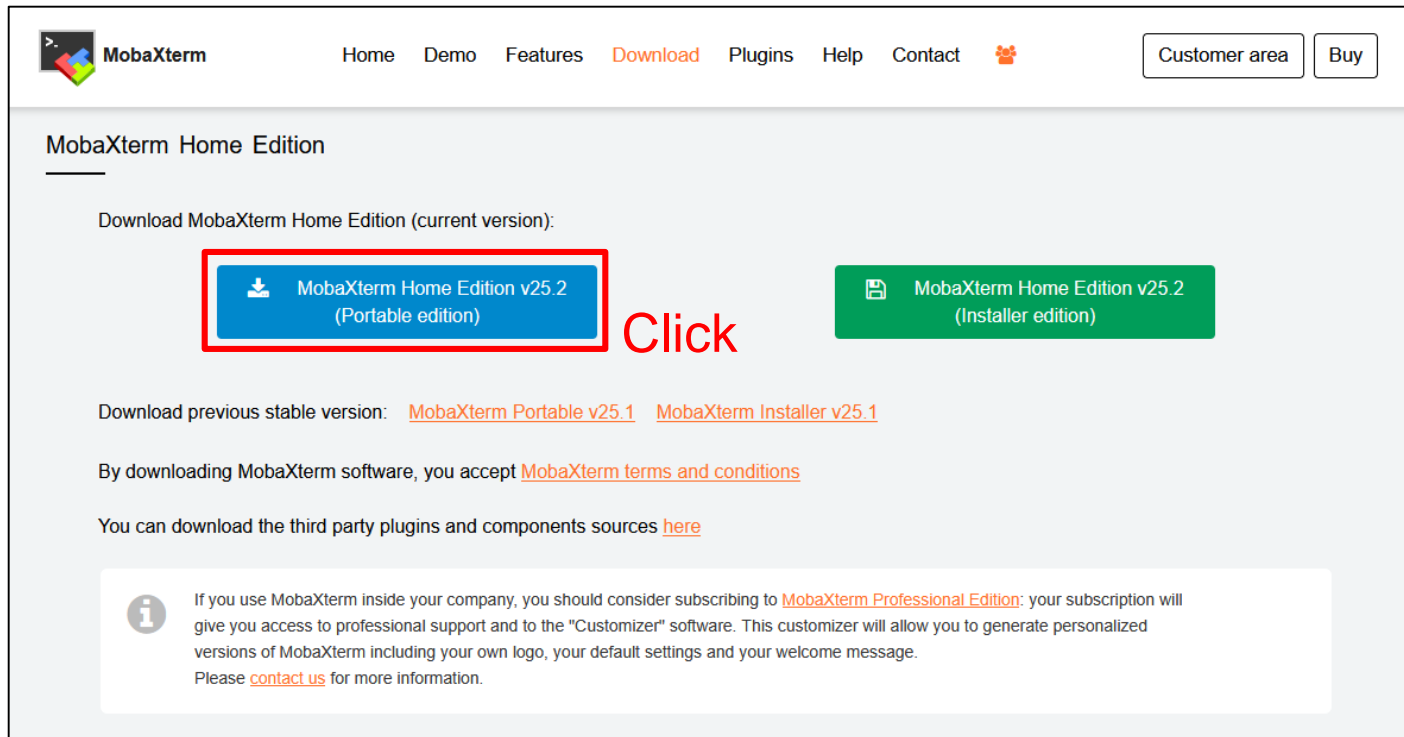
☐ Delayed submission will result in penalty!

Appendix A: Installing MobaXterm and Connecting to the Server

Installing MobaXterm

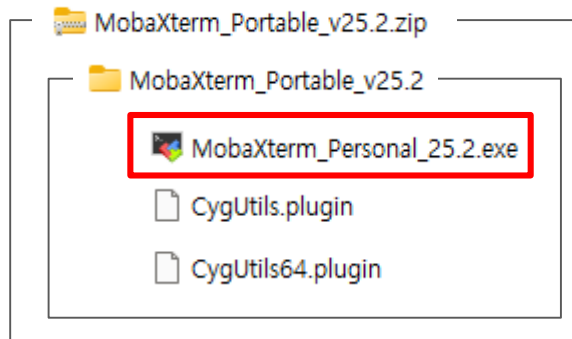
❑ Enter the link and download the file

- <https://mobaxterm.mobatek.net/download-home-edition.html>

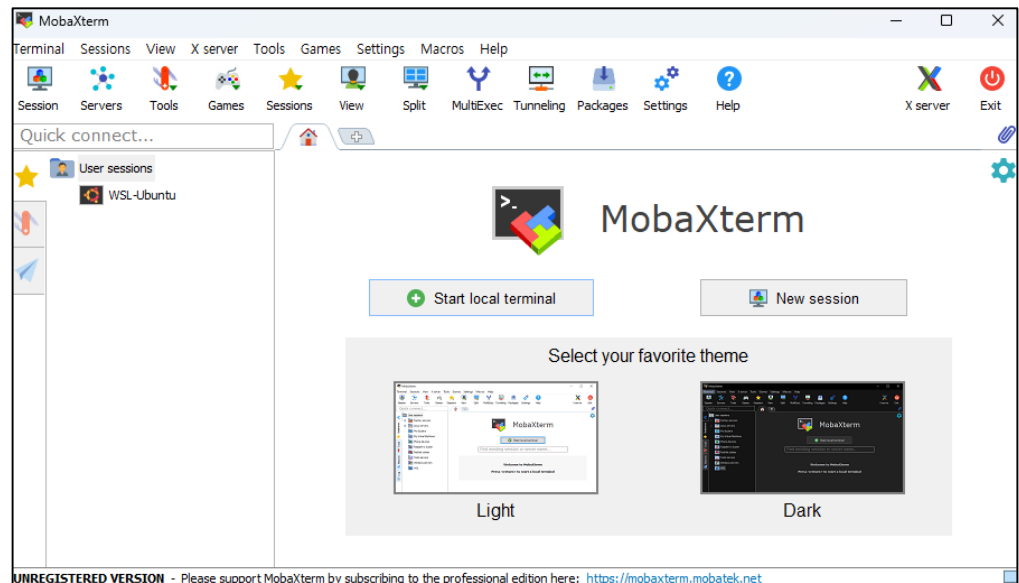


Installing MobaXterm

- ❑ Unzip the file and double-click the program

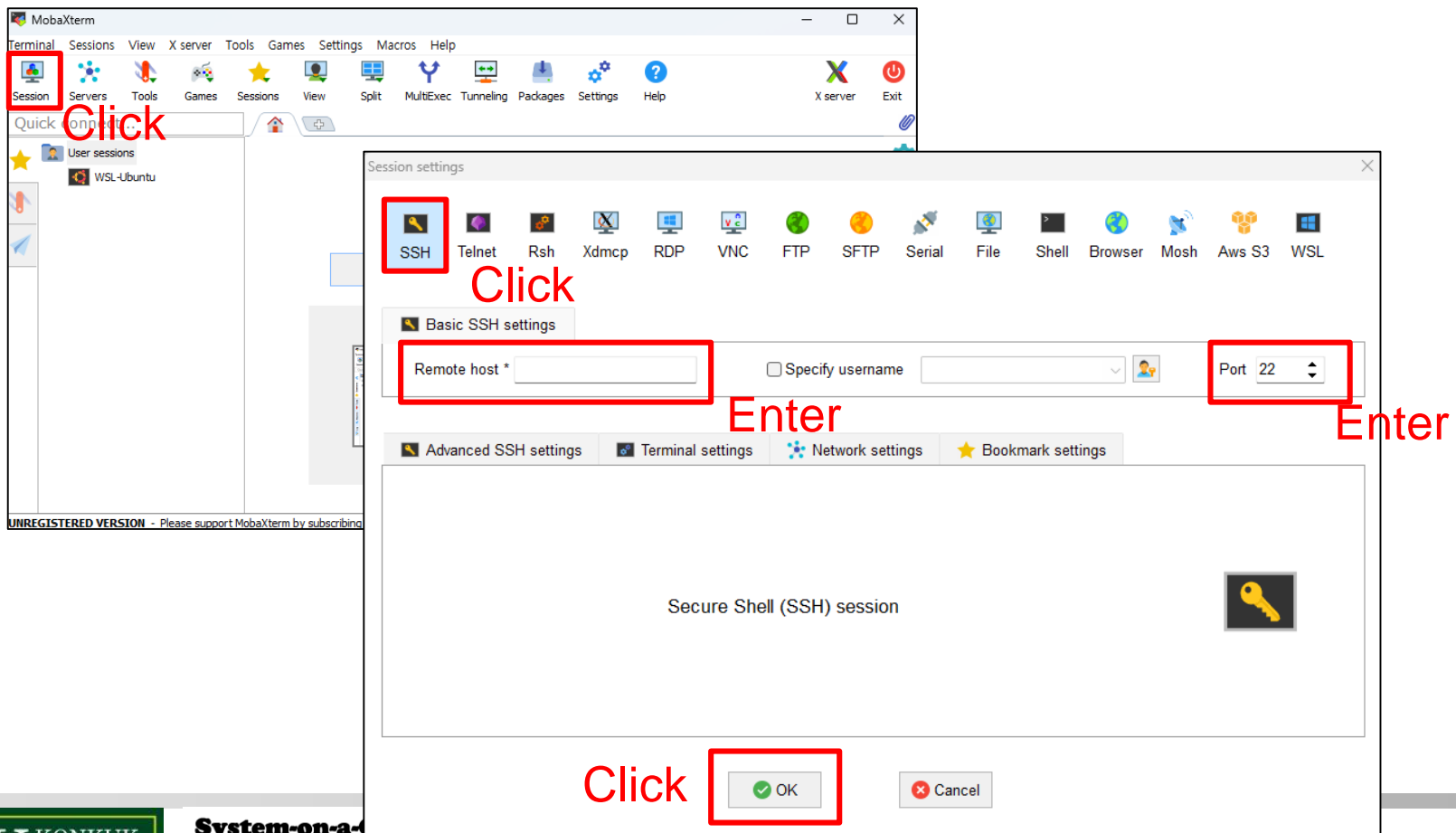


Double Click



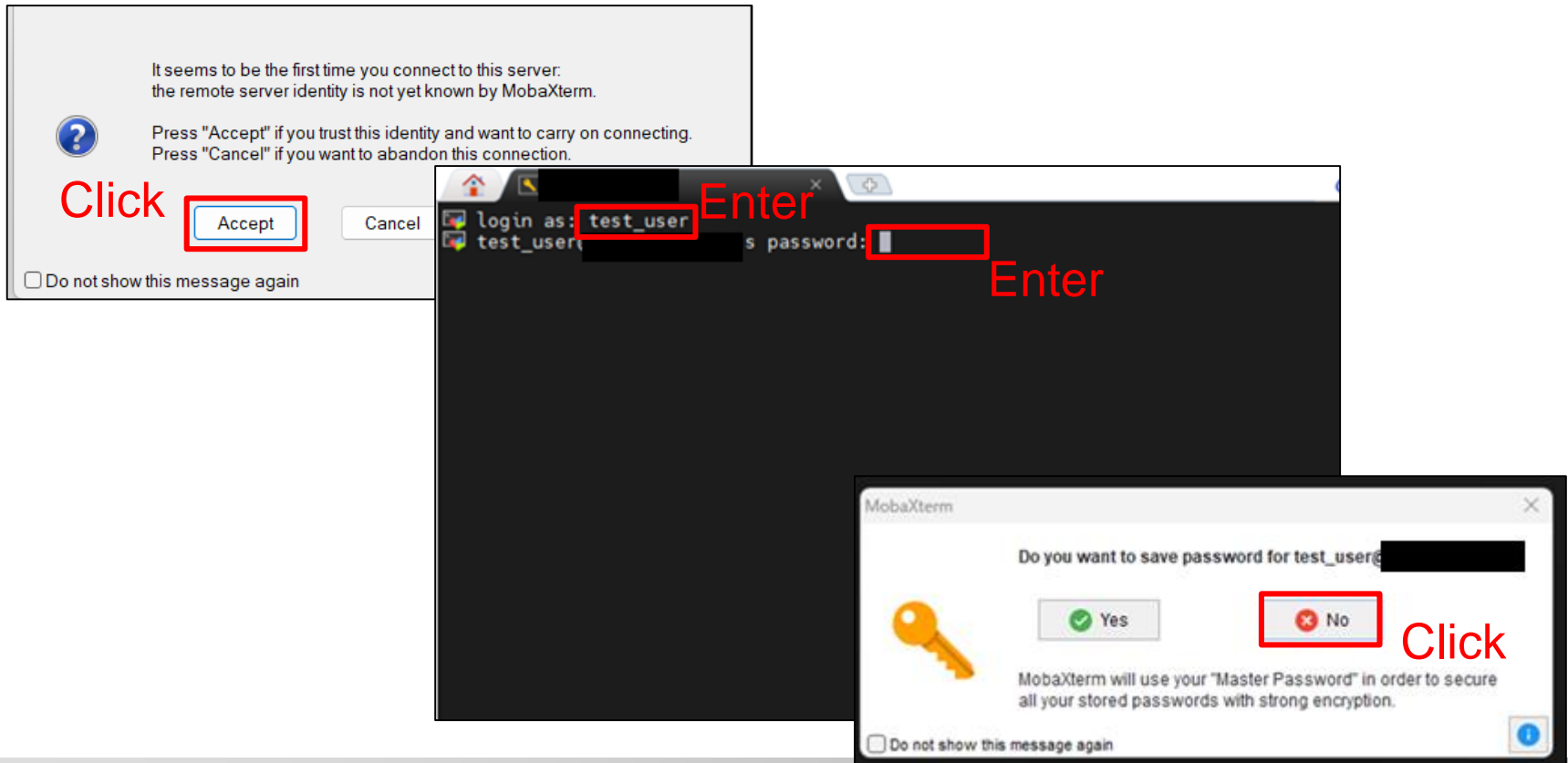
Connecting to the Server

- ❑ Click the icons and enter '**Remote host**' and '**Port**' fields
 - Refer to the Notice page in the Ecampus



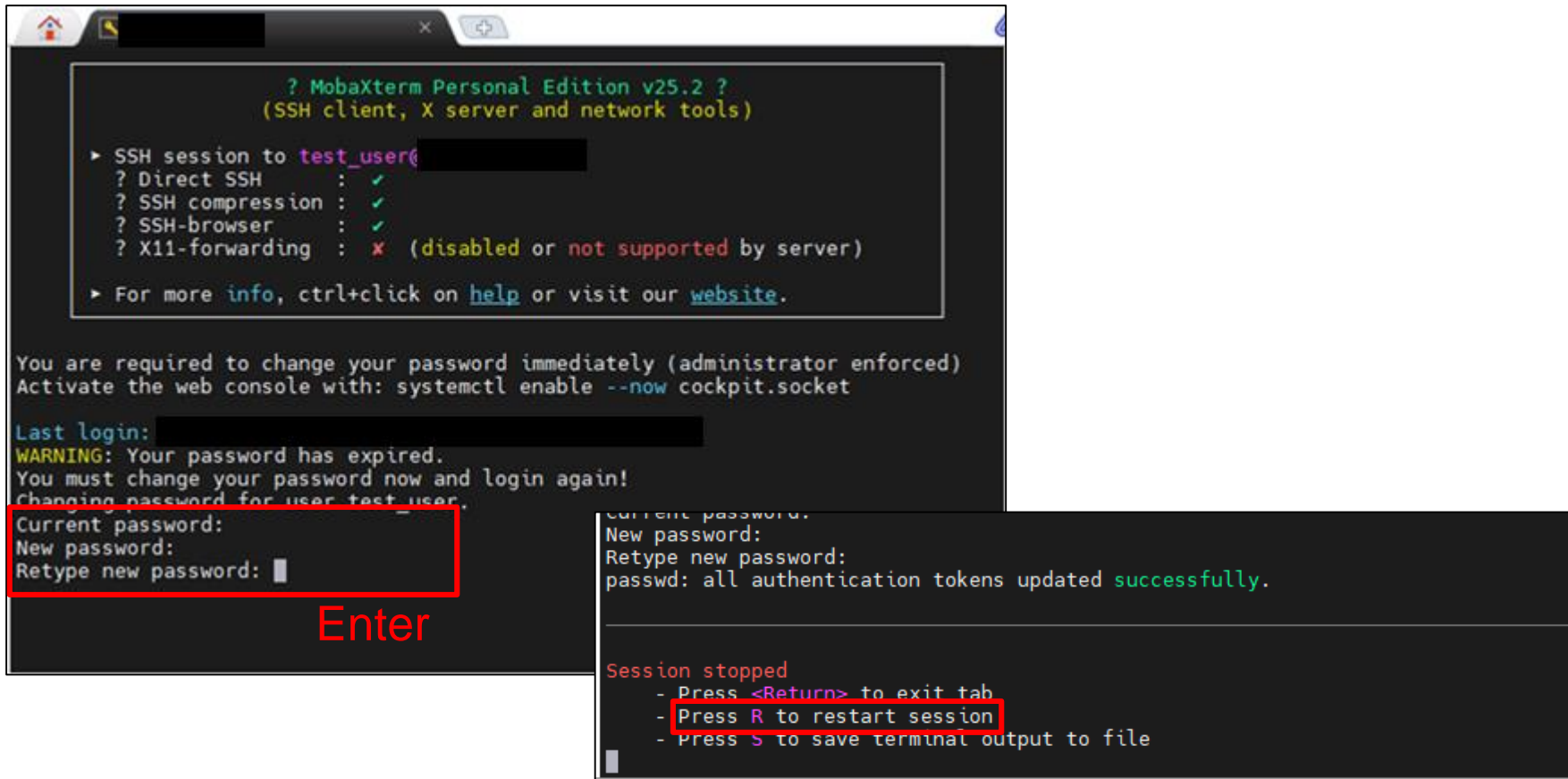
Connecting to the Server

- ❑ Click the icons and enter ***the username*** and ***the initial password***
 - Refer to the Notice page in the Ecampus



Connecting to the Server

- ❑ Enter **a new password** of your choice and press **R** to reconnect to the server



```
? MobaXterm Personal Edition v25.2 ?
(SSH client, X server and network tools)

> SSH session to test_user@
? Direct SSH      : ✓
? SSH compression : ✓
? SSH-browser     : ✓
? X11-forwarding  : ✗ (disabled or not supported by server)

> For more info, ctrl+click on help or visit our website.

You are required to change your password immediately (administrator enforced)
Activate the web console with: systemctl enable --now cockpit.socket

Last login:
WARNING: Your password has expired.
You must change your password now and login again!
Changing password for user test_user.
Current password:
New password:
Retype new password:

Enter

Current password:
New password:
Retype new password:
passwd: all authentication tokens updated successfully.

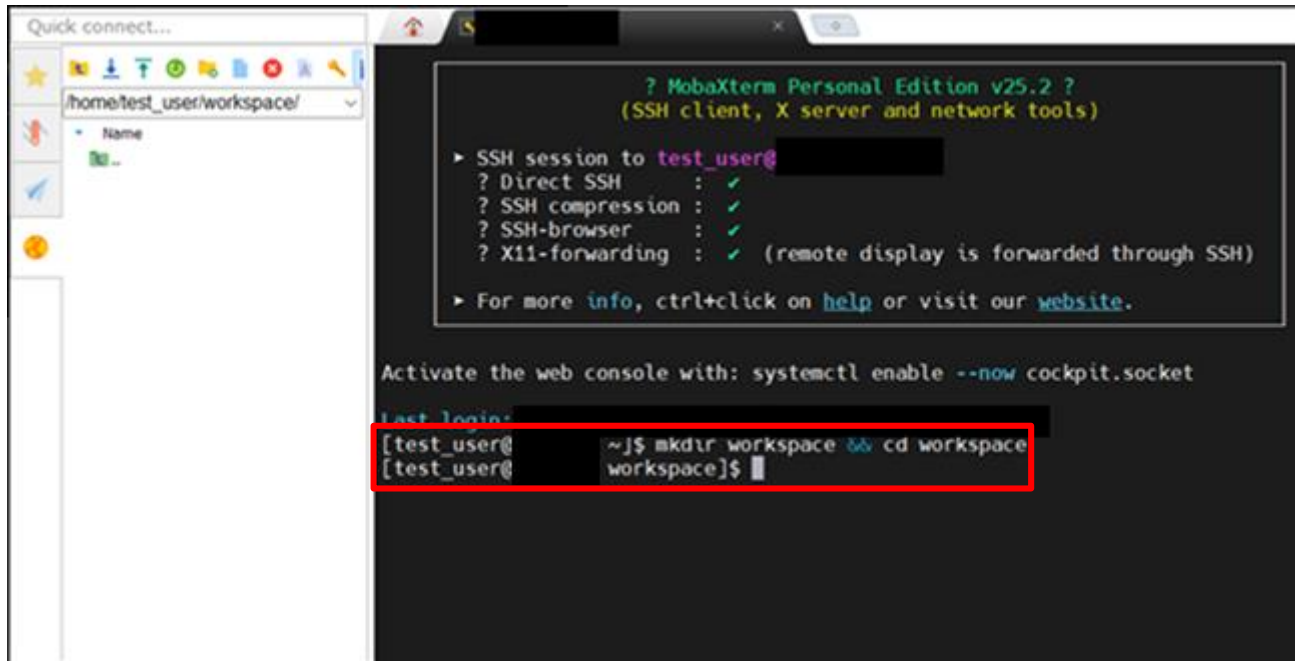
Session stopped
- Press <Return> to exit tab
- Press R to restart session
- Press S to save terminal output to file
```

Appendix B: Building Project and Running Simulation

Building Project

- ☐ Connect to the server (see **Appendix A**) and enter the following commands

mkdir workspace && cd workspace



Building Project

- ❑ Upload '**TP_MP25.zip**' and unzip the file

unzip TP_MP25.zip

The image displays three screenshots illustrating the steps to upload and unzip a file in a MobaXterm environment:

- Top Left:** A 'Quick connect...' dialog box showing the file explorer for `/home/test_user/workspace/`. The file `TP_MP25.zip` is visible. A red box highlights the upload icon, with the word 'Click' written in red.
- Bottom Left:** A 'Choose which file(s) to upload...' dialog box. The file `TP_MP25.zip` is selected. A red box highlights the file name, with the word 'Click' written in red. The '열기(O)' (Open) button is also highlighted with a red box and the word 'Click' written in red.
- Right:** A terminal window showing the MobaXterm interface. The terminal output includes:
 - SSH session to `test_user@`
 - SSH session configuration details (Direct SSH, compression, browser, X11-forwarding).
 - Instructions to activate the web console: `systemctl enable --now cockpit.socket`.
 - Terminal commands and output:

```
Last login: [test_user@ ~]$ mkdir workspace && cd workspace
[test_user@ workspace]$ unzip TP_MP25.zip
Archive: TP_MP25.zip
  creating: TP_MP25/
  creating: TP_MP25/build_UNIX/
 extracting: TP_MP25/build_UNIX/lst_include.lst
 inflating: TP_MP25/build_UNIX/lst_src.lst
```

Building Project

- ❑ Change directory and build project

```
cd TP_MP25/build_UNIX/
make
```

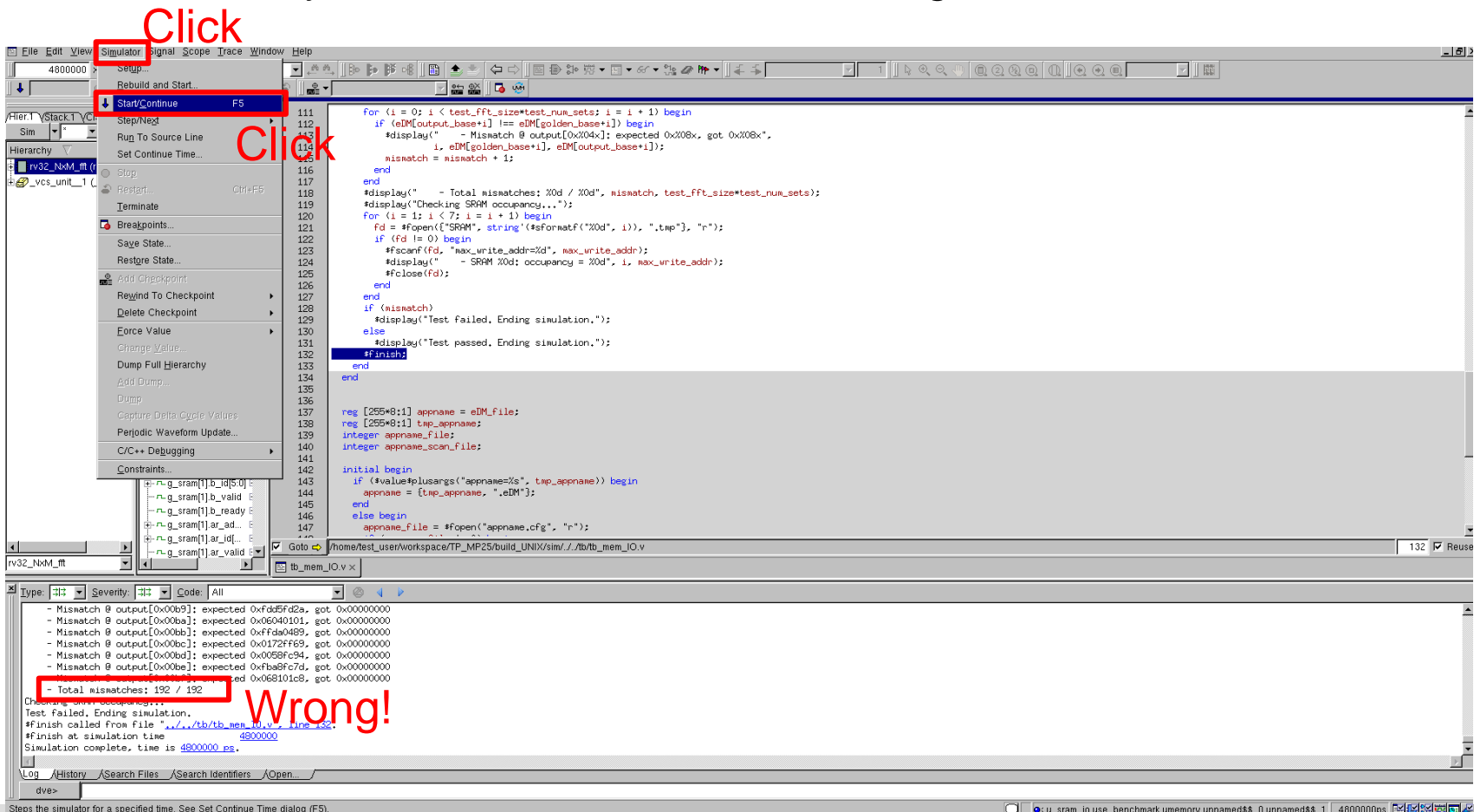
The image shows a terminal window and an IDE. The terminal window displays the following commands and output:

```
inflating: TP_MP25/tb/par_emulator.v
inflating: TP_MP25/tb/tb_mem_I0.v
inflating: TP_MP25/tb/tb_mem_PMb.v
[test_user@workspace]$ cd TP_MP25/build_UNIX/
[test_user@build_UNIX]$ make
/tools/binutils/riscv/riscv64-unknown-elf/bin/as -march=rv32i
space/TP_MP25/build_UNIX/./sw/data_m1.s
/tools/binutils/riscv/riscv64-unknown-elf/bin/as -
space/TP_MP25/build_UNIX/./sw/data_m2.s
```

The IDE shows a C code file with various macros and variables. The code includes a macro definition for `localparam` and a function `main` that initializes variables and calls `main`.

Running Simulation

- ❑ Press F5 or click the icons to run simulation
 - Write your own ASM code and run again

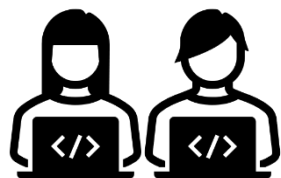


Appendix C:

Documenting The Ablation Study

Ablation Study

- ❑ Propose your ideas with the **metrics**(execution time)
 - For each idea you've implemented,
 - ✓ explain the idea briefly
 - ✓ and show the measurement of the speedup achieved with it.



Idea A

"Without our idea, it was..."

Idea B

Idea C

Idea A

❑ We changed ...
- reference code vs. changed

```

void fft_ref(my_complex* out, my_complex* input, my_complex* h_in)
{
    for (n = 0; n < N; n++)
    {
        for (k = 0; k < stage; k++)
        {
            stage[n + 1] = (stage[n] * h_in[k]) + op(stage[n]);
            stage[n + 1] = (stage[n] * h_in[k]) + op(stage[n]);
        }
    }
}
  
```

"We changed this code as..."

```

void fft_opt(my_complex* out, my_complex* input, my_complex* h_in)
{
    for (n = 0; n < N; n++)
    {
        for (k = 0; k < stage; k++)
        {
            stage[n + 1] = (stage[n] * h_in[k]) + op(stage[n]);
            stage[n + 1] = (stage[n] * h_in[k]) + op(stage[n]);
        }
    }
}
  
```

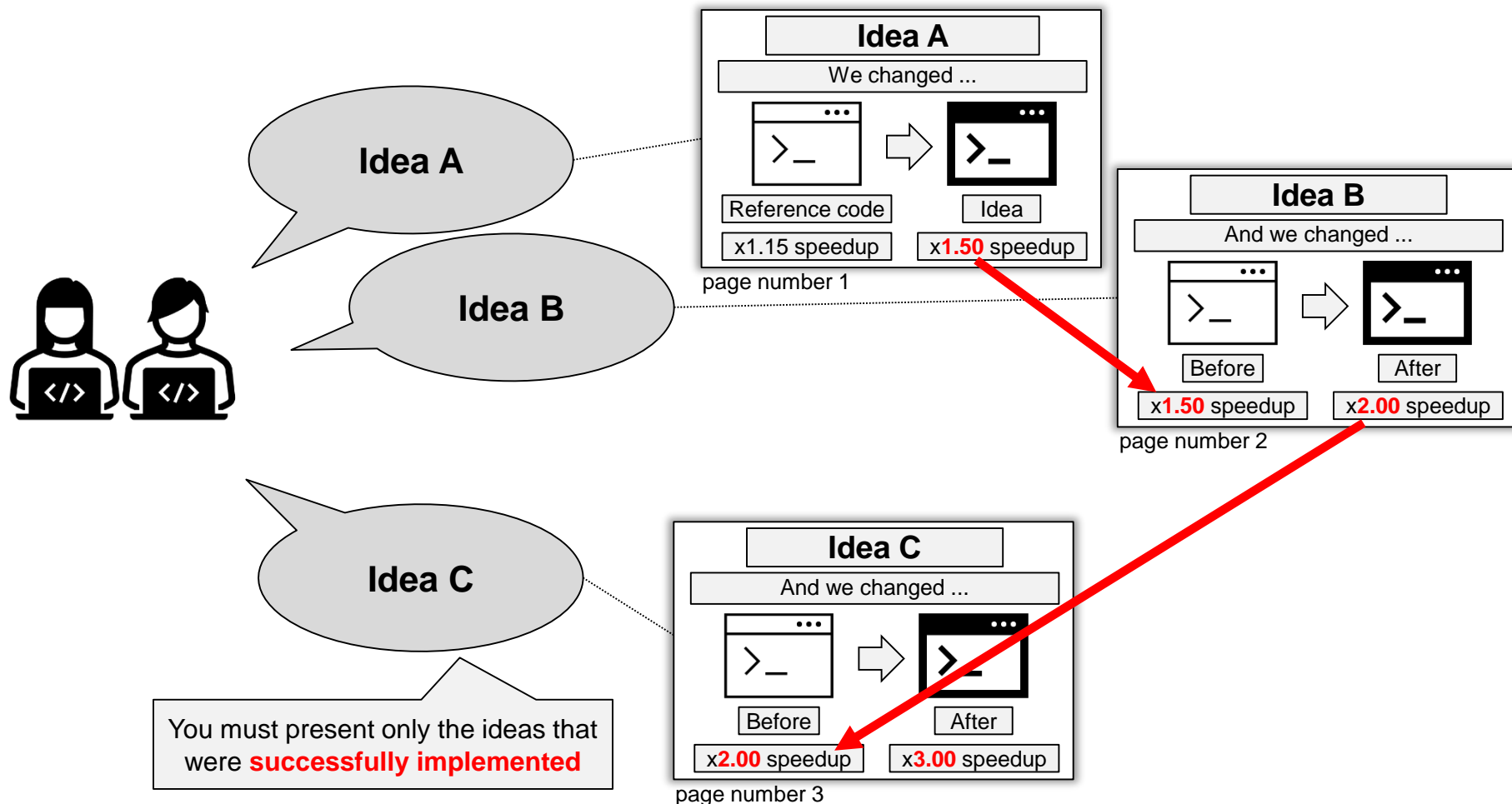
"And we got x#.# speedup"

measured Accuracy: 100.00% - Inf
 Benchmarking Start---
 Case 0: FFT Reference
 Run: 100000, 1218754, 1218754, 1218754, 1218754
 Case 1: FFT Optimized
 Run: 100000, 1218754, 1218754, 1218754, 1218754
 Benchmarking Complete---
 Optimized FFT is x1.15 faster than Reference

KU KONKUK UNIVERSITY System-on-a-Chip Design LAB

Ablation Study

- ❑ Present **all successfully implemented** ideas

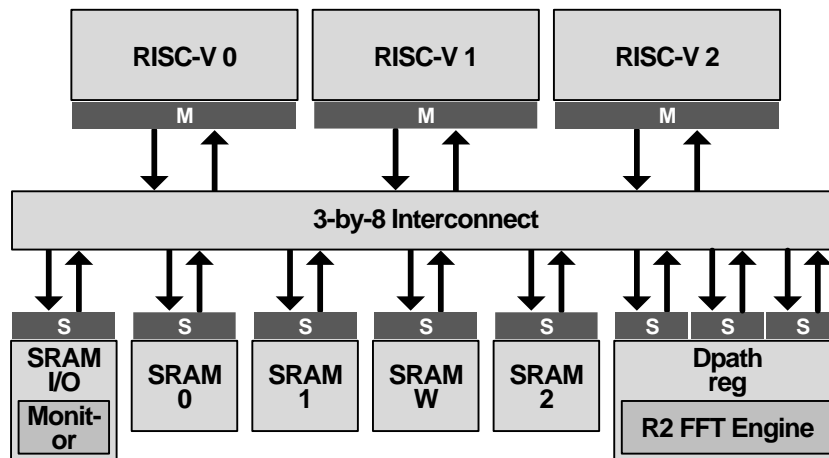


Appendix D: Effective Memory Capacity

Effective Memory Capacity

□ Example*

- Only **lower 256/256/8-byte address region** for SRAM 0/1/2 required for 3 input/output sets



Lower 8 bytes

Lower 256 bytes

Lower 256 bytes

Address	Name
0xFFFF_FFFF	RESERVED
0x0700_0004	Dpath reg (port 2)
0x0700_0003	
0x0700_0000	RESERVED
0x06FF_FFFF	
0x0600_0008	Dpath reg (port 1)
0x0600_0007	
0x0600_0000	RESERVED
0x05FF_FFFF	
0x0500_0008	Dpath reg (port 0)
0x0500_0007	
0x0500_0000	RESERVED
0x04FF_FFFF	
0x0401_0000	SRAM 2
0x0400_FFFF	
0x0400_0000	RESERVED
0x03FF_FFFF	
0x0301_0000	SRAM W
0x0300_FFFF	
0x0300_0000	RESERVED
0x02FF_FFFF	
0x0201_0000	SRAM 1
0x0200_FFFF	
0x0200_0000	RESERVED
0x01FF_FFFF	
0x0101_0000	SRAM 0
0x0100_FFFF	
0x0100_0000	RESERVED
0x00FF_FFFF	
0x0001_0000	SRAM I/O
0x0000_FFFF	
0x0000_0000	

* The effective memory capacity may be proposed to be more or less than in this example (the less capacity you propose, the better score you will get!)