INDIAN INSTITUTE OF TECHNOLOGY JODHPUR

Lab5 – FPGA Synthesis
EEL7210 – Hardware Software Co-Design

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Maximum Points: 4 Deadline: None

The code for this assignment is at the following github repo:

https://github.com/m21aie249/eel7210-lab5

Problem Statement:

Synthesize and simulate the given C design description.

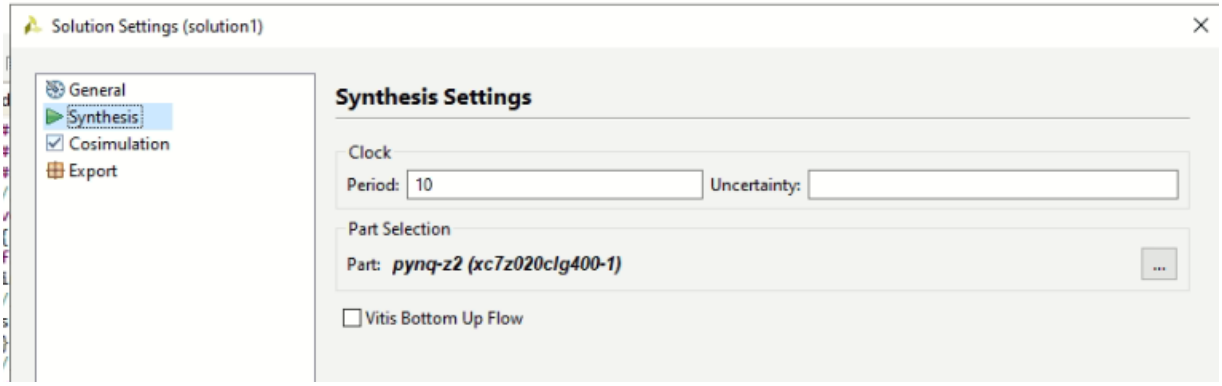
Do the following tasks:

a) Report FPGA utilization from the synthesis results.

Tool used: Vivado HLS 2019.2.1

Top Module Setting: modulator

Board: PYNQ-Z2



Utilization Results (Summary. Detailed .html report on github repo)

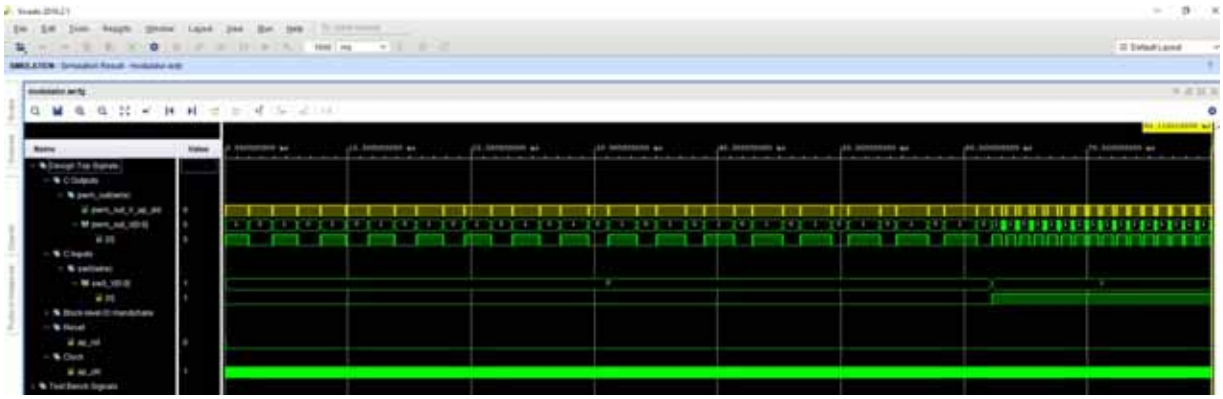
Utilization Estimates

- **Summary**

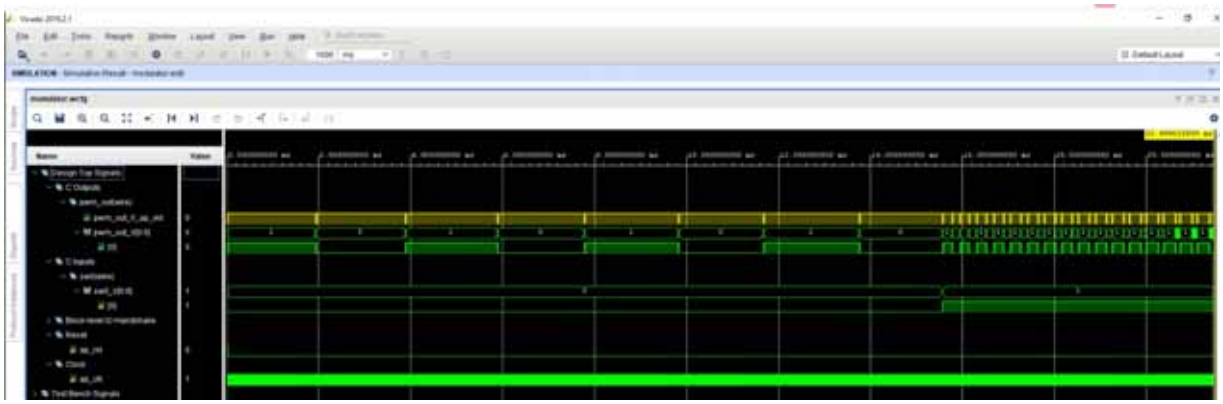
Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	897	-
FIFO	-	-	-	-	-
Instance	-	3	823	1429	-
Memory	1	-	0	0	-
Multiplexer	-	-	-	192	-
Register	-	-	438	-	-
Total	1	3	1261	2518	0
Available	280	220	106400	53200	0
Utilization (%)	~0	1	1	4	0

b) Simulate the design with some test cases.

Simulation waveform of the default code: (Sine waves 1Hz and 3.5Hz)



Simulation waveform of the test case: (Sine waves 1Hz and 10Hz)



c) What is the functionality of the design?

The code is simulating a PWM modulator. It is simulating the PWM signal being modulated by 2 different sine waves (1Hz and 3.5Hz frequencies), selected with the setting of signal sw0. The waveform shows the PWM out duty cycle changing as the sw0 signal is flipped