Synthesis Report for 'modulator'

General Information

Date: Thu Mar 30 19:05:56 2023
Version: 2019.2.1 (Build 2724168 on Thu Dec 05 05:19:09 MST 2019)
Project: lab5
Solution: solution1
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	8.300 ns	1.25 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
?	?	?	?	?	?	none

  - **Detail**
    - **Instance**

N/A

    - **Loop**

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- onloop	?	?	1	-	-	?	no
- offloop	?	?	1	-	-	?	no

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-

Expression	-	-	0	897	-
FIFO	-	-	-	-	-
Instance	-	3	823	1429	-
Memory	1	-	0	0	-
Multiplexer	-	-	-	192	-
Register	-	-	438	-	-
Total	1	3	1261	2518	0
Available	280	220	106400	53200	0
Utilization (%)	~0	1	1	4	0

- **Detail**
  - **Instance**

Instance	Module	BRAM_18K	DSP48E	FF	LUT	URAM
modulator_fmul_32bkb_U1	modulator_fmul_32bkb	0	3	143	321	0
modulator_sitofp_dEe_U3	modulator_sitofp_dEe	0	0	340	554	0
modulator_uitofp_cud_U2	modulator_uitofp_cud	0	0	340	554	0
Total	3	0	3	823	1429	0

  - **DSP48E**

N/A

  - **Memory**

Memory	Module	BRAM_18K	FF	LUT	URAM	Words	Bits	Banks	W*Bits*Banks
sine_V_U	modulator_sine_V	1	0	0	0	256	12	1	3072
Total	1	1	0	0	0	256	12	1	3072

  - **FIFO**

N/A

  - **Expression**

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln700_fu_544_p2	+	0	0	15	8	1
j_V_1_fu_538_p2	+	0	0	27	20	1
j_V_fu_336_p2	+	0	0	27	20	1
ret_V_fu_345_p2	-	0	0	19	14	13
sub_ln281_1_fu_396_p2	-	0	0	15	8	9
sub_ln281_fu_194_p2	-	0	0	15	8	9
sub_ln294_1_fu_408_p2	-	0	0	15	1	9
sub_ln294_fu_206_p2	-	0	0	15	1	9
sub_ln461_1_fu_519_p2	-	0	0	27	1	20
sub_ln461_fu_317_p2	-	0	0	27	1	20
icmp_ln278_1_fu_390_p2	icmp	0	0	18	31	1
icmp_ln278_fu_188_p2	icmp	0	0	18	31	1

icmp_ln282_1_fu_402_p2	icmp	0	0	11	8	8
icmp_ln282_fu_200_p2	icmp	0	0	11	8	8
icmp_ln284_1_fu_434_p2	icmp	0	0	13	9	1
icmp_ln284_fu_232_p2	icmp	0	0	13	9	1
icmp_ln285_1_fu_439_p2	icmp	0	0	13	9	5
icmp_ln285_fu_237_p2	icmp	0	0	13	9	5
icmp_ln295_1_fu_414_p2	icmp	0	0	13	9	5
icmp_ln295_fu_212_p2	icmp	0	0	13	9	5
icmp_ln887_1_fu_532_p2	icmp	0	0	18	20	20
icmp_ln887_fu_330_p2	icmp	0	0	18	20	20
lshr_ln286_1_fu_444_p2	lshr	0	0	69	24	24
lshr_ln286_fu_242_p2	lshr	0	0	69	24	24
or_ln278_1_fu_481_p2	or	0	0	2	1	1
or_ln278_fu_279_p2	or	0	0	2	1	1
select_ln22_fu_145_p3	select	0	0	31	1	31
select_ln278_1_fu_485_p3	select	0	0	20	1	1
select_ln278_2_fu_312_p3	select	0	0	20	1	20
select_ln278_3_fu_514_p3	select	0	0	20	1	20
select_ln278_fu_283_p3	select	0	0	20	1	1
select_ln285_1_fu_491_p3	select	0	0	20	1	20
select_ln285_2_fu_304_p3	select	0	0	20	1	20
select_ln285_3_fu_506_p3	select	0	0	20	1	20
select_ln285_fu_289_p3	select	0	0	20	1	20
select_ln288_1_fu_461_p3	select	0	0	2	1	2
select_ln288_fu_259_p3	select	0	0	2	1	2
select_ln295_1_fu_499_p3	select	0	0	20	1	20
select_ln295_fu_297_p3	select	0	0	20	1	20
select_ln303_1_fu_525_p3	select	0	0	20	1	20
select_ln303_fu_323_p3	select	0	0	20	1	20
shl_ln297_1_fu_476_p2	shl	0	0	53	20	20
shl_ln297_fu_274_p2	shl	0	0	53	20	20
Total	43	0	0	897	359	499

- **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	129	28	1	28
grp_fu_118_p0	15	3	32	96
grp_fu_118_p1	15	3	32	96
pwm_out_V	15	3	1	3
t_V_1_reg_107	9	2	20	40
t_V_reg_96	9	2	20	40
Total	192	41	106	303

- **Register**

Name	FF	LUT	Bits	Const Bits
ap_CS_fsm	27	0	27	0

counter_V	8	0	8	0
icmp_ln278_1_reg_681	1	0	1	0
icmp_ln278_reg_603	1	0	1	0
icmp_ln282_1_reg_694	1	0	1	0
icmp_ln282_reg_616	1	0	1	0
icmp_ln295_1_reg_704	1	0	1	0
icmp_ln295_reg_626	1	0	1	0
or_ln278_1_reg_709	1	0	1	0
or_ln278_reg_631	1	0	1	0
p_Result_4_reg_592	1	0	1	0
p_Result_5_reg_670	1	0	1	0
reg_128	32	0	32	0
reg_V_1_reg_664	32	0	32	0
reg_V_reg_586	32	0	32	0
select_ln22_reg_581	17	0	32	15
select_ln278_1_reg_714	20	0	20	0
select_ln278_reg_636	20	0	20	0
select_ln285_2_reg_641	20	0	20	0
select_ln285_3_reg_719	20	0	20	0
sine_V_load_reg_565	12	0	12	0
sub_ln281_1_reg_687	9	0	9	0
sub_ln281_reg_609	9	0	9	0
sub_ln294_1_reg_699	9	0	9	0
sub_ln294_reg_621	9	0	9	0
t_V_1_reg_107	20	0	20	0
t_V_2_reg_555	8	0	8	0
t_V_reg_96	20	0	20	0
tmp_3_reg_659	32	0	32	0
tmp_reg_576	32	0	32	0
trunc_ln283_1_reg_675	20	0	20	0
trunc_ln283_reg_597	20	0	20	0
Total	438	0	453	15

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	modulator	return value
ap_rst	in	1	ap_ctrl_hs	modulator	return value
ap_start	in	1	ap_ctrl_hs	modulator	return value
ap_done	out	1	ap_ctrl_hs	modulator	return value
ap_idle	out	1	ap_ctrl_hs	modulator	return value
ap_ready	out	1	ap_ctrl_hs	modulator	return value
sw0_V	in	1	ap_none	sw0_V	scalar

pwm_out_V	out	1	ap_vld	pwm_out_V	pointer
pwm_out_V_ap_vld	out	1	ap_vld	pwm_out_V	pointer