INDIAN INSTITUTE OF TECHNOLOGY JODHPUR

Lab6 – Data Compression Implementation
EEL7210 – Hardware Software Co-Design

Submitted by Rohit Mathur (M21AIE249)

Maximum Points: 4 Deadline: None

The code for this assignment is at the following github repo:

https://github.com/m21aie249/eel7210-lab6

Problem Statement:

This lab implements run-length encoding (RLE) data compression technique. Details can be found here at https://en.wikipedia.org/wiki/Run-length_encoding

The design file and testbench is supplied herewith. Go through them and complete the below tasks:

a) simulate the design with some test-cases. Is the design working as per expectation? fix if anything is wrong in the design.

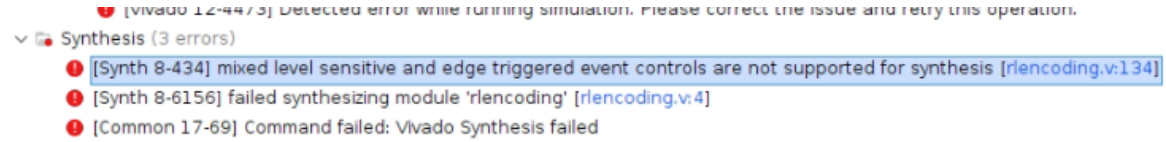
On running the code as-is, we see that data_out has data loss (Is XX), byte F8. Input data is 88 C8 E8 F8. This is happening because the FIFO is empty and we are trying to read. We need to correct this by changing the test case for assertions and de-assertions of the read_signal.

To help debug, added datacount as a port and enabled its waveform dump.

Updated waveform:

b) is the design synthesizable? if yes, synthesize it. if not, please fix the synthesis errors.

The design is not synthesizable. Synthesis errors were observed on trying to synthesize the code as-is.



The error message points to this statement in the code:

always @(posedge fast_clk,nstate)

Synthesis of this statement is not supported. State machine needs to be sensitive to edge triggered events only while nstate is a level sensitive event. We need to remove it from the sensitivity list. On doing this and changing the top to rlencoder, and re-running the synthesis, it is successfully completed.

c) report the design synthesis results.

The Synthesis report (Utilization) is pasted below. Also available on the repo.

| Tool Version : Vivado v.2022.1 (lin64) Build 3526262 Mon Apr 18 15:47:01 MDT 2022

| Date : Wed Apr 5 09:42:37 2023

| Host : lab-linux running 64-bit Ubuntu 22.04.2 LTS

| Command : report_utilization -file rlencoding_utilization_synth.rpt -pb rlencoding_utilization_synth.pb

| Design : rlencoding

| Device : xczu7ev-ffvc1156-2-e

| Speed File : -2

| Design State : Synthesized

Utilization Design Information

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1. CLB Logic

+----------+------+-------+-----------+----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------+------+-------+-----------+----------+-------+

| CLB LUTs* | 258 | 0 | 0 | 230400 | 0.11 |

| LUT as Logic | 178 | 0 | 0 | 230400 | 0.08 |

| LUT as Memory | 80 | 0 | 0 | 101760 | 0.08 |

| LUT as Distributed RAM | 80 | 0 | | | |

| LUT as Shift Register | 0 | 0 | | | |

| CLB Registers | 49 | 0 | 0 | 460800 | 0.01 |

| Register as Flip Flop | 49 | 0 | 0 | 460800 | 0.01 |

| Register as Latch | 0 | 0 | 0 | 460800 | 0.00 |

| CARRY8 | 6 | 0 | 0 | 28800 | 0.02 |

| F7 Muxes | 0 | 0 | 0 | 115200 | 0.00 |

| F8 Muxes | 0 | 0 | 0 | 57600 | 0.00 |

| F9 Muxes | 0 | 0 | 0 | 28800 | 0.00 |

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* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

+-------+--------------+-------------+--------------+

| Total | Clock Enable | Synchronous | Asynchronous |

+-------+--------------+-------------+--------------+

| 0 | _ | - | - |

| 0 | _ | - | Set |

| 0 | _ | - | Reset |

| 0 | _ | Set | - |

| 0 | _ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 0 | Yes | - | Reset |

| 1 | Yes | Set | - |

| 48 | Yes | Reset | - |

+-------+--------------+-------------+--------------+

2. BLOCKRAM

+----------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------------+------+-------+------------+-----------+-------+

| Block RAM Tile | 0 | 0 | 0 | 312 | 0.00 |

| RAMB36/FIFO* | 0 | 0 | 0 | 312 | 0.00 |

| RAMB18 | 0 | 0 | 0 | 624 | 0.00 |

| URAM | 0 | 0 | 0 | 96 | 0.00 |

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* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E2 or one FIFO18E2. However, if a FIFO18E2 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E2

3. ARITHMETIC

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-----------+------+-------+------------+-----------+-------+

| DSPs | 0 | 0 | 0 | 1728 | 0.00 |

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4. I/O

+------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| Bonded IOB | 51 | 0 | 0 | 360 | 14.17 |

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5. CLOCK

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------------------+------+-------+------------+-----------+-------+

| GLOBAL CLOCK BUFFERs | 2 | 0 | 0 | 544 | 0.37 |

| BUFGCE | 2 | 0 | 0 | 208 | 0.96 |

| BUFGCE_DIV | 0 | 0 | 0 | 32 | 0.00 |

| BUFG_GT | 0 | 0 | 0 | 144 | 0.00 |

| BUFG_PS | 0 | 0 | 0 | 96 | 0.00 |

| BUFGCTRL* | 0 | 0 | 0 | 64 | 0.00 |

| PLL | 0 | 0 | 0 | 16 | 0.00 |

| MMCM | 0 | 0 | 0 | 8 | 0.00 |

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* Note: Each used BUFGCTRL counts as two GLOBAL CLOCK BUFFERs. This table does not include global clocking resources, only buffer cell usage. See the Clock Utilization Report (report_clock_utilization) for detailed accounting of global clocking resource availability.

6. ADVANCED

+-----------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| GTHE4_CHANNEL | 0 | 0 | 0 | 20 | 0.00 |

| GTHE4_COMMON | 0 | 0 | 0 | 5 | 0.00 |

| OBUFDS_GTE4 | 0 | 0 | 0 | 10 | 0.00 |

| OBUFDS_GTE4_ADV | 0 | 0 | 0 | 10 | 0.00 |

| PCIE40E4 | 0 | 0 | 0 | 2 | 0.00 |

| PS8 | 0 | 0 | 0 | 1 | 0.00 |

| SYSMONE4 | 0 | 0 | 0 | 1 | 0.00 |

| VCU | 0 | 0 | 0 | 1 | 0.00 |

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7. CONFIGURATION

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| BSCANE2 | 0 | 0 | 0 | 4 | 0.00 |

| DNA_PORTE2 | 0 | 0 | 0 | 1 | 0.00 |

| EFUSE_USR | 0 | 0 | 0 | 1 | 0.00 |

| FRAME_ECCE4 | 0 | 0 | 0 | 1 | 0.00 |

| ICAPE3 | 0 | 0 | 0 | 2 | 0.00 |

| MASTER_JTAG | 0 | 0 | 0 | 1 | 0.00 |

| STARTUPE3 | 0 | 0 | 0 | 1 | 0.00 |

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8. Primitives

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| Ref Name | Used | Functional Category |

+----------+------+---------------------+

| RAMD64E | 80 | CLB |

| LUT6 | 79 | CLB |

| FDRE | 48 | Register |

| LUT5 | 42 | CLB |

| LUT2 | 40 | CLB |

| OBUF | 36 | I/O |

| LUT4 | 36 | CLB |

| LUT3 | 15 | CLB |

| INBUF | 15 | I/O |

| IBUFCTRL | 15 | Others |

| CARRY8 | 6 | CLB |

| BUFGCE | 2 | Clock |

| LUT1 | 1 | CLB |

| FDSE | 1 | Register |

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9. Black Boxes

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| Ref Name | Used |

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10. Instantiated Netlists

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| Ref Name | Used |

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