Course Title:			Software Design Architecture		
Course Number:			COE692		
Semester/Year:			W2022		
Instructor:		Dr. Faezeh Ensan			
Assignment/Lab Number:			Lab 5		
Assignment/Lab '	Γitle:		Lab 5 Part 3		
Submission Date:			TBD		
Due Date:			TBD		
Last Name:	First Name:	Student 1	D:	Section:	*Signature:

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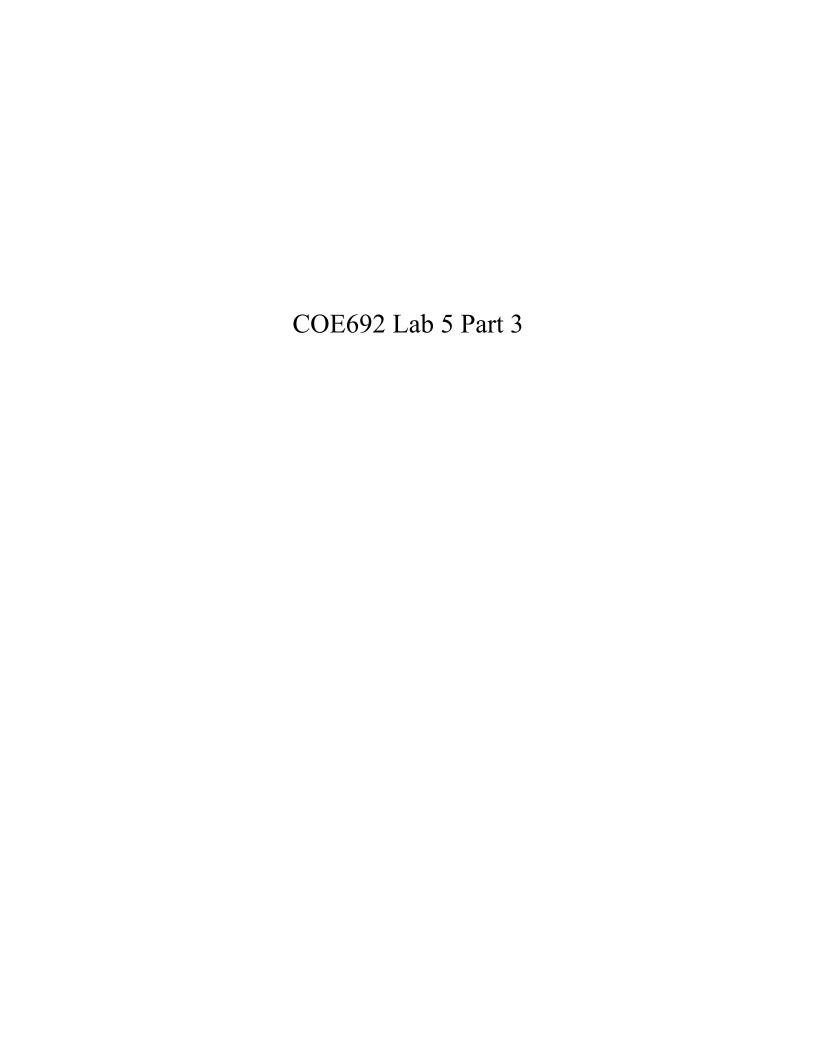
Faisal

Patel

Mahir

Dhaval

<sup>\*</sup>By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <a href="http://www.ryerson.ca/senate/current/pol60.pdf">http://www.ryerson.ca/senate/current/pol60.pdf</a>



NAME	READY	STATUS	RESTARTS	AGE
additem-64478f54c7-2626j	1/1	Running	0	35m
additemdb-59bcf76669-hqlgm	1/1	Running	0	35m
frontend-67b54449b-wql9d	1/1	Running	0	35m
searchdb-bdbf7577-2dssd	1/1	Running	0	35m
searchitem-6d564b45bf-2stb8	1/1	Running	0	35m

NAME TYPE CLUSTER-IP EXTERNAL-IP PORT(S) AGE LoadBalancer 10.60.12.231 34.95.31.249 frontend 80:31434/TCP 36m

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