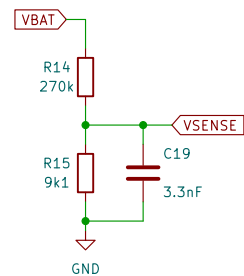
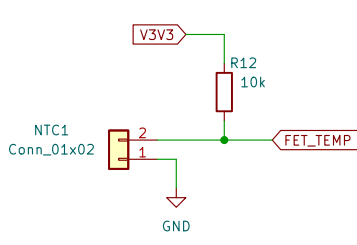
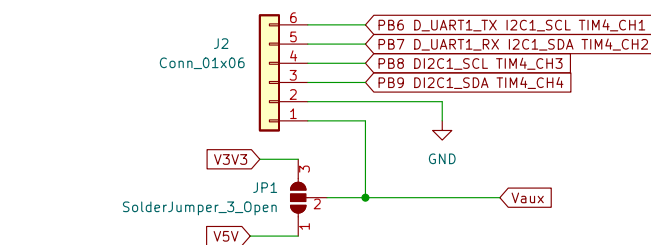
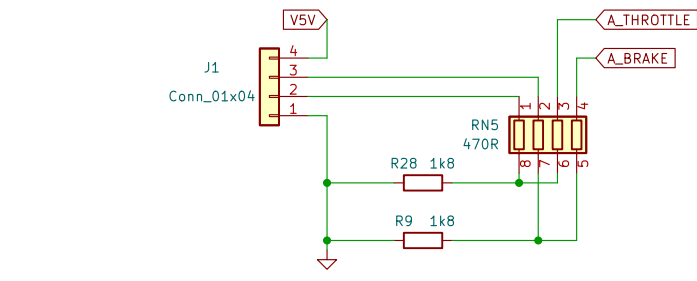
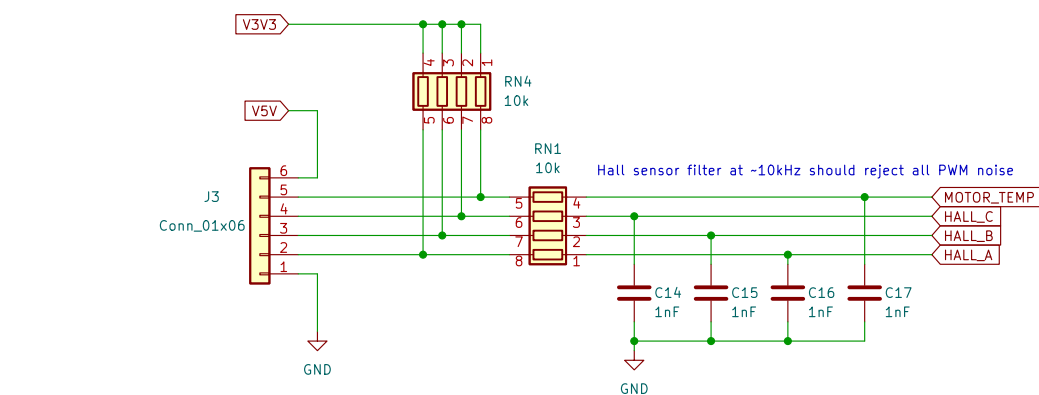
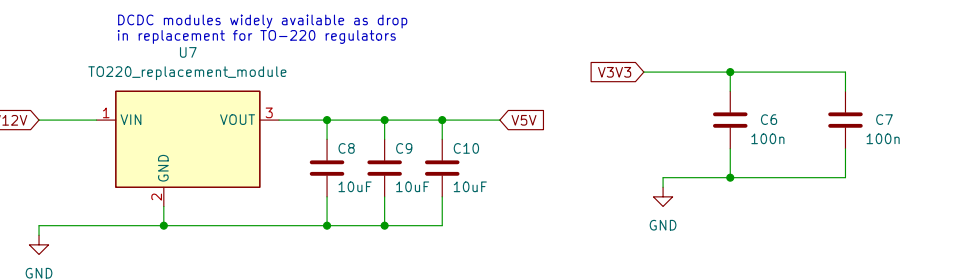
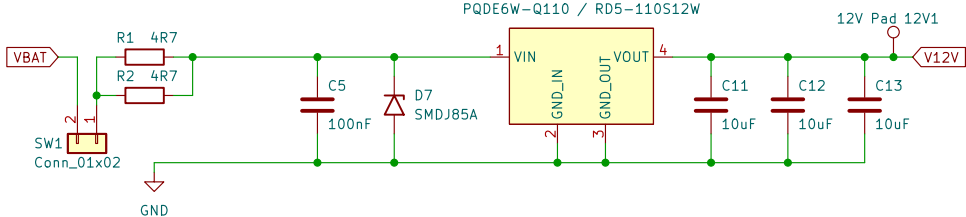
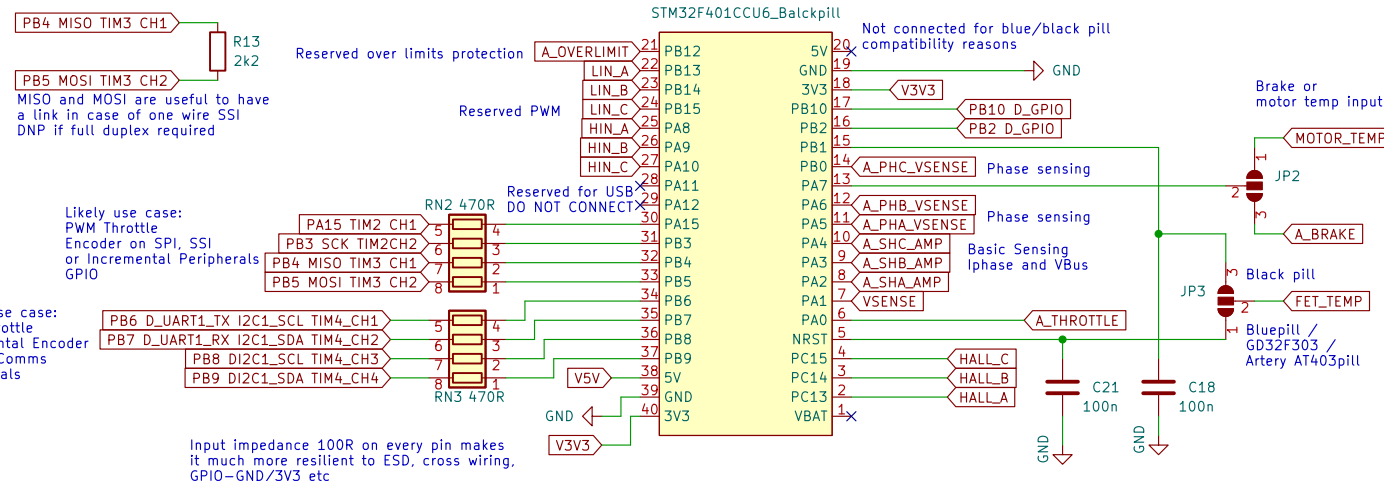


Footprint for CUI isolated module for up to 160V operation.
Only allows 500mA.
HiLink HLK-10011012
CUI PQDE6W-Q110
Or anything that exceeds your battery voltage and gives 12V out



Resistor values are designed to give good overvoltage protection for a 17...20s battery (100V fets).
For 13s...16s batteries (80V FETs) use 270k and 11k resistors.
For 21s...24s batteries (125V+ FETs) use 330k abd 9k1 resistors.

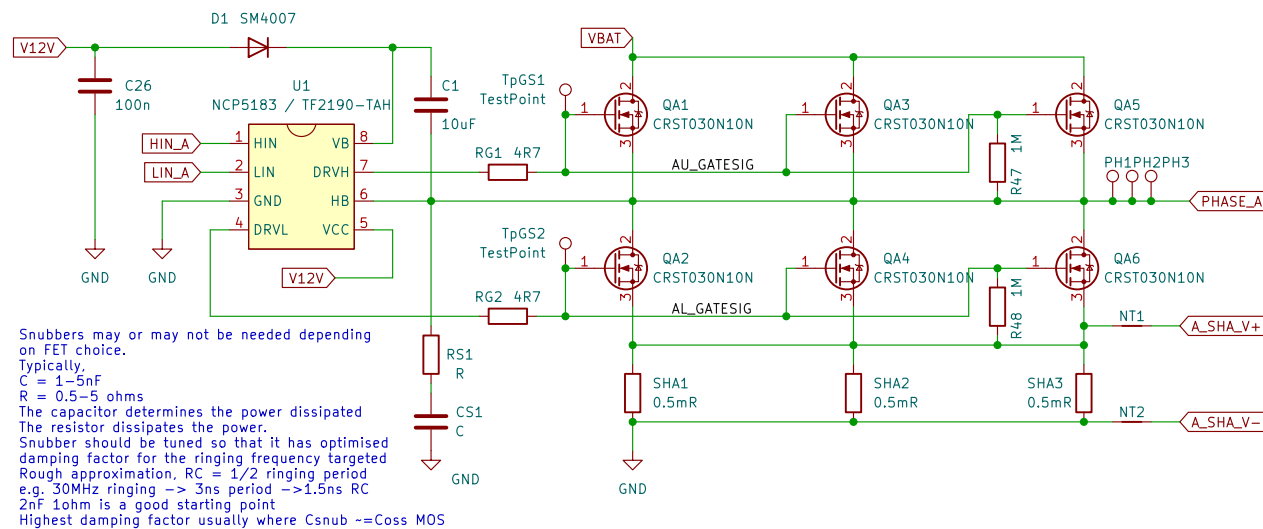
The "Pill" is chosen as a generic STM32 module that should allow easy compatibility with multiple firmwares:
VESC with GD32F303CG pill (Netzplüschler mod. note CG)
EBICS with F103 Bluepill (Stancecoke)
SmartESC V3 (Casainho)
SmartESC V2 (Netzplüschler/Kox3)
MESC with F401 Blackpill (MxiemmingFOC)
STM32 Motor Control Workbench (F401, F103)
Maybe others?
Pills are simply boards with an MCU, a regulator, USB and Boot0 button.



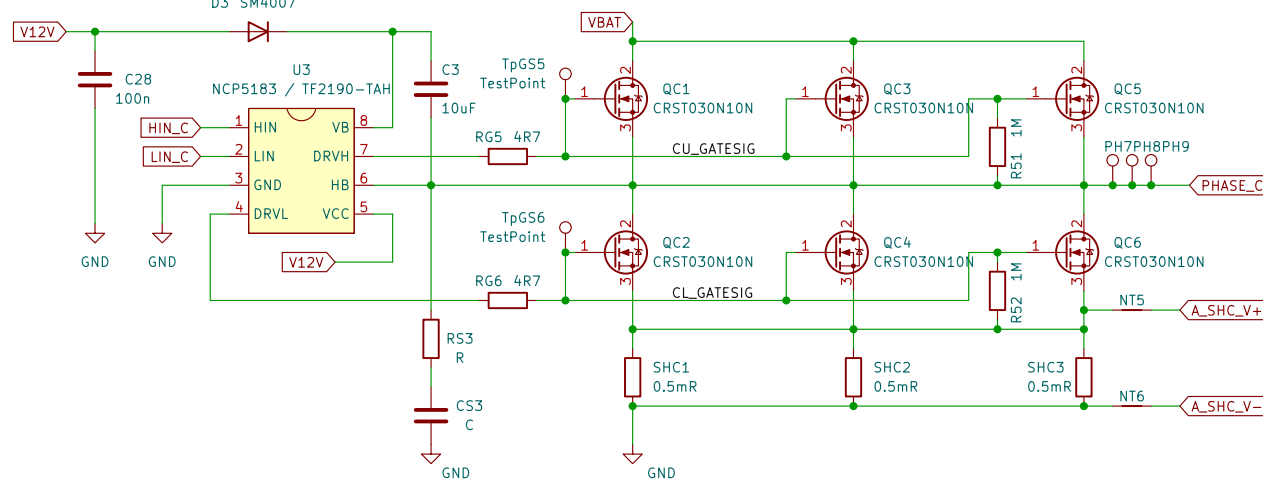
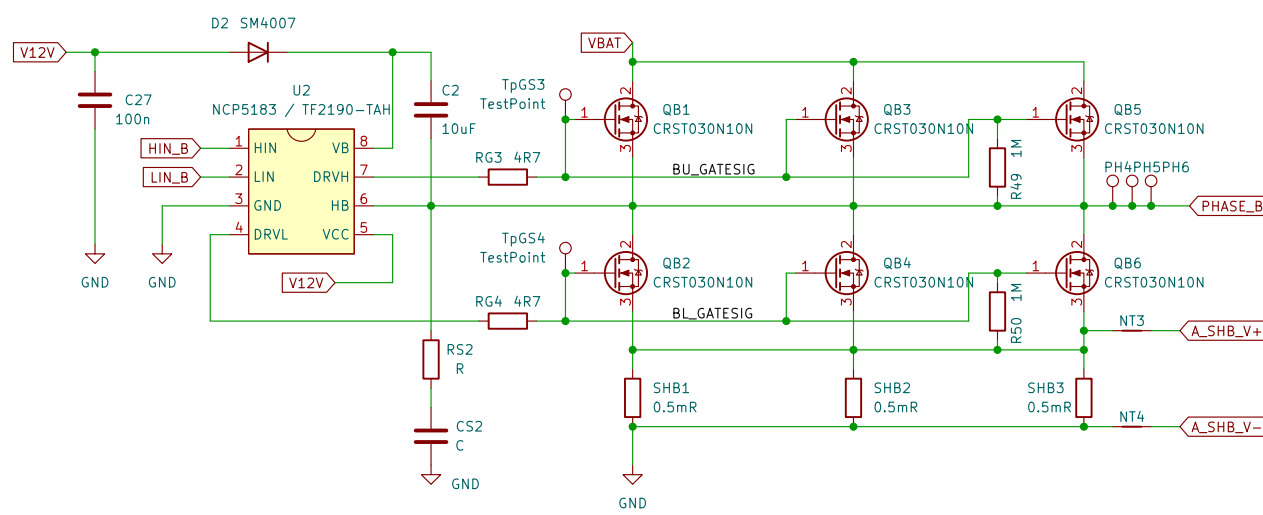
Input impedance 100R on every pin makes it much more resilient to ESD, cross wiring, GPIO-GND/3V3 etc

Notes on power stage design:

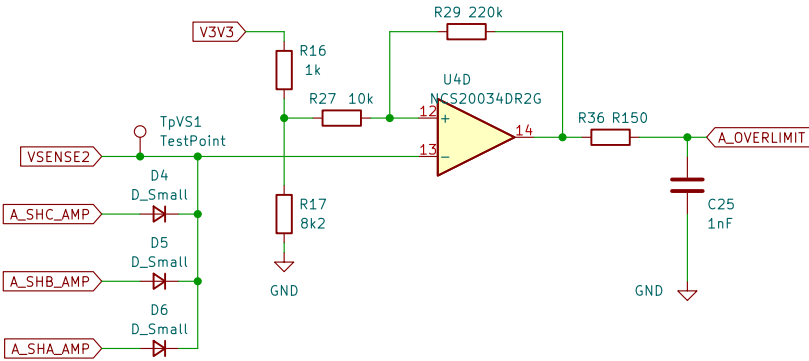
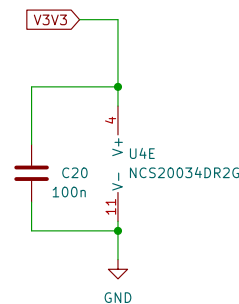
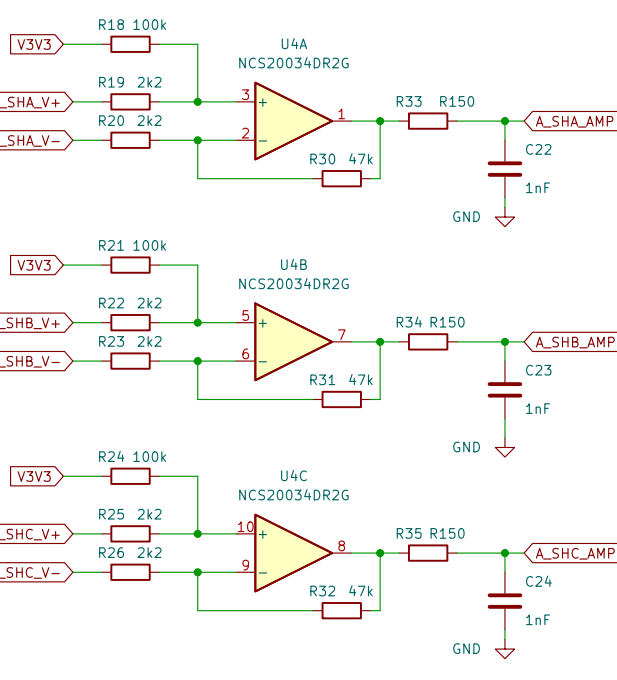
Pulldowns optional, most gate drivers pull down the FETs when UVLO
Acceptable to just have a single gate resistor since MOS usually has ~20hm gate resistors internally
MOS should have good Ciss/Crss ratio
Ciss/Crss>Vbat minimises the chance of parasitic turn-on.
Target gate time constant ~200ns:
 $R_g = \frac{2 \cdot 50hm \cdot (gate\ driver)}{4 \cdot 70hm \cdot (R_{ext})} + R_g/nFETs = \sim 80hm$
 $C_g = C_{iss} \times nFETs = \sim 30nF$
 $RC = 30nF \times 80hm = 240ns$



Snubbers may or may not be needed depending on FET choice.
Typically:
 $C = 1 \sim 5nF$
 $R = 0.5 \sim 5\ ohms$
The capacitor determines the power dissipated
The resistor dissipates the power.
Snubber should be tuned so that it has optimised damping factor for the ringing frequency targeted
Rough approximation, $RC = 1/2$ ringing period
e.g. 30MHz ringing -> 3ns period -> 1.5ns RC
2nF 1ohm is a good starting point
Highest damping factor usually where $C_{snub} \sim C_{oss}$ MOS



Opamp is a standard 50IC14 pinout. There are many that will fit. However, certain characteristics are needed:
GBP (GBW) Gain BandWidth Product >=4MHz
Rail to rail output
No phase inversion with exceeded limits
Input includes lower rail
Options are plentiful, preferred:
NCS20034 (NCS20074 might work)
TLV824
Current sensing ultimately defines the performance of your FOC algorithm, don't skip on this part.
Using the wrong opamp can cause nasty failures like phase inverted currents, saturated outputs...



Use low forward voltage diodes
1N5817 or 1N5819 is a good choice
Forward voltage at 1mA >0.3V will render this useless

