ECEE 434 Lab #4 - D-latch

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November 10, 2017

Contents

Introduction & Background

A D-latch circuit is a combination circuit consisting of CMOS inverters, transmission gates, and a clock signal. This circuit will transmit the signal on the D input line to the Q output when the CLK signal is high.

Procedure

This lab experiment began with creating the D-latch circuit shown in the lab write-up. The circuit uses three inverters (created in previous labs), two transmission gates, and a clock driving the circuit. See the schematic figure for the design.

Next, clock inputs were provided to the circuit along with a square wave used to represent data input. The function of the circuit was then observed using Virtuoso's simulator. After proper operation was verified, the clock frequency was increased to a failure point. The failure was then analyzed to determine what caused the circuit to fail.

Results

Conclusion