```
1   // HW#1 Question #4 testbench
2   module test_tb1();
3
4   reg [4:0] one,two,three,four,five,six,seven,eight;
5   wire [4:0] out;
6   reg [2:0] key;
7
8   test
    test(.one(one),.two(two),.three(three),.four(four),.five(five),.six(six),.seven(seven),.e
    ight(eight),
9   .key(key),.out(out));
10
11
12  initial begin
13
14  key = 3'b001;
15
16  one = 5'b00001;
17  two = 5'b01001;
18  three = 5'b01001;
19  four = 5'b01010;
20  five = 5'b00101;
21  six = 5'b00101;
22  seven = 5'b01110;
23  eight = 5'b01011;
24  #10;
25
26
27  end
28
29  endmodule
```