

```

1  module HW2Q2_tb ();
2
3  reg restart_tb, pause_tb, goto_third_tb;
4  wire odd_tb, even_tb, terminal_tb;
5  wire [2:0] out1_tb, out2_tb;
6
7  HW2Q2 HW2Q2(.restart(restart_tb), .pause(pause_tb), .goto_third(goto_third_tb),
8  .out1(out1_tb), .out2(out2_tb), .odd(odd_tb), .even(even_tb), .terminal(terminal_tb)) ;
9
10 initial begin
11 restart_tb = 1; pause_tb = 0; goto_third_tb = 0;
12 #1;
13
14 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
15 #1;
16
17 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
18 #1;
19
20 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
21 #1;
22
23 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
24 #1;
25
26 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
27 #1;
28
29 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
30 #1;
31
32 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
33 #1;
34
35 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
36 #1;
37
38 restart_tb = 1; pause_tb = 1; goto_third_tb = 1;
39 #1;
40
41 restart_tb = 1; pause_tb = 0; goto_third_tb = 1;
42 #1;
43
44 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
45 #1;
46
47 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
48 #1;
49
50 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
51 #1;
52
53 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
54 #1;
55
56 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
57 #1;
58
59 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
60 #1;
61
62 restart_tb = 0; pause_tb = 0; goto_third_tb = 0;
63 #1;
64
65 restart_tb = 0; pause_tb = 1; goto_third_tb = 0;
66 #1;
67 end
68 endmodule

```