

```

1  module HW2Q1_tb();
2
3  reg pause_tb, restart_tb, clk_tb, rst_tb;
4  wire odd_tb, even_tb, terminal_tb;
5  wire [1:0] state_tb;
6
7  fsm fsm(.state(state_tb), .odd(odd_tb), .even(even_tb), .terminal(terminal_tb),
8         .pause(pause_tb), .restart(restart_tb), .clk(clk_tb), .rst(rst_tb));
9
10
11  initial forever begin
12
13  clk_tb = 1; #1;
14  clk_tb = 0; #1;
15
16  end
17
18  initial begin
19  rst_tb = 0; #1;
20  rst_tb = 1; #1;
21  rst_tb = 0; #1;
22
23  restart_tb = 0; pause_tb = 1;
24  #1;
25  restart_tb = 1; pause_tb = 1;
26  #1;
27  restart_tb = 0; pause_tb = 0;
28  #1;
29  restart_tb = 0; pause_tb = 1;
30  #1;
31  restart_tb = 1; pause_tb = 1;
32  #1;
33  restart_tb = 0; pause_tb = 0;
34  #1;
35  restart_tb = 0; pause_tb = 0;
36  #1;
37  restart_tb = 0; pause_tb = 1;
38  #1;
39  restart_tb = 0; pause_tb = 0;
40  #1;
41  restart_tb = 0; pause_tb = 1;
42  #1;
43  restart_tb = 0; pause_tb = 0;
44  #1;
45  restart_tb = 0; pause_tb = 1;
46  #1;
47  restart_tb = 0; pause_tb = 0;
48  #1;
49  restart_tb = 0; pause_tb = 0;
50  #1;
51  restart_tb = 0; pause_tb = 1;
52  #1;
53
54  end
55
56  endmodule
57

```