Designing class A amplifiers to meet specified tolerances

Easy-to-follow method, which can be quickly carried out on a pocket calculator, takes the worry out of designing an optimized bipolar-transistor amplifier to specifications

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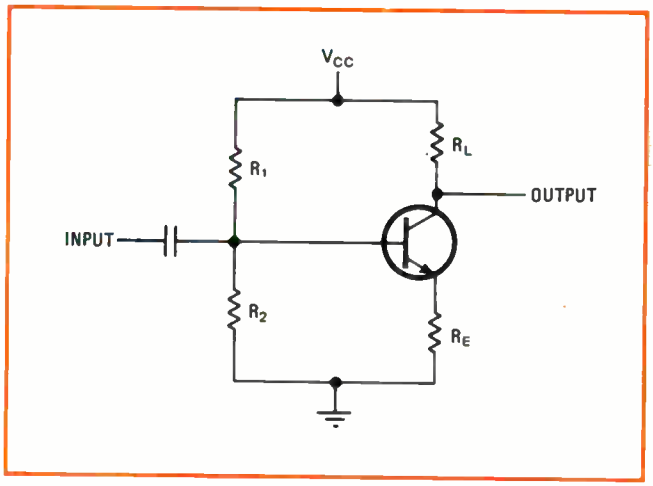
☐ At first thought, designing a class A amplifier stage may seem to be a simple, easy problem that is also well documented. But this is not true. Although nearly all electronics textbooks cover the selection of biasing components for a bipolar-transistor class A amplifier, no textbook presents a clear-cut method to design an optimum stage.

Instead, these texts often define various individual stability parameters, which are essentially partial derivatives of the amplifier's idling current with respect to some transistor parameter. A good design minimizes these partial derivatives, the reader is told, but no general technique is ever given to achieve this goal.

A design procedure that delivers

However, a simple, direct design procedure can be followed when specific design objectives must be met. The technique guarantees that the quiescent current of a class A amplifier will lie within a specified range for any given temperature environment and any type (number) of bipolar transistor. Furthermore, with this method, only the transistor specifications normally given on a data sheet need be known. There is also another advantage—the procedure is organized so that desired design values be computed on a calculator.



1. Standard stage. Location of the quiescent operating point of this class A power amplifier is critical. The design technique developed in this article takes worst-case operating conditions into consideration, as well as variations between devices in transistor parameters and the self-heating effects of a transistor junction.

The standard configuration for a class A transistor stage is shown in Fig. 1. The power gain of this stage will be optimized, while restricting the shift in the operating point to a specified value for a given temperature range and set of transistor parameters.

If the emitter resistor is bypassed by a large electrolytic capacitor, the gain of the amplifier can be increased significantly without sacrificing bias stability. However, such a capacitor is expensive, and the optimization of a bypassed stage requires complex procedures, as well as careful selection of the parameter to be optimized.

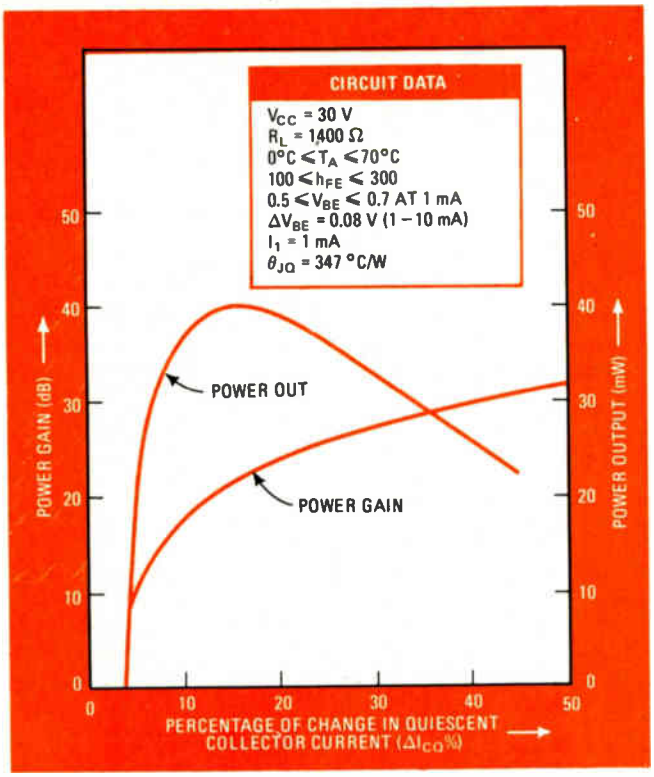
This design technique takes into account the variation of the transistor's base-emitter voltage (V_{BE}) and forward current-transfer ratio (h_{FE}) with junction temperature and collector current. The statistical spread between devices in the values of a transistor parameter is also taken into consideration.

Since the computation is carried out on a worst-case basis, the actual operating-point shift should be considerably smaller than the maximum allowed in the design. Under no condition, within design limits, will the transistor's collector current exceed its specified maximum allowable value (I_{Cmax}) or be less than its specified minimum value (I_{Cmin}). All other important transistor factors are also accounted for, including the self-heating of the junction.

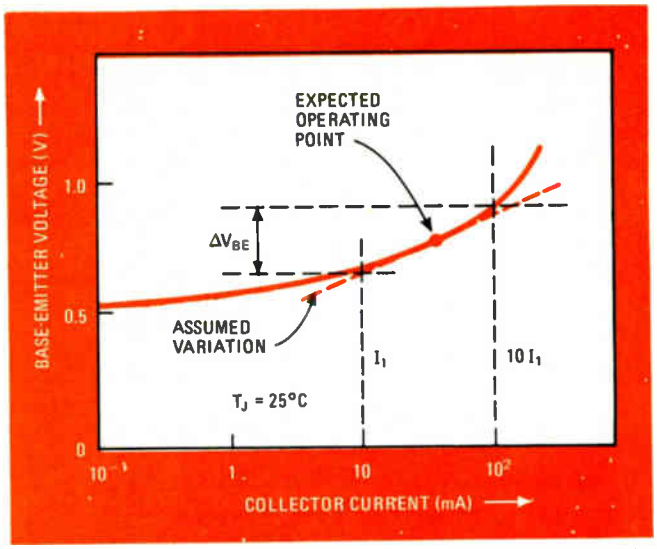
The complete design procedure is summarized for easy reference in "Calculating a class A amplifier design," p. 117. To begin with, a suitable power-supply voltage (V_{CC}) must be chosen so that V_{CC} is regulated within reasonable limits, say ±5%. This is particularly important for a class A amplifier because the quiescent transistor collector current (I_{CQ}) does not vary with signal level. The maximum allowable collector-current variation is selected at this point. If this current limit is set tighter than ±10%, the amplifier's output power is generally reduced because the value of the emitter resistor (R_E) must be greatly increased.

Figure 2 shows the variation in amplifier power output and power gain versus the percentage of shift in quiescent collector current (ΔI_{CQ}) for a small-signal transistor. The power gain increases monotonically as ΔI_{CQ} becomes larger, but the maximum power output decreases because the output voltage swing becomes smaller. A reasonable choice for ΔI_{CQ} is ±20%. Clearly, output voltage swing may be traded for power gain.

The next step in the design procedure is to determine



2. Trading off gain and swing. For large variations in quiescent collector current, power gain increases, but power output decreases because the output-voltage swing becomes smaller. The change in collector current should be some reasonable value like ±20%.



3. A reasonable assumption. The change in transistor base-emitter voltage can be regarded as constant over a (log) decade variation in collector current, so long as the current is not too large.

several key parameters from the transistor's data sheet. Figure 3 shows how to find the typical base-emitter voltage change (ΔV_{BE}) from the device's plot of V_{BE} versus I_C. A convenient decade of collector current, which should bracket the desired operating point, is selected to establish currents I_1 and $10I_1$.

This information is used to predict the variation of V_{BE} with collector current. The base-emitter voltage is assumed to be proportional to the logarithm of the collector current. For an ideal transistor junction at room temperature, the proportion coefficient is 60 millivolts per decade of change in the collector current. Real devices deviate from this value, particularly at high currents. Under very-high-current conditions, the logarithmic assumption also breaks down. However, by careful selection of the I_1 current point, the error may be made quite small, as illustrated in Fig. 3.

The unit-to-unit statistical variation of V_{BE} at current I_1 is accounted for by determining two additional parameters: V_{BE1min}, the minimum base-emitter voltage at current I_1 and at a junction temperature of 25°C; and V_{BE1max}, the maximum base-emitter voltage at 25°C.

The transistor's thermal resistance (θ_{JA}) also must be computed:

$$\theta_{JA} = (T_{Jmax} - 25°C)/P_D \quad (1)$$

where T_{Jmax} is the maximum junction temperature rating, and P_D is the maximum rated transistor power dissipation at 25°C. If the transistor is mounted on a heat sink, the ambient temperature is taken to be the transistor's case temperature.

With the next step, the actual design procedure begins. Initially, the emitter resistance is assumed to be 10% of the collector load resistance. This assumption is merely a convenient starting point and does not prejudice the final value of R_E. The minimum load resistance (R_{LI}) that the transistor can drive within its thermal limits is determined first:

$$R_{L1} = \theta_{JA}V_{CC}^2/[4.4(T_{Jmax} - T_{Amax})] = R_{Ln} \quad (2)$$

where T_{Amax} is the maximum ambient temperature. A larger value of R_L may be employed and, if desired, should be specified at this point in the procedure. The emitter resistance is computed next:

$$R_{E1} = R_{L1} \times 10\% = R_{En} \quad (3)$$

Now find the operating point for the maximum output voltage swing:

$$I_{CQ} = V_{CC}/[2(R_{Ln} + R_{En})] \quad (4)$$

If a different quiescent current is desired, it should be specified at this point. The operating-point current limits are also found:

$$I_{Cmax} = I_{CQ}(1 + \Delta I_{CQ}) \quad (5)$$
$$I_{Cmin} = I_{CQ}(1 - \Delta I_{CQ}) \quad (6)$$

where ΔI_{CQ} is the maximum percentage change in quiescent current.

Determining the bias components

The pertinent biasing equations are then solved to determine the minimum emitter resistance for stable operation and maximum power gain. The approximate maximum temperature that the transistor junction will attain is computed first. This temperature should be less than the absolute maximum rating, T_{Jmax}:

$$T_{max} = \theta_{JA}I_{CQ}[V_{CC} - (R_{Ln} + R_{En})I_{CQ}] + T_{Amax} \quad (7)$$

The actual V_{BE} voltage at T_{max} is then determined:

$$V_{BEX} = V_{BE1min} + \Delta V_{BE}\, log(I_{Cmax}/I_1) - 0.0022(T_{max} - 25°C) \quad (8)$$

Next, the minimum junction temperature of the tran-

Calculating a class A amplifier design

A class A amplifier stage built with a bipolar transistor can be designed by means of these fairly simple computations on a pocket calculator.

- Set design objectives. Choose a suitable bipolar transistor type and the regulated power-supply voltage (V_{CC}). Establish:

  ΔI_{CQ} = *maximum desired percentage variation of quiescent current*
  T_{Amax} = *maximum ambient temperature (use the maximum case temperature for a transistor mounted on a heat sink)*

- From the transistor's data sheet, determine:

  T_{Jmax} = *maximum junction temperature rating*
  P_D = *maximum rated power dissipation at 25°C*
  I_1 = *collector current, usually selected for convenience so that I_1 and $10I_1$ bracket the expected operating point*
  ΔV_{BE} = *typical base-emitter voltage change over the range of I_1 to $10I_1$ at 25°C*
  V_{BE1min} = *minimum base-emitter voltage at I_1, 25°C*
  V_{BE1max} = *maximum base-emitter voltage at I_1, 25°C*

- Calculate the transistor's thermal resistance:

$$\theta_{JA} = (T_{Jmax} - 25°C)/P_D$$

- Estimate the minimum load resistance (R_{L1}) and the emitter resistance (R_{E1}):

$$R_{L1} = \theta_{JA}V_{CC}^2/[4.4(T_{Jmax} - T_{Amax})] = R_{Ln}$$
$$R_{E1} = R_{L1} \times 10\% = R_{En}$$

- Calculate the quiescent current and its limits:

$$I_{CQ} = V_{CC}/[2(R_{Ln} + R_{En}]$$
$$I_{Cmax} = I_{CQ}(1 + \Delta I_{CQ})$$
$$I_{Cmin} = I_{CQ}(1 - \Delta I_{CQ})$$

- Calculate the base-emitter voltage (V_{BEX}) under hot, high-current conditions:

$$T_{max} = \theta_{JA}I_{CQ}[V_{CC} - (R_{Ln} + R_{En})I_{CQ}] + T_{Amax}$$
$$V_{BEX} = V_{BE1min} + \Delta V_{BE}\, log(I_{Cmax}/I_1) - 0.0022(T_{max} - 25°C)$$

- Calculate the base-emitter voltage (V_{BEN}) under cold, low-current conditions:

$$T_{min} = \theta_{JA}I_{Cmin}[V_{CC} - (R_{Ln} + R_{En})I_{Cmin}] + T_{Amin}$$
$$V_{BEN} = V_{BE1max} + \Delta V_{BE}\, log(I_{Cmin}/I_1) - 0.0022(T_{min} - 25°C$$

- Make a better estimate for the emitter resistance:

$$R_{E(n+1)} = [-2(V_{BEX} - V_{BEN})]/[I_{Cmax} - I_{Cmin}]$$

If V_{BEX} is greater than V_{BEN}, R_E may be set to zero, and the value for R_L increased by 10%. Then repeat the design procedure with the new resistance values. The design procedure must also be repeated if $R_{E(n+1)}$ differs from R_{En} by more than 5%, or if T_{max} is more than T_{Jmax}. In the case of the latter condition, the value of R_L must be increased slightly.

- From the transistor's data sheet, determine:

  h_{FEmax} = *maximum worst-case current gain at T_{max} or T_{min} and I_{Cmax} or I_{Cmin}*
  h_{FEmin} = *minimum worst-case current gain at T_{max} or T_{min} and I_{Cmax} or I_{Cmin}*

- Calculate the Thevenin-equivalent resistance (R_B) and voltage (V_{BB}) for the amplifier's bias network:

$$R_B = [h_{FEmax}h_{FEmin}[R_{E(n+1)}(I_{Cmax} - I_{Cmin}) + V_{BEX} - V_{BEN}]]/[h_{FEmax}I_{Cmin} - h_{FEmin}I_{Cmax}]$$
$$V_{BB} = V_{BEN} + I_{Cmin}[(R_B/h_{FEmin}) + R_{E(n+1)}]$$

- Calculate the values of resistors R_1 and R_2:

$$R_1 = R_BV_{CC}/V_{BB}$$
$$R_2 = R_BV_{CC}/(V_{CC} - V_{BB})$$

- Check the minimum power gain of the stage:

$$A_P = [R_BR_Lh_{FEmin}]/[R_E(R_B + h_{FEmin}R_E)]$$

- Check the minimum signal power of the stage:

$$P_S = (1 - \Delta I_{CQ})^2[V_{CC}^2R_L/8(R_L + R_E)^2]$$

If the minimum power gain is not large enough, another transistor type should be selected— one whose h_{FEmin} value is higher.

sistor is found, with junction self-heating effects taken into consideration:

$$T_{min} = \theta_{JA}I_{Cmin}[V_{CC} - (R_{Ln} + R_{En})I_{Cmin}] + T_{Amin} \quad (9)$$

And the base-emitter voltage at T_{min} is calculated:

$$V_{BEN} = V_{BE1max} + \Delta V_{BE}\, log(I_{Cmin}/I_1) - 0.0022(T_{min} - 25°C) \quad (10)$$

Normally, V_{BEX} is less than V_{BEN}, making it necessary to include an emitter resistor. But if V_{BEX} is greater than V_{BEN}, R_E can be eliminated ($R_E = 0$), and the load resistance (R_L) increased by 10%. Then repeat the design procedure, using the new values for R_E and R_L.

Now a better estimate can be obtained for R_E:

$$R_{E(n+1)} = [-2(V_{BEX} - V_{BEN})]/[I_{Cmax} - I_{Cmin}] \quad (11)$$

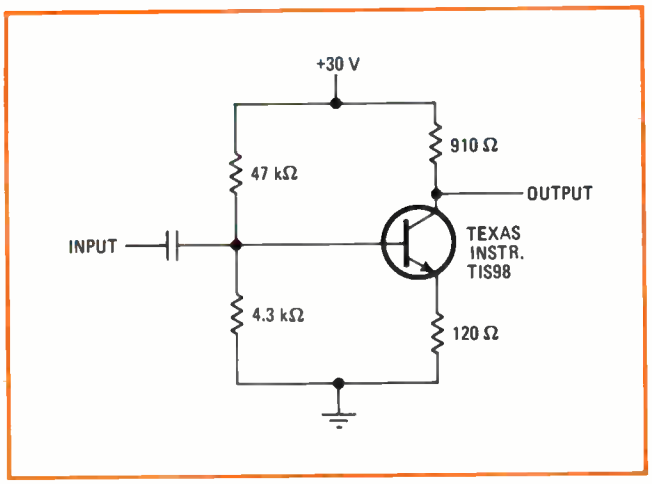
If $R_{E(n+1)}$ is not within ±5% of the R_{En} value, the design procedure must be repeated to this point. Moreover, when T_{max} exceeds T_{Jmax}, R_L must be made slightly larger. This process converges rapidly and seldom requires more than two iterations. If $R_{E(n+1)}$ should continue to increase and approach the value of R_L, then ΔI_{CQ} is too small and cannot be realized with the transistor type selected while retaining reasonable power gain. Possibly, an emitter-follower should be used instead of a common-emitter amplifier.

The transistor's data sheet is now consulted again to find the maximum and minimum values of current gain (h_{FE}). These two values are determined by using the worst-case combination between T_{max} or T_{min} and I_{Cmax} or I_{Cmin}. The h_{FEmax} and h_{FEmin} values must be known accurately in order to predict the minimum power gain of the stage.

Next, the Thevenin-equivalent circuit values are found for the amplifier's biasing network:

$$R_B = [h_{FEmax}h_{FEmin}[R_{E(n+1)}(I_{Cmax} - I_{Cmin}) + V_{BEX} - V_{BEN}]]/[h_{FEmax}I_{Cmin} - h_{FEmin}I_{Cmax}] \quad (12)$$
$$V_{BB} = V_{BEN} + I_{Cmin}[(R_B/h_{FEmin}) + R_{E(n+1)}] \quad (13)$$

Resistors R_1 and R_2 are now easily computed:



4. For instance. Amplifier stage, designed with the procedure described here, is optimized for maximum power output (22.8 decibels) and maximum power gain (61.8 milliwatts) from 0°C to 70°C.

$$R_1 = R_B V_{CC}/V_{BB} \quad (14)$$
$$R_2 = R_B V_{CC}/(V_{CC} - V_{BB}) \quad (15)$$

The closest standard-value resistances are usually good enough to use for R_1 and R_2. These last equations are valid provided that:

$$(h_{FEmax}/h_{FEmin}) \text{ is greater than } (I_{Cmax}/I_{Cmin})$$

which is a condition that is generally satisfied because most transistors have a large spread of h_{FE} values.

To check the usefulness of the stage, its minimum power gain must be calculated:

$$A_P = [R_B R_L h_{FEmin}]/[R_E(R_B + h_{FEmin} R_E)] \quad (16)$$

The stage's minimum signal gain must also be checked:

$$P_S = (1 - \Delta I_{CQ})^2 [V_{CC}^2 R_L/8(R_L + R_E)^2] \quad (17)$$

If either A_P or P_S is insufficient, a heat sink can be added to the transistor, or a transistor type having a higher h_{FEmin} can be substituted. In the equations for A_P and P_S, the static forward-current transfer ratio is used instead of the more correct dynamic h_{FEmin} value. Since the static h_{FEmin} is a worst-case minimum value, the minimum power gain computed with it is a bit lower than the gain actually will be.

The entire design procedure, which may appear to be somewhat complicated, is really quite simple and rapid when done on a pocket calculator, especially one like the HP-35 or the HP-45. A programable calculator makes the procedure even easier to run through. The technique, of course, also can be written as a Basic or Fortran program.

Solving a practical problem

A design example will help to clarify the procedure. A single-stage class A amplifier is needed to operate from a 30-v power supply. The maximum power output and maximum power gain must be obtained from a Texas Instruments type TIS98 transistor over an ambient temperature range of 0°C to 70°C, with a maximum quiescent-current variation of ±20%.

From the transistor's data sheet, determine:

$T_{Jmax} = 150°C$
$P_D = 0.36\ W$
$\Delta V_{BE} = 0.10\ V$ *from 3 to 30 mA*
$V_{BE1min} = 0.54\ V$ *at 3 mA at 25°C*
$V_{BE1max} = 0.74\ V$ *at 3 mA at 25°C*
$I_1 = 0.001\ A$

Now the transistor's thermal resistance can be computed from Eq. 1:

$$\theta_{JA} = (150 - 25)/0.36 = 347\,°C/W$$

The load and emitter resistances are found next from Eqs. 2 and 3:

$$R_{L1} = (347)(30^2)/4.4(150 - 70) = 888 \text{ ohms}$$
$$R_{E1} = 888 \times 10\% = 89 \text{ ohms}$$

Three iterations of the design procedure are needed to produce a better estimate for the emitter resistance: Equations 4 through 11 are used to do this:

PARAMETER	ITERATION 1	2	3
R_L (ohms)	888	910	910
I_{CQ} (mA)	15.4	14.7	14.6
I_{Cmax} (mA)	18.4	17.7	17.5
I_{Cmin} (mA)	12.3	11.8	11.7
T_{max} (°C)	150	146.5	146.1
V_{BEX} (V)	0.344	0.350	0.351
T_{min} (°C)	77	73.6	73.1
V_{BEN} (V)	0.687	0.693	0.694
$R_{E(n+1)}$ (ohms)	112.4	116.1	118.3
% change	26%	3.3%	1.8%

The nearest standard-value resistor—120 ohms—is chosen for R_E.

Once again, the transistor's data sheet is read to obtain the properly and carefully scaled values needed for transistor current gain:

$h_{FEmax} = 600$ *at 150°C at 18 mA*
$h_{FEmin} = 100$ *at 80°C at 12 mA*

These gain values are then used to find the Thevenin-equivalent circuit values for the amplifier's biasing network. The nearest standard resistance value should be substituted for R_E (120 ohms) and R_L (910 ohms). From Eq. 12:

$$R_B = \frac{600(100)[120(0.0175 - 0.0117) + 0.351 - 0.694]}{600(0.0117) - 100(0.0175)}$$
$$R_B = 4{,}019 \text{ ohms}$$

And from Eq. 13:

$$V_{BB} = 0.694 + 0.0117[(4{,}019/100) + 120]$$
$$V_{BB} = 2.568\ V$$

The values of biasing resistors R_1 and R_2 can now be calculated by using Eqs. 14 and 15:

$$R_1 = 4{,}019(30)/2.568 = 47 \text{ kilohms}$$
$$R_2 = 4{,}019(30)/(30 - 2.568) = 4.3 \text{ kilohms}$$

The power gain of the stage (Eq. 16) will be:

$$A_P = \frac{4{,}019(910)(100)}{120[4{,}019 + 100(120)]} = 190 = 22.8\ dB$$

And the stage's signal power (Eq. 17) will be:

$$P_S = (1 - 0.20)^2[(30^2)(910)/8(850 + 120)^2]$$
$$P_S = 61.8\ mW$$

Figure 4 shows the final, complete amplifier design. □