

Swakeup

PROJECT REPORT

within the lecture of Programming Embedded Systems

 ${\rm at~Uppsala~University} \\ {\rm in~the~Departement~of~Information~Technology}$

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1 Introduction

2 Background and Analysis

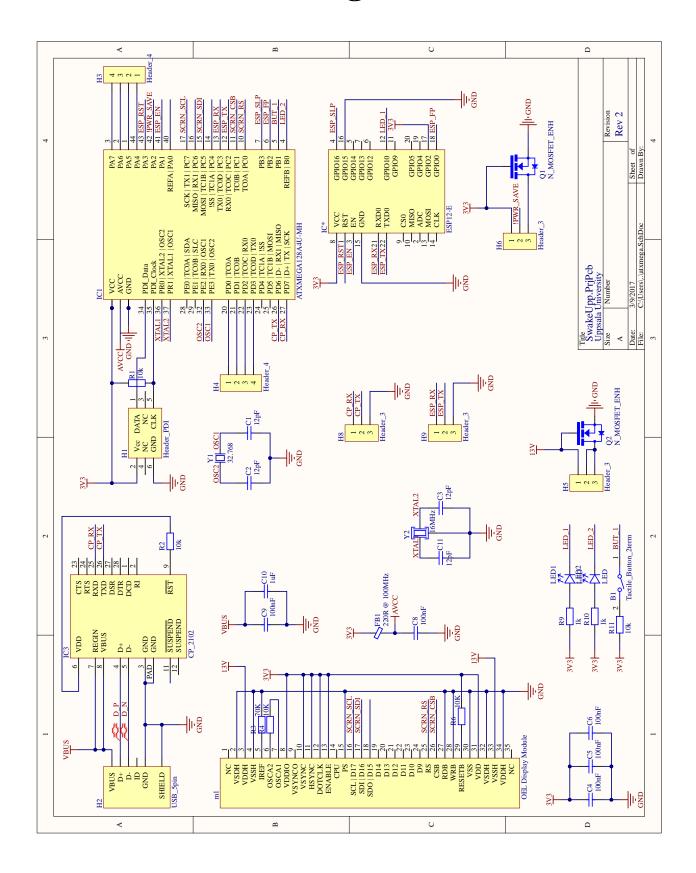
3 Design

4 Implementation

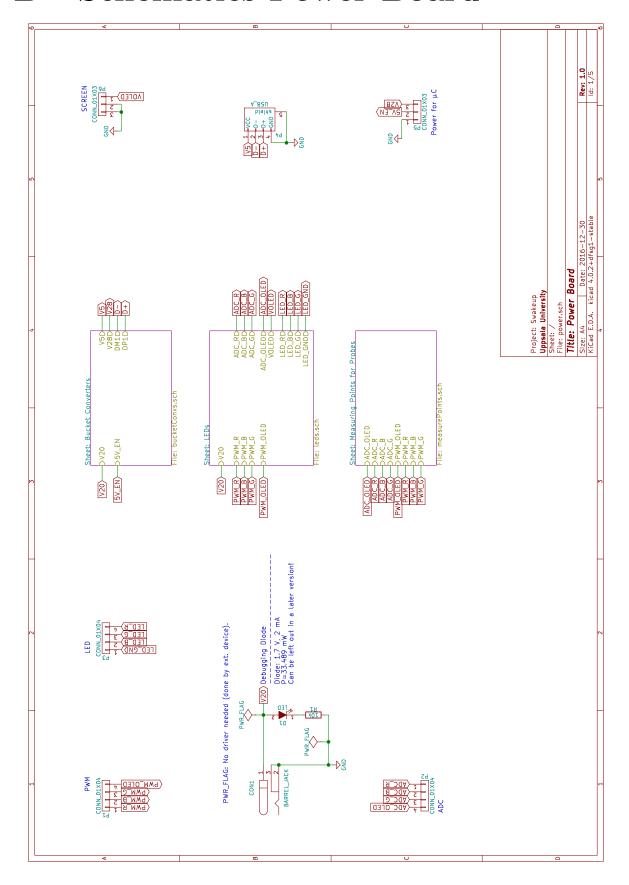
5 Testing

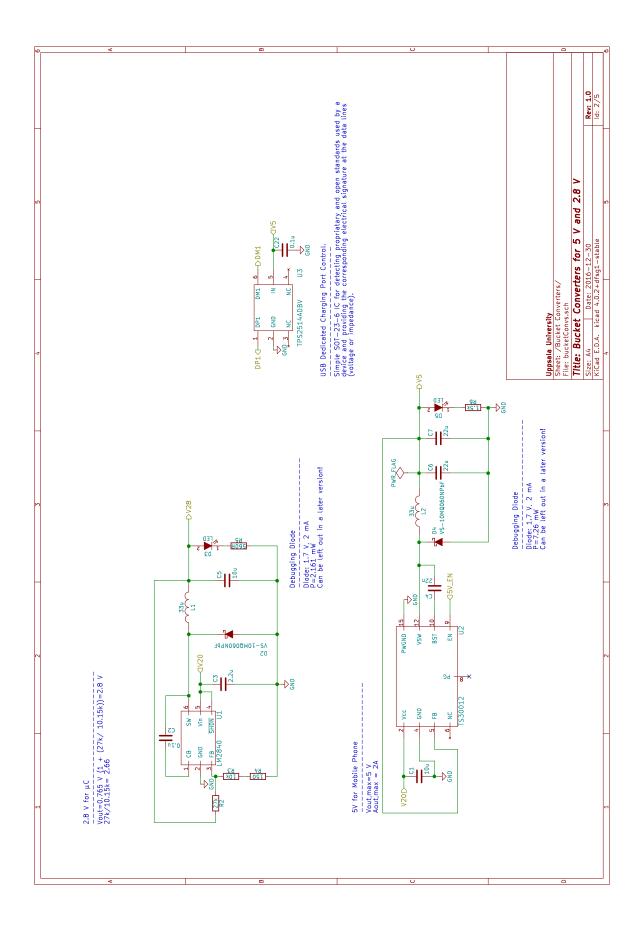
6 Conclusion

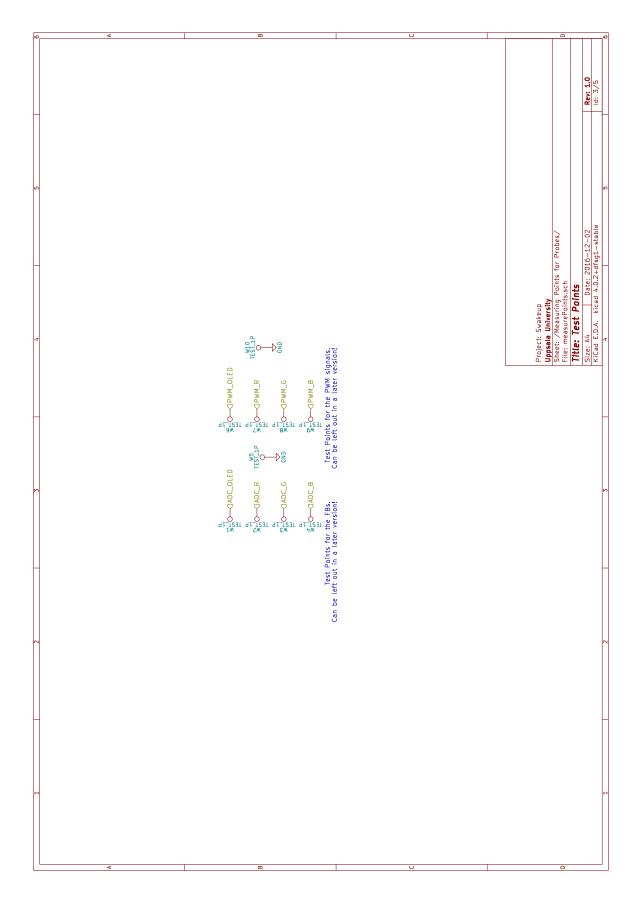
A Schematics Logic Board

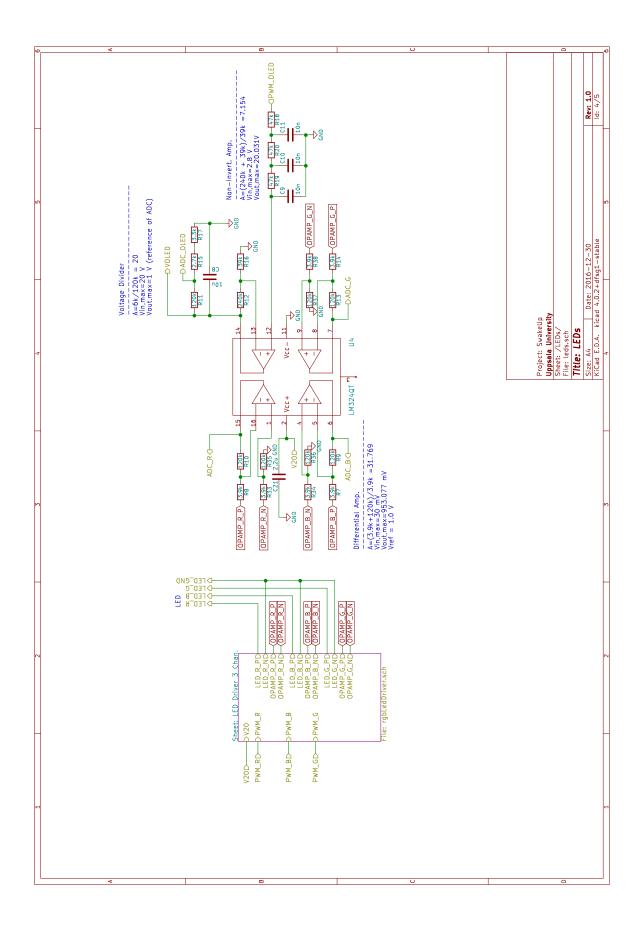


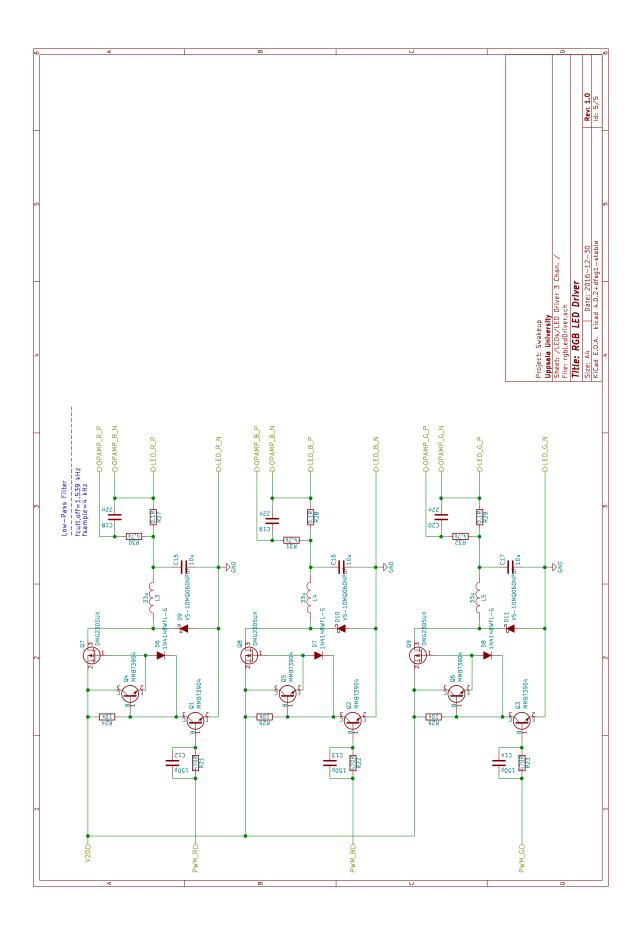
B Schematics Power Board











C USART interrupt generation

```
#define USARTRXCISR(NAME, PORT, USART_ID, REC_FC)
1
     ISR(NAME##_RXC_vect) {
2
             uint8_t read = PORT.DATA;
             if (writeInBuf(read, &PORT)) {
             REC_FC(read);
             uint8\_t i = 0;
6
             for (; i < UART_MAX_DELIMITERS; i++) {</pre>
                     if (delimiters[USART_ID][i].delimiter != 0) {
                              delimiters[USART_ID][i].length++;
9
                              if (read == delimiters[USART_ID][i].delimiter) {
10
                                      delimiters[USART_ID][i].port = &PORT;
11
                                      event_fire(&EVENT_UART_DELIMITER,
12
                                      SYSTEM_ADDRESS_CAST (&delimiters[USART_ID][i])); \
13
15
16
             } else {/*buffer full */
17
                     CP_PORT.CTRLA &= ~(USART_RXCINTLVL_LO_qc); \
18
19
20
21
     #define USARTDREISR(NAME, PORT, USART_ID) \
22
     ISR(NAME##_DRE_vect) {
23
             uint8_t size = uartStatus[USART_ID].outBuffer_size;
24
             if (size > 0) { \
                     if (softlock(USART_ID)) {\
                              uint8_t tail = uartStatus[USART_ID].outBuffer_tail;\
27
                              PORT.DATA = outBuffer[USART_ID][tail]; \
28
                              uartStatus[USART_ID].outBuffer_size--; \
29
                              tail++; \
30
                              if (tail >= UART_MAX_OUT_BUFFER) tail = 0;\
31
                              uartStatus[USART_ID].outBuffer_tail = tail;\
32
                              unlock(USART_ID); \
33
34
             } else {\
35
                      sending[USART_ID] = 0;\
36
                     PORT.CTRLA &= ~(USART_DREINTLVLO_bm); \
37
             71
38
39
```