SmartXX LT OPX

Software Developer Documentation

PV SysCVer5 Rev0.20

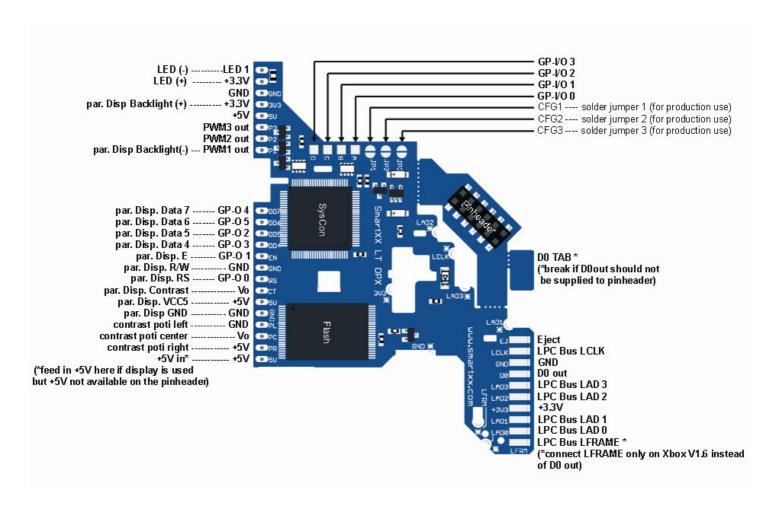
Preliminary

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1. HARDWARE DIAGRAM

1-1 SmartXX LT OPX Overview:



2. REGISTER MAP

TABLE 1: REGISTER MAP OVERVIEW

Address (hex)	Name Funktion	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POWER-ON Reset
F700h read	GP-I/O Input	-	-	1	1	GP-I/O 3	GP-I/O 2	GP-I/O 1	GP-I/O 0	*1
F700h write	GP-O (Display Port)	1	GP-O 5 (Data 6)	GP-O 4 (Data 7)	GP-O 3 (Data 4)	GP-O 2 (Data 5)	GP-O 1 (E)	GP-O 0 (RS)	-	-000 000-
F701h read	Chip Version	-	-	-	-		SysCon Cl	nip Version		1001 *2
F701h write	PWM1 Out (Brightnes Control)	-	PWM Value (PWM 1 out, Value 0 to 127)						-000 0000 *3	
F702h read	Solder Jumper State	1	1	1	1	-	CFG3	CFG2	CFG1	*4
F702h write	LED Controll	-	1	1	1	-	-	-	Led	0x *5
F70Ah write	GP-I/O Output	-	-	-	-	GP-I/O 3	GP-I/O 2	GP-I/O 1	GP-I/O 0	0000
F70Bh write	GP-I/O Direction Control	-	-	-	-	GP-I/O 3		GP-I/O 1	GP-I/O 0	1111 *6
F70Ch write	PWM2 Out (Brightnes Control)	-				PWM Value out, Value				-000 0000 *3
F70Dh write	PWM3 Out (Brightnes Control)	-				PWM Value out, Value				-000 0000 *3

Leaend:

Logona.		
Shaded boxes	=	Not implemented or not used
-	=	Not implemented. For future compatibility write '0', read value may undefinded and have to be mask
*1	=	Also initial state depends on connected hardware
*2	=	To be changed on newer Syscon Revisions
*3	=	PWM values from '0' to '127' are allowed to write.
		Value '0' => output is open collector all the time, value '127' => output is low all the time. Value in between cause the output to toggle between those two states with the value defined ratio
*4	=	Depends on setup of Solder Jumper configuration (soldered or not soldered together)
*5	=	When '0' then LED is 'ON', when '1' LED is 'OFF'
		'x' states the D0 level (SmartXX is ON or OFF)
()	=	GP-O function as used from OS already (build V3331)

2-1 GP-I/O REGISTER

FIGURE 2-1-1: GP-I/O READ REGISTER (ADDRESS:F700h)

	_	_		GP-I/O 3	GP-I/O 2	GP-I/O 1	GP-I/O 0
bit 7	bit 6	Bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	Sit 0	Dit 0	DIC 1	Dit 0	DR 2	Dit 1	510 0
bit 7:	not used						
bit 6:	not used						
bit 5:	not used						
bit 4:	not used						
bit 3:	read level from C	GP-I/O 3					
bit 2:	read level from C	GP-I/O 2					
bit 1:	read level from C	GP-I/O 1					
bit 0:	read level from C	GP-I/O 0					
NOTE:							
=	this bit is not use	ed, read value	is undefind an	d should be m	ask		

FIGURE 2-1-2: GP-I/O WRITE REGISTER (ADDRESS:F70Ah)

		, , , , , , , , , , , , , , , , , , , ,		DDI(LOO.II	. •		
_	_	_	_	GP-I/O 3	GP-I/O 2	GP-I/O 1	GP-I/O 0
bit 7	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0
bit 7:	not used						
bit 6:	not used						
bit 5:	not used						
bit 4:	not used						
bit 3:	write level to GP	-I/O 3					
bit 2:	write level to GP	-I/O 2					
bit 1:	write level to GP	-I/O 1					
bit 0:	write level to GP	-I/O 0					
NOTE:							
_ =	this bit is not use	ed, write to it ha	as not affect, fo	or future comp	atibility there s	hould be writte	en a '0'

FIGURE 2-1-3: GP-I/O DIRECTION CONTROL REGISTER (ADDRESS:F70Bh)

				GP-I/O 3	GP-I/O 2	GP-I/O 1	GP-I/O 0
				0	0 0 2	0	0 0
bit 7	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0

If bit is set to '1' the corespondig GP-I/O is input, if set to '0' coresponding GP-I/O is a output.

bit 7: not used

bit 6: not used

bit 5: not used

bit 4: not used

bit 3: set direction of GP-I/O 3

bit 2: set direction of GP-I/O 2

bit 1: set direction of GP-I/O 1

bit 0: set direction of GP-I/O 0

NOTE:

— = this bit is not used, write to it has not affect, for future compatibility '1' should be written

2-2 GP-O REGISTER

FIGURE 2-2-1: GP-O WRITE REGISTER (ADDRESS:F700h)

GP-O function as used from OS already (build V3331)

	00.05	00.04	00.04	00.00	00.04	00.00	
_	GP-O 5	GP-0 4	GP-0 4	GP-0 2	GP-O 1	GP-O 0	_
	(Data 6) [SPI-OUT]	(Data 7) [SPI-CS2]	(Data 4)	(Data 5)	(E)	(RS)	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
bit 7:	not used						
bit 6:	write level to GP	-O 5 (paral	lel Display sigr	nal 'Data 6')			
bit 5:	write level to GP	-O 4 (paral	lel Display sigr	nal 'Data 7')			
bit 4:	write level to GP	-O 3 (paral	lel Display sigr	nal 'Data 4')			
bit 3:	write level to GP	-O 2 (paral	lel Display sigr	nal 'Data 5')			
bit 2:	write level to GP	-O 1 (paral	lel Display sigr	nal 'E')			
bit 1:	write level to GP	-O 0 (paral	el Display sigr	nal 'RS')			
bit 0:	not used						

NOTE:

()

this bit is not used, write to it has not affect, for future compatibility '0' should be written

2-3 SPECIAL WRITE REGISTER

FIGURE 2-3-1: PWM1 OUTPUT WRITE REGISTER (ADDRESS:F701h)

___ PWM Value
bit 7 bit 6 bit 5 Bit 4 bit 3 bit 2 bit 1 bit 0

7 Bit Pulse Wide Modulation (PWM) output controll register:

This feature is mainly implemented to allow LED or EL Backlight units, normaly build into standard LCD Displays, to be controlled by software. If not used for this purpose, this output could even be used for other functions like simple brightness control of hooked up LED's or even as single digital output.

bit 7 not used

bit 6 - bit 0: Pulse Wide Modulation (PWM) Value

Value Range: '0' to '127',

where '0' means output is always 'high' (open collector)

and '127' means output is always 'low' (GND)

Values in between '0' and '127' defines the ratio between 'low' to 'high' time.

NOTE:

— = this bit is not used, write to it has not affect, for future compatibility '0' should be written

FIGURE 2-3-2: PWM2 OUTPUT WRITE REGISTER (ADDRESS:F70Ch)

ı								
					PWM Value			
	bit 7	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0

Extended 7 Bit Pulse Wide Modulation (PWM) output controll register:

This output could be used for functions like simple brightness control of hooked up LED's or even as single digital output.

bit 7 not used

bit 6 – bit 0: Pulse Wide Modulation (PWM) Value

Value Range: '0' to '127',

where '0' means output is always 'high' (open collector)

and '127' means output is always 'low' (GND)

Values in between '0' and '127' defines the ratio between 'low' to 'high' time.

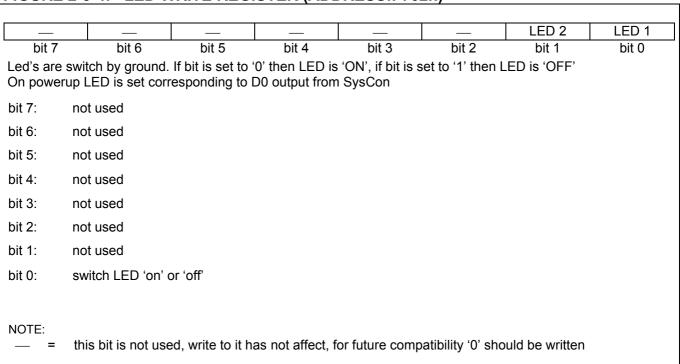
NOTE:

— = this bit is not used, write to it has not affect, for future compatibility '0' should be written

FIGURE 2-3-3: PWM3 OUTPUT WRITE REGISTER (ADDRESS:F70Dh)

				PWM Value			
bit 7	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0
	it Pulse Wide Mould be used for	,	, .		hooked up LE	D's or even as	s single digita
bit 7	not used						
bit 6 – bit 0:	Pulse Wide M	odulation (PW	/M) Value				
		ins output is a	lways 'high' (o _l lways 'low' (Gl	,			
	Values in betw	veen '0' and '1	27' defines the	e ratio betweei	n 'low' to 'high'	time.	
NOTE							
NOTE: = th	is bit is not use	d, write to it ha	as not affect, fo	or future comp	atibility '0' sho	uld be written	

FIGURE 2-3-4: LED WRITE REGISTER (ADDRESS:F702h)



2-4 SPECIAL READ REGISTER

FIGURE 2-4-1: CFG SOLDER JUMPER READ REGISTER (ADDRESS:F702h)

	_		_		CFG3	CFG2	CFG1
bit 7	bit 6	Bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4 not sold	ered CFG Solder .	Jumper read's	as '1', if solde	ered it will rea	d as '0'		
bit 7:	not used						
bit 6:	not used						
bit 5:	not used						
bit 4:	not used						
bit 3:	not used						
bit 2:	CFG3 Solder Jui	mper state					
bit 1:	CFG2 Solder Jui	mper state					
bit 0:	CFG1 Solder Jui	mper state					
NOTE:							
_ =	this bit is not use	ed, read value	is undefind an	d should be n	nask		

2-5 SYSCON CHIP INTERNALS

FIGURE 2-5-1: SYSCON VERSION READ REGISTER (ADDRESS:F701h)

				SysCon Chip Version					
bit 7	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0		
bit 7	not used								
bit 6:	not used								
bit 5:	not used								
bit 4:	not used								
bit 3 – bit 0:	This version	register shoul	d always read t Nerions functi		ing any other fu changes.	unctions on the	Chip, to		
NOTE:									
= 1	this bit is not u	sed, read valu	ie is undefind a	nd should be	mask				