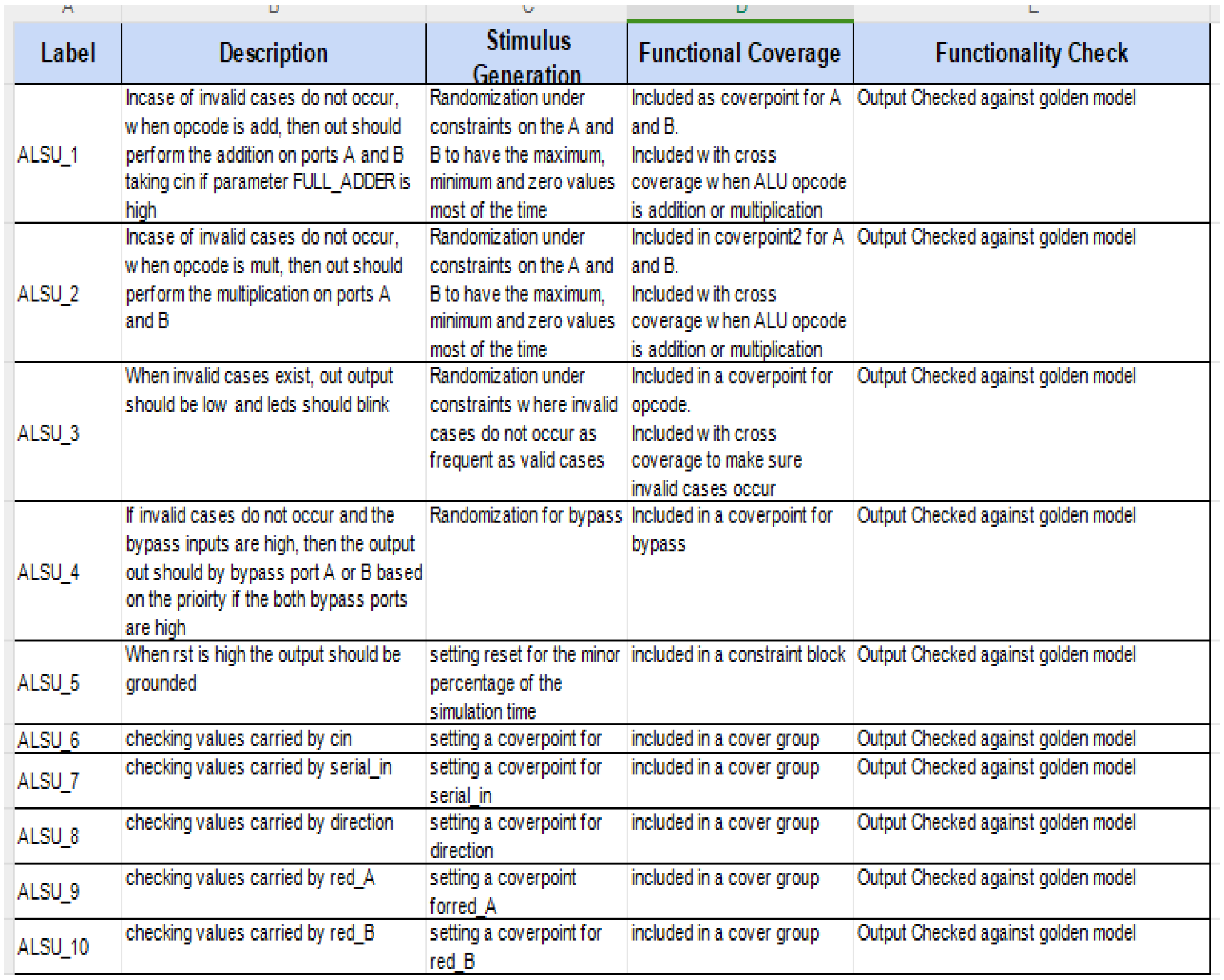
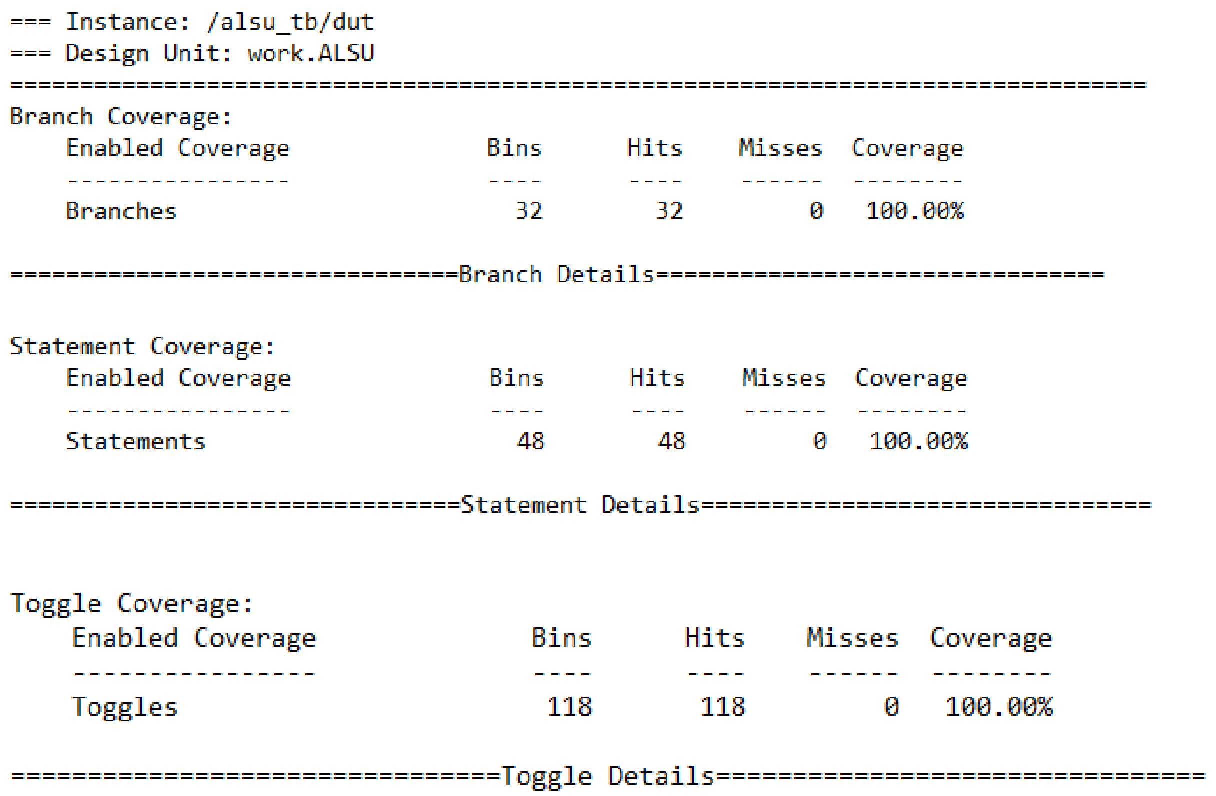
Verification Requirement Document



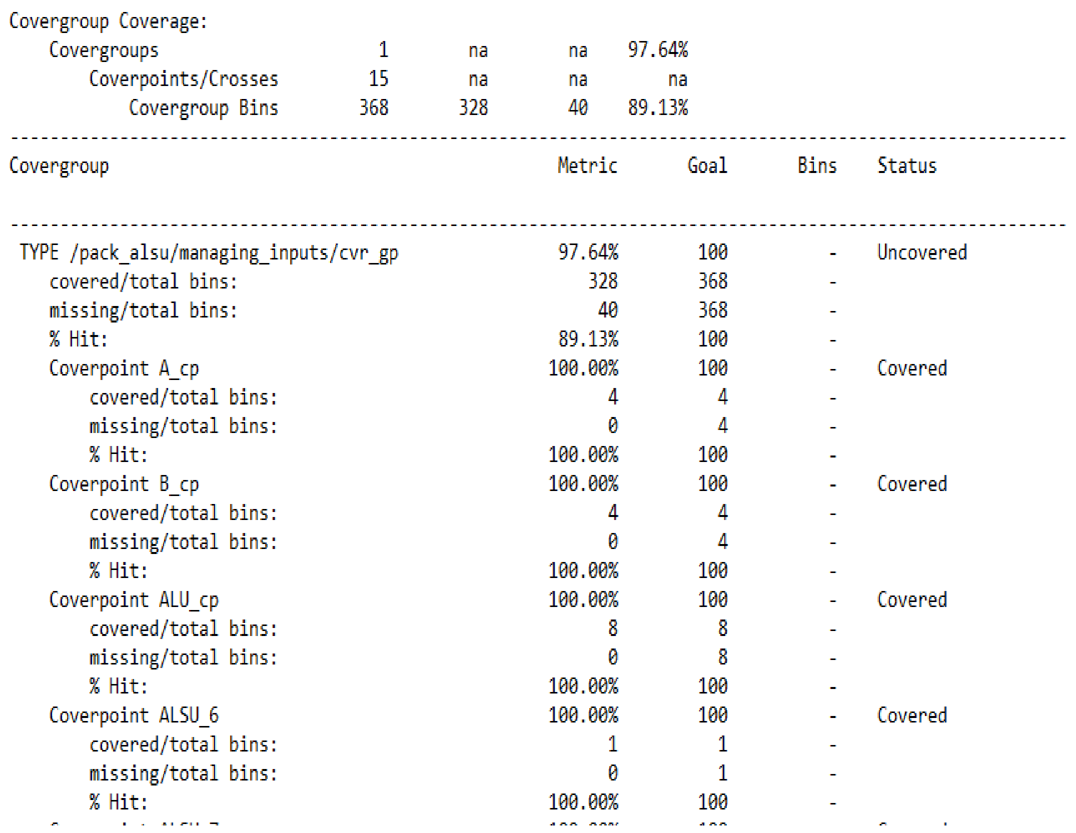
Label	Description	Stimulus Generation	Functional Coverage	Functionality Check
ALSU_1	Incase of invalid cases do not occur, w hen opcode is add, then out should perform the addition on ports A and B taking cin if parameter FULL_ADDER is high	Randomization under constraints on the A and B to have the maximum, minimum and zero values most of the time	Included as coverpoint for A and B. Included w ith cross coverage w hen ALU opcode is addition or multiplication	Output Checked against golden model
ALSU_2	Incase of invalid cases do not occur, w hen opcode is mult, then out should perform the multiplication on ports A and B	Randomization under constraints on the A and B to have the maximum, minimum and zero values most of the time	Included in coverpoint2 for A and B. Included w ith cross coverage w hen ALU opcode is addition or multiplication	Output Checked against golden model
ALSU_3	When invalid cases exist, out output should be low and leds should blink	Randomization under constraints w here invalid cases do not occur as frequent as valid cases	Included in a coverpoint for opcode. Included w ith cross coverage to make sure invalid cases occur	Output Checked against golden model
ALSU_4	If invalid cases do not occur and the bypass inputs are high, then the output out should by bypass port A or B based on the prioirty if the both bypass ports are high	Randomization for bypass	Included in a coverpoint for bypass	Output Checked against golden model
ALSU_5	When rst is high the output should be grounded	setting reset for the minor percentage of the simulation time	included in a constraint block	Output Checked against golden model
ALSU_6	checking values carried by cin	setting a coverpoint for	included in a cover group	Output Checked against golden model
ALSU_7	checking values carried by serial_in	setting a coverpoint for serial_in	included in a cover group	Output Checked against golden model
ALSU_8	checking values carried by direction	setting a coverpoint for direction	included in a cover group	Output Checked against golden model
ALSU_9	checking values carried by red_A	setting a coverpoint forred_A	included in a cover group	Output Checked against golden model
ALSU_10	checking values carried by red_B	setting a coverpoint for red_B	included in a cover group	Output Checked against golden model

Code and Functional Coverage



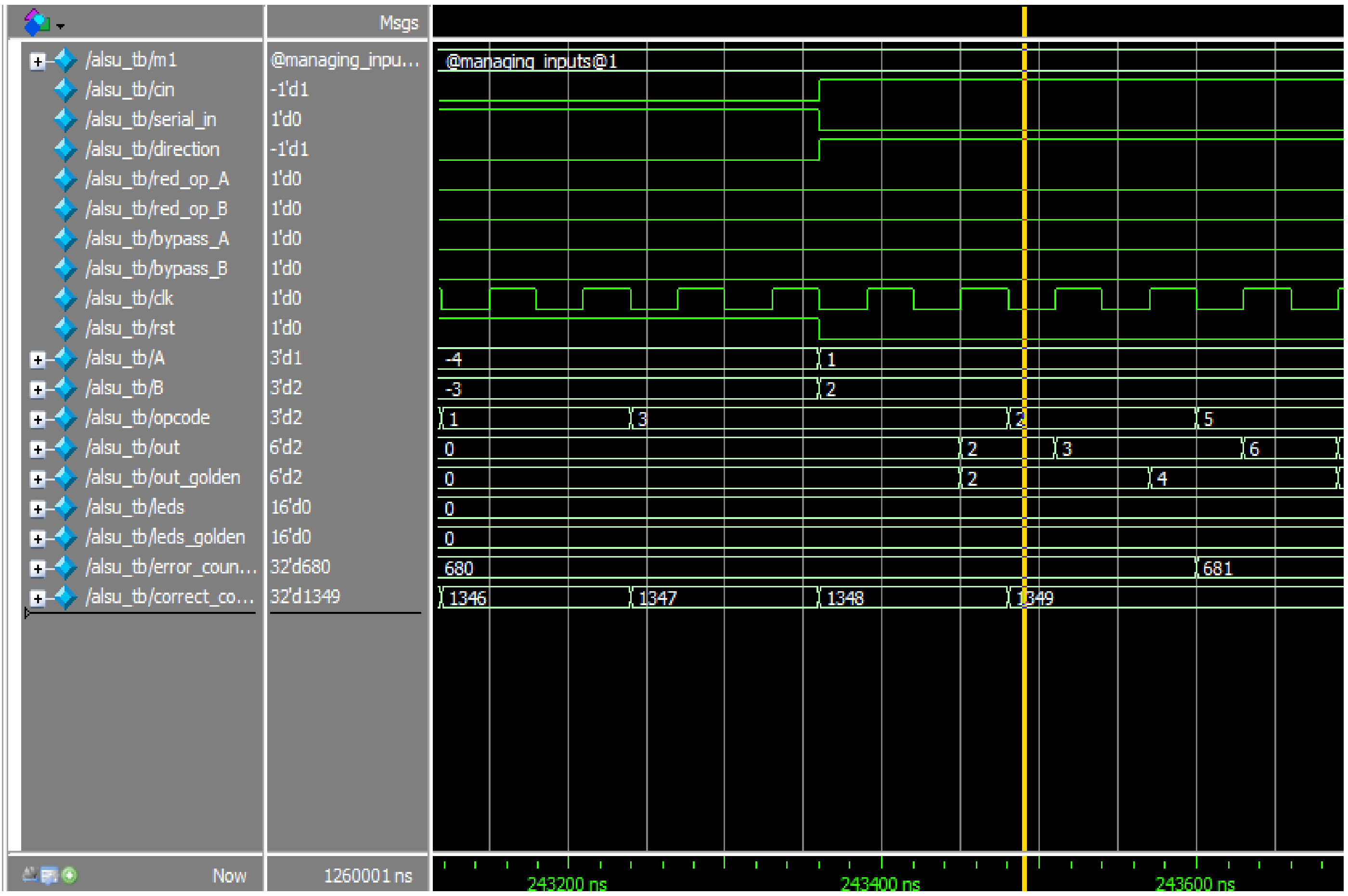
```
=== Instance: /alsu_tb/dut
=== Design Unit: work.ALSU
=====================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        32        32         0   100.00%

================================Branch Details================================

Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      48        48         0   100.00%

================================Statement Details================================


Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        118       118         0   100.00%

================================Toggle Details================================
```

I tried to reach 100% functional coverage but I couldn’t due to the auto generated bins, I tried to cancel this but it didn’t work. You can check the attached report in the same folder.

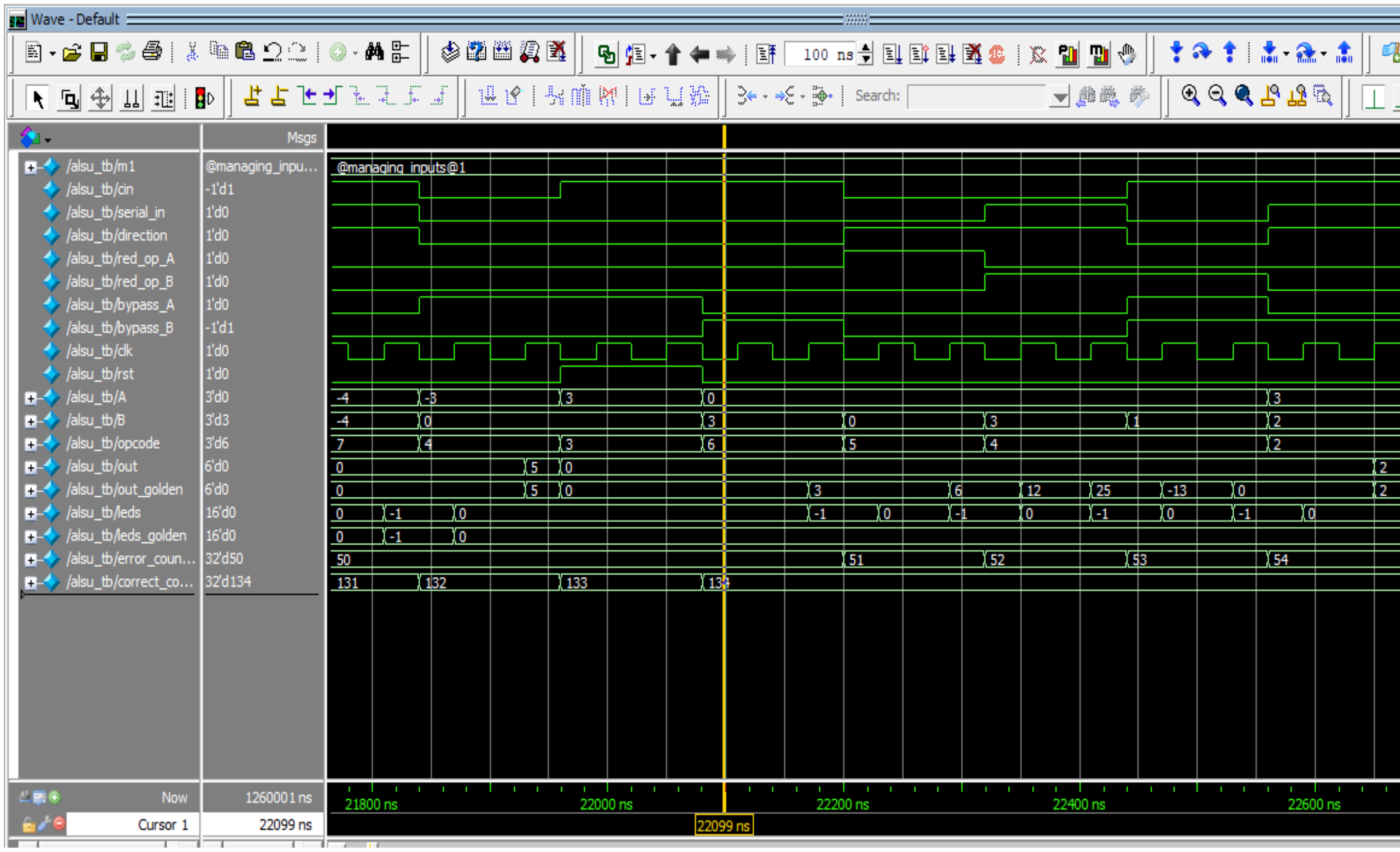


```
Covergroup Coverage:
    Covergroups                    1         na         na     97.64%
        Coverpoints/Crosses       15         na         na         na
            Covergroup Bins      368        328         40     89.13%
----------------------------------------------------------------------------------------------------------
Covergroup                                             Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------
 TYPE /pack_alsu/managing_inputs/cvr_gp                97.64%        100          -    Uncovered
    covered/total bins:                                   328        368          -
    missing/total bins:                                    40        368          -
    % Hit:                                             89.13%        100          -
    Coverpoint A_cp                                   100.00%        100          -    Covered
        covered/total bins:                                 4          4          -
        missing/total bins:                                 0          4          -
        % Hit:                                        100.00%        100          -
    Coverpoint B_cp                                   100.00%        100          -    Covered
        covered/total bins:                                 4          4          -
        missing/total bins:                                 0          4          -
        % Hit:                                        100.00%        100          -
    Coverpoint ALU_cp                                 100.00%        100          -    Covered
        covered/total bins:                                 8          8          -
        missing/total bins:                                 0          8          -
        % Hit:                                        100.00%        100          -
    Coverpoint ALSU_6                                 100.00%        100          -    Covered
        covered/total bins:                                 1          1          -
        missing/total bins:                                 0          1          -
        % Hit:                                        100.00%        100          -
```

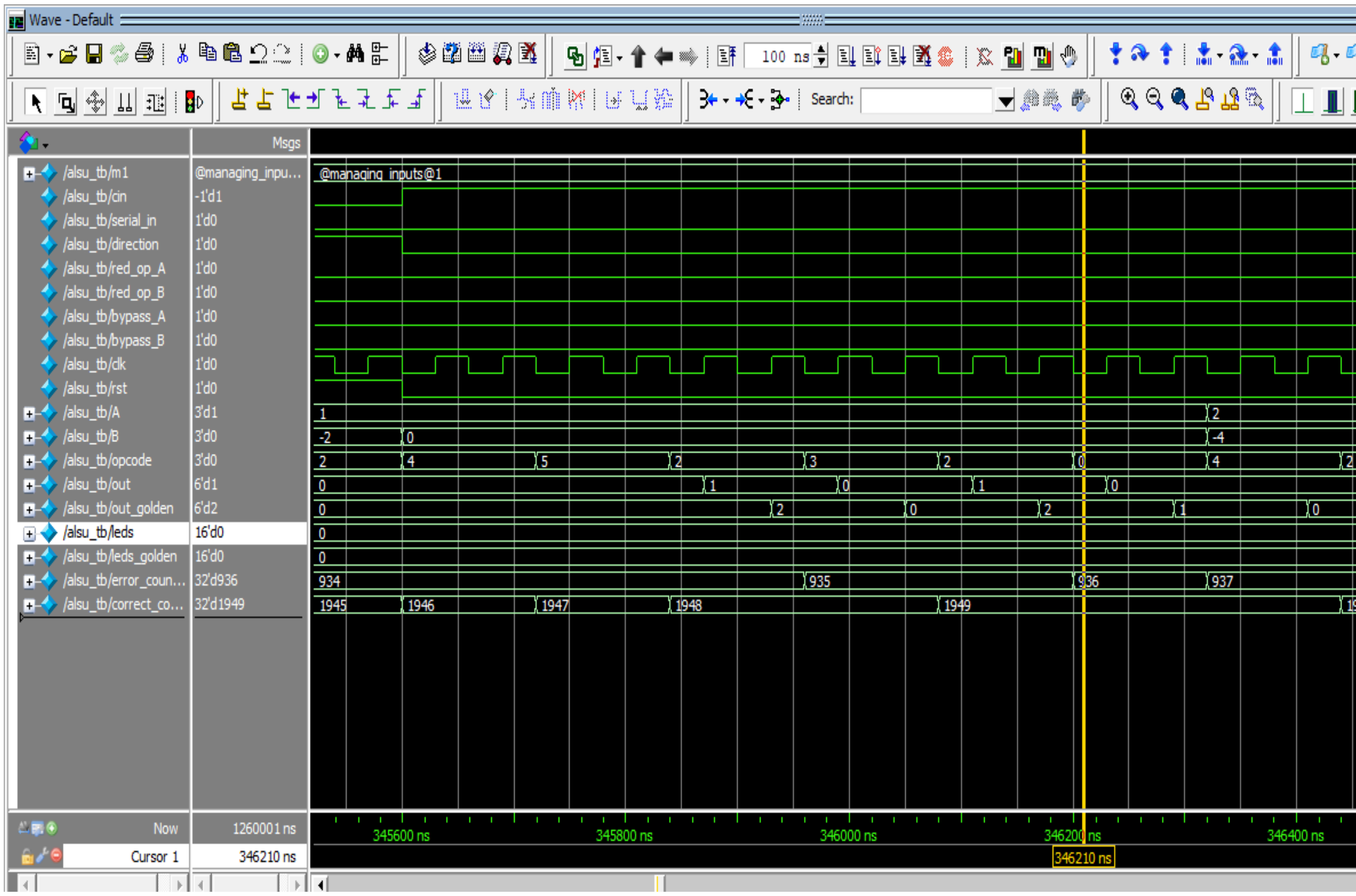
Wave form snippets showing the design bugs before correction



```
                                 Msgs
/alsu_tb/m1              @managing_inpu...
/alsu_tb/cin             -1'd1
/alsu_tb/serial_in       1'd0
/alsu_tb/direction       -1'd1
/alsu_tb/red_op_A        1'd0
/alsu_tb/red_op_B        1'd0
/alsu_tb/bypass_A        1'd0
/alsu_tb/bypass_B        1'd0
/alsu_tb/clk             1'd0
/alsu_tb/rst             1'd0
/alsu_tb/A               3'd1
/alsu_tb/B               3'd2
/alsu_tb/opcode          3'd2
/alsu_tb/out             6'd2
/alsu_tb/out_golden      6'd2
/alsu_tb/leds            16'd0
/alsu_tb/leds_golden     16'd0
/alsu_tb/error_coun...   32'd680
/alsu_tb/correct_co...   32'd1349

Now                      1260001 ns
```

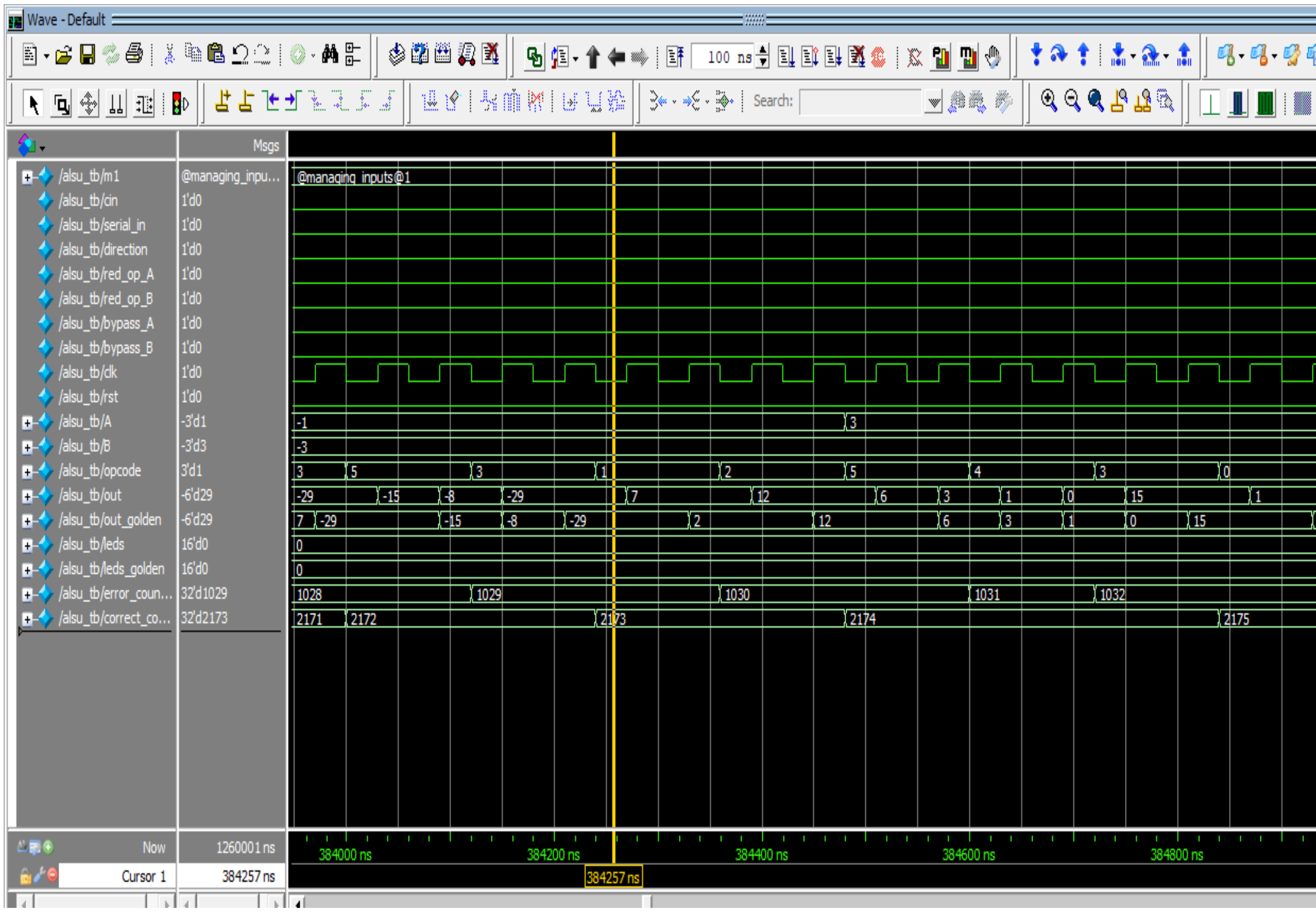


```
/alsu_tb/m1               @managing_inpu...
/alsu_tb/cin              -1'd1
/alsu_tb/serial_in        1'd0
/alsu_tb/direction        1'd0
/alsu_tb/red_op_A         1'd0
/alsu_tb/red_op_B         1'd0
/alsu_tb/bypass_A         1'd0
/alsu_tb/bypass_B         -1'd1
/alsu_tb/clk              1'd0
/alsu_tb/rst              1'd0
/alsu_tb/A                3'd0
/alsu_tb/B                3'd3
/alsu_tb/opcode           3'd6
/alsu_tb/out              6'd0
/alsu_tb/out_golden       6'd0
/alsu_tb/leds             16'd0
/alsu_tb/leds_golden      16'd0
/alsu_tb/error_coun...    32'd50
/alsu_tb/correct_co...    32'd134
Now                       1260001 ns
Cursor 1                  22099 ns
```



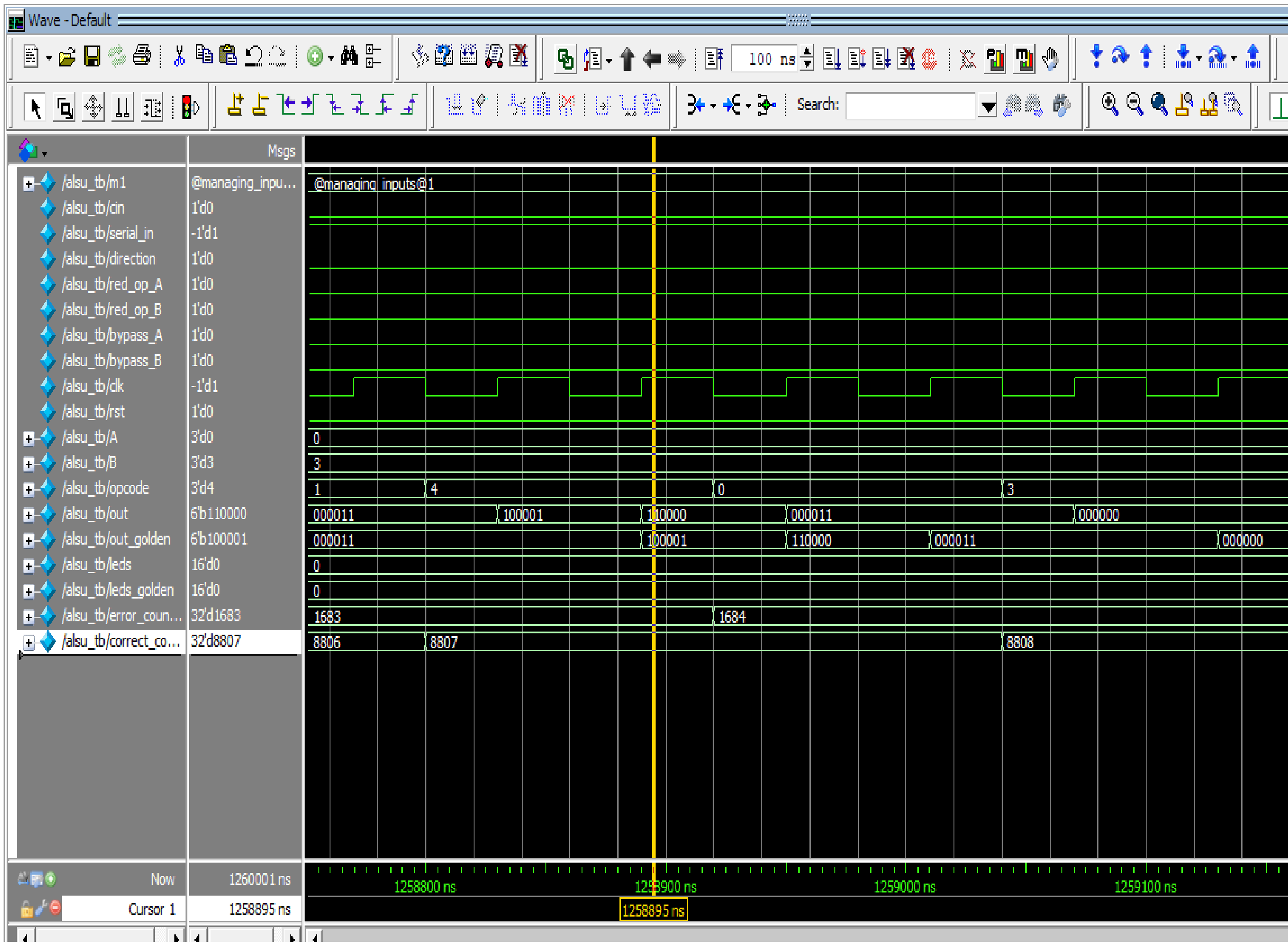
	Msgs
/alsu_tb/m1	@managing_inpu...
/alsu_tb/cin	-1'd1
/alsu_tb/serial_in	1'd0
/alsu_tb/direction	1'd0
/alsu_tb/red_op_A	1'd0
/alsu_tb/red_op_B	1'd0
/alsu_tb/bypass_A	1'd0
/alsu_tb/bypass_B	1'd0
/alsu_tb/clk	1'd0
/alsu_tb/rst	1'd0
/alsu_tb/A	3'd1
/alsu_tb/B	3'd0
/alsu_tb/opcode	3'd0
/alsu_tb/out	6'd1
/alsu_tb/out_golden	6'd2
/alsu_tb/leds	16'd0
/alsu_tb/leds_golden	16'd0
/alsu_tb/error_coun...	32'd936
/alsu_tb/correct_co...	32'd1949
Now	1260001 ns
Cursor 1	346210 ns

```
m1          @managing_inputs@1
A           1                                                        2
B           -2   0                                                   -4
opcode      2    4     5     2     3     2     0                     4      2
out         0                  1     0     1    0
out_golden  0                    2     0     2          1      0
leds        0
leds_golden 0
error_count 934                  935                936        937
correct_co  1945 1946  1947  1948        1949
```


Wave - Default

	Msgs
/alsu_tb/m1	@managing_inpu...
/alsu_tb/cin	1'd0
/alsu_tb/serial_in	1'd0
/alsu_tb/direction	1'd0
/alsu_tb/red_op_A	1'd0
/alsu_tb/red_op_B	1'd0
/alsu_tb/bypass_A	1'd0
/alsu_tb/bypass_B	1'd0
/alsu_tb/clk	1'd0
/alsu_tb/rst	1'd0
/alsu_tb/A	-3'd1
/alsu_tb/B	-3'd3
/alsu_tb/opcode	3'd1
/alsu_tb/out	-6'd29
/alsu_tb/out_golden	-6'd29
/alsu_tb/leds	16'd0
/alsu_tb/leds_golden	16'd0
/alsu_tb/error_coun...	32'd1029
/alsu_tb/correct_co...	32'd2173

```
Now       1260001 ns
Cursor 1  384257 ns
```



```
                       Msgs
/alsu_tb/m1            @managing_inpu...   @managing_inputs@1
/alsu_tb/cin           1'd0
/alsu_tb/serial_in     -1'd1
/alsu_tb/direction     1'd0
/alsu_tb/red_op_A      1'd0
/alsu_tb/red_op_B      1'd0
/alsu_tb/bypass_A      1'd0
/alsu_tb/bypass_B      1'd0
/alsu_tb/clk           -1'd1
/alsu_tb/rst           1'd0
/alsu_tb/A             3'd0        0
/alsu_tb/B             3'd3        3
/alsu_tb/opcode        3'd4        1        4                 0                  3
/alsu_tb/out           6'b110000   000011        100001   110000   000011              000000
/alsu_tb/out_golden    6'b100001   000011                 100001   110000   000011              000000
/alsu_tb/leds          16'd0       0
/alsu_tb/leds_golden   16'd0       0
/alsu_tb/error_coun... 32'd1683    1683                   1684
/alsu_tb/correct_co... 32'd8807    8806     8807                             8808

Now        1260001 ns     1258800 ns    1258900 ns    1259000 ns    1259100 ns
Cursor 1   1258895 ns                   1258895 ns
```