FPGA team Presents

Vivado Tutorial

Outline:

- Why do we need Vivado?
- HDL Files
- Custom and built-in IP blocks
- From block design to HDL again
- Elaboration and the schematic viewing
- Synthesis and IO planning
- What is constraints file (XDC) ?
- Implementation (PnR) and bitstream generation
- Design reports
- Verifying the design

Why do we need Vivado?

- **Working on FPGA projects based on Xilinix kits starting from placing the basic blocks till verifying the functionality of the whole project.**

HDL files

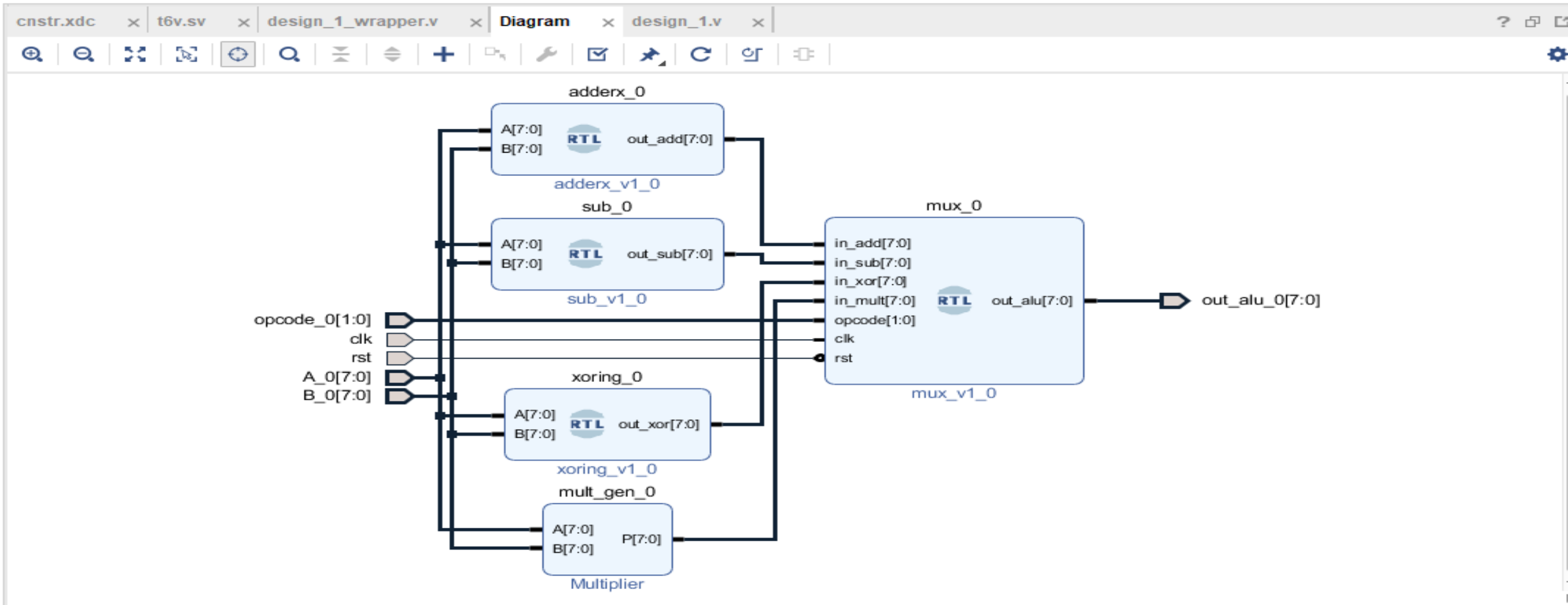
They are basically for describing how the module works but they became now essential in the design process and used for the creation of custom blocks.

multiplexer.v

```
1   module mux (in_add,in_sub,in_xor,in_mult,opcode,out_alu,clk,rst);
2   parameter INPUT_WIDTH=8;
3   parameter OPCODE_WIDTH=2;
4   input [INPUT_WIDTH-1:0] in_add,in_mult,in_sub,in_xor ;
5   input [OPCODE_WIDTH-1:0] opcode;
6   input clk,rst;
7   output [INPUT_WIDTH-1:0] out_alu;
8   reg [INPUT_WIDTH-1:0] out_alu_reg;
9   always @(negedge clk) begin
10      if(rst) begin
11          out_alu_reg<=0;
12      end
13      else begin
14          case (opcode)
15              2'b00 : out_alu_reg<=in_add;
16              2'b01 : out_alu_reg<=in_sub;
17              2'b10 : out_alu_reg<=in_xor;
18              2'b11 : out_alu_reg<=in_mult;
19          endcase
20      end
21  end
22  assign out_alu=out_alu_reg;
23  endmodule
```

Custom and built-in IP blocks

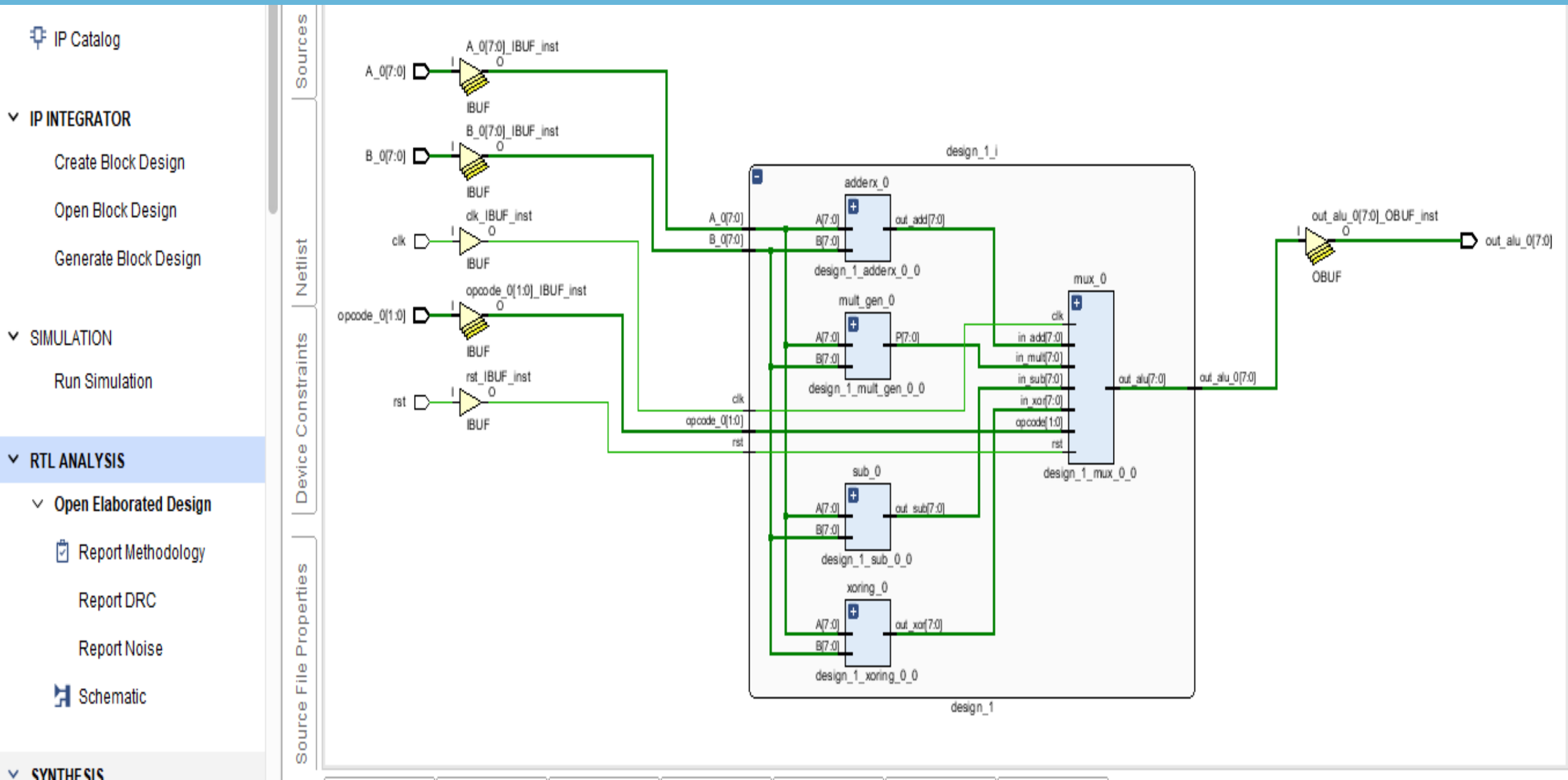
- Vivado supports either adding built-in IPs from the given list or adding blocks from your own design using the block design



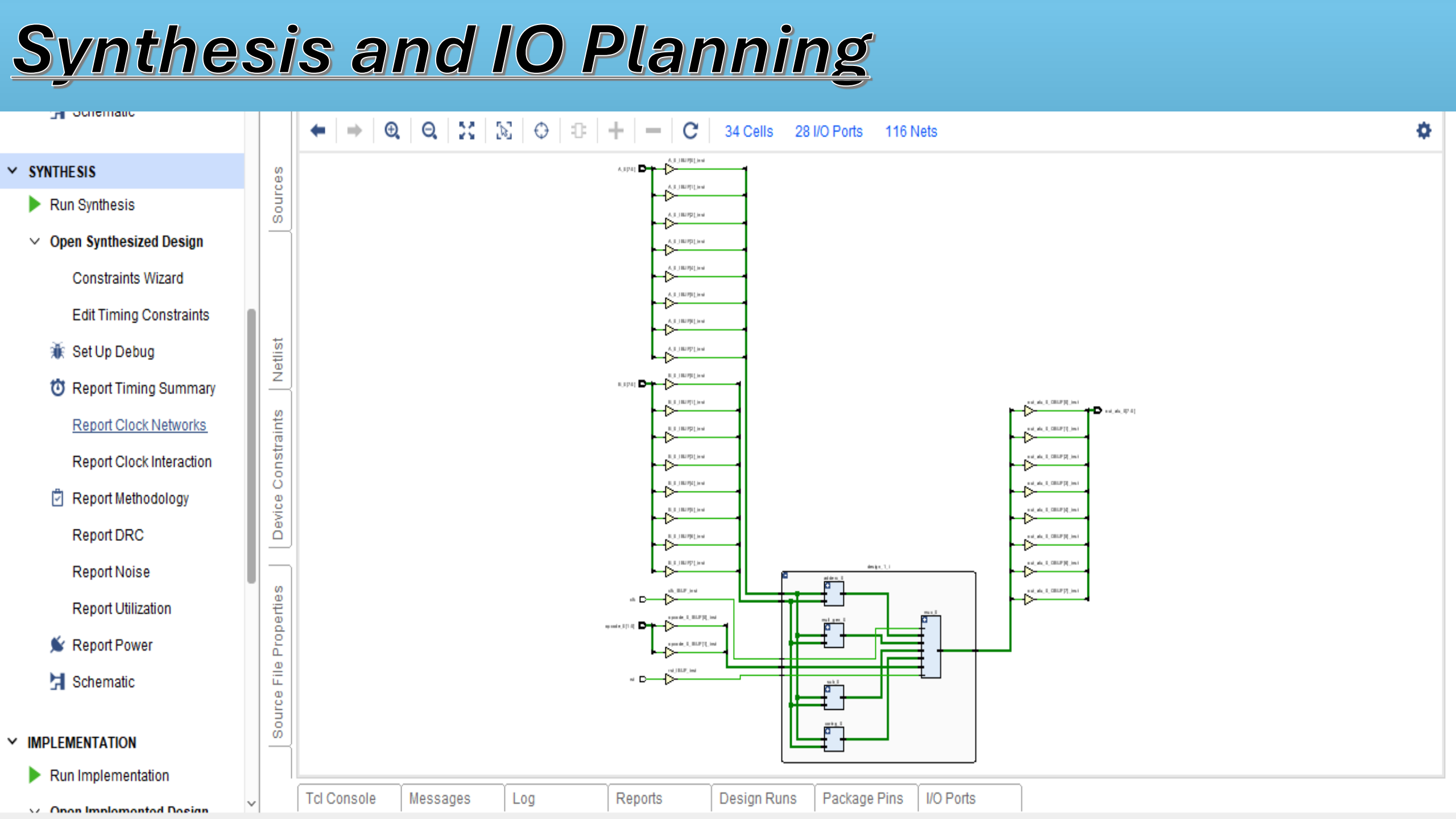
From block design to HDL again

- Convert your block design into reusable HDL code using create wrapper

Elaboration and the schematic viewing



Synthesis and IO Planning



Synthesis and IO Planning

SYNTHESIZED DESIGN - synth_1 | xc7vx485tffg1157-1 (active)

Tcl Console | Messages | Log | Reports | Design Runs | Package Pins | **I/O Ports**

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type
All ports (28)										
a_intf_21493 (8)	IN			✓	(Multiple)	LVCMOS18	1.800			
A_0 (8)	IN			✓	(Multiple)	LVCMOS18	1.800			
A_0[7]	IN		A16	✓	38	LVCMOS18	1.800			
A_0[6]	IN		A15	✓	38	LVCMOS18	1.800			
A_0[5]	IN		A14	✓	38	LVCMOS18	1.800			
A_0[4]	IN		A13	✓	38	LVCMOS18	1.800			
A_0[3]	IN		A11	✓	39	LVCMOS18	1.800			
A_0[2]	IN		A10	✓	39	LVCMOS18	1.800			
A_0[1]	IN		A9	✓	39	LVCMOS18	1.800			
A_0[0]	IN		A8	✓	39	LVCMOS18	1.800			
Scalar ports (0)										
b_intf_21493 (8)	IN			✓	(Multiple)	LVCMOS18	1.800			
CLK.CLK_54576 (1)	IN			✓	37	LVCMOS18	1.800			
RST.RST_54576 (1)	IN			✓	37	LVCMOS18	1.800			
opcode_0 (2)	IN			✓	34	LVCMOS18	1.800			
out_alu_0 (8)	OUT			✓	(Multiple)	LVCMOS18	1.800		12	SLOW
Scalar ports (0)										

What is constraints file (XDC)?

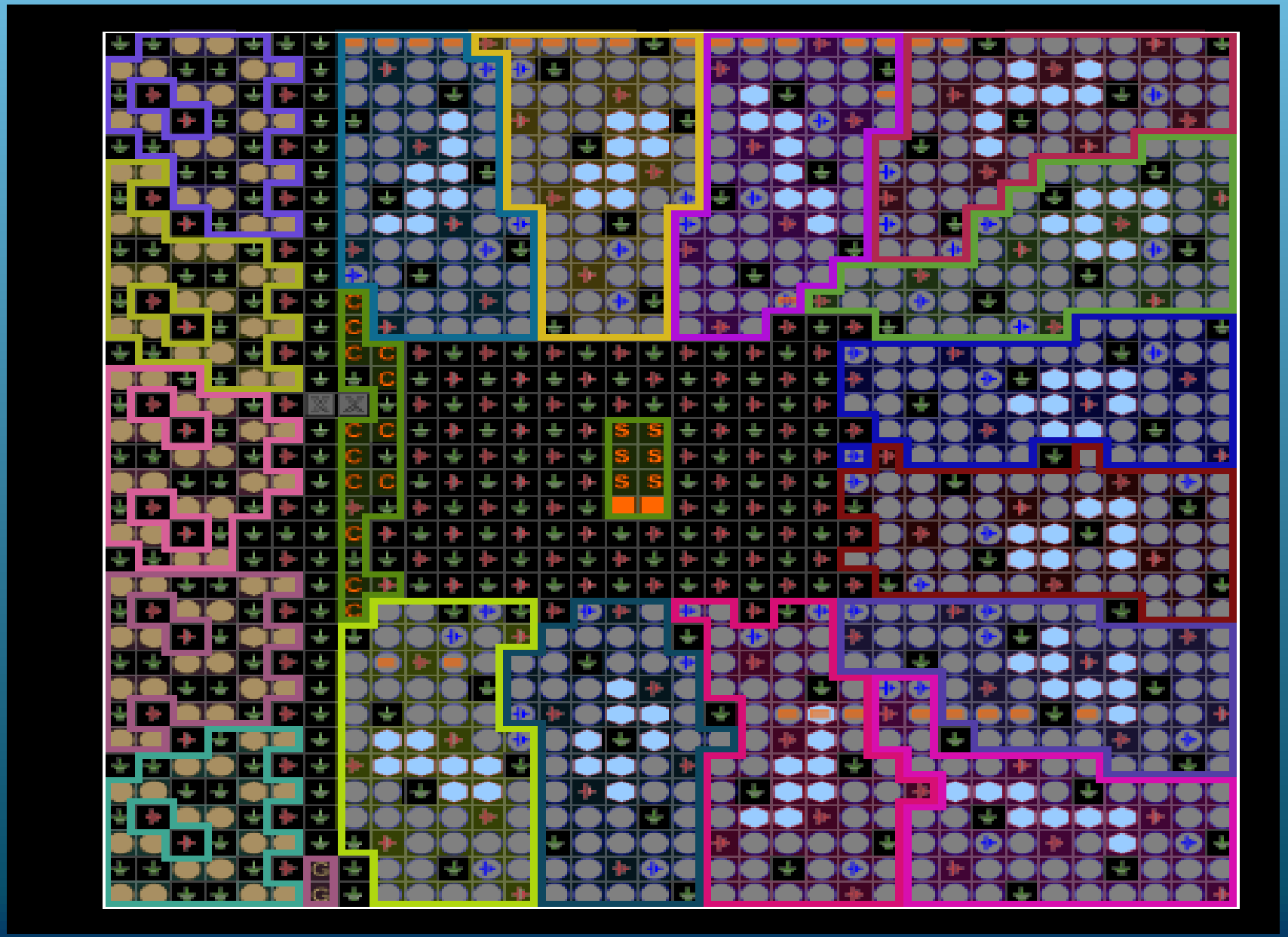
Sources | Netlist | Device Constraints | Source File Properties

Package | Device | cnstr.xdc | t6v.sv | design_1_wrapper.v | design_1.v | Schematic

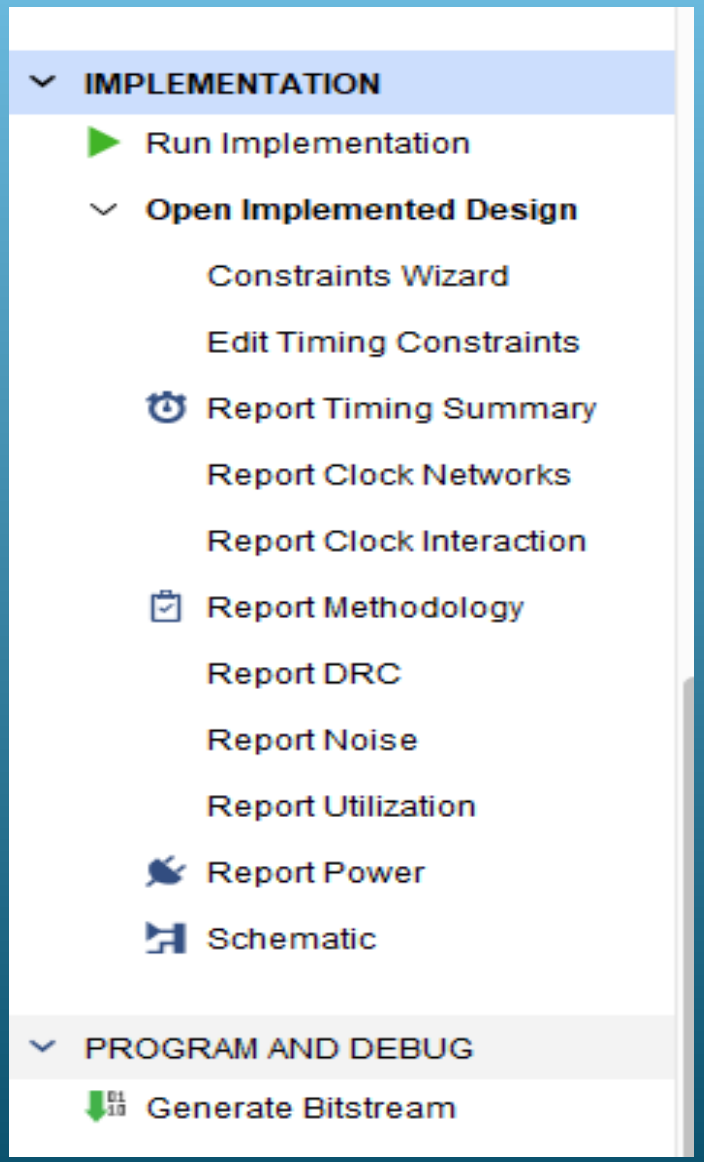
D:/Digital Electronics/Sonar/t6/project_3/project_3.srcs/constrs_1/new/cnstr.xdc

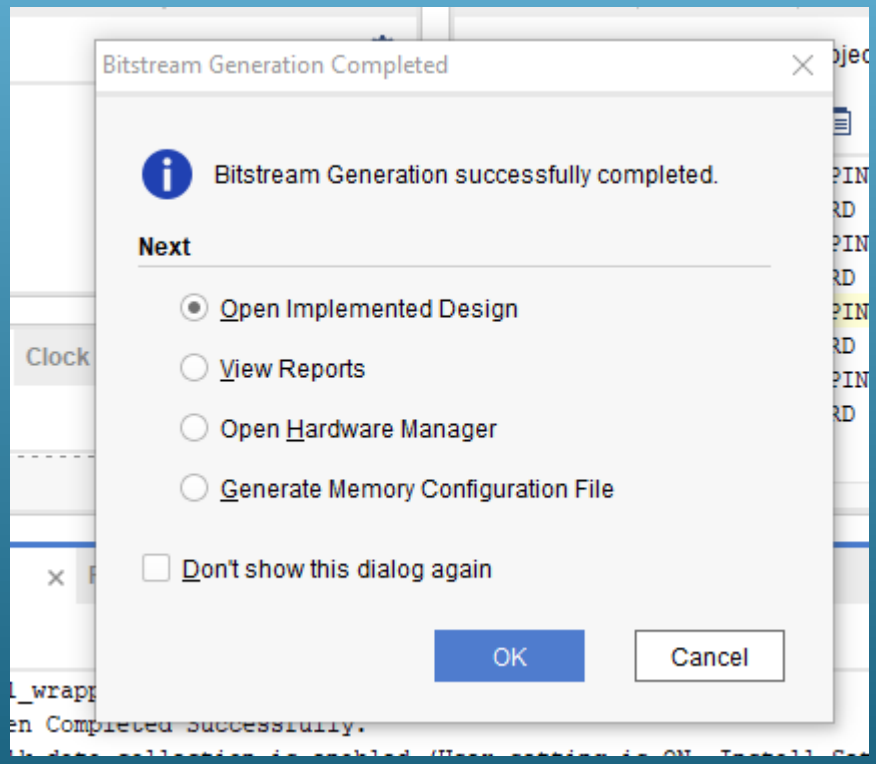
```
1  set_property PACKAGE_PIN A8 [get_ports {A_0[0]}]
2  set_property IOSTANDARD LVCMOS18 [get_ports {A_0[0]}]
3  set_property PACKAGE_PIN A9 [get_ports {A_0[1]}]
4  set_property IOSTANDARD LVCMOS18 [get_ports {A_0[1]}]
5  set_property PACKAGE_PIN A10 [get_ports {A_0[2]}]
6  set_property IOSTANDARD LVCMOS18 [get_ports {A_0[2]}]
7  set_property PACKAGE_PIN A11 [get_ports {A_0[3]}]
8  set_property IOSTANDARD LVCMOS18 [get_ports {A_0[3]}]
9  set_property PACKAGE_PIN A13 [get_ports {A_0[4]}]
10 set_property IOSTANDARD LVCMOS18 [get_ports {A_0[4]}]
11 set_property PACKAGE_PIN A14 [get_ports {A_0[5]}]
12 set_property IOSTANDARD LVCMOS18 [get_ports {A_0[5]}]
13 set_property PACKAGE_PIN A15 [get_ports {A_0[6]}]
14 set_property IOSTANDARD LVCMOS18 [get_ports {A_0[6]}]
15 set_property PACKAGE_PIN A16 [get_ports {A_0[7]}]
16 set_property IOSTANDARD LVCMOS18 [get_ports {A_0[7]}]
17 set_property PACKAGE_PIN A18 [get_ports {B_0[0]}]
18 set_property IOSTANDARD LVCMOS18 [get_ports {B_0[0]}]
19 set_property PACKAGE_PIN A19 [get_ports {B_0[1]}]
20 set_property IOSTANDARD LVCMOS18 [get_ports {B_0[1]}]
21 set_property PACKAGE_PIN A20 [get_ports {B_0[2]}]
22 set_property IOSTANDARD LVCMOS18 [get_ports {B_0[2]}]
23 set_property PACKAGE_PIN A21 [get_ports {B_0[3]}]
24 set_property IOSTANDARD LVCMOS18 [get_ports {B_0[3]}]
25 set_property PACKAGE_PIN A23 [get_ports {B_0[4]}]
26 set_property IOSTANDARD LVCMOS18 [get ports {B_0[4]}]
```

Implementation (PnR) and bitstream generation

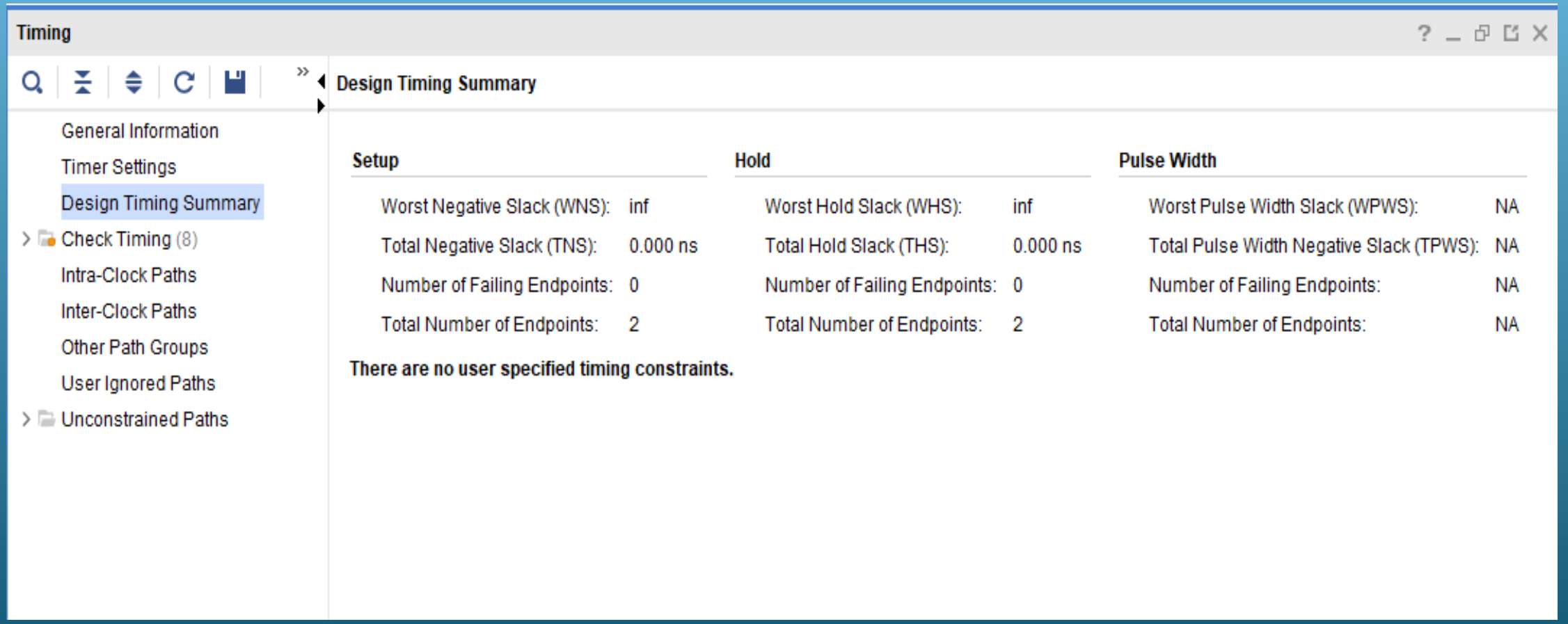


Implementation (PnR) and bitstream generation

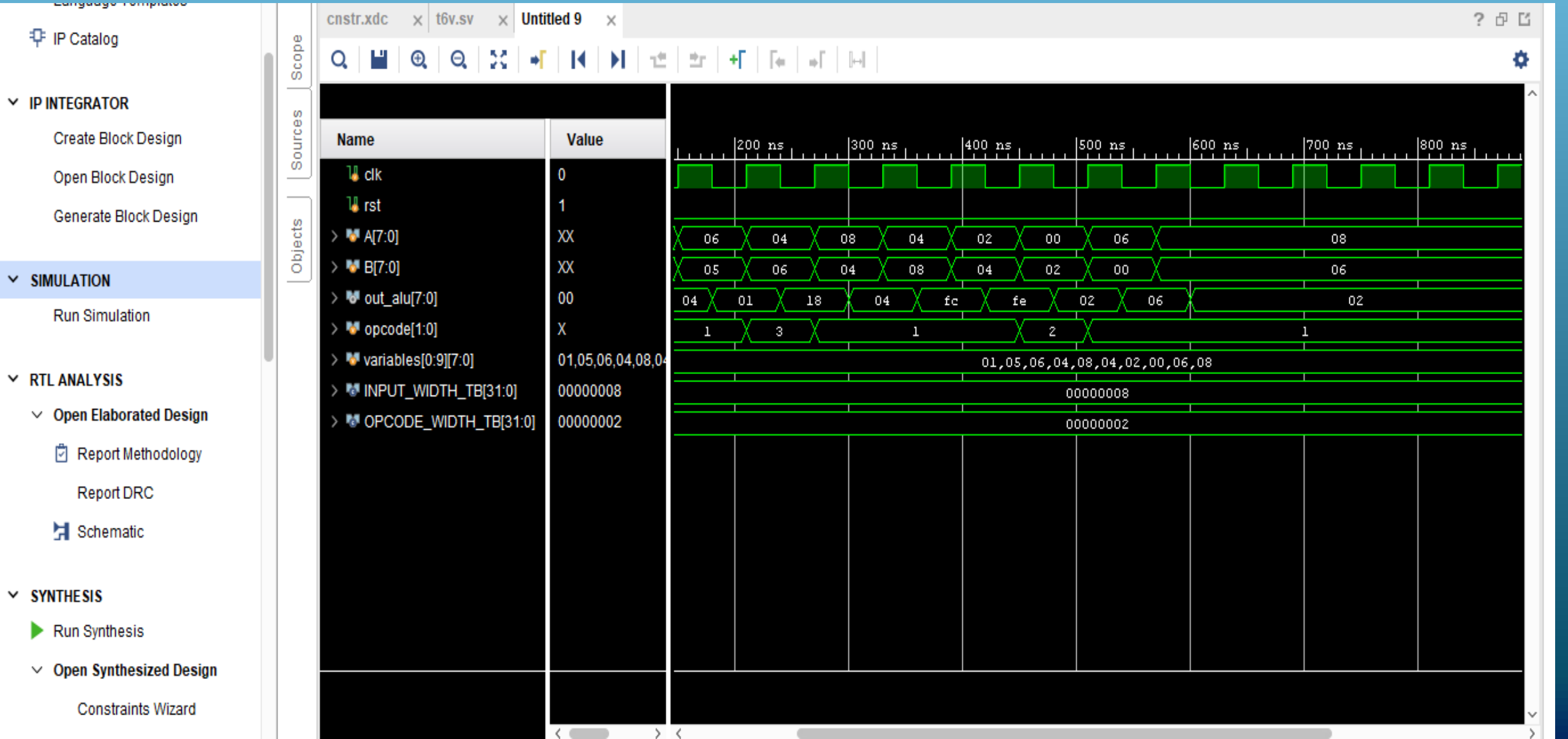




Design Reports



Verifying the design



Thank You