Instruction Register

Table 1

2-bits for mode	6-bits for opcode	8-bits for destination	8-bits for source 2	8-bits for source 1

Address Mode Table

Table 2

Mode Bits	Mode
00	Register Mode
01	Direct Mode for source 1
10	Indirect mode for source 1
11	Immediate value for source 1

Opcode To Instruction Table

Table 3

Opcode in Binary	Instruction
000000	ADD
000001	SUB
010000	INC source 1
010001	DEC source 1
100000	AND
100001	OR
100010	XOR
010010	INV source 1
001000	SHR
001001	SHL
001010	ROR
001011	ROL
010101	Load M [source1]=>source2
101010	Store M [source1]<=source2
110011	Incr PC by the value in source 1

Control Word

Opcode 6-bits	Pc-src (either incr by 1 for selpc=0 or source1 for selpc=1) 1 bit	Sel R1 5-bits	Sel R2 5-bits	Loaded R 5-bits	Read 1-bit	Write 1-bit	M Address 8-bits

Instruction Set Table

Instr.	Opcode	Mode	Microoperation	Control Word
ADD	000000	00 01 10 11	T2:R3<-R2+R1 T2:R3<-R2+M [R1] T2:R4<-M [R1] , T3:R3<-R2+M [R4] T2:R3<-R2+ Instr [15:8]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
SUB	000001	00 01 10 11	T2:R3<-R2-R1 T2:R3<-R2-M [R1] T2:R4<-M [R1] , T3:R3<-R2-M [R4] T2:R3<-R2- Instr [15:8]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
INC source 1	010000	00 01 10 11	 For all T2:R1<-R1+1	 For all 01 00 01 x x x
DEC source 1	010001	00 01 10 11	 For all T2:R1<-R1-1	For all 01 00 01 x x x
AND	100000	00 01 10 11	T2:R3<-R2&R1 T2:R3<-R2&M [R1] T2:R4<-M [R1] , T3:R3<-R2&M [R4] T2:R3<-R2&Instr [15:8]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
OR	100001	00 01 10 11	T2:R3<-R2|R1 T2:R3<-R2|M [R1] T2:R4<-M [R1] , T3:R3<-R2|M [R4] T2:R3<-R2| Instr [15:8]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
XOR	100010	00 01 10 11	T2:R3<-R2^R1 T2:R3<-R2^M [R1] T2:R4<-M [R1] , T3:R3<-R2^M [R4] T2:R3<-R2^ Instr [15:8]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
INV source 1	010010	00 01 10 11	For all T2:R1<-!R1	For all 01 xx 01 x x x

SHR	001000	00 01 10 11	T2:R3<-R2[0],R1[7:1] T2:R3<-M[R1][0],R1[7:1] T2:R4<-M[R1] T3:R3<-M[R4][0],R2[7:1] T2:R3<-Instr[0],R1[15:8]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
SHL	001001	00 01 10 11	T2:R3<-R1[6:0],R2[0] T2:R3<-R1[6:0],M[R1][0] T2:R4<-M[R1] T3:R3<-R2[6:0],M[R4][0] T2:R1[6:0],Instr[0]	01 10 11 x x x `d32 10 11 1 0 01 xx xx 100 1 0 01 `d32 10 11 1 0 100 `d33 10 11 x x x
ROR	001010	00 01 10 11	For all T2:R1<-R1[0],R1[7:1]	01 xx 01 x x x
ROL	001011	00 01 10 11	For all T2:R1[6:0],R1[7]	01 xx 01 x x x
Load M [source1]=>source2	010101	xx	T2:R2<-M[R1]	xx xx 10 1 0 01
Store M [source1]<=source2	101010	xx	T2:M[R1]<-R2	10 xx xx 0 1 01
Incr PC by source 1	110011	xx	T2:PC<-PC+R1	1 01 xx xx x x x

Processor Architecture Schematic