

VLSI Project – Phase 2

Group 4

Team 13 - CNN Module

Team Members:

Omar Mohammad	Sec. 2	B.N. 09
Mohammad Emad	Sec. 2	B.N. 21
Walid Mohammad	Sec. 2	B.N. 30
Yahia Ali	Sec. 2	B.N. 32

Finite State Machine states:

- Cond1: only in the first time. At CNN start, we load number of layers to process and assume it is not more than three Layers and set the image pointer and the new image pointer (pointer to where write the image).
- Cond2: Load the layer data (as shown in Phase 1 delivery) including number of filters,in depth, out depth, filter size,etc....
- Cond3: load new rows if needed to process.
- Cond4: load filter if needed
- Cond5: calculate the result of convolution and pooling.
- Cond6: add the new pixel result to the row to be stored later in the RAM.
- Cond7_sub: save the new row in the RAM when it's done.
- Cond8: reset any signal needed to to start over and decide which state the program will return to.

Project file tree:

Control unit (Control_unit.vhd): this file contains the whole logic and FSM states implementation. The file uses the following entities:

- a. Counter.vhd: contains an 8-bit counter used in state_counter (which controls the states of the FSM), filters_covered_counter, rows_covered_counter
- b. Counter_ptrs: contains a custom 16-bit counter.
- c. Counter_filters.vhd: contains a custom counter used to track the filters address and layers data addresses.
- d. Xor_1bit_out.vhd: in order to avoid using "PROCESS" a lot; this file contain an entity that returns '1' when the two inputs are equal and '0' otherwise.
- e. Window_selection_logic.vhd: select the window to process from the row currently held in the registers.
- f. bias_selection_logic.vhd: selects the correct bias for convolution .
- g. Add_new_row_logic.vhd: adds the CNN result to new_row to be stored later.
- h. Swap_algorithm.vhd: swap image pointer to the new value every layer.
- i. Mux_5x1.vhd
- j. Mux_3x1.vhd
- k. Tristate.vhd: contains a regular tri-state buffer.
- l. CNN_pyramid: this module is responsible for making the calculations including multiplication, addition and any operations in the convolution/pooling process.

Modules(Entities) description:

1. CNN_pyramid:

Input	Output
CLK	Result (the operation output)
Conv/Pool (type of operation)	
Five (1 bit state the window size 5 or 3)	
Bias (zero in case of pooling)	
Filter (if exists)	
Window of pixels	

2. Window_selection_logic: in case window size is 3x3, the last two rows in the window and the most significant two pixels are set to zero.

Input	Output
CLK	The window to process in the next stage of the FSM
Window_en (enable the operation)	
Five rows of the image	
Size of the window	
Window of pixels	

3. xor_1bit_out:

Input	Output
Variable 1	F (1 if they are equal else 0)
Variable 2	

4. bias_selection_logic:

Input	Output
CLK	Bias (the bias to use in the calculations with this filter)
bias_en (enable every time we use new filter)	
Biases (200 bit long signal contain the layer biases values)	

5. add_new_row_logic:

Input	Output
CLK	new_row (with the result added to it)
Enable(allow to write the result in the row)	
Reset(clear the row)	
Result (the value to store)	
Row_is_done (signal indicate is row is full and ready to be stored)	
out_size(to know when the row is done)	

6. Mux_3x1:

Input	Output
SEL1 (1 bit)	F (selected input)
SEL 2 (1 bit)	
A (selection input)	
B (selection input)	
C (selection input)	

7. Mux_5x1:

Input	Output
SEL	F (selected input)
filter_size	
A (selection input)	
B (selection input)	
C (selection input)	
D (selection input)	
E (selection input)	

8. **Swap_algorithm**: to optimize ram size we set only two addresses to use in the CNN module. We first use address1 and write in address2, and then, in the following layer, we use address2 and write in address1, and so on.

Input	Output
Enable	New_image pointer (the start address of the image)
Image pointer 1 address	
Image pointer 2 address	
Current image pointer address	
New image pointer address	

9. Remaining modules are just counters used in controlling the flow of the system including:

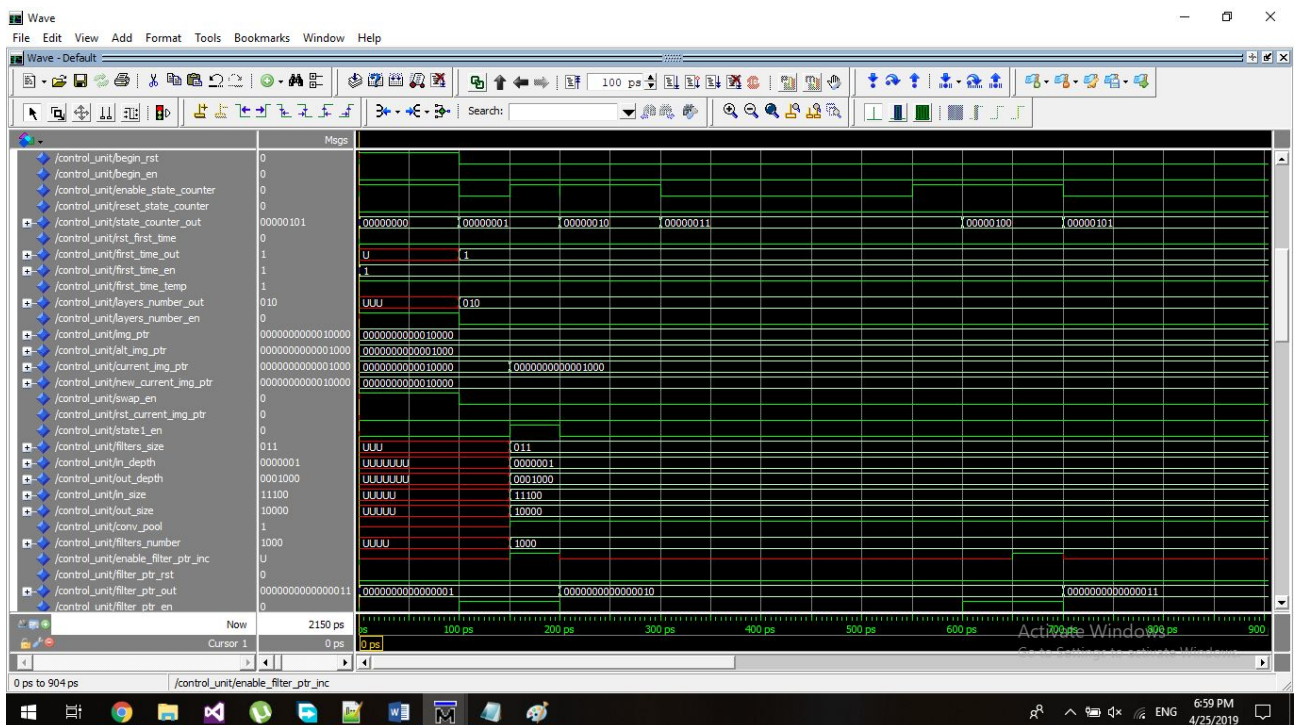
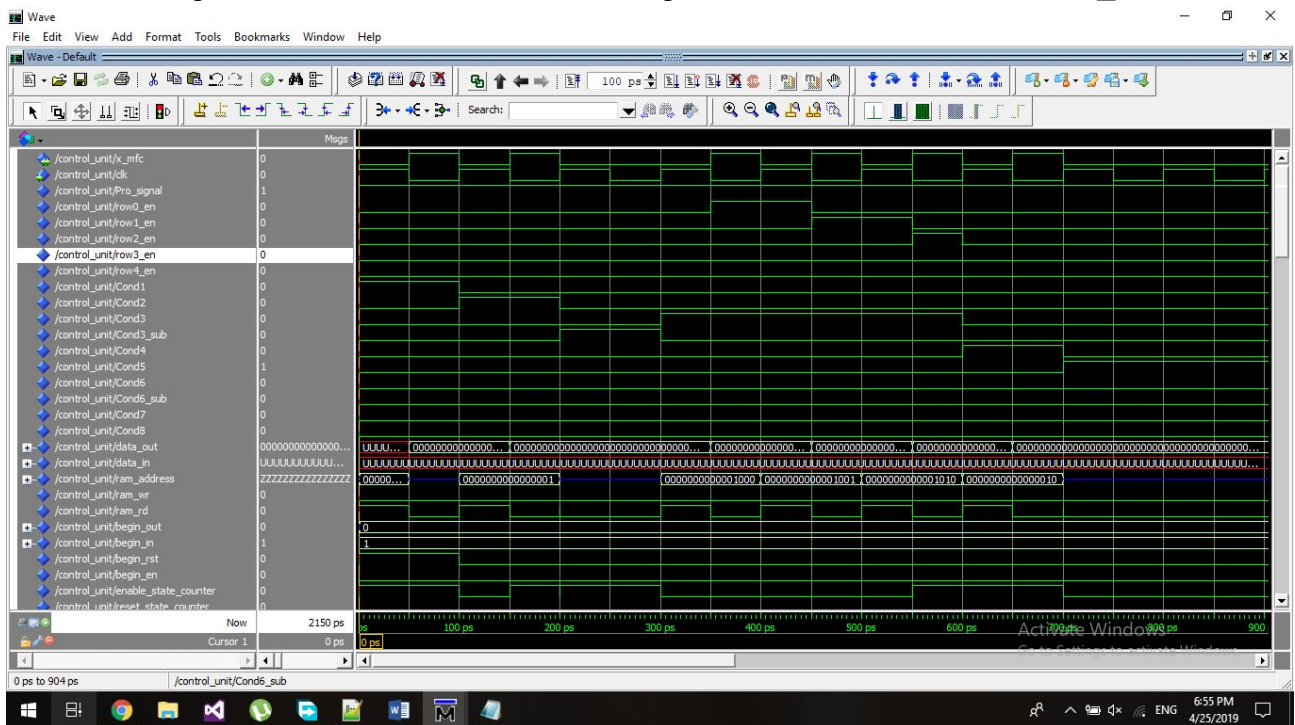
- Counter
- Counter_ptr
- Counter_filters
- State_counter

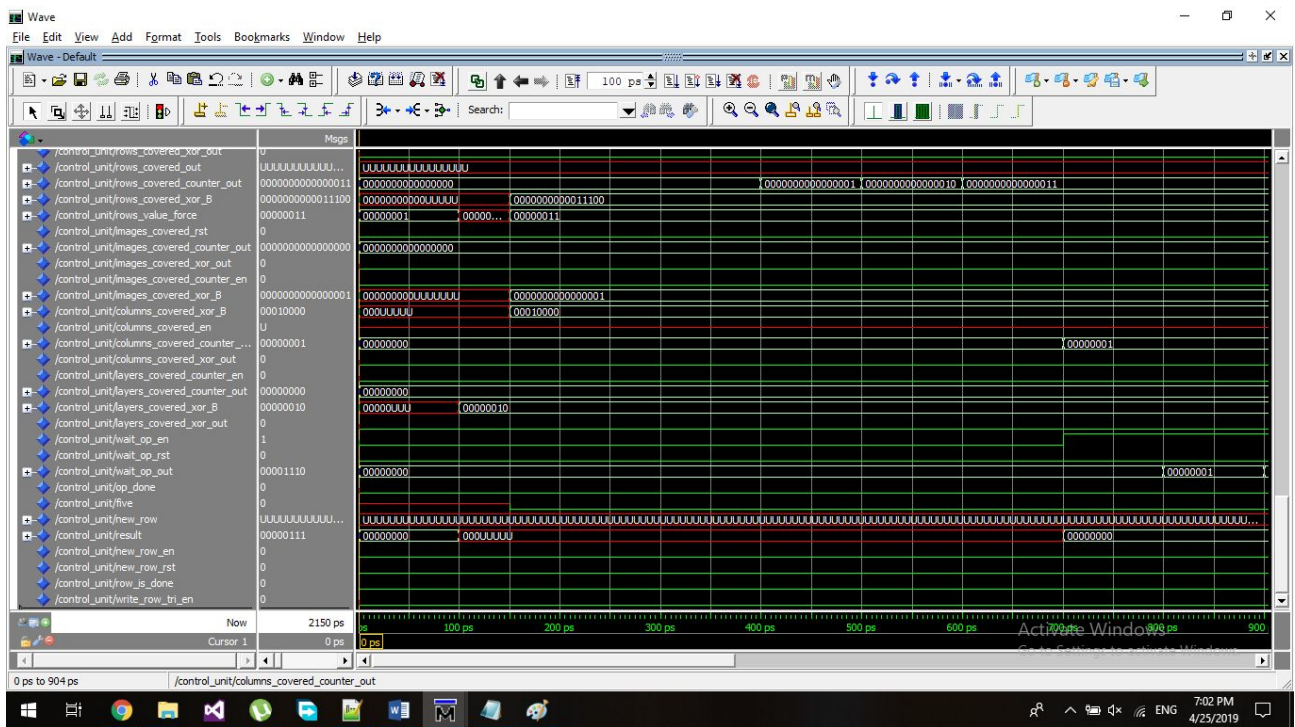
10. We use 42 modules in total, but only these modules are ours. The rest is booth multiplication logic which is **done by the FC team** and duplicate common files like adders between the two teams.

IO description:

CLK	GLOBAL
Pro_signal	Signal to start (from the previous module)
RST	Reset the system signal (Global)
FC_start	Signal for FC module to start

Time Diagram (of control unit): this is the diagram of the Control unit but it is too big, so, we attached the do file that generate it under the name “cu_do.txt”





Design flow reports:

We still have problems in the control unit synthesized file, the output file is missing a lot of things and it's not working and we're still fixing it. The following numbers reflect this. But all the other modules have synthesized successfully.

data required time	20.00
data arrival time / slack	10.99 / 9.01
Number of gates	11242
Clock Cycle Duration	20ns