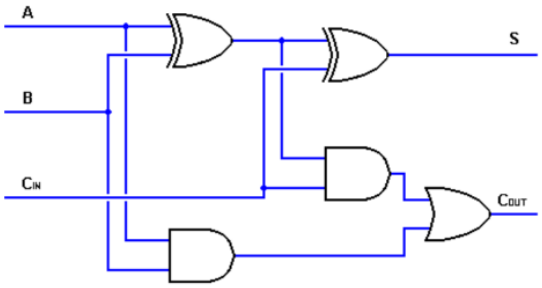
**EE496 Computer Architecture and VHDL**

Assignment 1: Adder/Subtractor
Due date: 31 October 2018 (week 6)
(10% weighting of the final module mark)

1. One-bit full adder (FA)




One-bit full adder circuit

1.1 Write a VHDL model for a one-bit full adder

[10 marks]

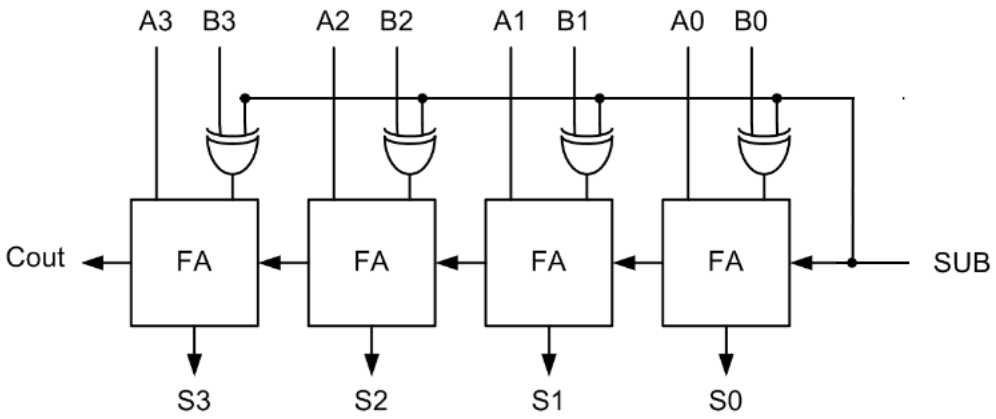
1.2 Write a test bench for the one-bit full adder

[5 marks]

1.3 Present the simulation results of the one-bit full adder using the test bench

[5 marks]

2. 4-bit adder/substractor




4-bit adder (when sub=0) and substractor (when sub = '1') circuit

2.1 Use the 4-bit adder as component to build a 4-bit adder/substractor (hint: A minus B equals A plus the two's complement of B, i.e. A – B = A + (invert of B) + 1). What's the range of numbers that can be represented by a 4-bit two's complement number?

[15 marks]

2.2 Write a test bench for the 4-bit adder/substractor.

[9 marks]

2.3 Present the simulation results of the 4-bit adder/substractor using the test bench.

[9 marks]

3. The 4-bit adder/substractor designed in part 2 above can be used to add or substract unsigned numbers or two's complement numbers. Extend the 4-bit adder/substractor with the following flags.

   3.1 *Negative flag (**N**),* which indicates the result is negative (i.e. most significant bit is 1).
   [4 marks]

   3.2 *A zero flag (**Z**)*, which indicates that the result is 0 (i.e. all bits of the result are 0).
   [4 marks]

   3.3 *Carry Flag (**C**),* which indicates the adder/subtractor produced a carry, i.e. overflow in unsigned arithmetic. It is also used for propagating the carry between words in multiple-precision arithmetic.
   [4 marks]

   3.4 *Overflow flag (**V**)*, which indicates that the result of the addition or subtraction of two two's complement numbers overflowed (i.e. outside the range of numbers that can be represented using a 4-bit two's complement number, i.e. outside the range of -8 to 7 in this case).
   [8 marks]

   3.5 Write a test bench for the 4-bit adder/substractor extended with output flags
   [9 marks]

   3.6 Present the simulation results of the test bench to show that the added flags work as expected.
   [9 marks]

## What to Turn In

Please submit your lab report to the loop page of the course. Be sure to label each section and organize them in the following order. Messy or disorganized labs will lose points.
1. Please indicate how many hours you spent on this lab. This will be helpful for calibrating the workload for next time the course is taught.

2. Write a few sentences describing the purpose of this lab.

3. Did your full adder pass tests for all eight possible inputs?

4. How did you test your 4-bit adder/subtractor?

If you have suggestions for further improvements of this lab, you're welcome to include them at the end of your lab.

Documentation and presentation [9 marks]

Reference:

[1] https://www.quora.com/How-can-a-full-adder-be-converted-to-a-full-subtractor-with-the-addition-of-one-inverter-circuit

**[End of Assignment 1]**

## Assignment 1 marking scheme

| 1.1 One bit adder VHDL code | 1.2 One bit adder testbench | 1.3 One bit adder simulation | 2.1 4-bit adder/ Subtractor | 2.2 4-bit adder/ subtractor testbench | 2.3 4-bit adder/ subtractor simulation | 3.1 Negative flag | 3.2 Zero flag | 3,3 Carry flag | 3.4 Overflow flag | 3.5 Testbench | 3.6 Simulation | Documentation and presentation | Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 5 | 5 | 15 | 9 | 9 | 4 | 4 | 4 | 8 | 9 | 9 | 9 | 100 |