Jahangirnagar University

Institute of Information Technology

2nd Year 1st Semester B.Sc. (Honors) Final Examination-2020

Course No. # ICT 2103
Course Title# Digital logic Design

Examination Roll No. #	192340
Registration No. #	2019365028 3
Academic Session #	2018 - 2019

Total no of written pages in the script # 3

Exam Date: 16, Aug **, 2021**

Instructions:

1. Examinee must write his/her exam roll no. and page no. at the top of every page of the script.
2. Do not write your name or any identification mark anywhere of the script.
3. Total time for exam is 45 minutes. You will get 15 additional minutes for submission.
4. Delay in submission is not acceptable.
5. You have to submit your exam script in PDF format.
6. The examinee must submit the examination script **through online (Google classroom/email/google form etc.)** as prescribed by the examiner.
7. You must use **your EXAM ID** only for naming your submitted file.
8. After completing the exam, you must write the total number of pages used for the exam in the top sheet.

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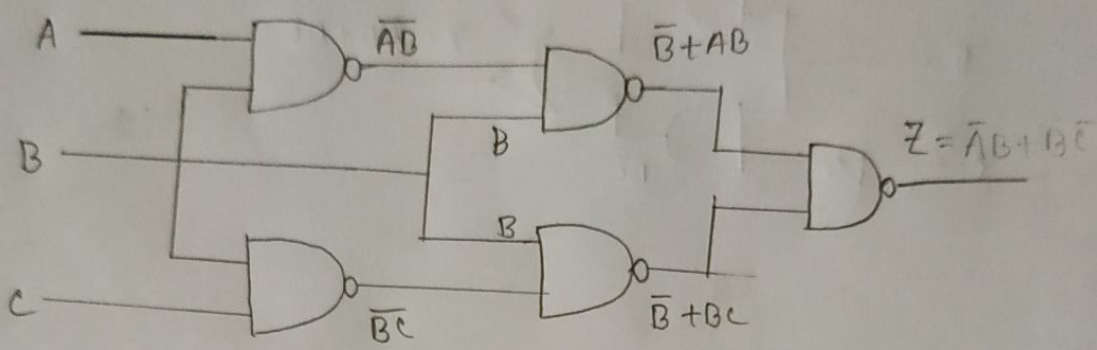
Answer to the question no - 1

a.



The first step is to determine the expression for the output $Z = \overline{\overline{AB}.B \quad \overline{BC}.B}$

Once the expression is determined break down large inverter signs by De Morgan's theorems

$$Z = \overline{\overline{AB}.B \quad \overline{BC}.B}$$

$$= \overline{\overline{AB}.B} + \overline{\overline{BC}.B}$$

$$= \overline{AB}.B + \overline{BC}.B$$

$$= (\bar{A}+\bar{B})B + (\bar{B}+\bar{C})B$$

$$= \bar{A}B + B.\bar{B} + B.\bar{B} + B\bar{C}$$

$$= \bar{A}B + B\bar{C} \qquad \because B.\bar{B} = 0$$

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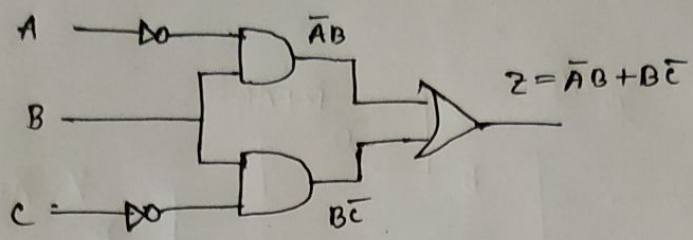
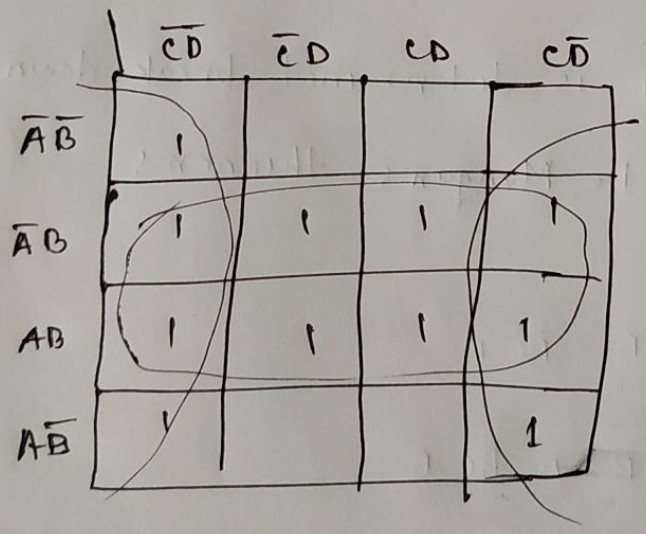
simplifed logic circuit



b.

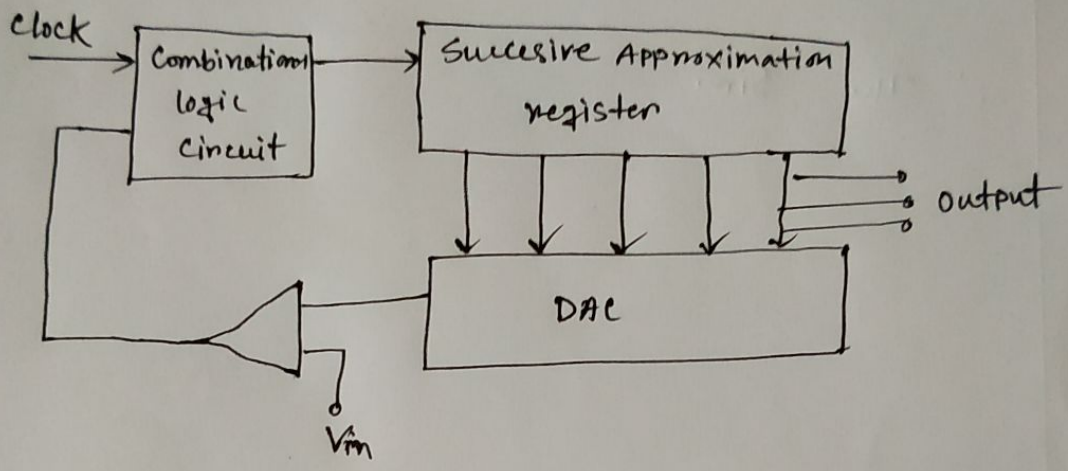
$$F(A,B,C,D) = B\bar{C} + \bar{D}(A+\bar{B}) + BCD + \bar{A}BC$$



There are 2 loops in K-map from loop-1 we get the value : B

Answer to the question no-3

Block diagram of succesive approximation Analog to Digital is shown below:



Output of SAR register is Converted in analog signal by Digital to analog Converter. This analog voltage a is Compared with input analog Voltage. Vin. Opamp output when high clock signal Contened into Combination logic. In first compasion MSB is set high. This digital signal get Conected to analog by DAC and again Compand with Vin.