INSTITUTE OF INFORMATION TECHNOLOGY

JAHANGIRNAGAR UNIVERSITY

Number of Assignment : 03

Name of Assignment : Designing Combinational Logic Circuits.

Course Tittle : Digital Logic Design

Course Code : ICT – 2103

Submission Date : 24/12/2020

Submitted To

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IIT – JU

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Roll – 2023

2nd year 1st Semester

IIT – JU

1. Decade synchronous down counter.

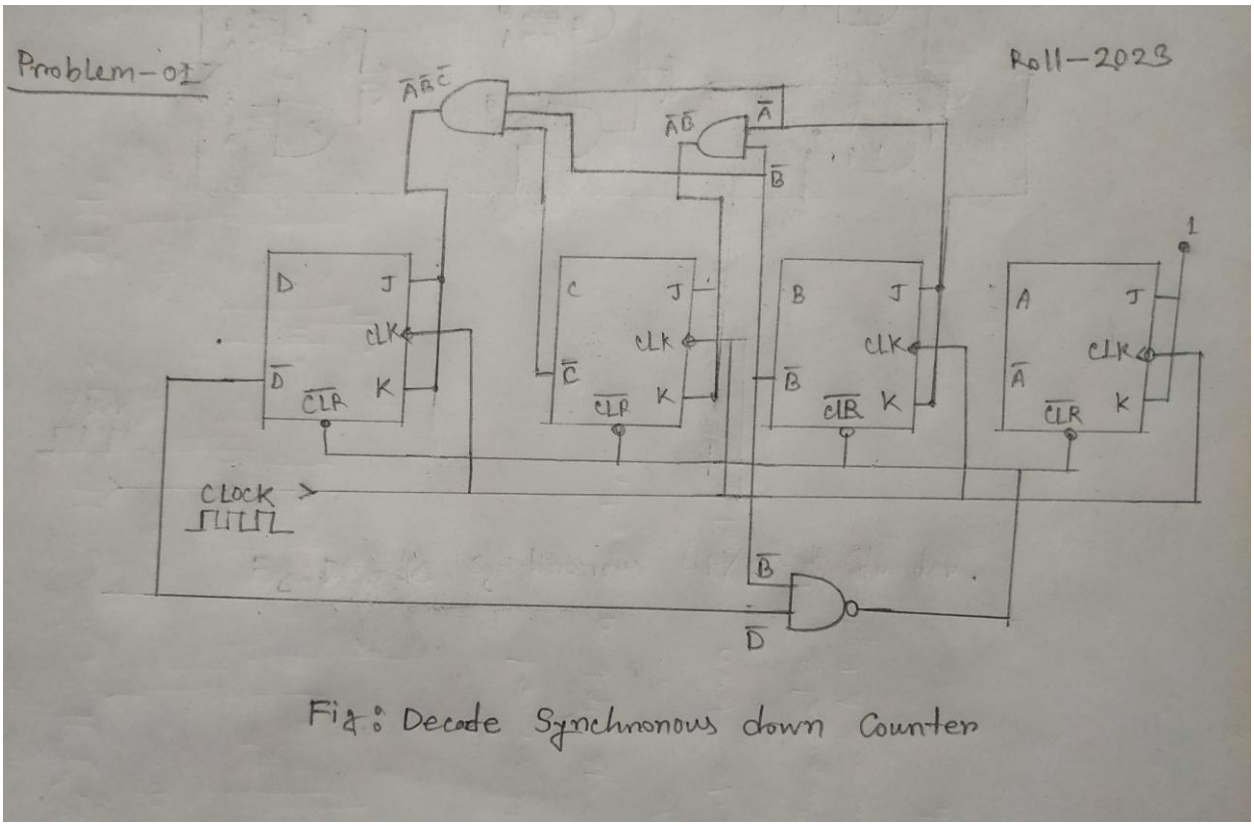
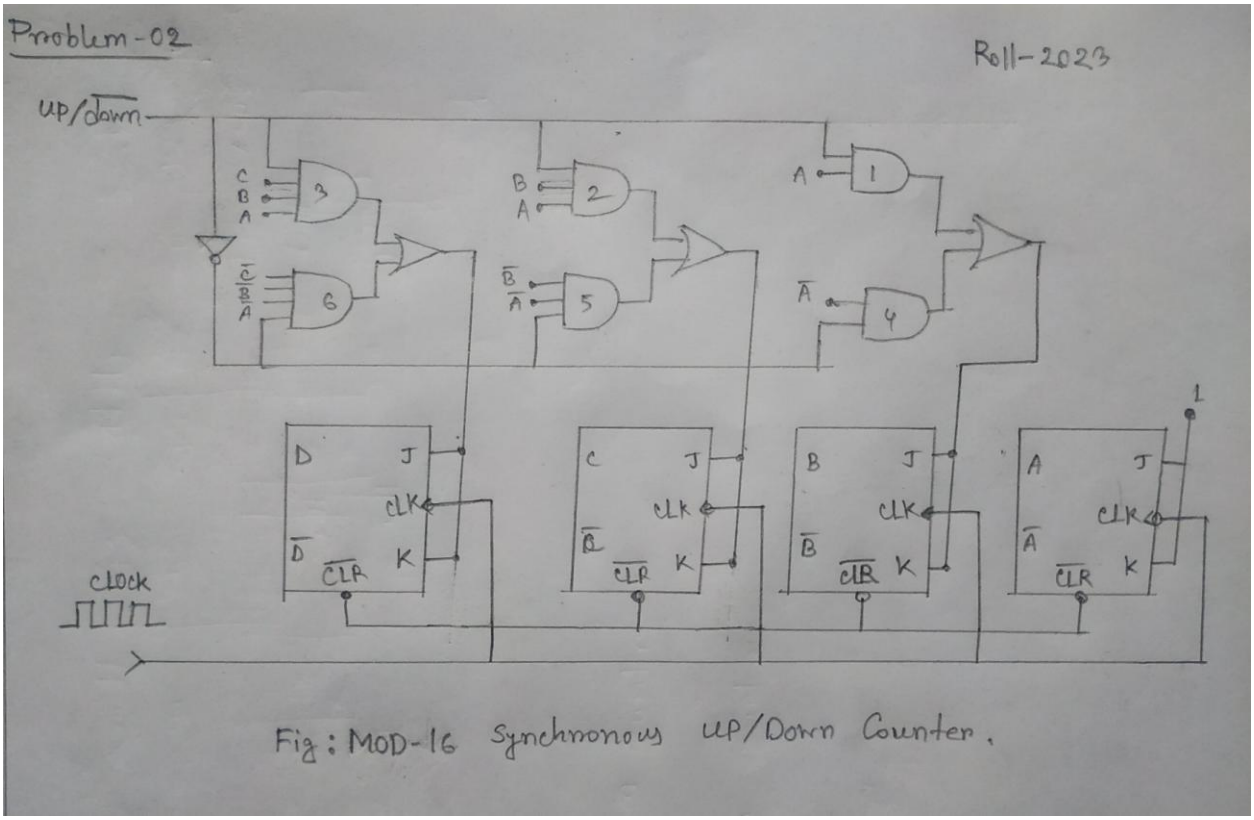


Fig: Decade Synchronous down Counter

2. Mod-16 synchronous up/down counter.



3. Decade synchronous up/down counter.