



INSTITUTE OF INFORMATION TECHNOLOGY
JAHANGIRNAGAR UNIVERSITY

Number of Assignment : 04

Name of Assignment : Designing Combinational Logic Circuits.

Course Title : Digital Logic Design

Course Code : ICT – 2103

Submission Date : 12/01/2021

Submitted To

Dr. Md. Sazzadur Rahman

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IIT – JU

Submitted By

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Roll – 2023

2nd year 1st Semester

IIT – JU

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Roll - 2023

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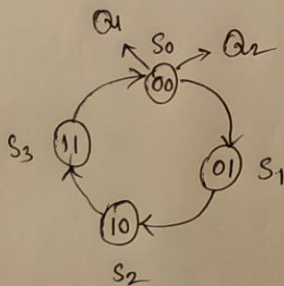
ESOS - 11/21

Application of Counter in Industry

JK Flip flop

| Q_n | Q_{n+1} | J | K |
|-------|-----------|---|---|
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |

State diagram



| | | |
|---|---|---|
| 1 | 0 | 1 |
| x | x | 0 |
| 1 | 0 | 1 |

| | | |
|---|---|---|
| 1 | 0 | 1 |
| 1 | 0 | 0 |
| x | x | 1 |

| | | |
|---|---|---|
| 1 | 0 | 1 |
| 1 | x | 0 |
| 1 | x | 1 |

| | | |
|---|---|---|
| 1 | 0 | 1 |
| x | 1 | 0 |
| x | 1 | 1 |

Roll - 2023

Assignment 1/1/2023 2/1/23

8:30:00 - 11:27

ckt excitation table:-

| Q_1 | Q_2 | Q_1 | Q_2 | J_1 | K_1 | J_2 | K_2 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 1 | 0 | x | 1 | x |
| 0 | 1 | 1 | 0 | 1 | x | x | 1 |
| 1 | 0 | 1 | 1 | x | 0 | 1 | x |
| 1 | 1 | 0 | 0 | x | 1 | x | 1 |

for J_1

| Q_1 | Q_2 |
|-------|-------|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

$$J_1 = Q_2$$

for K_1

| Q_1 | Q_2 |
|-------|-------|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

$$K_1 = Q_2$$

for J_2

| Q_1 | Q_2 |
|-------|-------|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

$$J_2 = 1$$

for K_2

| Q_1 | Q_2 |
|-------|-------|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

$$K_2 = 1$$



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