ARM Cortex-M3

- Implement Thumb-2 instruction subset of ARM Instruction Set.
- Most Thumb-2 instructions are 16-bit wide that are expanded internally to a full 32-bit ARM instructions.
- ARM CPUs are capable of performing multiple low-level operations in parallel.
- A hardware sign extender convert 8-16 bit operands to 32-bit
- Load store architecture.
- Barrel shifter allows operand R_m to beshited first and then ALU can perform another operation (e.g. add, subtract, mul etc.)
- Barrel shifter can do $5X = X + 2^2X$; $-7X = X-2^3X$.
- MAC is memory address calculator for different addressing of arrays and repetitive address calculations.
- R_0-R_{12} GPR, R_{13}-R_{15} special purpose registers i.e. SP, PC and LR (that holds the return address when a subroutine is called.

Bit Banding

- Memory mapped I/O, 4GB memory address space organized in bytes.
- 4GB is very large for small embedded applications.
- Bit-banding happens by taking advantage of this large memory space.
- Uses two different regions of the address space to refer the same physical data in the memory.
- In primary bit-band region each address corresponds to single data byte.
- In the bit-band alias each address corresponds to 1-bit of the same data.
- It allows the access of a bit of data (read or write) by a single instruction.
- LDR can load a single bit and STR can write a single bit of data.
- Two bit band alias regions can be used to access individual status and control bit of I/O devices or to implement a set of 1-bit Boolean flags that can be used to implement a set of mutex objects.
- Bit-band hardware does not allow interruption of read-modify write.

Bit_band alias address = Bit_band base +128 x word_offset + 4 x bit #

If bit-3 at address 20001000_{16} is to be modified the bit-band alias is

$22000000_{16} + 128_{10} \times 1000_{16} + 4 \times 3 = 2208000C_{16}$

PSR: Program Status Register

Divided into three bit fields

- Application Program Status Register (APSR)
- Interrupt Program Status Register (IPSR)
- Execution Program Status Register (EPSR)

Q-bit is the sticky saturarion bit and supports two rarely used instructions (SSAT and USAT)
SSAT{cond} Rd, #sat, Rm{, shift}

- EPSR holds the exception number is exception processing.
- ICI/IT bits holds the state information of for IT block instructions or instructions that are suspended during interrupt processing.
- T bit is always 1 to indicate Thumb instructions.

SSAT: Saturate Instruction

Consider two numbers 0xFFFF FFFE and 0×0000 0002. A 32-bit mathematical addition would result in 0×1 0000 0001 which contain 9 hex digits or 33 binary bits. If the same arithmetic is done in a 32 bit processor ideally the carry flag will be set and the result in the register will be 0×0000 0001.
If the operation was done by any comparison instruction this would not cause any harm but during any addition operation this may lead to unpredictable results if the code is not designed to handle such operations. Saturate arithmetic says that when the result crosses the extreme limit the value should be maintained at the respective maximum/minimum (in our case result will be maintained at 0xFFFF FFFF which is the largest 32-bit number).

Saturate instructions are very useful in implementing certain DSP algorithms like audio processing where we have a cutoff high in the amplitude. For instance the highest amplitude is expressed by a 32-bit value and if my audio filter gives an output more than this I need not programatically monitor the result. Rather the value automatically saturates to the max limit.

Also a new flag field called ‘Q’ has been added to the ARM processor to show us if there had been any such saturation taken place or the natural result itself was the maximum

Interrupt Latency Reduction

Time from interrupt request to the corresponding interrupt handler begins to execute.

1. Suspend or Abandon Instruction Execution:
No need to suspend single cycle instruction but multiple cycle ones such as LDM, STM, PUSH and POP that transfer multiple words to/from memory.

2. Late Arrival Processing:
CPU has begun an interrupt response sequence and another high priority interrupt arrive during the stacking operation. The CPU will redirect the remainder of the interrupt response so that it can handle the late arriving (higher priority) interrupt.

3. Tail Chaining:
In most CPUs when two ISRs execute back to back, the state information (8 word of CPU state) is popped off the stack at the end of 1st interrupt only to be pushed back at the beginning of the 2nd (next) interrupt.
M3 completely eliminates this useless pop-push sequence with a technique called tail-chaining, lowering the ISR transition time from 24 down to 6 clock cycles.

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CPSIE  i  ; Enable External Interrupts
CPSID  i  ; Disable External Interrupts
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