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Note: Design of FPGA based system identification module with application to atomic force microscopy

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The science of system identification is widely utilized in modeling input-output relationships of diverse systems. In this article, we report field programmable gate array (FPGA) based implementation of a real-time system identification algorithm which employs forgetting factors and bias compensation techniques. The FPGA module is employed to estimate the mechanical properties of surfaces of materials at the nano-scale with an atomic force microscope (AFM). The FPGA module is user friendly which can be interfaced with commercially available AFMs. Extensive simulation and experimental results validate the design. *Published by AIP Publishing.* https://doi.org/10.1063/1.5034016

This article details an embedded implementation of a real-time system identification algorithm first reported in Ref. 1 with application to atomic force microscopes (AFMs). The dynamic mode of AFM operation[2] creates minimal mechanical wear on the sample under investigation and is suitable for soft material investigation. With the development of novel system theoretical perspectives of the dynamic mode AFM,[3,4] it is possible to employ real-time system identification methods for estimating the stiffness and dissipative properties of materials.[1,4,5] Field Programmable Gate Arrays (FPGAs) provide attractive embedded solutions since they offer high speed of operation, supported protocols, reconfigurable capability, and design reuse.[6] We selected the Xilinx ML605 digital signal processing (DSP) kit as the FPGA platform to host our high precision system identification algorithm, namely, the bias-compensated exponentially weighted recursive least square (BCEWRLS) algorithm.[1] This algorithm employs a forgetting factor for prioritizing the recent measurement data compared to the past data. Prior work on the BCEWRLS algorithm[1] emphasized its effectiveness for AFM applications. However, an in-depth understanding of the selection of the forgetting factor was missing which we present in this article. As outlined in this article, a judicious choice of the forgetting factor plays a vital role to strike a compromise between the accuracy of the estimates and the bandwidth of estimation. FPGA implementation of the BCEWRLS algorithm was introduced briefly in Refs. 4 and 5; however, the FPGA design strategy was not discussed. In this article, we provide the detailed FPGA-based design of the BCEWRLS algorithm. The module reported in this article is user friendly and can be interfaced easily with commercially available AFMs to estimate stiffness-dissipative properties of samples.

A flexible cantilever with a sharp tip which scans over the sample surface and deflects according to the interactive forces between the tip and sample forms the main component of AFM (see Fig. 1). In the dynamic mode, the cantilever is oscillated sinusoidally and it interacts with the sample intermittently. The cantilever interacting periodically with the sample (see Fig. 1) can be modeled as an equivalent cantilever which follows the dynamics[4,7]

$$\ddot{p} + \frac{2\pi f_{eq}}{Q_{eq}}\dot{p} + (2\pi f_{eq})^2 p = g(t), \tag{1}$$

where g represents the cantilever excitation signal and p denotes the cantilever deflection. f_{eq} and Q_{eq} are referred to as the equivalent resonant frequency and equivalent quality factor, respectively. Here[4,5]

$$f_{eq}^2 = f_0^2 - \frac{\Phi_C}{4\pi^3 a^2 m f_d}, \frac{f_{eq}}{Q_{eq}} = \frac{f_0}{Q_0} + \frac{\Phi_D}{4\pi^3 a^2 m f_d^2}, \tag{2}$$

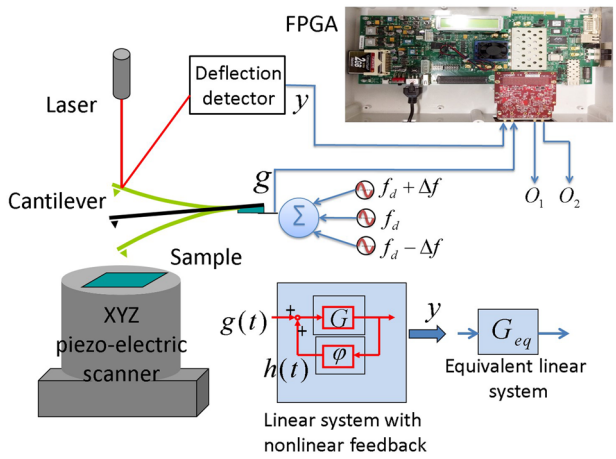

FIG. 1. In the dynamic mode of operation, the AFM cantilever is oscillated sinusoidally with drive frequency f_d near or at resonant frequency f_0. $h(t)$ denotes the interactive forces per unit mass between the sample and cantilever tip. The system including the cantilever and the interactive forces is modeled with an equivalent cantilever specified by parameters f_{eq} and Q_{eq}. The additional excitation signals at frequencies $f_d - \Delta f$ and $f_d + \Delta f$ are necessary for the system identification module implemented on FPGAs. The outputs O_1 and O_2 can be configured to access estimated (f_{eq}, Q_{eq}) as well as the conservative power, Φ_C, and dissipative power, Φ_D, due to the tip-sample interaction.

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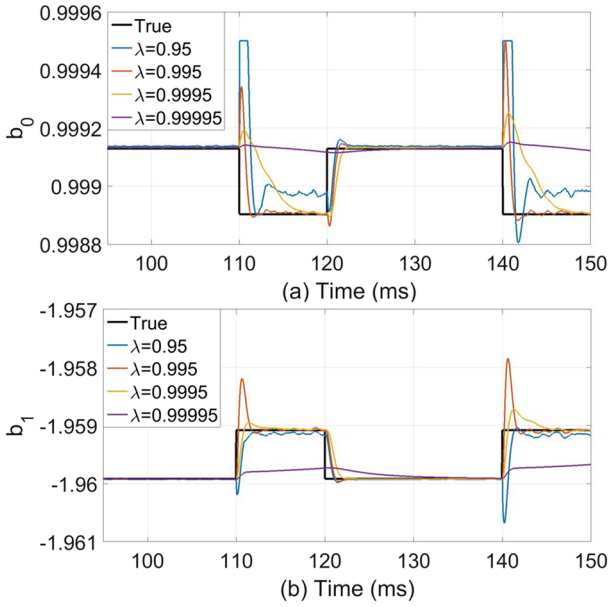

FIG. 2. (a) Estimated b_0 and (b) b_1 using BCEWRLS with the corresponding true value from simulation. $\lambda = 0.99995$ creates very slow estimation rendering the method ineffective. $\lambda = 0.95$ yields fast but incorrect convergence. $\lambda = 0.995$ and 0.9995 create correct convergence of estimated b_0 and b_1 to their true values.

where f_d is the drive frequency. f_0 and Q_0 represent the natural frequency and quality factor, respectively, which are measured in the absence of the sample. m is the mass of the cantilever, and a denotes the amplitude of cantilever oscillations. The average storage and dissipative powers due to tip-sample interactive forces can be shown to be Φ_C and Φ_D, respectively.[4,5] In (2), Φ_C and Φ_D can be determined once f_{eq} and Q_{eq} are estimated using the real-time system identification algorithm outlined below.

Dynamics of a general second order discrete time system corresponding to its continuous time counterpart (1) are described by

$$y(k) + b_1 y(k-1) + b_0 y(k-2) = u(k) + e(k), \tag{3}$$

where $u(k) = a_2 g(k) + a_1 g(k-1) + a_0 g(k-2)$ and $e(k)$ represents measurement noise. $y(k)$ and $g(k)$ denote the digitally sampled deflection and external forcing of the cantilever, respectively, which are acquired at time $t = kT_s$ with T_s denoting the sampling interval. It is observed that the parameters (a_2, a_1, a_0) in (3) do not change much in experiments and, hence, can be treated as constants.[1,4] It follows from (3) that

$$y'(k) = \underbrace{[-y(k-1) \;\; -y(k-2)]}_{\phi^T(k)} \underbrace{\begin{bmatrix} b_1 \\ b_0 \end{bmatrix}}_{\theta} + e(k), \tag{4}$$

where θ represents the vector of unknown parameters and $y'(k) = y(k) - a_2 g(k) - a_1 g(k-1) - a_0 g(k-2)$ is measured from experiments. A recursive least square estimator (denoted by $\hat{\theta}_{LS}$) can be obtained as follows:

$$\hat{\theta}_{LS}(k) = \arg\min_{\hat{\theta}(k)} \sum_{i=1}^{k} \lambda^{k-i} \left(y(i) - \phi^T(i)\theta(k)\right)^2, \tag{5}$$

where a forgetting factor $\lambda \in (0, 1)$ is introduced to emphasize on recent observations compared to the past observation data. With additional necessities for bias correction due to the correlated noise, the bias compensated exponentially weighted recursive least square (BCEWRLS) algorithm (see the supplementary material) is proposed in Ref. 1 which is adopted for FPGA implementation in this article. Once the estimate for $\theta = [b_1 b_0]^T$ is available, the parameters f_{eq} and Q_{eq} of the continuous time system (1) can be determined (see the supplementary material).

The effectiveness of the BCEWRLS algorithm is first verified by simulation using a hypothetical cantilever which switches between two known dynamical models. A cantilever model with resonant frequency 63.147 kHz (f_0) and quality factor 227.849 (Q_0) is chosen as model 1, where its discrete time dynamics (3) at sampling frequency of 2 MHz are described by the parameters $\{a_2, a_1, a_0, b_1, b_0\} = \{3.972\times10^{-4},$

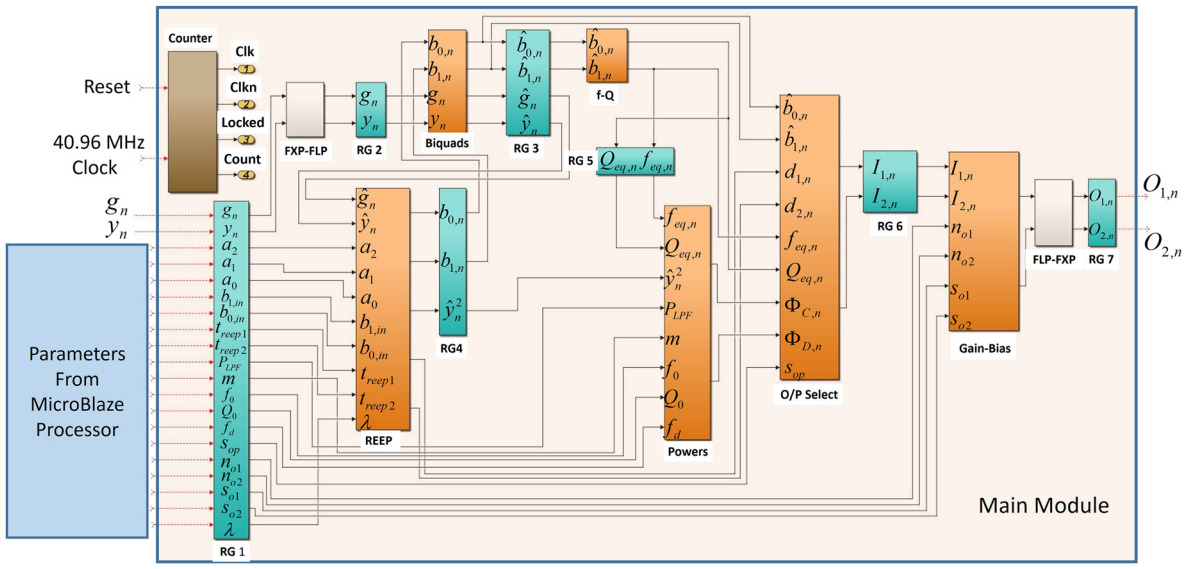

FIG. 3. Modules and flow of signals inside the Main Module.

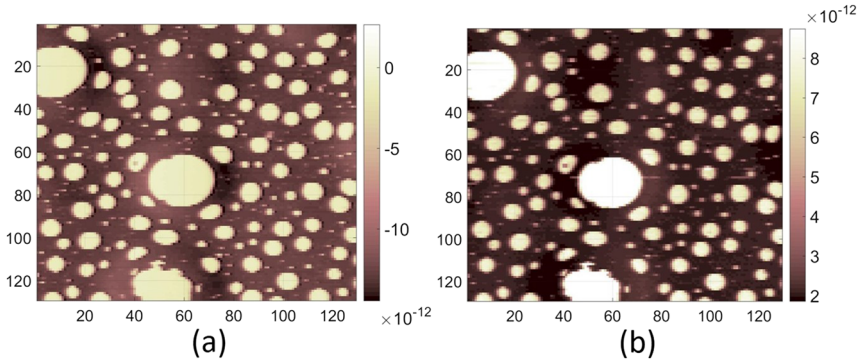

FIG. 4. (Experimental data) (a) Estimated conservative power Φ_C (in watt) and (b) dissipative power Φ_D (in watt) due to the periodic tip-sample interaction estimated using the FPGA module. The color bars specify corresponding ranges.

-2.036×10^{-4}, -4.990×10^{-4}, -1.9599, $0.9991\}$. Another cantilever model with resonant frequency $f_0 + 0.5$ kHz and quality factor $0.8Q_0$ is chosen to represent model 2, where the discrete time dynamics are specified by $\{b_1, b_0\} = \{-1.9591, 0.9989\}$, while the other parameters (a_2, a_1, a_0) are the same as model 1. In Fig. 2, the cantilever behavior switches between model 1 and model 2 randomly with a duration of 10 ms. The BCEWRLS algorithm is implemented in MATLAB to estimate $\{b_1, b_0\}$ for different λ, as shown in Fig. 2. λ very close to 1 (0.999 95) results in slow estimation (over-tuning). The rate of convergence improves with lower λ; $\lambda = 0.9995$ and 0.995 yield correct estimation within the bit duration (10 ms). However, further lowering of λ to 0.95 creates incorrect convergence of b_0 and b_1 (under-tuning). In prior work,[1] the major bottleneck for fast estimation was speculated to be the measurement noise. However, here we demonstrate that even in ideal noiseless situations, the BCEWRLS algorithm will converge to inaccurate values when λ is chosen to be too small. Thus the user needs to avoid not only over-tuning but also under-tuning as well. Typically, we found that $\lambda = 0.9995$ is a good starting point for experiments.

A schematic of the FPGA-based system identification module is shown in Fig. 3. This module is hosted by using a Xilinx ML605 Digital Signal Processing (DSP) development kit with a FPGA Mezzanine Card (FMC) 151 ADC-DAC (analog-to-digital and digital-to-analog converter) unit. Each of the modules inside the Main Module except the register modules and the Counter is designed with the same architectural backbone, details of which are discussed in the supplementary material. Such an architectural backbone allows the designer to use a common and flexible framework, based on which different modules can be built. As demonstrated in Fig. 3, the Main Module contains different component modules such as the REEP, Biquads, Powers, O/P select, and Gain-Bias module. The implementation details of these modules including the computational cores, data precision, and output latency are described extensively in the supplementary material. Here we briefly outline example results.

An AC240TS cantilever from Asylum Research with a resonant frequency of 72.7 kHz and a quality factor of 142.9 is utilized for dynamic mode imaging with MFP 3D AFM from Asylum Research. The sample which consists of a blend of polylauryl methacrylate (PLMA) and polybutyl methacrylate (PBMA) polymers coated over a silica substrate is scanned at a speed of 0.25 Hz (1 line is scanned in 4 s). The system identification module is implemented on the FPGA with a forgetting factor $\lambda = 0.9995$. The excitation signal to the cantilever g and the measured deflection signal y are inputs to the FPGA. The resulting images for the conservative power Φ_C and dissipative power Φ_D due to interactive forces between the cantilever tip and sample evaluated by the FPGA module for a 10 μm × 10 μm sample are shown in Figs. 4(a) and 4(b), respectively. The circular regions in Fig. 4(a) corresponding to the brighter domains represent the PLMA regions which are distributed over the PBMA background. Figure 4(b) demonstrates that Φ_D is consistently higher on PLMA domains compared to the PBMA film, which indicates that PLMA is more dissipative than PBMA at room temperature. Furthermore, less negative values of Φ_C in Fig. 4(a) on the PLMA domains indicate that the equivalent cantilever frequency f_{eq} is less [see (2)] on PLMA regions compared to the PBMA film. Such a property indicates that PLMA is softer at the surface compared to PBMA at room temperature. Additional images for other properties such as the height, amplitude, phase, equivalent frequency, and quality factor of the same sample are shown in the supplementary material.

Thus, we demonstrated the effectiveness of the FPGA-based system identification module. The systematic design procedure, especially the architectural backbone shown in the supplementary material, is employable to design different FPGA-based measurement systems, where data are sampled from analog input signals and processed using high precision mathematical operations and the final data are obtained in analog form. Applicability of the FPGA module is not limited to this particular example but extendable to a wide variety of samples such as other soft polymers, cells, DNA, and proteins.

See supplementary material for a detailed description of the FPGA design, the architectural backbone, and the timing schedules for different modules utilized in the Main Module, as shown in Fig. 3.

[1] P. Agarwal and M. Salapaka, Appl. Phys. Lett. **95**, 083113 (2009).
[2] R. García, *Amplitude Modulation Atomic Force Microscopy* (John Wiley & Sons, 2011).
[3] A. Sebastian, A. Gannepalli, and M. Salapaka, IEEE Trans. Control Syst. Technol. **15**, 952 (2007).
[4] S. Ghosal, A. Gannepalli, and M. Salapaka, Nanotechnology **28**, 325703 (2017).
[5] G. Saraswat, P. Agarwal, G. Haugstad, and M. Salapaka, Nanotechnology **24**, 265706 (2013).
[6] A. Malinowski and H. Yu, IEEE Trans. Ind. Inf. **7**, 244 (2011).
[7] S. Ghosal, G. Saraswat, and M. Salapaka, Automatica **74**, 171 (2016).