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A Robust Scheme for Distributed Control of Power Converters in DC Microgrids with Time-Varying Power Sharing

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Abstract— **This paper addresses the problem of output voltage regulation for multiple DC/DC converters connected to a microgrid, and prescribes a scheme for sharing power among different sources. This architecture is structured in such a way that it admits quantifiable analysis of the closed-loop performance of the network of converters; the analysis simplifies to studying closed-loop performance of an equivalent *single-converter* system. The proposed architecture allows for the proportion in which the sources provide power to vary with time; thus overcoming limitations of our previous designs in [1]. Additionally, the proposed control framework is suitable to both centralized and decentralized implementations, i.e., the same control architecture can be employed for voltage regulation irrespective of the availability of common load-current (or power) measurement, without the need to modify controller parameters. The performance becomes quantifiably better with better communication of the demanded load to all the controllers at all the converters (in the centralized case); however guarantees viability when such communication is absent. Case studies comprising of battery, PV and generic sources are presented and demonstrate the enhanced performance of prescribed optimal controllers for voltage regulation and power sharing.**

I. INTRODUCTION

Utility grid is most stressed during peak power demands resulting in significant increase in real-time power prices and congestion in the local power distribution zone. Microgrids can help reduce the requirement for additional utility generation and thus minimize the demand on the utility grid by enabling integration of renewable energy sources such as solar and wind energy, distributed energy resources (DERs), energy storage, and demand response. Microgrids are localized grid systems that are capable of operating in parallel with, or independently from, the existing traditional grid [2]. Fig. 1 shows a schematic of a microgrid with multiple DC sources providing power for AC loads. Existing control architectures for traditional grids, which are designed for relatively large conventional sources (power plants) of predictable and *dispatchable* electric power, cannot adequately manage *uncertain* power sources such as solar or wind generations. Limited predictability with such resources result in intermittent power generation; moreover time-varying loads, practicability and economics factors pose additional challenges in efficient operation of microgrids. Thus it is required to develop efficient distributed control technologies for reliable operation of smart microgrids [3].

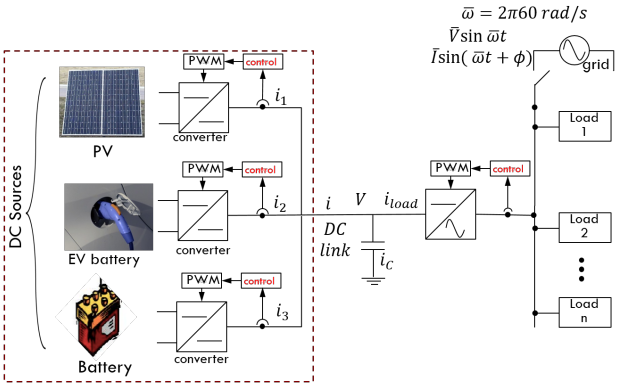

Fig. 1: A schematic of a microgrid. An array of DC sources provide power for AC loads. Power sources provide power at DC-link, their common output bus, at a voltage that is regulated to a set-point. The control system at the respective DC-DC converter that interfaces with a source is responsible for regulating the voltage at the DC-link.

In such smart grids, multiple DC power sources connected in parallel, each interfaced with DC-DC converter, provide power at their common output, the DC-link, at a regulated voltage; this power can directly feed DC loads or be used by an inverter to interface with AC loads (see Fig. 1). By appropriately controlling the switch duty-cycle of DC-DC converter at each power source, it becomes possible to manipulate electrical quantities such as the power output by the power source and the voltage at the DC-link. The main goals of the control design is to regulate voltage at the DC-link and ensuring a prescribed sharing of power between different sources; for instance, economic considerations can dictate that power provided by the sources should be in a certain proportion or according to a prescribed priority (e.g. PV provides the maximum power it can to satisfy load demand, and the deficit is provided by battery). The main challenges arise from the uncertainties in the size and the schedules of loads, the complexity of a coupled multi-converter network, the uncertainties in the model parameters at each converter, and the adverse effects of interfacing DC power sources with AC loads, such as the 120 Hz ripple that has to be provided by the DC sources.

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Problems pertaining to robust and optimal control of converters have received recent attention. Conventional PID-based controllers often fail to address the problem of robustness and modeling uncertainties. In [4], a linear-matrix-inequality (LMI) based robust control design is presented for boost converters which demonstrates significant improvements in voltage regulation over PID based control designs. In [5], [6], robust $\mathcal{H}_\infty$-control framework is employed in the context of inverter systems. While the issue of current sharing is extensively studied [7], most methods assume a single power source. A systematic control design that addresses all the challenges and objectives for the multi-converter control is still lacking.

The control architecture proposed in this paper addresses the following primary objectives - a) voltage regulation at the DC-link with guaranteed robustness margins, b) prescribed *time-varying* power sharing in a network of parallel converters, c) controlling the trade-off between 120Hz ripple on the total current provided by the power sources and the ripple on the DC-link voltage. While these objectives are partially addressed in our prior work [1] on the robust control of DC-DC converters, a main drawback of the design proposed in [1] is that the control framework does not allow for time-varying power sharing requirements. In this work, we propose a new architecture wherein the power requirements on each converter are imposed through external reference signals; this allows for time-varying power sharing/priority prescriptions. This is achieved without sacrificing any advantages of the design in [1].

An important feature of the proposed architecture is that it exploits structural features of the paralleled multi-converter system, which results in a modular and yet coordinated control design. Accordingly at each converter, it employs a nested (outer-voltage inner-current) control structure, where all converters share the same design for the outer-loop voltage controllers while the inner-loop current controllers are so chosen that the entire closed-loop multi-converter system can be reduced to an equivalent *single-converter* system in terms of the transfer function from the desired regulation setpoint V_{ref} to the voltage at the DC-link V. An interesting aspect of the proposed implementation is that the same control implementation works for both the *centralized* case, when the load power is known and communicated to all the controllers, and the *decentralized* case where the load is unknown. The architecture achieves better performance in voltage regulation and power sharing when load power information is communicated, while it guarantees electrical viability with quantifiable bounds on deviations from the targeted performances in the decentralized case.

II. MODELING OF CONVERTERS

In this section, we describe the differential equations that govern the dynamics of DC-DC converters. These converters belong to a class of switched-mode power electronics, where a semiconductor based high-frequency switching mechanism connected to a DC power source enables changing voltage and current characteristics at its output. The models presented below depict dynamics for signals that are averaged over a switch cycle.

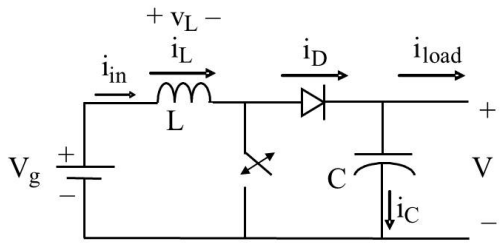

Fig. 2: A schematic of a Boost converter. The converters are assumed to operate in continuous-conduction-mode (CCM).

Fig. 2 shows a schematic of a Boost converter. Boost converter regulates a voltage V at its output which is larger than the input voltage V_g. The averaged dynamic model of a Boost converter is given by

$$\begin{aligned} L\dot{i}_L(t) &= -(1-d(t))V(t) + V_g, \\ C\dot{V}(t) &= (1-d(t))i_L(t) - i_{\text{load}}(t), \end{aligned} \tag{1}$$

where $d(t)$ represents the duty-cycle (or the proportion of *ON* duration) at time t. By defining $d'(t) := 1 - d(t)$ and $D' := \left(V_g/V_{\text{ref}}\right)$, where V_{ref} is the desired output voltage, (1) can be rewritten as,

$$\begin{aligned} L\frac{di_L(t)}{dt} &= \underbrace{V_g - d'(t)V(t)}_{\tilde{u}(t):=V_g-u(t)}, \\ C\frac{dV(t)}{dt} &= \underbrace{(D' + \hat{d}(t))}_{\approx D'} i_L(t) - i_{\text{load}}(t). \end{aligned} \tag{2}$$

Note that $\hat{d}(t) = d'(t) - D'$ is typically very small, and therefore allows for a linear approximation around the nominal duty-cycle, $D = 1 - D'$.

III. PROBLEM FORMULATION

This paper addresses the following primary objectives *simultaneously* (in context of Fig. 1) - (a) Regulation of DC-link voltage V to a prescribed value V_{ref} in presence of time-varying loads/generation and parametric uncertainties, (b) time-varying current (power) sharing among multiple sources, that is, ensuring that current (power) outputs i_k from each converter respectively track a time-varying signal i_{ref_k}, and (c) $120Hz$ ripple current sharing between the output currents i_k from each converter and the capacitor current i_C. The last objective is dealt in our prior work [1] and is addressed by an appropriate design of inner-controller described in Sec. IV-A and V. In this paper, we primarily focus on achieving the first two objectives, while inheriting the properties of the inner-controller for ripple current sharing.

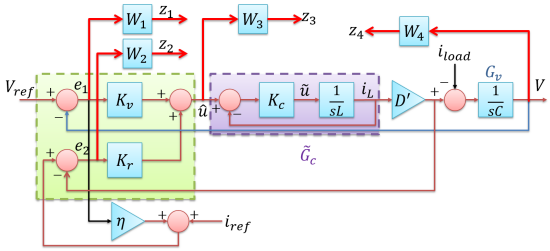

Fig. 3: Block diagram representation of the inner-outer control design. The *regulated variables* z_1, z_2, z_3 and z_4 correspond to weighted - (a) tracking error in DC-link voltage, (b) mismatch between i_{ref} and i_{load}, (c) control effort $\hat{u}$, and (d) output voltage tracking, respectively.

IV. CONTROL FRAMEWORK FOR SINGLE CONVERTER

In this section, we describe the *inner-outer* control design for a single Boost converter system. This design for a *single* converter forms the basis for the analysis and design of control architecture for multiple converters presented in Sec. V. While the design is easily extendable to include other converter types such as Buck and Buck-Boost, the discussion has been confined to Boost converters only for the sake of brevity. Note that in the proposed control architecture (see Fig. 3), the inputs to outer feedback controller include i_{ref} in addition to the typical V_{ref} and the measured DC-link voltage V. The requirements on current sharing are imposed through this additional i_{ref} signal (explained in Sec. V) by setting i_{ref} to measured (or communicated) load current i_{load} in the centralized case, and setting i_{ref} to estimated (or prespecified) signals in the decentralized case.

A. Design of the inner-loop controller

The design for the inner-loop controller K_c is inherited from our previous work [1]. The main objective for designing the inner-loop controller K_c is to decide the trade-off between the 120Hz ripple on the capacitor current i_C (equivalently on the output voltage V) and the inductor current i_L of the converter. Accordingly, K_c is designed such that the inner-shaped plant $\tilde{G}_c$ is given by

$$\tilde{G}_c(s) = \left(\frac{\tilde{\omega}}{s+\tilde{\omega}}\right)\left(\frac{s^2+2\zeta_1\omega_0 s+\omega_0^2}{s^2+2\zeta_2\omega_0 s+\omega_0^2}\right). \tag{3}$$

where $\omega_0 = 2\pi 120\text{rad/s}$ and $\tilde{\omega}, \zeta_1, \zeta_2$ are design parameters. The parameter $\tilde{\omega} > \omega_0$ and it is used to implement a low-pass filter to attenuate undesirable frequency content in i_L beyond $\tilde{\omega}$. Thus, the bandwidth of the inner closed-loop plant is decided by the choice of $\tilde{\omega}$. The ratio ζ_1/ζ_2 can be appropriately designed to achieve a specified trade-off between 120Hz ripple on i_C and i_L, and therefore between V and i_L. The readers are encouraged to refer to Sec. III in [1] for further details on the inner-loop control design.

B. Design of the outer-loop controller

For a given choice of inner-controller K_c, we present our analysis and design of controller in terms of transfer function block diagrams shown in Fig. 3. In this figure, $\tilde{G}_c$ represents the inner shaped plant. The outer controllers are denoted by K_v and K_r, and are designed to regulate the output DC voltage V to the desired reference voltage V_{ref} and the output current $D'i_L$ to the reference current i_{ref}, respectively. Note that from (2), $D'i_L$ is equal to i_{load} at steady-state. The augmentation of controller K_r forms the basis for time-varying power sharing and is explained in the next section. It should be remarked that the proposed design has a feature that if the load current measurement is available, i.e., $i_{\text{ref}} = i_{\text{load}}$, then the steady state DC output voltage is maintained at the reference voltage V_{ref}. However in the absence of i_{load} measurement, the outer controller K_r regulates the output current $D'i_L$ to $i_{\text{ref}} \neq i_{\text{load}}$ resulting in an output voltage $V \neq V_{\text{ref}}$. The mismatch in voltage tracking is captured by a pre-specified *droop*-like coefficient η in a controlled manner, the notable difference here being the application of droop to the *faster* current loop when compared with the conventional droop-based design acting on the *slower* voltage loop. This feature is mathematically quantified in the following discussion on the proposed control design.

The main objective for the design of the controllers K_v and K_r is to make the tracking errors small and simultaneously attenuate measurement noise to achieve high resolution. This is achieved by posing a *model-based* multi-objective optimization problem, where the required objectives are described in terms of norms of the corresponding transfer functions, as described below. Note that the regulated variables z_1, z_2, z_3 and z_4 correspond to weighted - (a) tracking error in DC-link voltage, (b) mismatch between i_{ref} and i_{load}, (c) control effort $\hat{u}$, and (d) output voltage tracking, respectively. From Fig. 3, the transfer function from exogenous inputs and auxiliary control input $w = [V_{\text{ref}}, i_{\text{ref}}, i_{\text{load}}, \hat{u}]^T$ to regulated output $z = [z_1, z_2, z_3, z_4, e_1, e_2]$ is given by

$$\underbrace{\begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ z_4 \\ e_1 \\ e_2 \end{bmatrix}}_{z} = \underbrace{\begin{bmatrix} W_1 & 0 & W_1G_v & -D'W_1G_v\tilde{G}_c \\ \eta W_2 & W_2 & \eta W_2 G_v & -D'(1+\eta G_v)W_2\tilde{G}_c \\ 0 & 0 & 0 & W_3 \\ 0 & 0 & -W_4G_v & D'W_4G_v\tilde{G}_c \\ 1 & 0 & G_v & -D'G_v\tilde{G}_c \\ \eta & 1 & \eta G_v & -D'(1+\eta G_v)\tilde{G}_c \end{bmatrix}}_{T_{wz}} \underbrace{\begin{bmatrix} V_{\text{ref}} \\ i_{\text{ref}} \\ i_{\text{load}} \\ \hat{u} \end{bmatrix}}_{w}. \tag{4}$$

The optimization problem is to find stabilizing controllers $K_{outer} = [K_v, K_r]^T$ such that the $\mathcal{H}_\infty$-norm of the above transfer function from w to z is minimized. Here the weights W_1, W_2, W_3 and W_4 are chosen to reflect the design specifications of robustness to parametric uncertainties, tracking bandwidth, and saturation limits on the control signal. More specifically, the weight functions $W_1(j\omega)$ and $W_2(j\omega)$ are chosen to be large in frequency range $[0, \omega_{BW}]$ to ensure small tracking errors $e_1 = V_{\text{ref}} - V$ and $e_2 = i_{\text{ref}} + \eta e_1 - D'i_L$ in this frequency range. The design of weight function $W_3(j\omega)$ entails ensuring that the control effort lies within saturation limits. The weight function W_4 is designed as a high-pass filter to ensure that the transfer function from i_{load} to V is small at high frequencies to

provide mitigation to measurement noise.

Note that for the system shown in Fig. 3, the voltage V at the DC-link is given by,

$$V = G_v\left(-i_{\text{load}} + D'\tilde{G}_c(K_v e_1 + K_r e_2)\right). \tag{5}$$

Using the fact that $e_1 = V_{\text{ref}} - V$ and $e_2 = i_{\text{ref}} + \eta e_1 - D'\tilde{G}_c(K_v e_1 + K_r e_2)$, the DC-link voltage in terms of exogenous quantities $V_{\text{ref}}, i_{\text{ref}}$ and i_{load} is given by

$$\begin{aligned} V(s) = &\left[\frac{D'\tilde{G}_c G_v(K_v+\eta K_r)}{1+D'\tilde{G}_c K_r + D'\tilde{G}_c G_v(K_v+\eta K_r)}\right] V_{\text{ref}}(s) \\ &+\left[\frac{D'\tilde{G}_c G_v K_r}{1+D'\tilde{G}_c K_r + D'\tilde{G}_c G_v(K_v+\eta K_r)}\right](i_{\text{ref}}(s) - i_{\text{load}}(s)) \\ &-\left[\frac{G_v}{1+D'\tilde{G}_c K_r + D'\tilde{G}_c G_v(K_v+\eta K_r)}\right] i_{\text{load}}(s). \end{aligned} \tag{6}$$

Let $S(s), T_{V_{\text{ref}}V}$ and $T_{i_{\text{ref}}V}$ denote the closed-loop sensitivity transfer function and complementary sensitivity transfer functions from V_{ref} to V and i_{ref} to V, respectively. Then (6) can be rewritten as

$$V(s) = T_{V_{\text{ref}}V} V_{\text{ref}}(s) + T_{i_{\text{ref}}V}\left(i_{\text{ref}}(s) - i_{\text{load}}(s)\right) - G_v S i_{\text{load}}(s).$$

The DC gains of above closed-loop transfer functions are given by (since $G_v = 1/sC$ has an infinite DC gain),

$$|T_{V_{\text{ref}}V}(j0)| = 1, \quad |T_{i_{\text{ref}}V}(j0)| = \frac{|K_r(j0)|}{|K_v(j0)+\eta K_r(j0)|} \quad \text{and}$$
$$|(G_v S)(j0)| = \frac{1}{D'\left(|K_v(j0)+\eta K_r(j0)|\right)}.$$

We now provide a sketch of the proposed design concept. Since K_v and K_r are chosen as high DC-gain controllers (obtained by solving the $\mathcal{H}_\infty$ optimization problem), we have $|G_v S((j\omega))| \approx 0$ at low-frequencies. Thus the effect of disturbance signal i_{load} is insignificant at low frequencies. Similarly $T_{V_{\text{ref}}V}(j\omega)$ has unity gain at low frequencies. Furthermore, if the load current i_{load} measurement is available (i.e. $i_{\text{ref}} = i_{\text{load}}$), then the Boost converter tracks the reference voltage with almost unity gain. However in the absence of i_{load} measurement, the tracking error depends on the mismatch between i_{ref} and i_{load}, i.e., the bound on the steady-state tracking error becomes proportional to $\frac{|K_r(j0)|}{|K_v(j0)+\eta K_r(j0)|}$ multiplied by the mismatch value $|i_{\text{ref}}(j0) - i_{\text{load}}(j0)|$. By choosing appropriate controllers K_v and K_r (i.e., $|T_{i_{\text{ref}}V}(j0)| << 1$), the tracking error can be made small.

V. EXTENSION TO A SYSTEM OF PARALLEL CONVERTERS

In this section we extend our control framework for a single converter to a system of DC-DC converters connected in parallel in the context of power sharing, keeping in mind the practicability and robustness to modeling and load uncertainties. In particular, we analyze the multi-converter system in Fig. 4 through an *equivalent* single-converter system (similar to the system shown in Fig. 3), where the multi-converter system inherits the performance and robustness achieved by a design for the single-converter system.

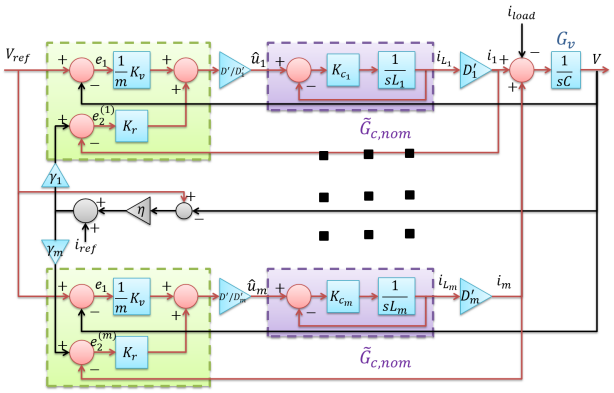

Fig. 4: Many-converters system with shaped inner plants $\tilde{G}_c$. In the proposed implementation, we adopt the same outer controller for different converters, i.e., $K_{v_1} = K_{v_2} = .. = K_{v_m} = \frac{1}{m}K_v$ and $K_{r_1} = K_{r_2} = .. = K_{r_m} = K_r$; γ_k represents the proportion of power demanded from the k^{th} source.

Fig. 4 represents the proposed inner-outer control framework for a system of m parallel connected converters. Note that the reference signal $i_{\text{ref}} + \eta(V_{\text{ref}} - V)$ is prescaled by a time-varying multiplier $\gamma_k, 0 \le \gamma_k \le 1$. The choice of γ_k dictates the power sharing requirements on the k^{th} converter. In fact, we later show that the proposed implementation distributes the output power in the ratios $\gamma_1 : \gamma_2 : .. : \gamma_m$. After noting that the voltage-regulation and current reference tracking is common to all the outer controllers, in our architecture, we impose the same design for outer-controllers for all the converters, i.e., $K_{v_1} = K_{v_2} = .. = K_{v_m}$ and $K_{r_1} = K_{r_2} = .. = K_{r_m}$. This imposition enables significant reduction in the overall complexity of the distributed control design for a parallel network of converters and power sources, thus ensuring the practicability of the proposed design which allows integration of power sources of different types and values.

We design inner-controllers K_{c_k} such that the inner-shaped plants from $\tilde{u}_k$ to i_{L_k} are same and given by,

$$\tilde{G}_{c,nom}(s) = \left(\frac{\tilde{\omega}}{s+\tilde{\omega}}\right)\left(\frac{s^2 + 2\zeta_{1,nom}\omega_0 s + \omega_0^2}{s^2 + 2\zeta_{2,nom}\omega_0 s + \omega_0^2}\right), \tag{7}$$

where the ratio $\zeta_{1,nom}/\zeta_{2,nom}$ determines the tradeoff of 120Hz ripple between the total output current $D'i_L = \sum_{k=1}^{m} D'_k i_{L_k}$ and the capacitor current i_C. Note that for given values of $\zeta_{1,nom}, \zeta_{2,nom}$ and inductance L_k, explicit design of K_{c_k} exists. Furthermore, we impose $K_{v_k} = \frac{1}{m}K_v$ and $K_{r_k} = K_r$.

Indeed, by our choice of inner and outer controllers, the transfer functions from external references V_{ref}, i_{ref} and i_{load} to the desired output V are identical for all converters. Hence the entire network of parallel converters can be analyzed in the context of an equivalent single converter system. This implies that K_{v_k} and K_{r_k} can be computed by solving $\mathcal{H}_\infty$-optimization problem (as discussed in the previous section) similar to the *single* converter case. We make these design specifications more precise and bring out the equivalence of

the control design for the single and multiple converter systems in the following theorem.

We say that the system representation in Fig. 3 is *equivalent* to that in Fig. 4, when the transfer functions from the reference voltage V_{ref}, reference current i_{ref} and load current i_{load} to the DC-link voltage V in Fig. 3 are identical to the corresponding transfer functions in Fig. 4.

Theorem *1:* Consider the single-converter system in Fig. 3 with inner-shaped plant $\tilde{G}_{c,nom}(s)$ as given in (7), outer controllers K_v, K_r, droop-coefficient η, and external references $V_{\text{ref}}, i_{\text{load}}, i_{\text{ref}}$; and the multi-converter system described in Figs. 4a and 4b with inner-shaped plants $\tilde{G}_{c_k} = \tilde{G}_{c,nom}(s)$ and outer controllers $K_{v_k} = \frac{1}{m}K_v$; $K_{r_k} = K_r$, droop-coefficient η, and same external references $V_{\text{ref}}, i_{\text{load}}$ and reference current i_{ref} prescaled by time-varying scalars $\gamma_k > 0$ for $1 \le k \le m$.

1. [System Equivalence]: If $\sum_{k=1}^{m} \gamma_k = 1$, then the system representation in Fig. 3 is *equivalent* to the system representation in Fig. 4.

2. [Power Sharing]: For any two converters k and l, $k, l \in \{1, \ldots, m\}$ in a multi-converter system shown in Fig. 4, the difference in the corresponding steady-state scaled output currents is given by

$$\left| \frac{D'_k i_{L_k}(j0)}{\gamma_k} - \frac{D'_l i_{L_l}(j0)}{\gamma_l} \right| \le \left(\eta |\tilde{T}_1(j0)| + \left| \frac{1}{\gamma_k} - \frac{1}{\gamma_l} \right| |\tilde{T}_2(j0)| \right) |e_1(j0)|, \tag{8}$$

where, $\tilde{T}_1 := \frac{D'\tilde{G}_{c,nom}K_r}{(1+D'\tilde{G}_{c,nom}K_r)}$ and $\tilde{T}_2 := \frac{D'\tilde{G}_{c,nom}K_v}{m(1+D'\tilde{G}_{c,nom}K_r)}$. Furthermore, the steady-state tracking error $e_1 \triangleq V_{\text{ref}} - V$ in DC-link voltage is upper bounded by,

Centralized case: $i_{\text{ref}} = i_{\text{load}}$

$$|e_1(j0)| \le \frac{1}{D'(|K_v(j0) + \eta K_r(j0)|)} |i_{\text{ref}}(j0)|$$

Decentralized case: $i_{\text{ref}} \neq i_{\text{load}}$

$$|e_1(j0)| \le \frac{|K_r(j0)|}{D'(|K_v(j0) + \eta K_r(j0)|)} |i_{\text{ref}}(j0)| + \frac{D'|K_r(j0)| + 1}{D'(|K_v(j0) + \eta K_r(j0)|)} |i_{\text{load}}(j0)|$$

Remark 1: If the steady-state tracking error in DC-link voltage is zero, i.e., $|e_1(j0)| = 0$, then (8) reduces to the following constraint:

$$\frac{|D'_k i_{L_k}(j0)|}{|D'_l i_{L_l}(j0)|} = \frac{\gamma_k}{\gamma_l}.$$

i.e., the closed-loop multi-converter system achieves output power sharing given by $|D'_1 i_{L_1}(j0)| : \ldots : |D'_m i_{L_m}(j0)| = \gamma_1 : \ldots : \gamma_l$.

Remark 2: For the *decentralized* implementation, it is required that each converter can measure its own inductor current i_{L_k} and DC-link voltage V only.

Proof: See Appendix.

VI. CASE STUDIES: SIMULATIONS AND DISCUSSIONS

In this section, we report some simulation studies that cover different aspects of the proposed distributed control design. All simulations are performed in MATLAB/Simulink using SimPower/SimElectronics library.

For simulations, we consider a parallel network of three boost converters powered by a Li-ion battery and two generic sources (nominal voltages $125V$), respectively. The effectiveness of the proposed control design is well illustrated by considering a challenging practical scenario with (*unknown*) fast time-varying load, large uncertainties in inductance and capacitance values, sensor noises and variation in input source voltages. Specifically, we consider the following simulation parameters:

- Battery State-Of-Charge: $120\%(\sim 135V)$
- Generic Sources: $125V$ and $130V$
- Inductance: $(L_1, L_2, L_3) = (.096, .12, .14)$mH
- Capacitance: $C = 400\mu$F
- Loading Conditions: $5kW \pm (2kW@1Hz)$
- Power Sharing Requirements:
  1) $(0.33 : 0.33 : 0.33), \quad t < 2s$
  2) $(0.5 : 0.2 : 0.3), \quad 2s \le t \le 19.5s$
- Desired Output Voltage: $V_{\text{ref}} = 250V$

To illustrate the robustness of the proposed approach, the nominal (or equivalent single converter) inductance, capacitance and steady-state complementary duty-cycle are chosen as $L = 0.12$mH, $C = 500\mu$F and $D' = V_g/V_{\text{ref}} = 0.5$. The design parameters for the inner-controller K_c are: Damping factors $\zeta_1 = 0.7$, $\zeta_2 = 2.2$, and bandwidth $\tilde{\omega} = 2\pi 300$rad/s.

The outer controllers K_v and K_r are obtained by solving the stacked $\mathcal{H}_\infty$ optimization problem (see Eq. (4)) [8] with the weighting functions:

$$W_1 = \frac{0.4167(s + 452.4)}{(s + 1.885)} \quad W_2 = \frac{0.4167(s + 1056)}{(s + 4.398)}$$
$$W_3 = 0.04 \quad W_4 = \frac{37.037(s + 314.2)}{(s + 3.142 \times 10^4)}$$

Inclusion and characterization of PV module: Photovoltaics are technically treated as *current* sources. In a microgrid setup, a PV module is interfaced with the DC-link through a Boost converter and is controlled using the maximum power point tracking (MPPT) algorithm. The output current of PV i_{PV} is directly proportional to the (time-varying) irradiance and is included in our proposed formulation by regarding i_{PV} as part of the disturbance signal, i.e., the net disturbance current is modeled as $i_{\text{load}} - i_{\text{PV}}$. In this simulation study, we squeeze worth 8 hours of insolation data into a total duration of $19.5s$ amounting to rapidly varying irradiance (and hence the disturbance current i_{PV}).

Results: The controllers derived for the nominal single converter system are then extended for a parallel multi-converter design as described in Sec. V. The initial DC-link voltage is considered at $0V$. Fig. 5 shows the voltage regulation at the DC-link to the reference $V_{\text{ref}} = 250V$ for the centralized (i_{load} measurement available) and decentralized implementations. Note

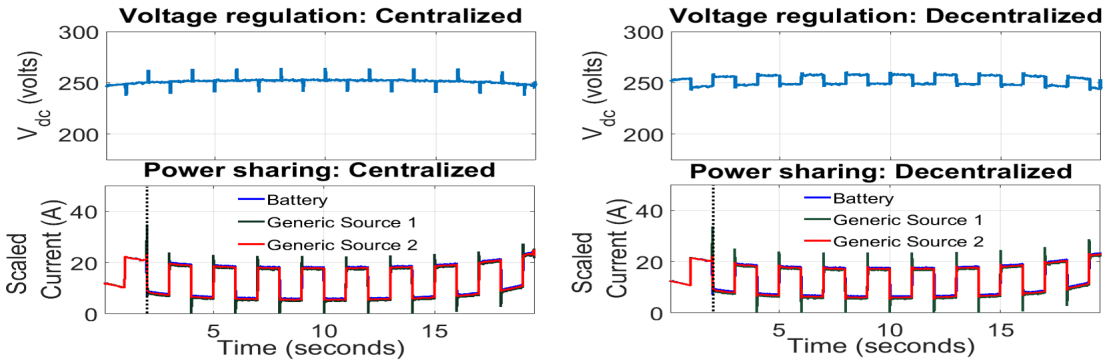

Fig. 5: DC-link voltage regulation and power sharing for centralized and decentralized scenarios.

that the DC-link load changes by $4kW$ every second ($3kW$ to $7kW$, and $7kW$ to $3kW$). The reference current is considered as $i_{\text{ref}} = 5kW/250V = 20A$. While in the centralized case, the voltage is maintained at $V_{\text{ref}} = 250V$ with small periodic spikes attributed to sudden load changes, the decentralized implementation results in controlled voltage droop of $10V$ peak-to-peak around the desired DC-link voltage. In order to demonstrate time-varying power sharing performance, the scaled output currents $D'i_L/\gamma$ are plotted in Fig. 5. Overlapping values of scaled currents depict excellent sharing performance; moreover, the control design achieves step-change in power sharing seamlessly at $t = 2s$.

APPENDIX

Sketch of Proof of Theorem 1: System Equivalence

Proof: The *equivalence* is a direct consequence of cleverly chosen architecture. Note that for the single converter system in Fig. 3 with $\tilde{G}_c(s) = \tilde{G}_{c,nom}(s)$, the error signal e_2 (input to controller K_r) is given by

$$e_2 = i_{\text{ref}} + (\eta - D'\tilde{G}_{c,nom})e_1 - D'\tilde{G}_{c,nom}K_r e_2. \tag{9}$$

For the multi-converter system in Fig. 4, we have $e_1^{(k)} = V_{\text{ref}} - V := e_1$. Let us denote the total error in current mismatch $\sum_{k=1}^{m} e_2^k$ by e_2. Therefore, from Fig. 4,

$$e_2^{(k)} = \gamma_k[i_{\text{ref}} + \eta e_1] - D'\tilde{G}_{c,nom}\left(\frac{1}{m}K_v e_1 + K_r e_2^{(k)}\right)$$

$$\underbrace{\sum_{k=1}^{m} e_2^{(k)}}_{e_2} = \sum_{k=1}^{m}\gamma_k[i_{\text{ref}} + \eta e_1] - D'\tilde{G}_{c,nom}\Big(K_v e_1 - K_r \underbrace{\sum_{k=1}^{m} e_2^{(k)}}_{e_2}\Big).$$

Using the fact that $\sum_{k=1}^{m}\gamma_k = 1$, the above equation reduces to (9). Similarly, the expression for tracking error in voltage $V_{\text{ref}} - V$ is identical for the single and multiple converters case. Moreover for the multi-converter system, the output voltage at the DC-link is given by $V = G_v(-i_{\text{load}} + D'\tilde{G}_{c,nom}(K_v e_1 + K_r e_2))$. Since the expressions for e_1 and e_2 are identical for the single and multiple converters case and are written in terms of the exogenous variables $V_{\text{ref}}, i_{\text{ref}}, i_{\text{load}}$, the corresponding transfer functions from the exogenous variables to the DC-link voltage V are also identical, and hence establishes the required *equivalence*. ■

Sketch of Proof of Theorem 1: Power Sharing

Proof: From (10), the error in current reference for the k^{th}-converter is given by

$$e_2^{(k)} = \left(\frac{\gamma_k}{1 + D'\tilde{G}_{c,nom}K_r}\right) i_{\text{ref}} + \left(\frac{\gamma_k\eta - \frac{D'}{m}\tilde{G}_{c,nom}K_v}{1 + D'\tilde{G}_{c,nom}K_r}\right) e_1. \tag{10}$$

From Fig. 4, the output current $i_k = D'_k i_{L_k}$ of the k^{th} converter is given by

$$i_k = D'\tilde{G}_{c,nom}\left[\frac{1}{m}K_v e_1 + K_r e_2^{(k)}\right]. \tag{11}$$

Thus from (10) and (11), we obtain

$$i_k = D'\tilde{G}_{c,nom}\left[\left(\frac{\gamma_k K_r}{1+D'\tilde{G}_{c,nom}K_r}\right) i_{\text{ref}} + \left(\frac{\frac{1}{m}K_v + \eta\gamma_k K_r}{1+D'\tilde{G}_{c,nom}K_r}\right) e_1\right].$$

Therefore, we have

$$\left|\frac{i_k(j0)}{\gamma_k} - \frac{i_l(j0)}{\gamma_l}\right| \le \left(\eta|\tilde{T}_1(j0)| + \left|\frac{1}{\gamma_k} - \frac{1}{\gamma_l}\right||\tilde{T}_2(j0)|\right)|e_1(j0)|$$

The expressions for the bounds on the tracking error for the two scenarios is directly obtained from (6) and the *system equivalence* described earlier. ■

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