ELETRÔNICA IV

Apostila de Aulas Práticas

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Sumário

1. Introdução

O conteúdo desta apostila consiste das aulas experimentais do curso de Eletrônica IV, ministrado no Departamento de Eletrônica da Escola de Engenharia. Cada capítulo corresponde a um experimento a ser montado e estudado em laboratório. Esses experimentos foram, ao longo dos anos, sendo aprimorados didaticamente, de forma a apresentar ao aluno a constatação experimental dos conceitos básicos, e essenciais, estudados na disciplina teórica. Também são fornecidos todos os manuais dos componentes usados nos experimentos, disponibilizando ao aluno todas as informações necessárias à realização dos projetos.

2. AMPLIFICADOR "PUSH-PULL" COM SAÍDA COMPLEMENTAR

ASSUNTO

Projeto de um amplificador de potência, classe AB, com transistores de saída em simetria complementar.

OBJETIVO

Familiarizar o aluno com as condições de operação e características particulares do circuito.

PROJETO

Fase 1- Projete o circuito da Figura 2-1 obedecendo as seguintes especificações:

1 - Potência C.A. de saída de 1W.

2 - Carga de 8Ω.

3 - Eficiência superior a 40%.

4 - Freqüência de corte inferior menor que 50Hz.

5 - Ganho de tensão o maior possível.

6 - Considerar nos cálculos os transistores: TIP29C, TIP30C, BC547 e BC557 (ou similares).

7 - Ajuste P_1 até obter a tensão DC no ponto A igual a zero.

Medidas:

COMPONENTES CALCULADOS	
R3 =	P =
R4 =	C1 =
R5 =	C2 =

POLARIZAÇÃO		
Teórico	**Simulado**	**Prático**
$V_{Bq\_Q_1}$ =	$V_{Bq\_Q_1}$ =	$V_{Bq\_Q_1}$ =
$V_{Bq\_Q_5}$ =	$V_{Bq\_Q_5}$ =	$V_{Bq\_Q_5}$ =
$V_{Bq\_Q_3}$ =	$V_{Bq\_Q_3}$ =	$V_{Bq\_Q_3}$ =
V_{oq} =	V_{oq} =	V_{oq} =
$I_{Cq\_Q_5}$ =	$I_{Cq\_Q_5}$ =	$I_{Cq\_Q_5}$ =

GANHO DE TENSÃO		
Teórico	**Simulado**	**Prático**

EXCURSÃO DE SINAL MÁXIMA NA SAÍDA (Sem Saturação)		
Teórico	**Simulado**	**Prático**

FREQUÊNCIAS DE CORTE		
Teórico	**Simulado**	**Prático**
Inferior =	Inferior = Superior =	Inferior = Superior =
POTÊNCIA MÁXIMA DE SAÍDA (Sem Saturação)		
Teórico	**Simulado**	**Prático**

Explique a função dos seguintes componentes do circuito: R_1, R_2, D_1, D_2, D_3, D_4, C_2 e C_5

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

Curto-circuitar os pontos B e C, e esboçar a forma de onda de saída

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

Fase 2- Projete o circuito da Figura 2-2 obedecendo as seguintes recomendações:

1 - Conservar os valores dos componentes calculados para o circuito da Figura 2-1, exceto o capacitor C_1.

2 - Identificar o tipo de realimentação empregada.

3 - Calcular R_6 para se obter um ganho de tensão realimentado de 4. Este ganho é necessário para que um sinal de entrada com 1V de amplitude produza potência máxima na saída do amplificador. Esta é uma especificação comum aos amplificadores de potência comerciais.

4 - Recalcular C_1 para manter a freqüência de corte inferior menor que 50Hz.

Medidas:

COMPONENTES CALCULADOS	
R6 =	C1 =

POLARIZAÇÃO		
Teórico	**Simulado**	**Prático**
$V_{Bq\_Q_1} =$	$V_{Bq\_Q_1} =$	$V_{Bq\_Q_1} =$
$V_{Bq\_Q_5} =$	$V_{Bq\_Q_5} =$	$V_{Bq\_Q_5} =$
$V_{Bq\_Q_3} =$	$V_{Bq\_Q_3} =$	$V_{Bq\_Q_3} =$
$V_{oq} =$	$V_{oq} =$	$V_{oq} =$
$I_{Cq\_Q_5} =$	$I_{Cq\_Q_5} =$	$I_{Cq\_Q_5} =$

Identificar o tipo de realimentação empregada

GANHO DE TENSÃO		
Teórico	**Simulado**	**Prático**

EXCURSÃO DE SINAL MÁXIMA NA SAÍDA		
Teórico	**Simulado**	**Prático**

FREQUÊNCIAS DE CORTE		
Teórico	**Simulado**	**Prático**
Inferior =	Inferior = Superior =	Inferior = Superior =

POTÊNCIA MÁXIMA DE SAÍDA		
Teórico	**Simulado**	**Prático**

EFICIÊNCIA COM $V_0=4V_{PP}$		
Teórico	**Simulado**	**Prático**

Curto-circuitar os pontos B e C, e esboçar a forma de onda de saída, comparando com a anterior

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

Fase 3- Projete o circuito da Figura 2-4 obedecendo as seguintes recomendações:

1 - Monte o circuito da Figura 2-3 (a) utilizando um microfone de eletreto e um resistor R_{10}=10kΩ.

2 - Fale ao microfone e observe a amplitude máxima do sinal AC em V_{mic}.

3 - Com a tensão V_{mic}, projete o pré-amplificador da Figura 2-3 (b) de tal forma a se obter uma tensão máxima V_{pre}=1V e freqüência de corte inferior menor que 50Hz. Conecte o pré-amplificador ao amplificador da Fase 2, conforme a Figura 2-4, substitua a carga R_L por um alto-falante de 8Ω e fale ao microfone.

Medidas:

COMPONENTES CALCULADOS		
R7 =	R8 =	C4 =

GANHO DE TENSÃO DO PRÉ-AMPLIFICADOR	
Teórico	**Prático**

FREQUÊNCIAS DE CORTE DO PRÉ-AMPLIFICADOR	
Teórico	**Prático**
Inferior =	Inferior =

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

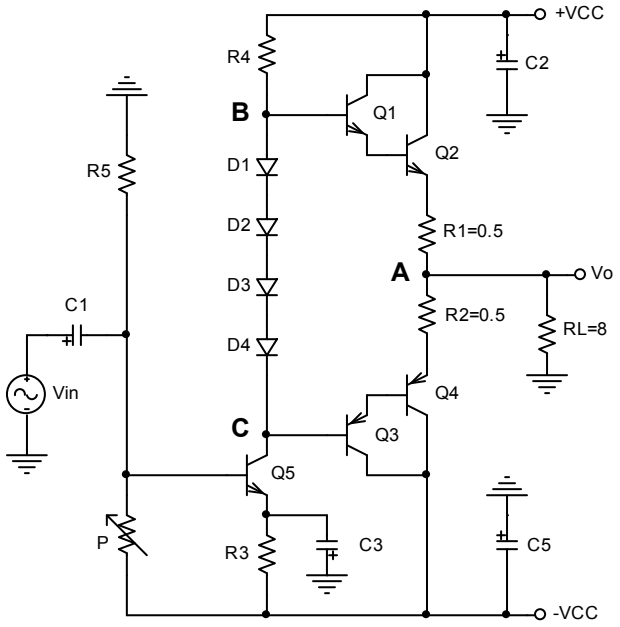


Figura 2-1: Amplificador Push-Pull.

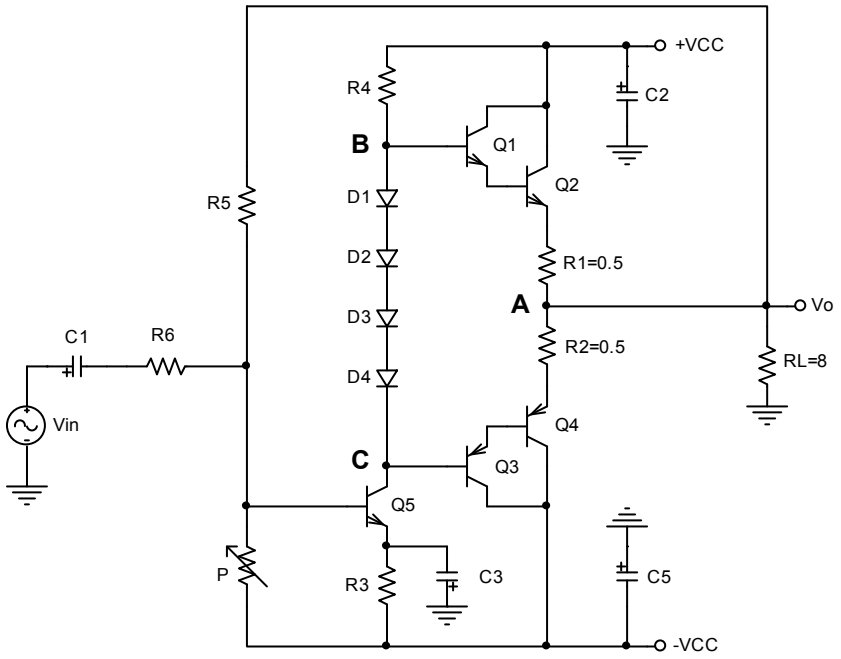
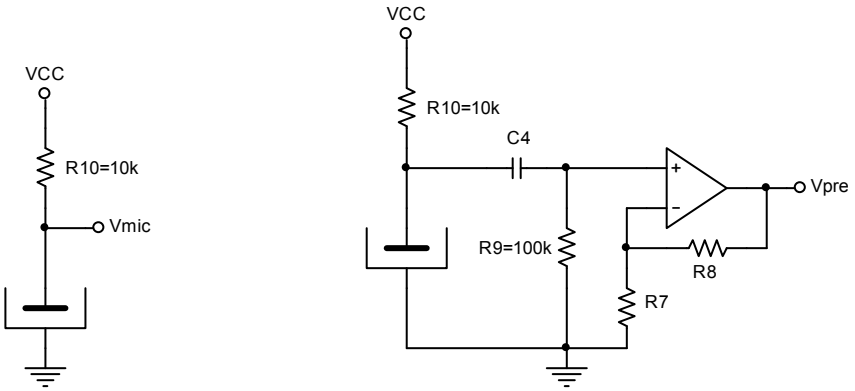


Figura 2-2: Amplificador Push-Pull com realimentação.



(a) (b)

Figura 2-3: Microfone de eletreto. a) Polarização. b) Microfone mais amplificador.

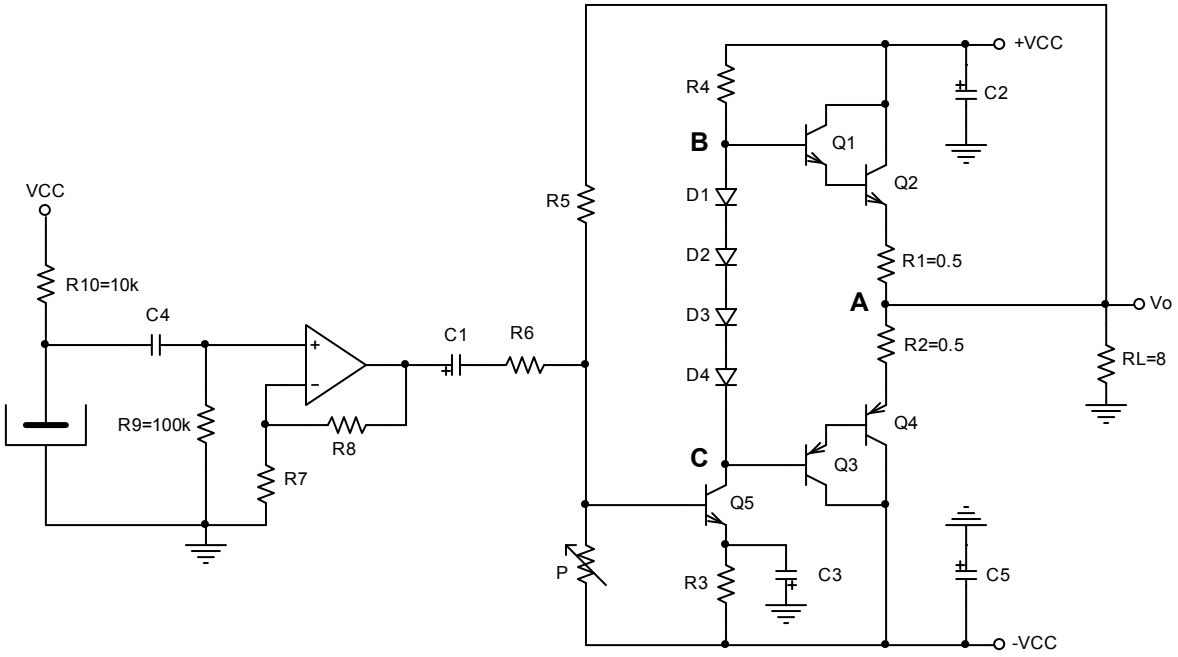
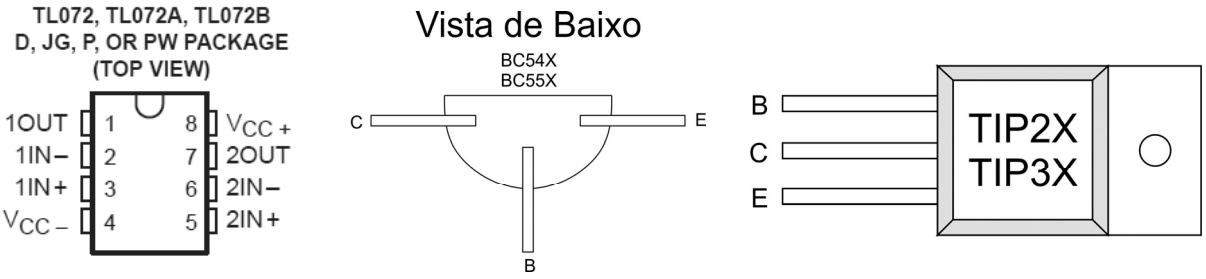


Figura 2-4: Amplificador Push-Pull mais microfone de eletreto.



3. AMPLIFICADOR SINTONIZADO

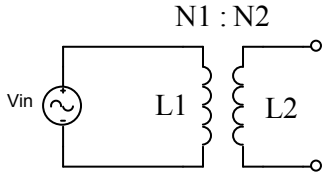
OBJETIVO

Estudo de um amplificador sintonizado e sua aplicação como amplificador seletivo e "mixer".

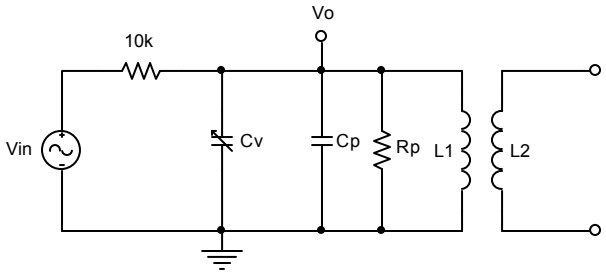
PROJETO

Fase 1- Caracterização da bobina

1 - Medir a relação de espiras N_1/N_2 dos indutores, aplicando um sinal senoidal de 100kHz. Considere $N_1 > N_2$.



2 - Medir os parâmetros do indutor, utilizando o esquema abaixo,



onde:

C_V é uma década capacitiva;

C_p é a capacitância parasita, que inclui a capacitância do osciloscópio, da fiação, residual da década e da própria bobina;

R_p é a resistência parasita em paralelo com a bobina.

3 - Ajuste a freqüência do gerador de sinais em 400kHz. Varie a capacitância da década até que o circuito esteja o mais próximo possível da sintonia, e anote o valor obtido C_{V1}. Faça o ajuste fino da freqüência do gerador, até obter o ponto exato de sintonia, e anote o valor desta freqüência f_1.

4 - Ainda com o circuito sintonizado, meça o ganho de tensão $A = V_o/V_{in}$ e calcule R_p.

$$A = \frac{R_p}{R_p + 10k} \quad \rightarrow \quad R_p = \left(\frac{A}{1-A}\right)10k$$

5 - Ajuste a freqüência do gerador de sinais em 300kHz. Varie a capacitância da década até que o circuito esteja o mais próximo possível da sintonia, e anote o valor obtido C_{V2}. Faça o ajuste fino da freqüência do gerador, até obter o ponto exato de sintonia, e anote o valor desta freqüência f_2.

6 - Calcule L_1 e C_p através do sistema de equações:

$$\begin{cases} f_1 = \dfrac{1}{2\pi\sqrt{L_1\left(C_p + C_{V1}\right)}} \\ f_2 = \dfrac{1}{2\pi\sqrt{L_1\left(C_p + C_{V2}\right)}} \end{cases} \rightarrow \begin{cases} L_1 = \dfrac{f_1^2 - f_2^2}{4\pi^2 f_1^2 f_2^2 \left(C_{V2} - C_{V1}\right)} \\ C_p = \dfrac{C_{V2} f_2^2 - C_{V1} f_1^2}{f_1^2 - f_2^2} \end{cases}$$

7 - Calcule o fator de qualidade do indutor na freqüência f_1.

$$Q_b = \frac{R_p}{2\pi f_1 L_1}$$

PARÂMETROS DO INDUTOR				
L_1 =	R_p =	C_p =	Q_b=	N_1/N_2=

Fase 1- Projetar um amplificador sintonizado, tomando por base, a Figura 3-1, com as seguintes características:

1 - $V_{CC} = 12V$;

2 - Frequência de sintonia $f_0 = 400kHz$;

3 - Ganho de tensão na frequência de sintonia $\left|A\left(j2\pi f_0\right)\right| = 20$;

4 - Seletividade igual a 10.

5 - Considere fator de qualidade igual a 60 para os capacitores de poliéster metalizado.

COMPONENTES CALCULADOS	
R1 = R2 = R3 = RL=	C1 = C2 = C3=

POLARIZAÇÃO		
Teórico	**Simulado**	**Prático**
V_{Bq} = V_{Eq} = I_{Cq} =	V_{Bq} = V_{Eq} = I_{Cq} =	V_{Bq} = V_{Eq} = I_{Cq} =

FREQUÊNCIA DE SINTONIA		
Teórico	**Simulado**	**Prático**

SELETIVIDADE DO CIRCUITO		
Teórico	**Simulado**	**Prático**

GANHO DE TENSÃO NA FREQUÊNCIA DE SINTONIA		
Teórico	**Simulado**	**Prático**

DIGA O QUE DEVE SER OBSERVADO NA SAÍDA, QUANDO O SINAL DE ENTRADA FOR:			
	Teórico	**Simulado**	**Prático**
senoidal de 400kHz			
senoidal de 200kHz			
senoidal de 133kHz			
senoidal de 800kHz			
quadrado de 400kHz			
quadrado de 200kHz			
quadrado de 133kHz			
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS			

Fase 2- Montar um "mixer", modificando o circuito conforme a Figura 3-2

O objetivo deste experimento é mostrar o efeito do batimento de frequências, muito utilizado nos receptores de rádio. Quando dois sinais senoidais, de frequências f_1 e f_2, são aplicados à base do transistor, e com amplitudes suficientemente elevadas para forçar a operação na região não linear, a

corrente de coletor é o somatório de várias senóides com frequências $f_1 - f_2$ e $\sum_{n=0,\, m=0}^{\infty} \left(nf_1 + mf_2\right)$. Caso uma destas frequências coincida com a sintonia do filtro, esta será amplificada e visível na saída, enquanto as outras serão fortemente atenuadas. Para obter este efeito, desligue o gerador G_2, ajuste a frequência de G_1 em 800kHz e a amplitude para que, no ponto A, exista uma senóide com $1V_{pico}$. Desligue o gerador G_1, ajuste a frequência de G_2 em $800\text{kHz} + f_1$ (f_1 sendo a sintonia medida para filtro) e a amplitude para que, no ponto A, exista uma senóide com $1V_{pico}$. Ligue os dois geradores e observe o sinal de saída.

FREQUÊNCIA DO SINAL DE SAÍDA	
Teórico	**Prático**
$f =$	$f =$

ESBOCE A FORMA DE ONDA OBSERVADA NA SAÍDA

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

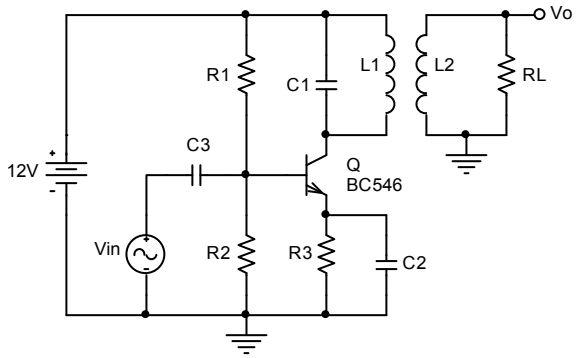


Figura 3-1: Amplificador sintonizado.

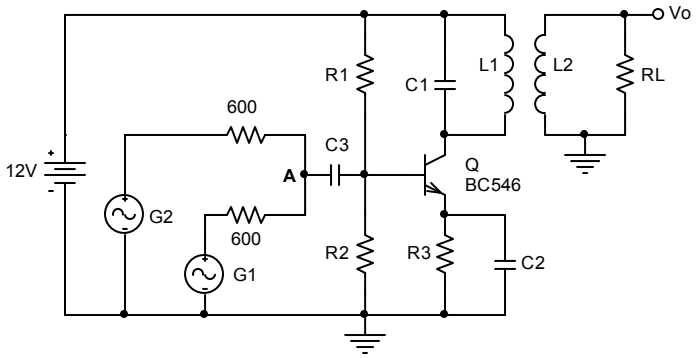


Figura 3-2: Amplificador sintonizado como “mixer”.

4. MODULADOR DE AMPLITUDE

OBJETIVO

Estudo de um circuito Modulador de Amplitude (AM), e um demodulador AM por detecção de pico de envoltória.

PROJETO

Fase1 - Projeto do modulador

Utilizando o mesmo indutor acoplado da experiência anterior, dimensione o modulador AM de alto nível da Figura 2-1, de forma a atender as especificações abaixo:

1 - Frequência da portadora igual a 400kHz;

2 - Frequência de corte inferior, para o sinal modulador, de 50Hz;

3 - Frequência de corte superior, para o sinal modulador, de 5kHz;

4 - Máxima excursão de sinal do oscilador, para qualquer nível de sinal de modulação;

5 - Tensão e polarização no emissor de Q_2 igual a 1V;

6 - Carga $R_L = 1k\Omega$.

7 - Considere fator de qualidade igual a 60 para os capacitores de poliéster metalizado.

8 - Calcular C_3 para frequência de corte de 100kHz.

PARÂMETROS DO INDUTOR				
L_1 =	R_p =	C_p =	Q_b=	N_1/N_2=

COMPONENTES CALCULADOS	
R1 = R2 = R3 = R4= RL=	C1 = C2 = C3= C4=

POLARIZAÇÃO		
Teórico	**Simulado**	**Prático**
V_{Bq1} =	V_{Bq1} =	V_{Bq1} =
V_{Eq1} =	V_{Eq1} =	V_{Eq1} =
V_{Bq2} =	V_{Bq2} =	V_{Bq2} =
V_{Eq2} =	V_{Eq2} =	V_{Eq2} =
I_{Cq2} =	I_{Cq2} =	I_{Cq2} =

FREQUÊNCIA DE OSCILAÇÃO		
Teórico	**Simulado**	**Prático**

Máximo Índice de Modulação sem Distorção, para um Sinal Modulador Senoidal de 50Hz	
Teórico	**Prático**

Máximo Índice de Modulação sem Distorção, para um Sinal Modulador Senoidal de 500Hz	
Teórico	**Prático**

Máximo Índice de Modulação sem Distorção, para um Sinal Modulador Senoidal de 5000Hz	
Teórico	**Prático**

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

Fase2 - Projeto do demodulador AM por detecção de pico de envoltória

Troque a carga do modulador por um detector de pico de envoltória, conforme a Figura 4-2. Calcule C_L e recalcule R_L para que o demodulador funcione adequadamente dentro da faixa de frequências especificada para o sinal modulador.

COMPONENTES CALCULADOS	
RL =	CL =
Resposta em frequência do Demodulador (pontos de queda de 3dB)	
Prático	
f_{CI}= f_{CS}=	
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS	

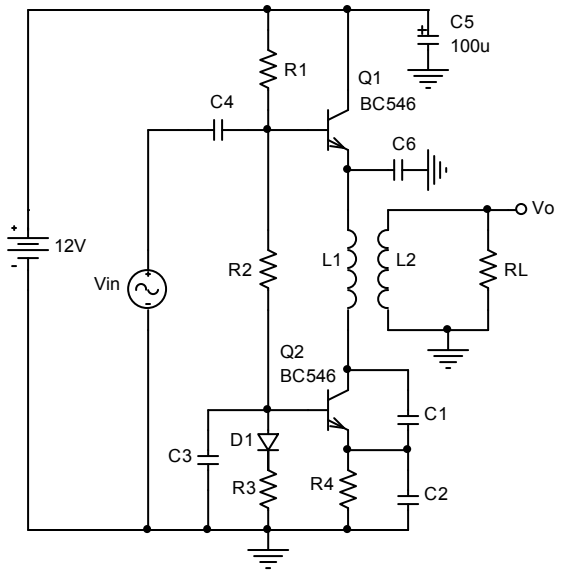


Figura 4-1: Modulador de amplitude.

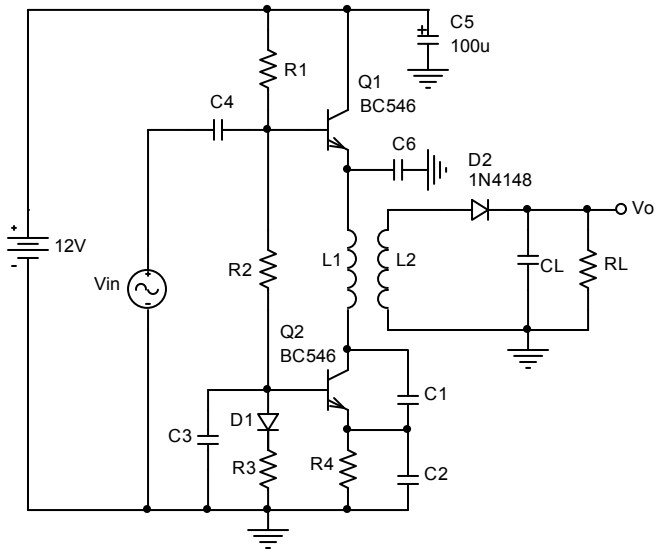


Figura 4-2: Modulador AM com detector de pico de envoltória.

5. MULTIPLICADORES ANALÓGICOS

OBJETIVO

Familiarizar o aluno quanto às técnicas de multiplicação de sinais analógicos variantes no tempo e sua aplicação como moduladores em amplitude com e sem portadora, detectores síncronos, detectores de fase, dobradores de frequência, etc.

INTRODUÇÃO

Durante muito tempo a multiplicação analógica foi conseguida através de várias técnicas como:

- método do quadrado da soma usando dispositivos não lineares que apresentem características quadráticas, predominantes ou não, como FET's, diodos ou transistores de junção, seguidos de filtros passa-faixa.
- método do quadrado da soma balanceada, usando os mesmos dispositivos anteriores, mas em circuitos onde a portadora é suprimida (mais de 40dB) ou reduzida (mais de 20dB). Em baixas frequências pode-se simular um dispositivo com características quadráticas com operacionais e redes de realimentação providas de resistores e diodos em série. Para cada tensão de entrada o ganho será diferente e a aproximação por partes poderá ser quadrática.
- método da modulação por largura de pulsos.
- método dos amplificadores logarítmicos.
- método dos amplificadores de transcondutância variável.

A presente prática será sobre os moduladores balanceados de transcondutância variável e com os coletores dos diferenciais cruzados, conhecidos como células de *Gilbert*. Estas células são comuns a vários integrados como multiplicadores de quatro quadrantes, moduladores, etc.

PROJETO

Fase 1 - Projeto do modulador

Montar um circuito modulador em amplitude da Figura 5-1, que possa funcionar como AM DSB e AM DSB SC numa frequência de portadora $\omega_c = 2\pi \times 100 \times 10^3\ rad/s$ e frequência da moduladora $\omega_m = 2\pi f_m$, f_m variando de 100Hz a 3kHz. Utilize o modelo da Figura 5-2 para realizar as simulações.

COMPONENTES CALCULADOS		
C1=	C2=	C3=

POLARIZAÇÃO (com o potenciômetro a meio curso)					
Teórico		**Simulado**		**Prático**	
V_1=	V_8=	V_1=	V_8=	V_1=	V_8=
V_2=	V_{10}=	V_2=	V_{10}=	V_2=	V_{10}=
V_3=	V_{12}=	V_3=	V_{12}=	V_3=	V_{12}=
V_4=	V_5=	V_4=	V_5=	V_4=	V_5=
V_6=		V_6=		V_6=	

Utilize como portadora uma onda senoidal de 100kHz com 500mV de amplitude, e uma senóide de 1kHz e 200mV de amplitude para a moduladora. Ajuste o potenciômetro para que o sinal observado em V_{o+} ou V_{o-} esteja modulado em amplitude e com portadora suprimida.

ESBOCE O SINAL OBSERVADO EM V_{o+} ou V_{o-}	
Simulado	**Prático**

Varie o potenciômetro e observe a modulação mudar gradativamente de portadora suprimida para com portadora.

ESBOCE O SINAL OBSERVADO EM V_{o+} ou V_{o-}, COM ÍNDICE DE MODULAÇÃO	
Igual a 100%	**Igual a 50%**

Ajuste o potenciômetro para obter índice de modulação de 100%. Varie a frequência do sinal modulador e, observando a forma do sinal de saída, determine a frequência de corte inferior do modulador.

FREQUÊNCIA DE CORTE INFERIOR DO MODULADOR	
Teórico	**Prático**
f_{CI} =	f_{CI} =
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS	

Fase 2 - Duplicador de frequência

O modulador balanceado pode ser usado, quando o sinal de entrada é senoidal, como duplicador, ou oitavador, de frequência. Para isto, basta aplicar V_{in} simultaneamente às entradas portadora e moduladora. Desta forma, o sinal observado nas saídas V_{o+} ou V_{o-} é proporcional a V_{in}^2, e pode ser representado como:

$$V_{in}^2(t) = V_m \sin(\omega_0 t)^2 = V_m^2 \left(1 - \cos(2\omega_0 t)\right)/2$$

Ajuste o potenciômetro para que não exista portadora nas saídas V_{o+} e V_{o-}, e aplique um sinal senoidal com 1kHz e 50mV de amplitude às entradas portadora e moduladora.

ESBOCE O SINAL OBSERVADO EM V_{o+} ou V_{o-}, E ANOTE A FREQUÊNCIA MEDIDA		
Teórico	**Simulado**	**Prático**
f =	f =	f =
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS		

Fase 3 - Detector de fase

O modulador balanceado pode ser usado como detector de fase, entre dois sinais de mesma frequência, conforme a Figura 5-3. A tensão $V_o(t)$ é o produto $V_1(t) \times V_2(t)$, e considerando estas tensões senoidais, tem-se:

$$V_o(t) = V_1 \sin(\omega_0 t) \times V_2 \sin(\omega_0 t + \theta) = V_1 V_2 \cos(\theta)/2 - V_1 V_2 \cos(2\omega_0 t + \theta)/2$$

Calculando R e C para que formem um filtro passa-baixas, com frequência de corte suficientemente pequena para eliminar a componente $V_1 V_2 \cos(2\omega_0 t + \theta)/2$, obtém-se:

$$V_o(t) \cong V_1 V_2 \cos(\theta)/2$$

O circuito da Figura 5-4 utiliza um filtro passa-tudo para criar dois sinais defasados, $V_1(t)$ e $V_2(t)$, onde $\measuredangle V_2(j\omega_o) - \measuredangle V_1(j\omega_o) = -2\tan^{-1}(\omega_o PC)$. Monte o circuito, e calcule os capacitores C para a frequência de corte de 500Hz na saída. Aplique um sinal $V_{in}(t)$ senoidal de 1kHz, com amplitude de 50mV. Ajuste o potenciômetro do defasador de forma que os sinais $V_1(t)$ e $V_2(t)$ estejam defasados de 90°. Em

seguida, ajuste o potenciômetro de injeção de portadora para que a tensão entre as saídas V_{o+} e V_{o-}, <u>medidas com o multímetro</u>, seja igual a zero. Este procedimento calibra o detector de fase. Varie o potenciômetro P, faça a gráfico $V_{o+ ou -} \times \theta$ e compare com a curva teórica.

ESBOCE O GRÁFICO $V_{o+ ou -} \times \theta$
COMPARE COM A CURVA TEÓRICA E COMENTE

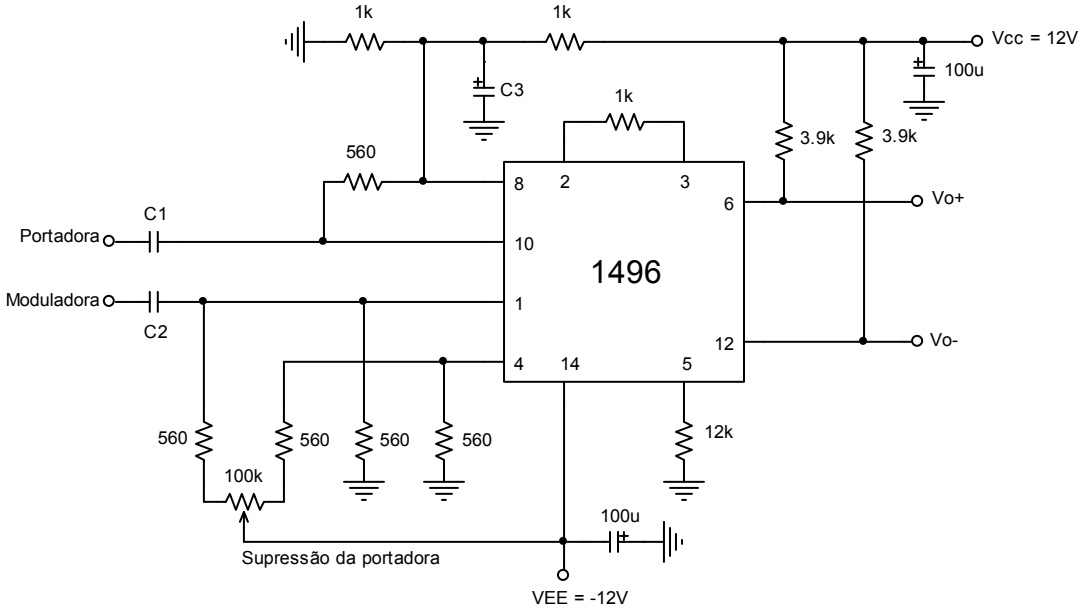


Figura 5-1: Modulador balanceado.

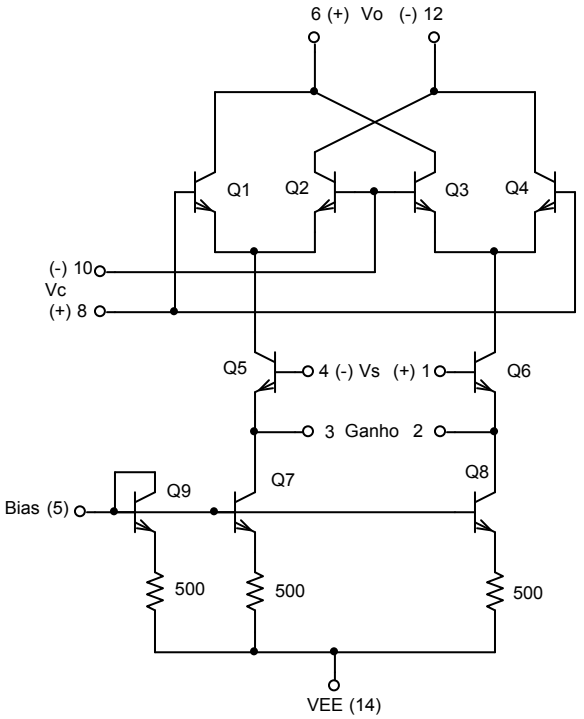


Figura 5-2: Modelo da célula de *Gilbert* para simulação.

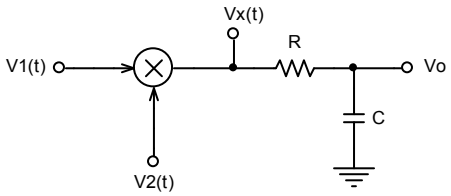


Figura 5-3: Detector de fase.

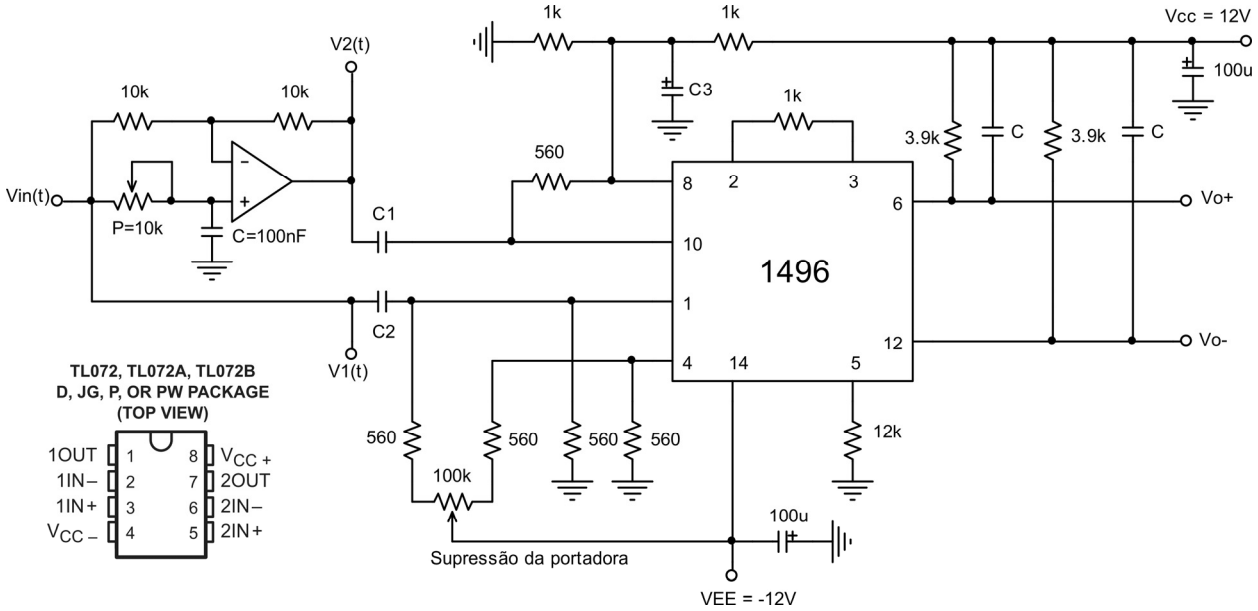


Figura 5-4: Implementação do detector de fase.

6. MODULADOR DE FM

OBJETIVO

Estudo de um circuito Modulador de Frequência (FM), e determinação do desvio de frequência pelo método do apagamento de portadora.

PROJETO

Fase 1 - Projeto do modulador

Projetar o circuito modulador de FM da Figura 6-1, para operar com frequência de portadora igual a 20MHz. O nível DC da tensão V_a deve ser igual a 6V e a função de transferência $H(s) = V_a / V_{in}$ deve possuir frequência de corte inferior igual a 50Hz e superior igual a 100kHz. O indutor deve ser construído com fio rígido esmaltado de 0.5mm de diâmetro, enrolado em uma fôrma de 1cm de diâmetro e 1cm de comprimento. Para o dimensionamento do indutor, utilize a fórmula abaixo:

$$L = \frac{0.394 r^2 N^2}{9r + 10h}$$

onde
L - é a indutância em μH.
r - é o raio da bobina em cm.
N - é o número de espiras.
h - é o comprimento da bobina em cm.

COMPONENTES CALCULADOS		
C1=	C2=	C3=
R1=	R2=	R3=

Fase 2 - Medida da constante k_O do VCO

No modulador de FM, a frequência é definida pela expressão $\omega(t) = \omega_0 + 2\pi \cdot \Delta f \cdot f(t)$, onde Δf é o desvio de frequência e $f(t)$ é o sinal modulador. Na sua forma canônica, o sinal modulador possui as seguintes características: $\max|f(t)| = 1$ e $\overline{f(t)} = 0$. Portanto, na saída do modulador de FM devemos ter $v_o(t) = A_C \cos\left(\omega_0 t + 2\pi \cdot \Delta f \cdot \int_t f(\tau) d\tau\right)$. No circuito real, a tensão de saída é dada por $v_o(t) = A_C \cos\left(\omega_0 t + 2\pi \cdot k_O \cdot \int_t v_{in}(\tau) d\tau\right)$ Ao aplicarmos $v_{in}(t) = V_m \cos(2\pi \cdot f_m \cdot t)$, obtemos $v_o(t) = A_C \cos(\omega_0 t + 2\pi \cdot V_m k_O / f_m \cdot \sin(2\pi \cdot f_m \cdot t))$, onde o termo $V_m k_O$ é o desvio de frequência Δf, e $V_m k_O / f_m$ é o índice de modulação β. Quando $\beta = 2.4$, obtemos o primeiro apagamento de portadora, e esta propriedade é muito utilizada para determinação do desvio de frequência dos moduladores de FM.

Faça $v_{in}(t) = 0$ e, com o auxilio do analisador de espectro, meça a frequência da portadora do modulador.

FREQUÊNCIA DA PORTADORA		
Teórico	**Simulado**	**Prático**
f_0=	f_0=	f_0=
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS		

Ajuste o gerador de sinais para a frequência de 25kHz, aumente gradativamente a amplitude de $v_{in}(t)$ e observe o aparecimento das raias laterais. Meça o espaçamento entre as raias.

ESPAÇAMENTO ENTRE AS RAIAS	
Teórico	**Prático**
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS	

Continue aumentando a amplitude de $v_{in}(t)$ até obter o primeiro apagamento de portadora, e calcule a constante k_O do VCO.

DESVIO DE FREQUÊNCIA
k_O=
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

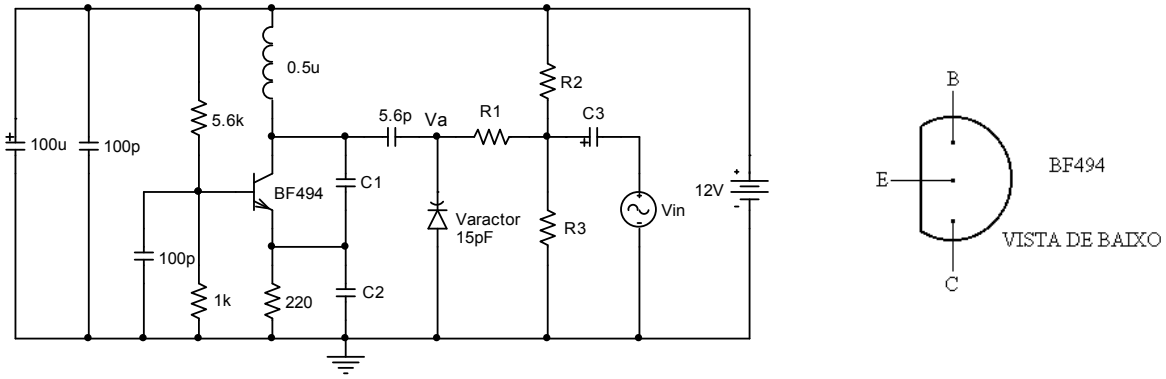


Figura 6-1: Circuito modulador de FM.

7. FONTES CHAVEADAS

OBJETIVO

Projetar e verificar o funcionamento dos conversores BOOST, BUCK-BOOST e BUCK.

PRÁTICA

a) Conversor Boost

O circuito da Figura 7-1 é um conversor Boost operando no modo descontínuo. Dimensione R_S e C_S de forma a obter V_S=20V com α=0.5 e uma variação máxima de 0.1V. A tensão V_{CC} deve ser ajustada em 5V, e V_p conforme a Figura 7-2. Assuma uma frequência de chaveamento de 20kHZ.

Equações de projeto:

Tempo de carregamento do indutor L, $T_C=\alpha T$, $0\leq\alpha\leq 0.5$.

Tempo de descarregamento do indutor L, $T_D=\alpha_1 T$, $0\leq\alpha_1\leq(1-\alpha)$.

Tensão de saída $V_S=(V_{CC}-V_T)\alpha/\alpha_1-V_D+V_{CC}$, onde V_T e V_D são as tensões de condução do transistor e diodo D_1 respectivamente.

Corrente média na carga $I_S=(V_{CC}-V_T)\alpha\alpha_1 T/2L$.

Corrente máxima acumulada no indutor L, $I_{L\max}=\alpha(V_{CC}-V_T)T/L$.

Capacitor em função da máxima variação de tensão na saída, $C_S=I_S(2-\alpha_1)^2 T/4\Delta V_S$.

Medidas:

TENSÃO DE SAÍDA V_S, COM O RESISTOR DE 100Ω EM CURTO-CIRCUITO		
Teórico	**Simulado**	**Prático**
V_S =	V_S =	V_S =
TENSÃO DE RIPPLE ΔV_S, COM O RESISTOR DE 100Ω EM CURTO-CIRCUITO		
Teórico	**Simulado**	**Prático**
ΔV_S =	ΔV_S =	ΔV_S =
Esboce a corrente de carga e descarga do indutor, observando a tensão no ponto A. $V_A=V_{CC}-10I$.		
Teórico	**Simulado**	**Prático**

Varie α de 0.2 a 0.5, e plote um gráfico de V_S em função de α.	
Simulado	**Prático**
COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS	

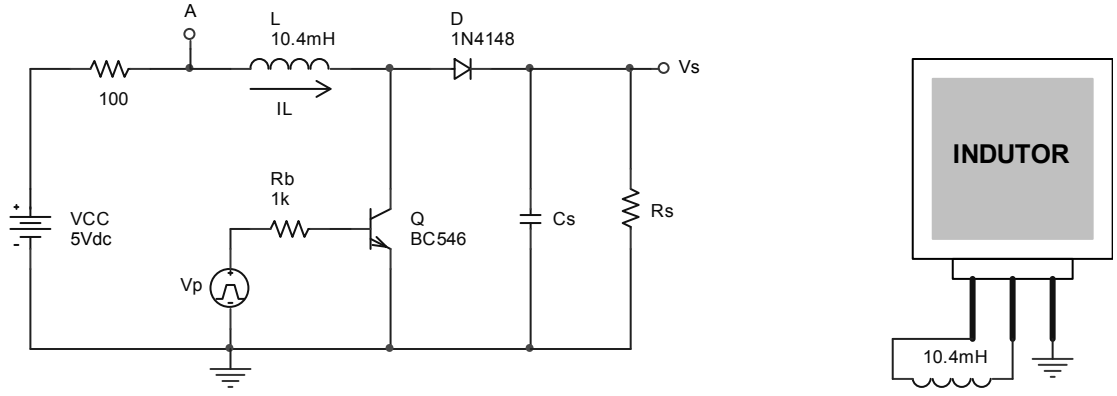


Figura 7-1: Conversor BOOST.

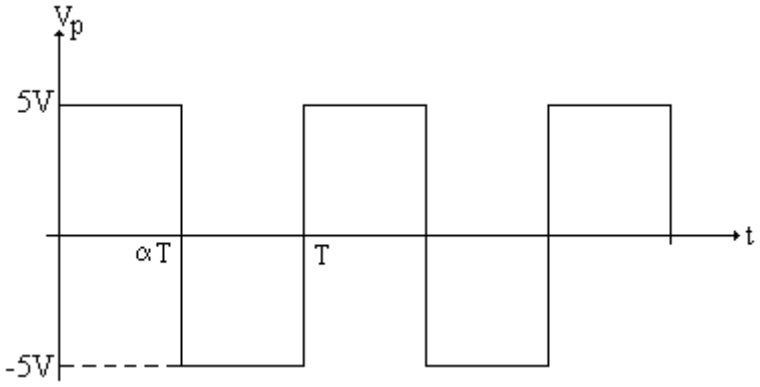


Figura 7-2: Fonte de excitação do conversor Boost.

b) Conversor Buck-Boost

O circuito da Figura 7-3 é um conversor Buck-Boost operando no modo descontínuo. Dimensione R_S e C_S de forma a obter V_S=-20V com α=0.5 e uma variação máxima de 0.1V. A tensão V_{CC} deve ser ajustada em 5V, e V_p conforme a Figura 7-4. Assuma uma frequência de chaveamento de 20kHZ.

Equações de projeto:

Tempo de carregamento do indutor L, $T_C=\alpha T$, $0\leq\alpha\leq 0.5$.
Tempo de descarregamento do indutor L, $T_D=\alpha_1 T$, $0\leq\alpha_1\leq(1-\alpha)$.
Tensão de saída $V_S = -\left(V_{CC} - V_T\right)\alpha / \alpha_1 + V_D$, onde V_T e V_D são as tensões de condução do transistor e diodo D respectivamente.
$I_S = \left(\alpha^2 \left(V_{CC} - V_T\right)^2 T\right) / \left(2\left(V_D - V_S\right)L\right)$, onde I_S é a corrente DC na carga R_S, e T o período de chaveamento.
Corrente máxima acumulada no indutor L, $I_{L\max} = \alpha\left(V_{CC} - V_T\right)T / L$.
Capacitor em função da máxima variação de tensão na saída, $C_S = I_S \left(2 - \alpha_1\right)^2 T / 4\Delta V_S$.

Medidas:

TENSÃO DE SAÍDA V_S, COM O RESISTOR DE 100Ω EM CURTO-CIRCUITO		
Teórico	**Simulado**	**Prático**
V_S =	V_S =	V_S =
TENSÃO DE RIPPLE ΔV_S, COM O RESISTOR DE 100Ω EM CURTO-CIRCUITO		
Teórico	**Simulado**	**Prático**
ΔV_S =	ΔV_S =	ΔV_S =
Esboce a corrente de carga e descarga do indutor, observando a tensão no ponto A. $V_A = 10I$.		
Teórico	**Simulado**	**Prático**

Varie α de 0.2 a 0.5, e plote um gráfico de V_S em função de α.	
Simulado	**Prático**

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

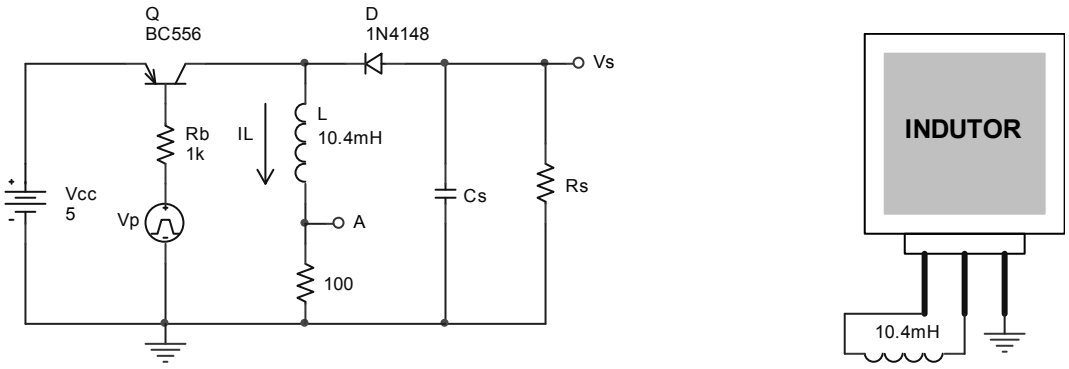


Figura 7-3: Conversor Buck-Boost.

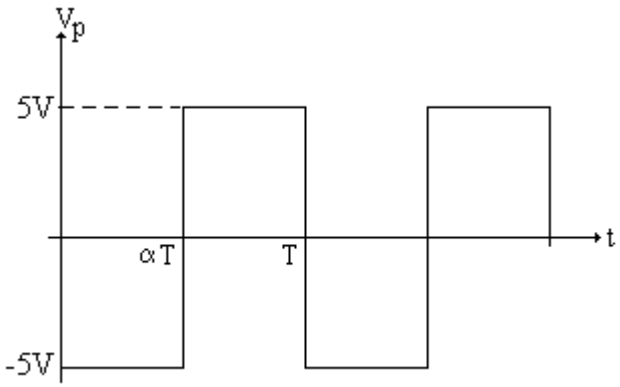


Figura 7-4: Fonte de excitação do conversor Buck-Boost.

c) Conversor Buck

O circuito da Figura 7-5 é um conversor Buck. Calcule α e dimensione R_S e C_S de forma a obter V_S=5V com uma atenuação mínima do filtro LC igual a 0.01 na frequência de chaveamento. A tensão V_{CC} deve ser ajustada em 10V, e V_p conforme a Figura 7-6. Assuma uma frequência de chaveamento de 20kHZ. Considere também a possibilidade α poder variar de um valor mínimo de 0.2 a um máximo de 0.8.

Equações de projeto:

Tempo de carregamento do indutor L, $T_C=\alpha T$, $0.2 \le \alpha \le 1$.

Tensão de saída $V_S = (V_{CC} - V_T)\alpha - V_D(1-\alpha)$, onde V_T e V_D são as tensões de condução do transistor e diodo D respectivamente.

Capacitor $C_S = T^2 / (4\pi^2 AL)$, onde A é a atenuação do filtro LC na frequência de chaveamento, T é o período de chaveamento.

A corrente mínima na carga I_{Smin} que garante a corrente I_L no indutor maior que zero, com α mínimo é $I_{S\min} = (V_{CC} + V_D - V_T)\alpha_{\min}(1-\alpha_{\min})T/2L$.

O resistor máximo admissível é $R_{S\max} = V_{S\min} / I_{S\min}$.

Medidas:

TENSÃO DE SAÍDA V_S, COM α CALCULADO		
Teórico	**Simulado**	**Prático**
V_S =	V_S =	V_S =
ATENUAÇÃO A DO FILTRO LC, COM α CALCULADO		
Teórico	**Simulado**	**Prático**
ΔV_S =	ΔV_S =	ΔV_S =
Varie α de 0.2 a 0.8, e plote um gráfico de V_S em função de α.		
Teórico	**Simulado**	**Prático**

COMENTÁRIOS SOBRE OS RESULTADOS OBTIDOS

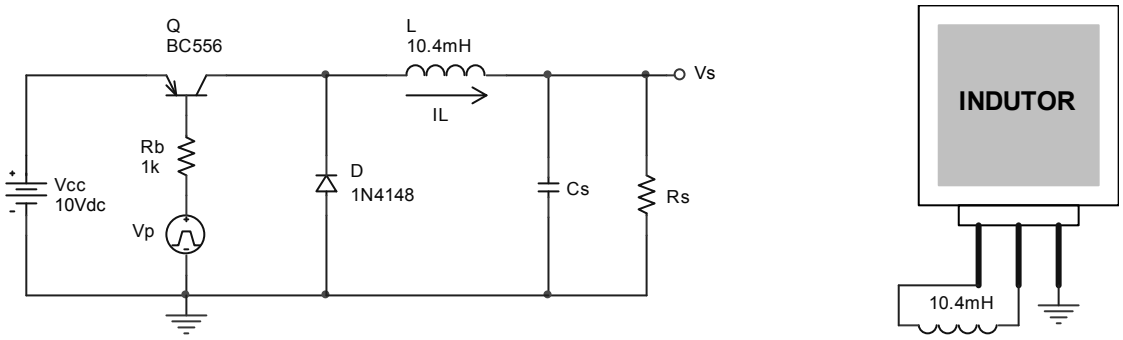


Figura 7-5: Conversor Buck.

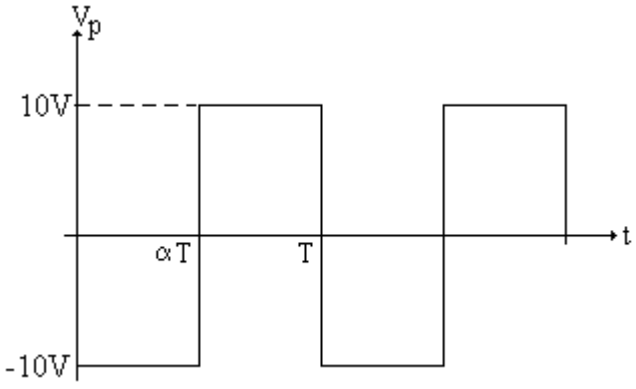


Figura 7-6: Fonte de excitação do conversor Buck.

DATASHEETS

High-speed diodes 1N4148; 1N4448

FEATURES

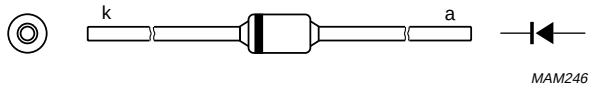
- Hermetically sealed leaded glass SOD27 (DO-35) package
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 75 V
- Repetitive peak reverse voltage: max. 75 V
- Repetitive peak forward current: max. 450 mA.

APPLICATIONS

- High-speed switching.

DESCRIPTION

The 1N4148 and 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.



The diodes are type branded.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	75	V
V_R	continuous reverse voltage		–	75	V
I_F	continuous forward current	see Fig.2; note 1	–	200	mA
I_{FRM}	repetitive peak forward current		–	450	mA
I_{FSM}	non-repetitive peak forward current	square wave; T_j = 25 °C prior to surge; see Fig.4			
		t = 1 μs	–	4	A
		t = 1 ms	–	1	A
		t = 1 s	–	0.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C

Note

1. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	see Fig.3			
	1N4148	I_F = 10 mA	–	1	V
	1N4448	I_F = 5 mA	0.62	0.72	V
		I_F = 100 mA	–	1	V
I_R	reverse current	V_R = 20 V; see Fig.5		25	nA
		V_R = 20 V; T_j = 150 °C; see Fig.5	–	50	µA
I_R	reverse current; 1N4448	V_R = 20 V; T_j = 100 °C; see Fig.5	–	3	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0; see Fig.6		4	pF
t_{rr}	reverse recovery time	when switched from I_F = 10 mA to I_R = 60 mA; R_L = 100 Ω; measured at I_R = 1 mA; see Fig.7		4	ns
V_{fr}	forward recovery voltage	when switched from I_F = 50 mA; t_r = 20 ns; see Fig.8	–	2.5	V

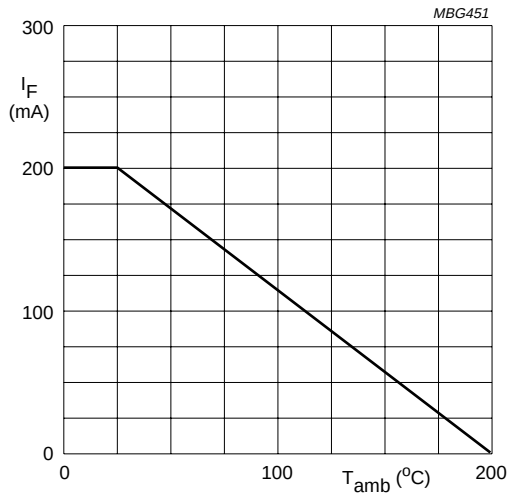
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point	lead length 10 mm	240	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	lead length 10 mm; note 1	350	K/W

Note

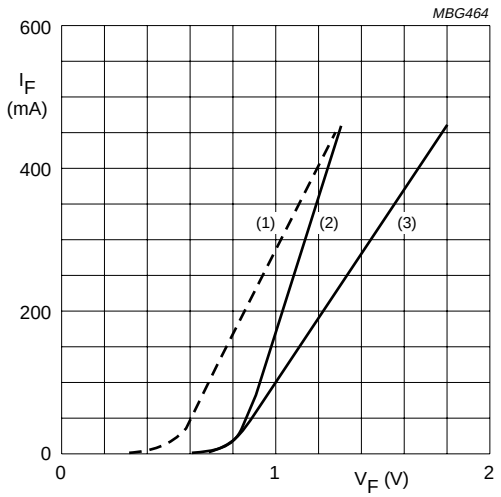
1. Device mounted on a printed circuit-board without metallization pad.

GRAPHICAL DATA



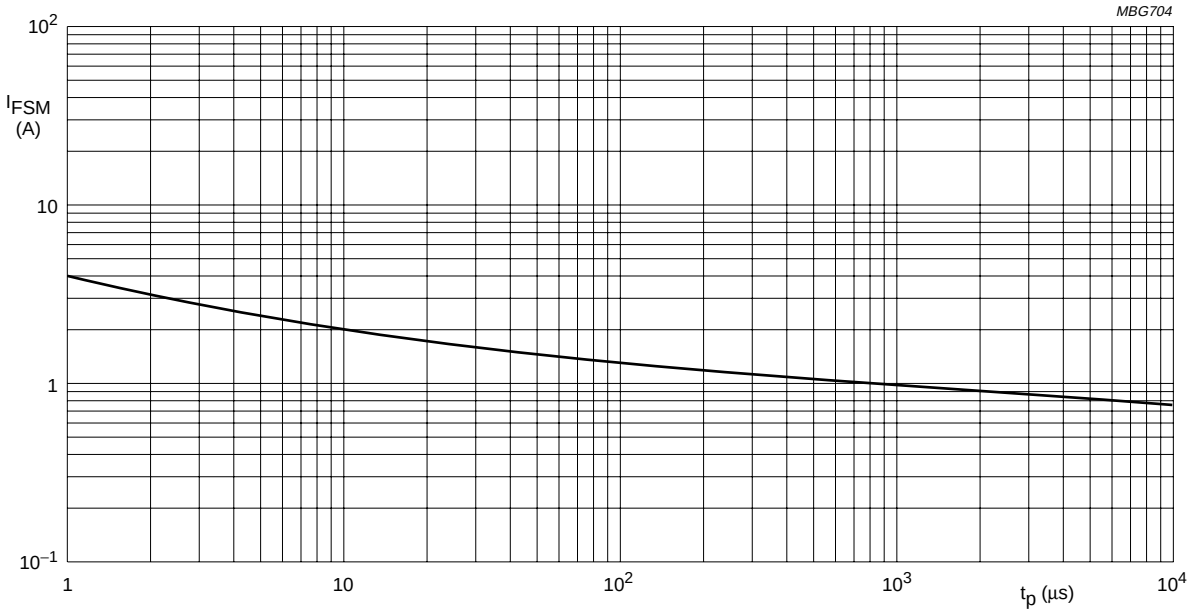
Device mounted on an FR4 printed-circuit board; lead length 10 mm.

Fig.2 Maximum permissible continuous forward current as a function of ambient temperature.



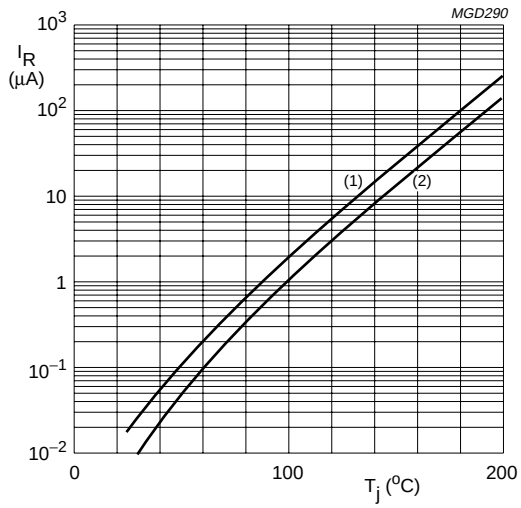
(1) T_j = 175 °C; typical values.
(2) T_j = 25 °C; typical values.
(3) T_j = 25 °C; maximum values.

Fig.3 Forward current as a function of forward voltage.



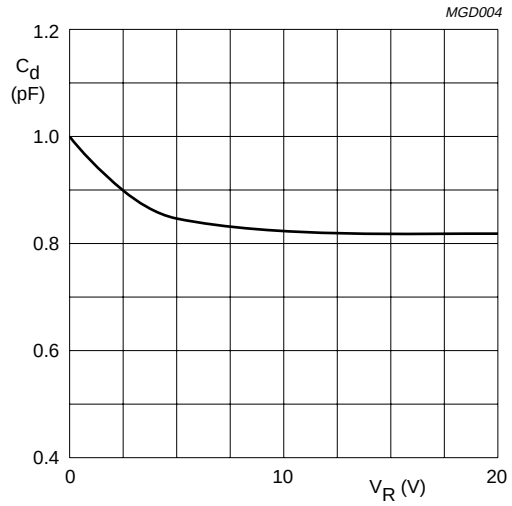
Based on square wave currents.
T_j = 25 °C prior to surge.

Fig.4 Maximum permissible non-repetitive peak forward current as a function of pulse duration.



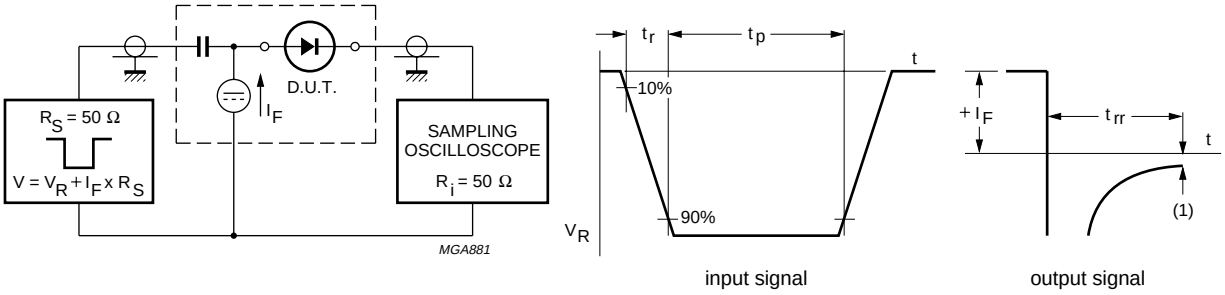
(1) V_R = 75 V; typical values.
(2) V_R = 20 V; typical values.

Fig.5 Reverse current as a function of junction temperature.



f = 1 MHz; T_j = 25 °C.

Fig.6 Diode capacitance as a function of reverse voltage; typical values.



(1) I_R = 1 mA.

Fig.7 Reverse recovery voltage test circuit and waveforms.

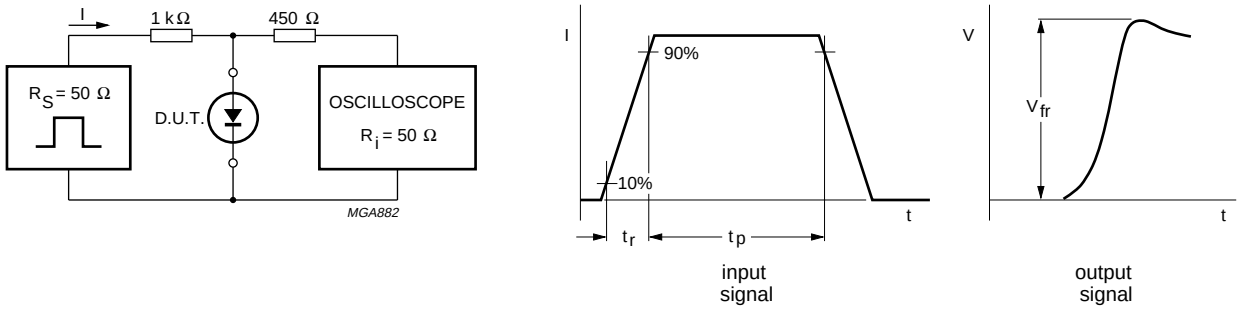


Fig.8 Forward recovery voltage test circuit and waveforms.

NPN general purpose transistors BC546; BC547

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 65 V).

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

NPN transistor in a TO-92; SOT54 plastic package.
PNP complements: BC556 and BC557.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector

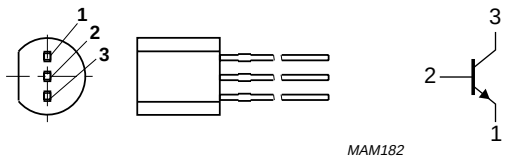


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BC546		–	80	V
	BC547		–	50	V
V_{CEO}	collector-emitter voltage	open base			
	BC546		–	65	V
	BC547		–	45	V
V_{EBO}	emitter-base voltage	open collector			
	BC546		–	6	V
	BC547		–	6	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	0.25	K/mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

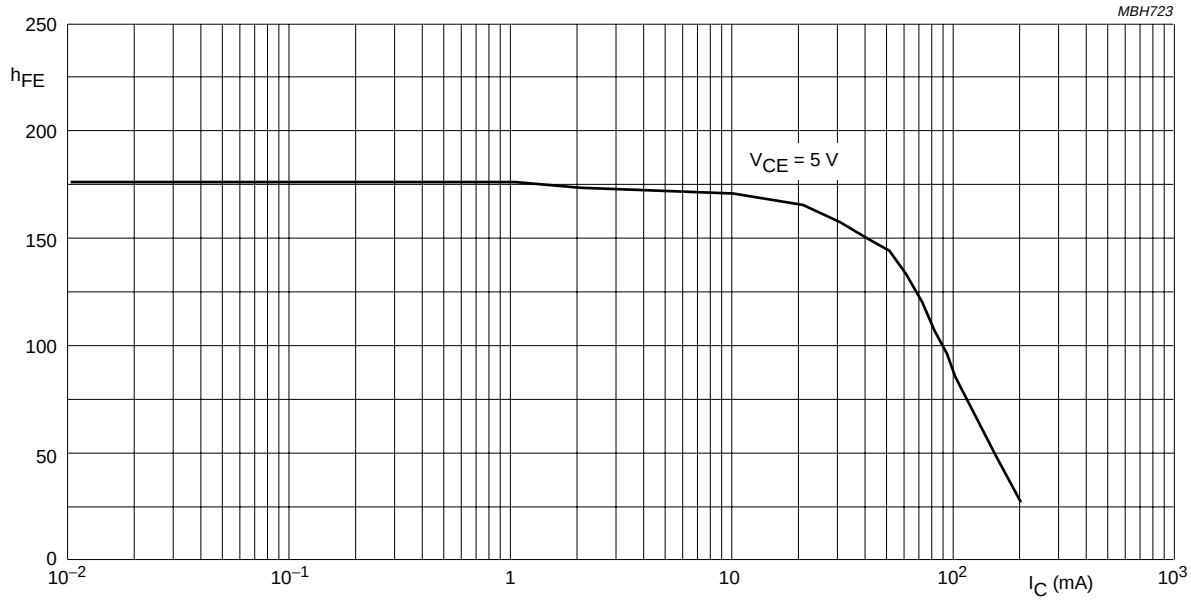
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 30 V	–	–	15	nA
		I_E = 0; V_{CB} = 30 V; T_j = 150 °C	–	–	5	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 5 V	–	–	100	nA
h_{FE}	DC current gain	I_C = 10 µA; V_{CE} = 5 V; see Figs 2, 3 and 4				
	BC546A		–	90	–	
	BC546B; BC547B		–	150	–	
	BC547C		–	270	–	
	DC current gain	I_C = 2 mA; V_{CE} = 5 V; see Figs 2, 3 and 4				
	BC546A		110	180	220	
	BC546B; BC547B		200	290	450	
	BC547C		420	520	800	
	BC547		110	–	800	
	BC546		110	–	450	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	–	90	250	mV
		I_C = 100 mA; I_B = 5 mA	–	200	600	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; note 1	–	700	–	mV
		I_C = 100 mA; I_B = 5 mA; note 1	–	900	–	mV
V_{BE}	base-emitter voltage	I_C = 2 mA; V_{CE} = 5 V; note 2	580	660	700	mV
		I_C = 10 mA; V_{CE} = 5 V	–	–	770	mV
C_c	collector capacitance	I_E = i_e = 0; V_{CB} = 10 V; f = 1 MHz	–	1.5	–	pF
C_e	emitter capacitance	I_C = i_c = 0; V_{EB} = 0.5 V; f = 1 MHz	–	11	–	pF
f_T	transition frequency	I_C = 10mA; V_{CE} = 5 V; f = 100 MHz	100	–	–	MHz
F	noise figure	I_C = 200 µA; V_{CE} = 5 V; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz	–	2	10	dB

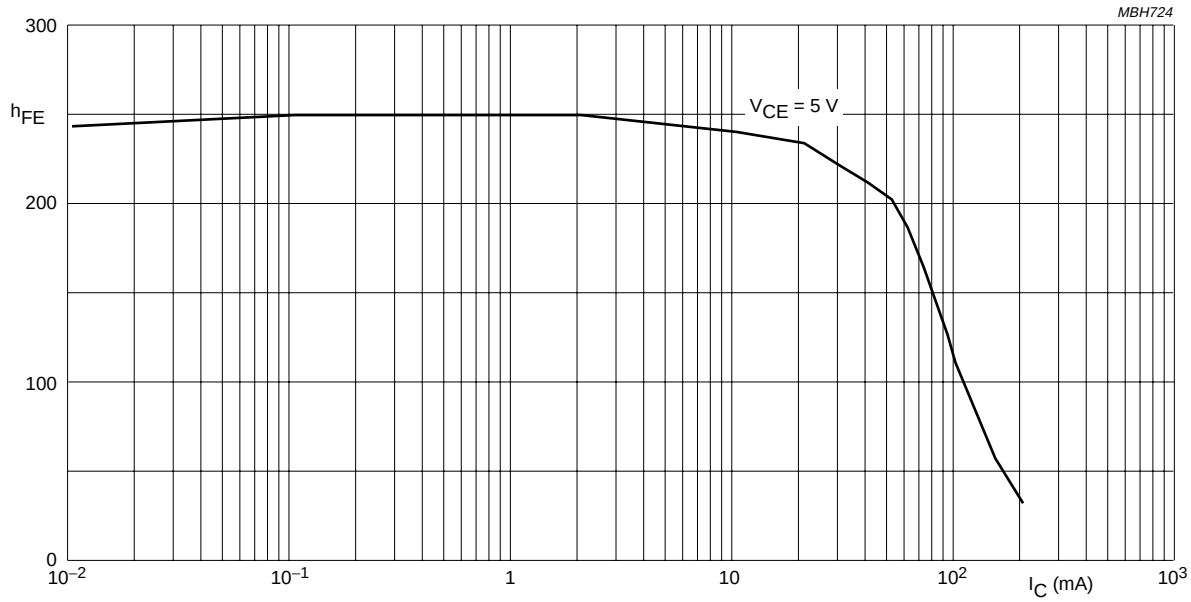
Notes

1. V_{BEsat} decreases by about 1.7 mV/K with increasing temperature.
2. V_{BE} decreases by about 2 mV/K with increasing temperature.



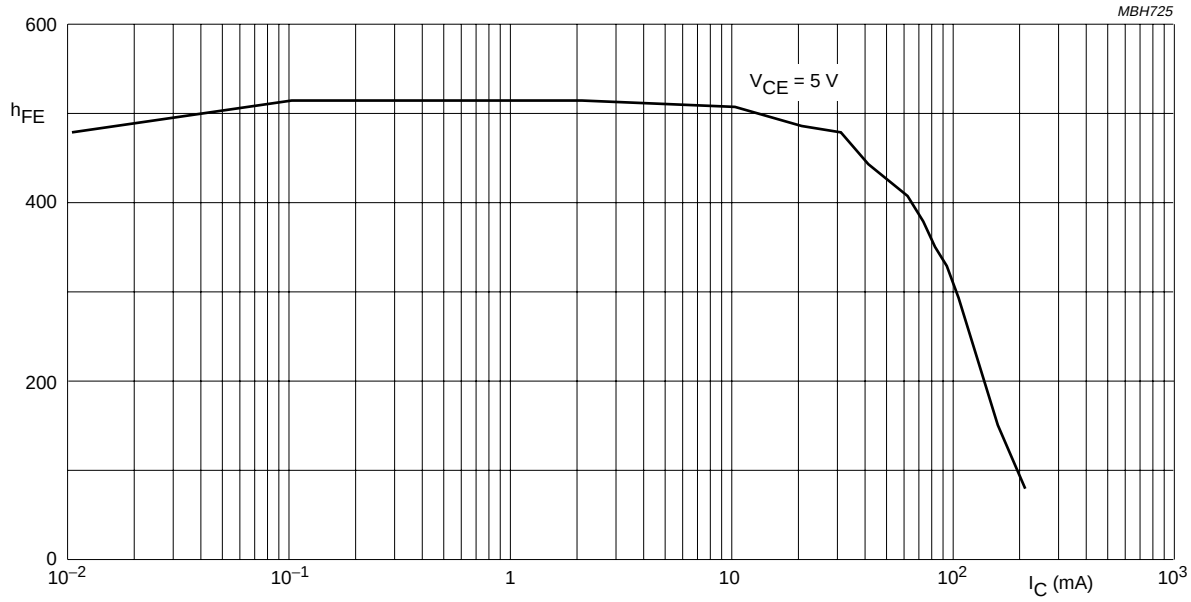
BC546A.

Fig.2 DC current gain; typical values.



BC546B; BC547B.

Fig.3 DC current gain; typical values.



BC547C.

Fig.4 DC current gain; typical values.

PNP general purpose transistors BC556; BC557

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 65 V).

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

PNP transistor in a TO-92; SOT54 plastic package.
NPN complements: BC546 and BC547.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector

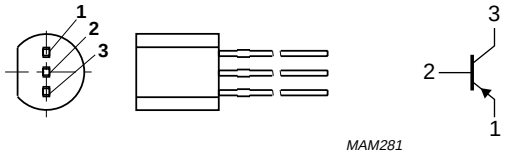


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BC556		–	–80	V
	BC557		–	–50	V
V_{CEO}	collector-emitter voltage	open base			
	BC556		–	–65	V
	BC557		–	–45	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–200	mA
I_{BM}	peak base current		–	–200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	250	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

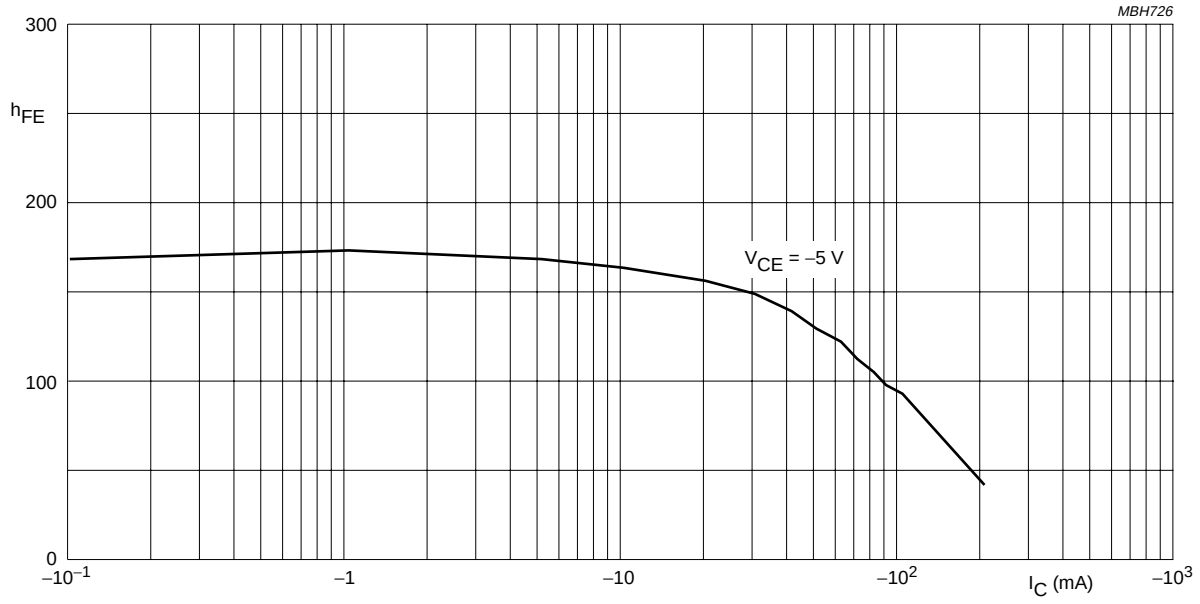
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = –30 V	–	–1	–15	nA
		I_E = 0; V_{CB} = –30 V; T_j = 150 °C	–	–	–4	µA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = –5 V	–	–	–100	nA
h_{FE}	DC current gain	I_C = –2 mA; V_{CE} = –5 V; see Figs 2, 3 and 4				
	BC556		125	–	475	
	BC557		125	–	800	
	BC556A		125	–	250	
	BC556B; BC557B		220	–	475	
	BC557C		420	–	800	
V_{CEsat}	collector-emitter saturation voltage	I_C = –10 mA; I_B = –0.5 mA	–	–60	–300	mV
		I_C = –100 mA; I_B = –5 mA	–	–180	–650	mV
V_{BEsat}	base-emitter saturation voltage	I_C = –10 mA; I_B = –0.5 mA; note 1	–	–750	–	mV
		I_C = –100 mA; I_B = –5 mA; note 1	–	–930	–	mV
V_{BE}	base-emitter voltage	I_C = –2 mA; V_{CE} = –5 V; note 2	–600	–650	–750	mV
		I_C = –10 mA; V_{CE} = –5 V; note 2	–	–	–820	mV
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = –10 V; f = 1 MHz	–	3	–	pF
C_e	emitter capacitance	$I_C = i_c$ = 0; V_{EB} = –0.5 V; f = 1 MHz	–	10	–	pF
f_T	transition frequency	I_C = –10 mA; V_{CE} = –5 V; f = 100 MHz	100	–	–	MHz
F	noise figure	I_C = –200 µA; V_{CE} = –5 V; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz	–	2	10	dB

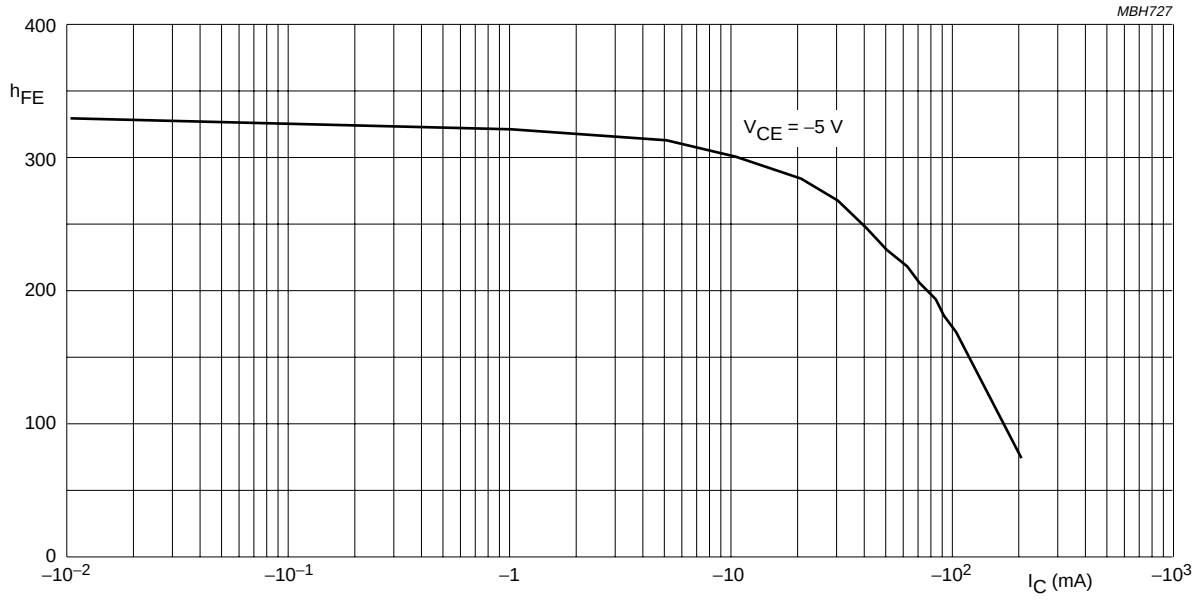
Notes

1. V_{BEsat} decreases by about –1.7 mV/K with increasing temperature.
2. V_{BE} decreases by about –2 mV/K with increasing temperature.



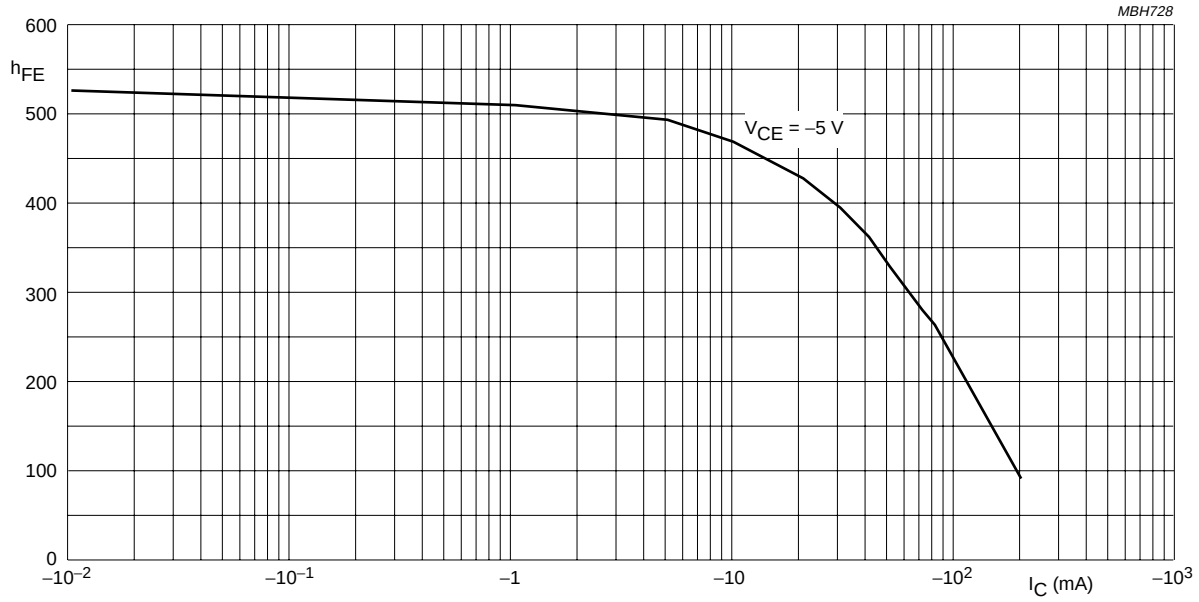
BC556A.

Fig.2 DC current gain; typical values.



BC556B; BC557B.

Fig.3 DC current gain; typical values.



BC557C.

Fig.4 DC current gain; typical values.

NPN medium frequency transistors BF494; BF495

FEATURES

- Low current (max. 30 mA)
- Low voltage (max. 20 V).

APPLICATIONS

- HF applications in radio and television receivers
- FM tuners
- Low noise AM mixer-oscillators
- IF amplifiers in AM/FM receivers.

DESCRIPTION

NPN medium frequency transistor in a TO-92; SOT54 plastic package.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector

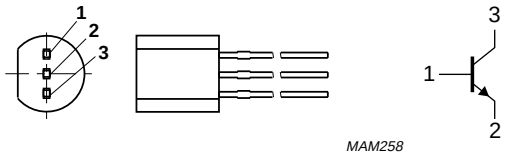


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	30	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
I_{CM}	peak collector current		–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	300	mW
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 10 V			
	BF494		67	220	
	BF495		35	125	
f_T	transition frequency	I_C = 1 mA; V_{CE} = 10 V; f = 100 MHz	120	–	MHz

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	30	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	30	mA
I_{CM}	peak collector current		–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	420	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

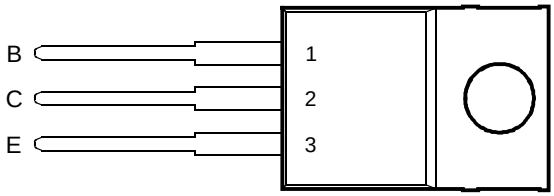
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 20$ V	–	100	nA
		$I_E = 0$; $V_{CB} = 20$ V; $T_{amb} = 150$ °C	–	4	µA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 4$ V	–	100	nA
h_{FE}	DC current gain	$I_C = 1$ mA; $V_{CE} = 10$ V			
	BF494		67	220	
	BF494B		100	220	
	BF495		35	125	
	BF495B		100	125	
V_{BE}	base-emitter voltage	$I_C = 1$ mA; $V_{CE} = 10$ V	650	740	mV
C_{re}	feedback capacitance	$I_C = 0$; $V_{CB} = 10$ V; f = 1 MHz	–	1	pF
f_T	transition frequency	$I_C = 1$ mA; $V_{CE} = 10$ V; f = 100 MHz	120	–	MHz

TIP29, TIP29A, TIP29B, TIP29C
NPN SILICON POWER TRANSISTORS

 JULY 1968 - REVISED MARCH 1997

- **Designed for Complementary Use with the TIP30 Series**
- **30 W at 25°C Case Temperature**
- **1 A Continuous Collector Current**
- **3 A Peak Collector Current**
- **Customer-Specified Selections Available**

TO-220 PACKAGE
(TOP VIEW)



Pin 2 is in electrical contact with the mounting base.

MDTRACA

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Collector-base voltage (I_E = 0)	TIP29	V_{CBO}	80	V
	TIP29A		100	
	TIP29B		120	
	TIP29C		140	
Collector-emitter voltage (I_B = 0)	TIP29	V_{CEO}	40	V
	TIP29A		60	
	TIP29B		80	
	TIP29C		100	
Emitter-base voltage		V_{EBO}	5	V
Continuous collector current		I_C	1	A
Peak collector current (see Note 1)		I_{CM}	3	A
Continuous base current		I_B	0.4	A
Continuous device dissipation at (or below) 25°C case temperature (see Note 2)		P_{tot}	30	W
Continuous device dissipation at (or below) 25°C free air temperature (see Note 3)		P_{tot}	2	W
Unclamped inductive load energy (see Note 4)		$½LI_C^2$	32	mJ
Operating junction temperature range		T_j	-65 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C
Lead temperature 3.2 mm from case for 10 seconds		T_L	250	°C

NOTES: 1. This value applies for $t_p \leq 0.3$ ms, duty cycle ≤ 10%.
2. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.
3. Derate linearly to 150°C free air temperature at the rate of 16 mW/°C.
4. This rating is based on the capability of the transistor to operate safely in a circuit of: L = 20 mH, $I_{B(on)}$ = 0.4 A, R_{BE} = 100 Ω, $V_{BE(off)}$ = 0, R_S = 0.1 Ω, V_{CC} = 20 V.

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 30 mA (see Note 5)	I_B = 0	TIP29 TIP29A TIP29B TIP29C	40 60 80 100			V
I_{CES}	Collector-emitter cut-off current	V_{CE} = 80 V V_{CE} = 100 V V_{CE} = 120 V V_{CE} = 140 V	V_{BE} = 0 V_{BE} = 0 V_{BE} = 0 V_{BE} = 0	TIP29 TIP29A TIP29B TIP29C			0.2 0.2 0.2 0.2	mA
I_{CEO}	Collector cut-off current	V_{CE} = 30 V V_{CE} = 60 V	I_B = 0 I_B = 0	TIP29/29A TIP29B/29C			0.3 0.3	mA
I_{EBO}	Emitter cut-off current	V_{EB} = 5 V	I_C = 0				1	mA
h_{FE}	Forward current transfer ratio	V_{CE} = 4 V V_{CE} = 4 V	I_C = 0.2 A I_C = 1 A	(see Notes 5 and 6)	40 15		 75	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = 125 mA	I_C = 1 A	(see Notes 5 and 6)			0.7	V
V_{BE}	Base-emitter voltage	V_{CE} = 4 V	I_C = 1 A	(see Notes 5 and 6)			1.3	V
h_{fe}	Small signal forward current transfer ratio	V_{CE} = 10 V	I_C = 0.2 A	f = 1 kHz	20			
$\|h_{fe}\|$	Small signal forward current transfer ratio	V_{CE} = 10 V	I_C = 0.2 A	f = 1 MHz	3			

NOTES: 5. These parameters must be measured using pulse techniques, t_p = 300 µs, duty cycle ≤ 2%.
6. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to case thermal resistance			4.17	°C/W
$R_{\theta JA}$	Junction to free air thermal resistance			62.5	°C/W

resistive-load-switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS †			MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	I_C = 1 A	$I_{B(on)}$ = 0.1 A	$I_{B(off)}$ = -0.1 A		0.5		µs
t_{off}	Turn-off time	$V_{BE(off)}$ = -4.3 V	R_L = 30 Ω	t_p = 20 µs, dc ≤ 2%		2		µs

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

TYPICAL DC CURRENT GAIN vs COLLECTOR CURRENT

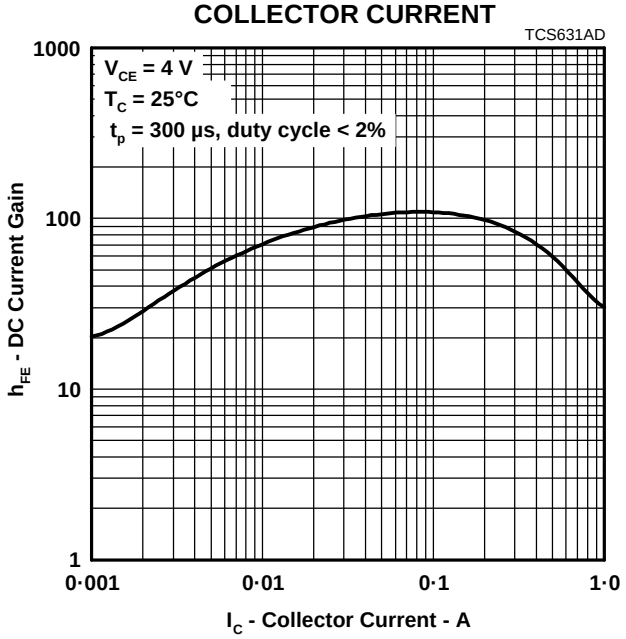


Figure 1.

COLLECTOR-EMITTER SATURATION VOLTAGE vs BASE CURRENT

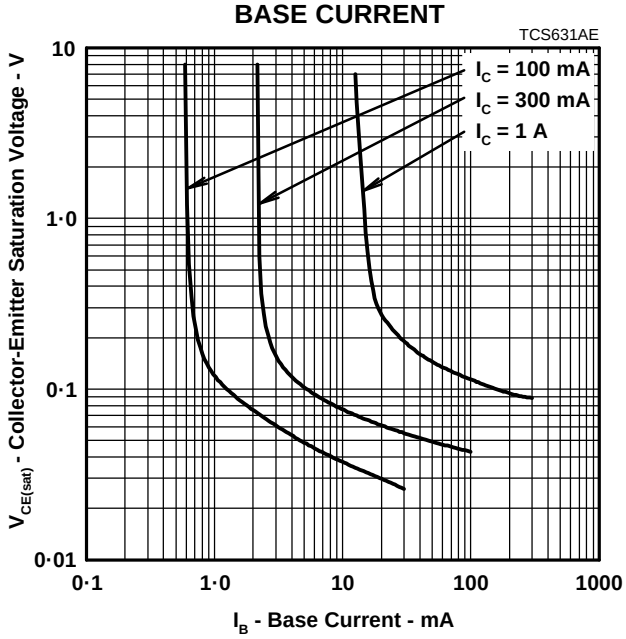


Figure 2.

BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT

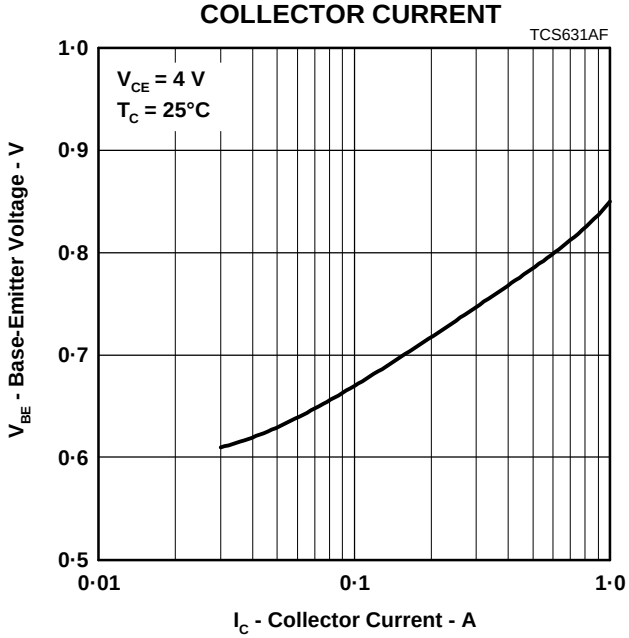


Figure 3.

MAXIMUM SAFE OPERATING REGIONS

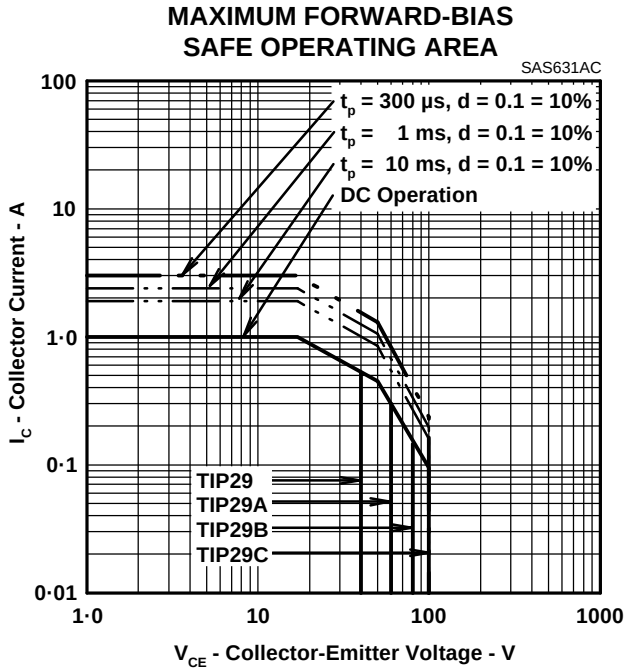


Figure 4.

THERMAL INFORMATION

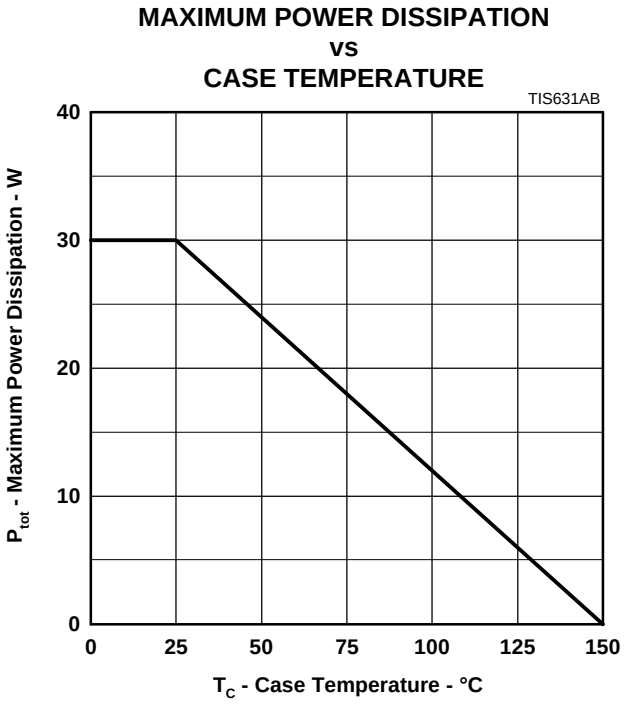


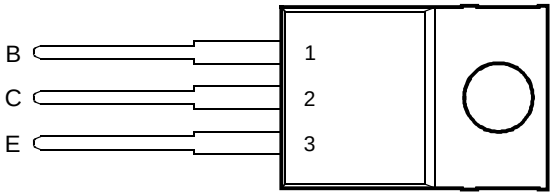
Figure 5.

PRODUCT INFORMATION

 JULY 1968 - REVISED MARCH 1997

- **Designed for Complementary Use with the TIP29 Series**
- **30 W at 25°C Case Temperature**
- **1 A Continuous Collector Current**
- **3 A Peak Collector Current**
- **Customer-Specified Selections Available**

TO-220 PACKAGE
(TOP VIEW)



Pin 2 is in electrical contact with the mounting base.

MDTRACA

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Collector-base voltage (I_E = 0)	TIP30	V_{CBO}	-80	V
	TIP30A		-100	
	TIP30B		-120	
	TIP30C		-140	
Collector-emitter voltage (I_B = 0)	TIP30	V_{CEO}	-40	V
	TIP30A		-60	
	TIP30B		-80	
	TIP30C		-100	
Emitter-base voltage		V_{EBO}	-5	V
Continuous collector current		I_C	-1	A
Peak collector current (see Note 1)		I_{CM}	-3	A
Continuous base current		I_B	-0.4	A
Continuous device dissipation at (or below) 25°C case temperature (see Note 2)		P_{tot}	30	W
Continuous device dissipation at (or below) 25°C free air temperature (see Note 3)		P_{tot}	2	W
Unclamped inductive load energy (see Note 4)		$½LI_C^2$	32	mJ
Operating junction temperature range		T_j	-65 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C
Lead temperature 3.2 mm from case for 10 seconds		T_L	250	°C

NOTES: 1. This value applies for $t_p \leq 0.3$ ms, duty cycle ≤ 10%.
2. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.
3. Derate linearly to 150°C free air temperature at the rate of 16 mW/°C.
4. This rating is based on the capability of the transistor to operate safely in a circuit of: L = 20 mH, $I_{B(on)}$ = -0.4 A, R_{BE} = 100 Ω, $V_{BE(off)}$ = 0, R_S = 0.1 Ω, V_{CC} = -20 V.

JULY 1968 - REVISED MARCH 1997

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = -30 mA (see Note 5)	I_B = 0	TIP30 TIP30A TIP30B TIP30C	-40 -60 -80 -100			V
I_{CES}	Collector-emitter cut-off current	V_{CE} = -80 V V_{CE} = -100 V V_{CE} = -120 V V_{CE} = -140 V	V_{BE} = 0 V_{BE} = 0 V_{BE} = 0 V_{BE} = 0	TIP30 TIP30A TIP30B TIP30C			-0.2 -0.2 -0.2 -0.2	mA
I_{CEO}	Collector cut-off current	V_{CE} = -30 V V_{CE} = -60 V	I_B = 0 I_B = 0	TIP30/30A TIP30B/30C			-0.3 -0.3	mA
I_{EBO}	Emitter cut-off current	V_{EB} = -5 V	I_C = 0				-1	mA
h_{FE}	Forward current transfer ratio	V_{CE} = -4 V V_{CE} = -4 V	I_C = -0.2 A I_C = -1 A	(see Notes 5 and 6)	40 15		 75	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_B = -125 mA	I_C = -1 A	(see Notes 5 and 6)			-0.7	V
V_{BE}	Base-emitter voltage	V_{CE} = -4 V	I_C = -1 A	(see Notes 5 and 6)			-1.3	V
h_{fe}	Small signal forward current transfer ratio	V_{CE} = -10 V	I_C = -0.2 A	f = 1 kHz	20			
$\|h_{fe}\|$	Small signal forward current transfer ratio	V_{CE} = -10 V	I_C = -0.2 A	f = 1 MHz	3			

NOTES: 5. These parameters must be measured using pulse techniques, t_p = 300 µs, duty cycle ≤ 2%.
6. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to case thermal resistance			4.17	°C/W
$R_{\theta JA}$	Junction to free air thermal resistance			62.5	°C/W

resistive-load-switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS †			MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	I_C = -1 A	$I_{B(on)}$ = -0.1 A	$I_{B(off)}$ = 0.1 A		0.3		µs
t_{off}	Turn-off time	$V_{BE(off)}$ = 4.3 V	R_L = 30 Ω	t_p = 20 µs, dc ≤ 2%		1		µs

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

TYPICAL DC CURRENT GAIN vs COLLECTOR CURRENT

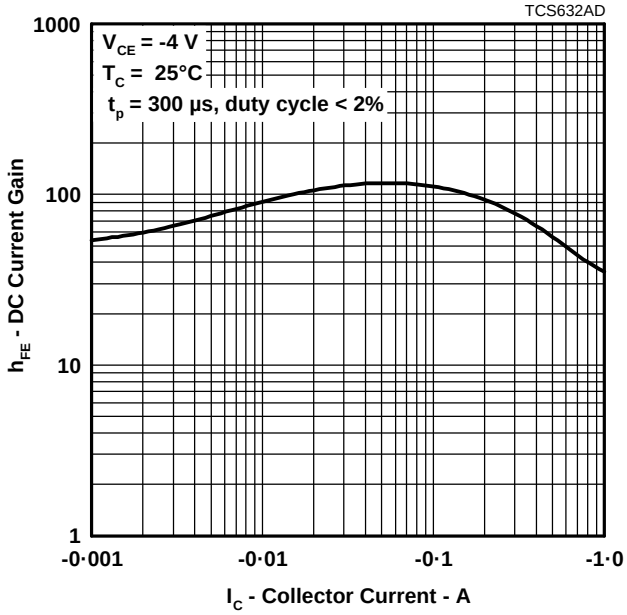


Figure 1.

COLLECTOR-EMITTER SATURATION VOLTAGE vs BASE CURRENT

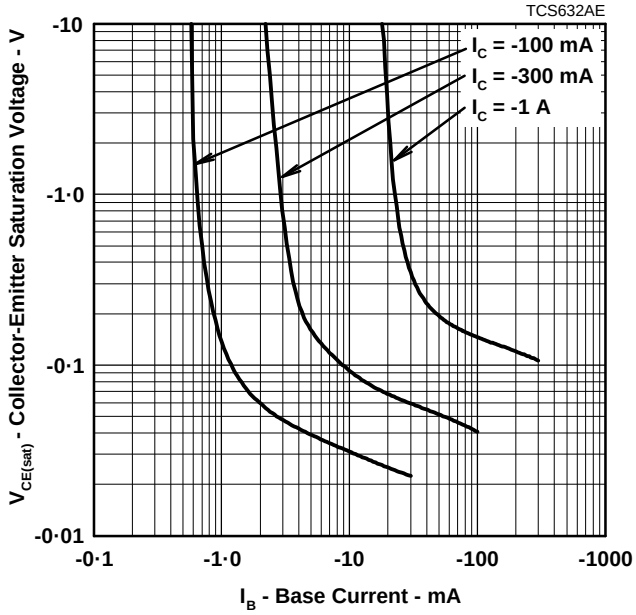


Figure 2.

BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT

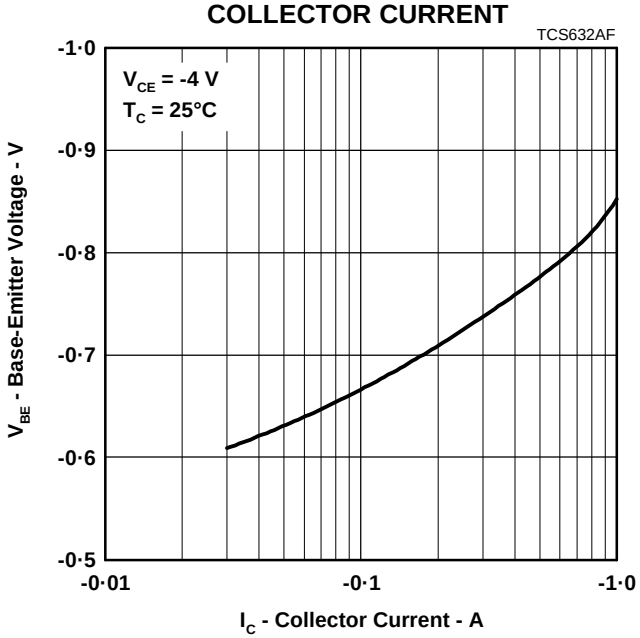


Figure 3.

MAXIMUM SAFE OPERATING REGIONS

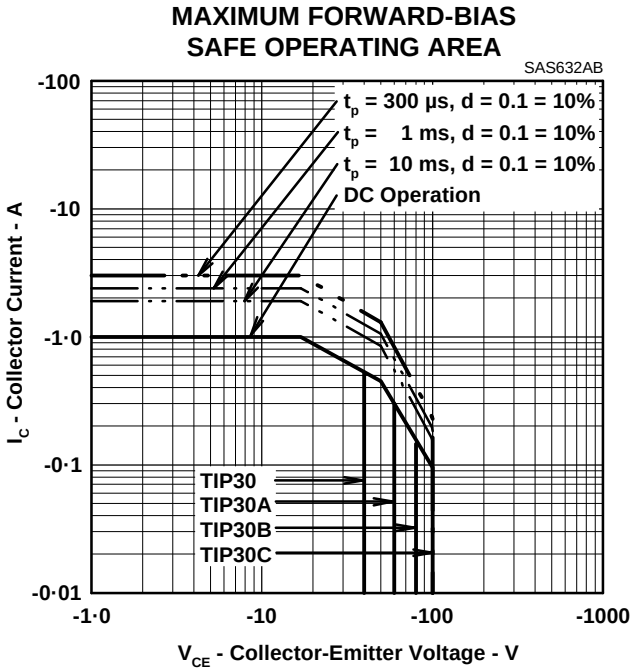


Figure 4.

THERMAL INFORMATION

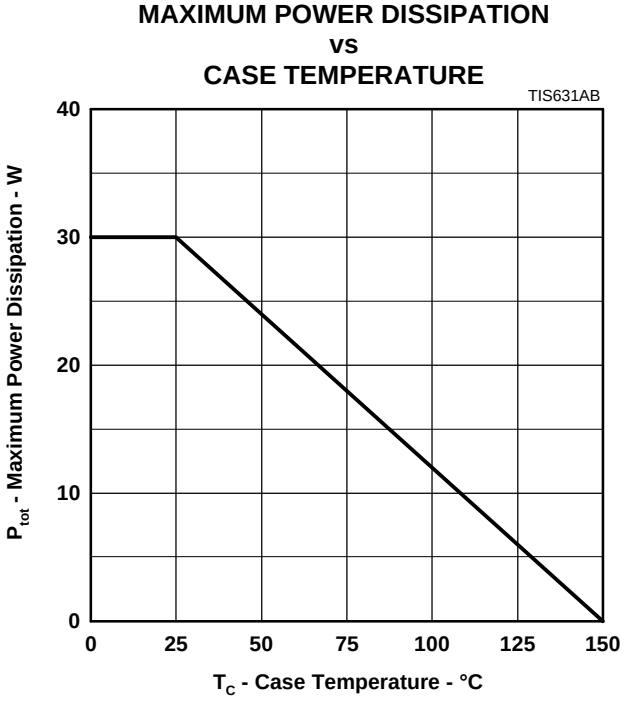


Figure 5.

PRODUCT INFORMATION

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion 0.003% Typ**
- **Low Noise V_n = 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **High Input Impedance . . . JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

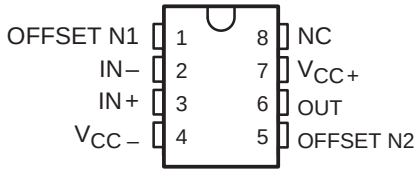
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE							
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
0°C to 70°C	10 mV	TL071CD	—	—	—	—	TL071CP	TL071CPWLE	—
	6 mV	TL071ACD					TL071ACP	—	
	3 mV	TL071BCD					TL071BCP	—	
	10 mV	TL072CD	—	—	—	—	TL072CP	TL072CPWLE	—
	6 mV	TL072ACD					TL072ACP	—	
	3 mV	TL072BCD					TL072BCP	—	
	10 mV	TL074CD	—	—	—	TL074CN	—	TL074CPWLE	—
	6 mV	TL074ACD				TL074ACN		—	
	3 mV	TL074BCD				TL074BCN		—	
–40°C to 85°C	6 mV	TL071ID	—	—	—	—	TL071IP	—	—
		TL072ID				—	TL072IP		
		TL074ID				TL074IN	—		
–55°C to 125°C	6 mV	—	TL071MFK	—	TL071MJG	—	—	—	—
	6 mV		TL072MFK	—	TL072MJG	—	TL072MP		—
	9 mV		TL074MFK	TL074MJ	—	TL074MN	—		TL074MW

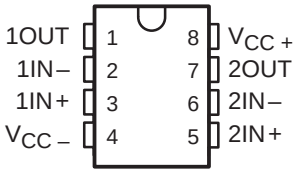
† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

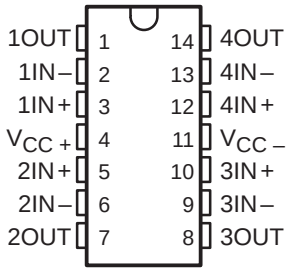
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



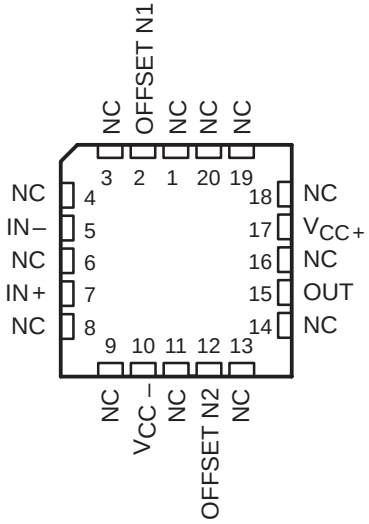
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



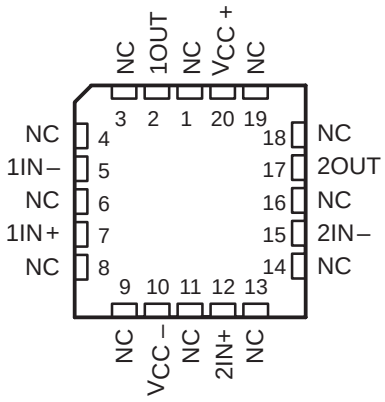
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



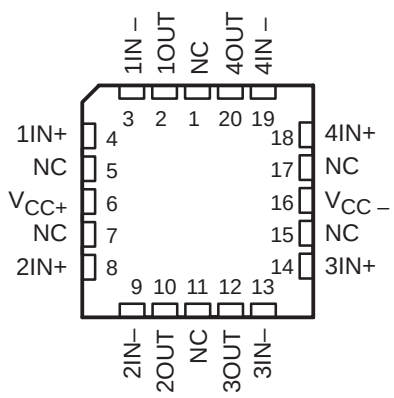
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



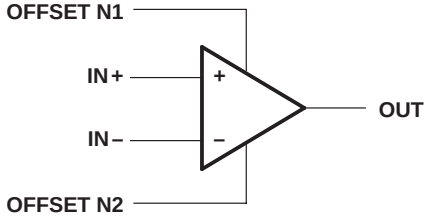
TL074
FK PACKAGE
(TOP VIEW)



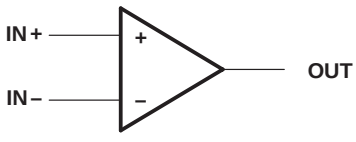
NC – No internal connection

symbols

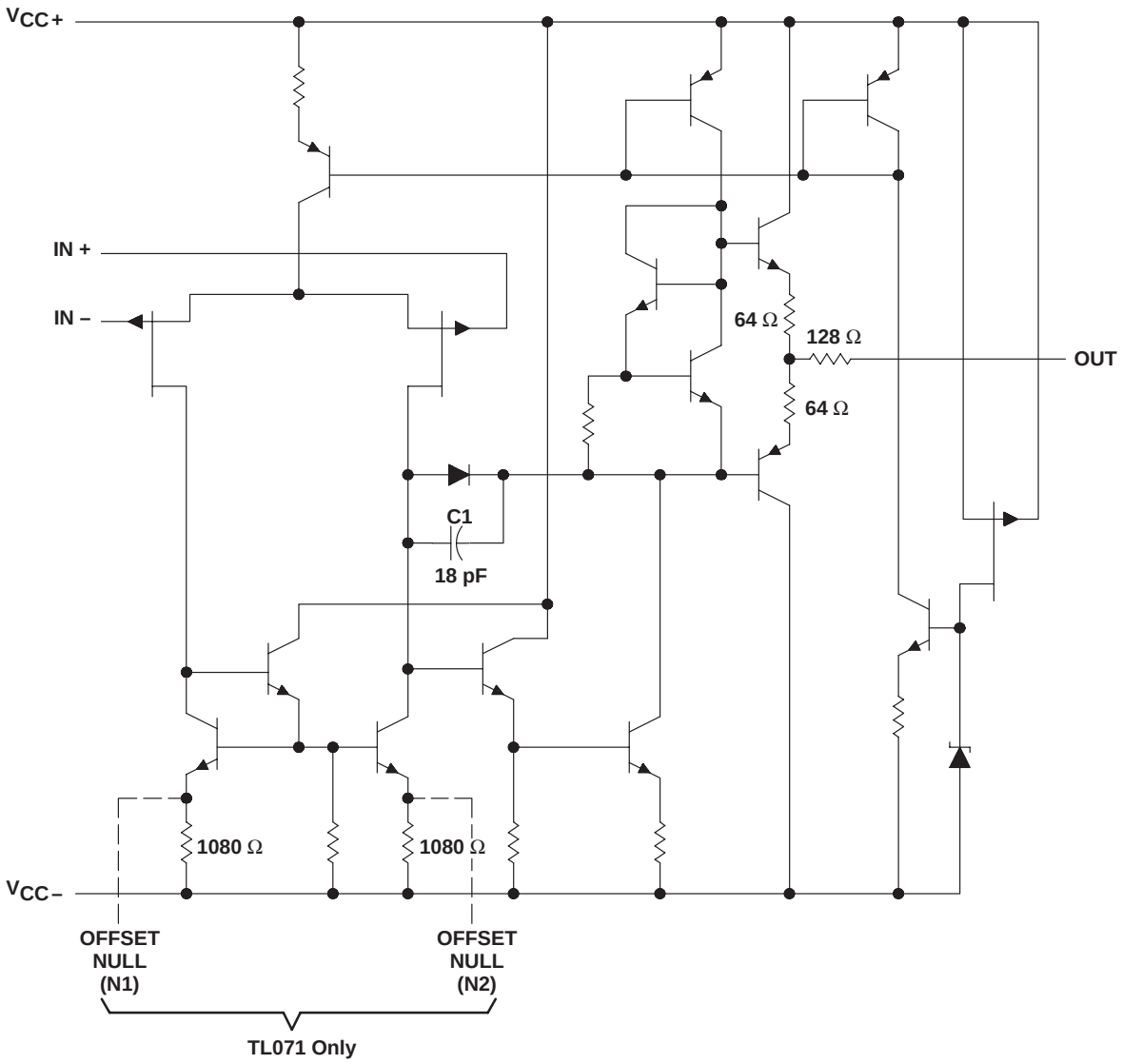
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . –18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±30 V
Input voltage, V_I (see Notes 1 and 3) . . . . . ±15 V
Duration of output short circuit (see Note 4) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
M suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = –40°C to 85°C for TL07_I.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is T_A = –55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, $R_L \geq 2$ kΩ, f = 1 kHz	A_{VD} = 1, $R_S \leq 1$ kΩ,		0.003%			0.003%		

PARAMETER MEASUREMENT INFORMATION

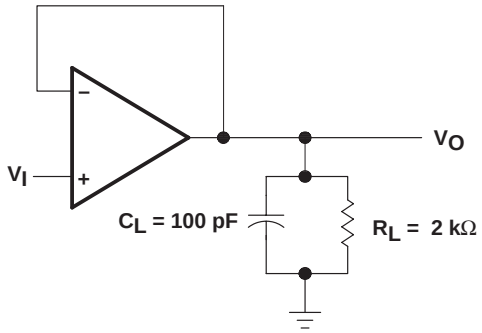


Figure 1. Unity-Gain Amplifier

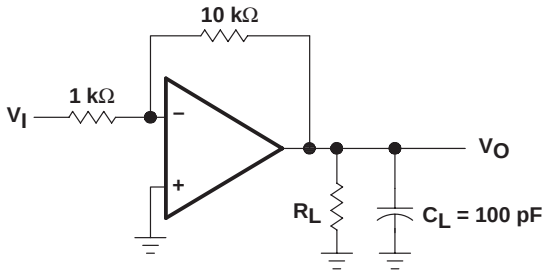


Figure 2. Gain-of-10 Inverting Amplifier

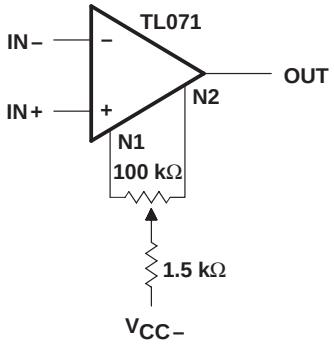


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Elapsed time	22

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

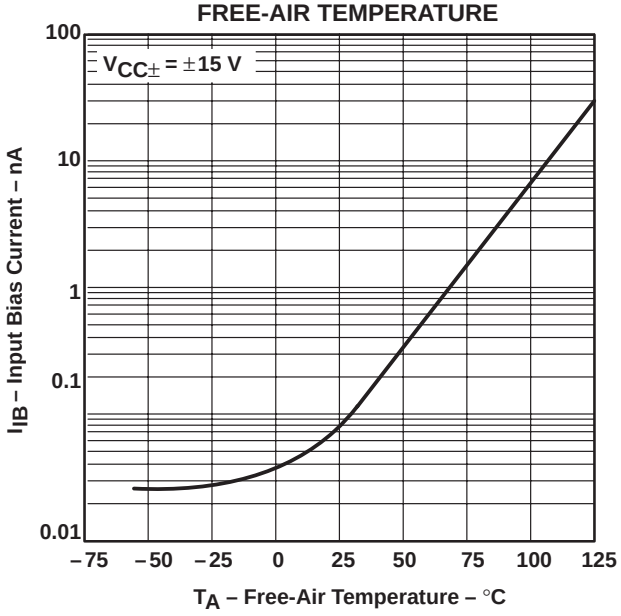


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

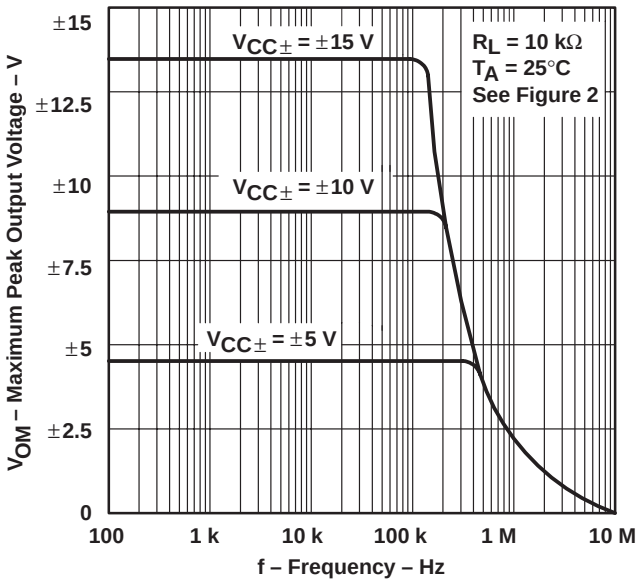


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

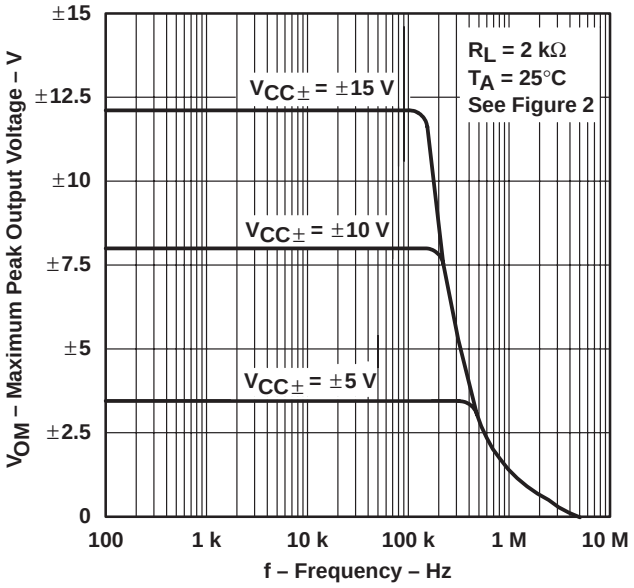


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

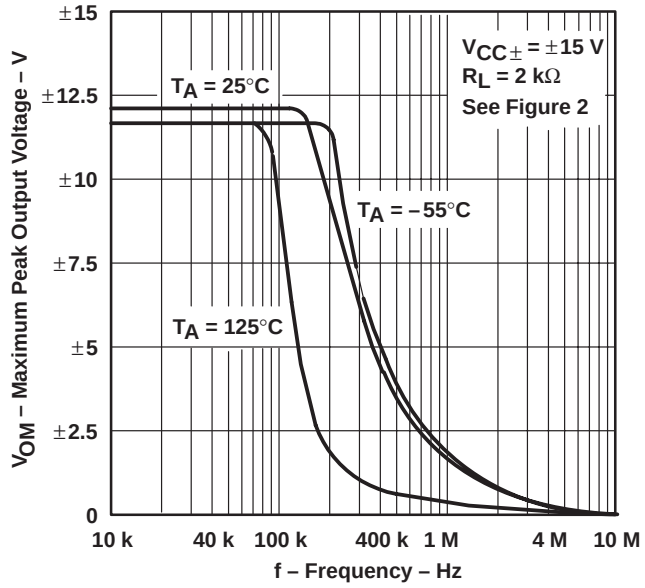


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

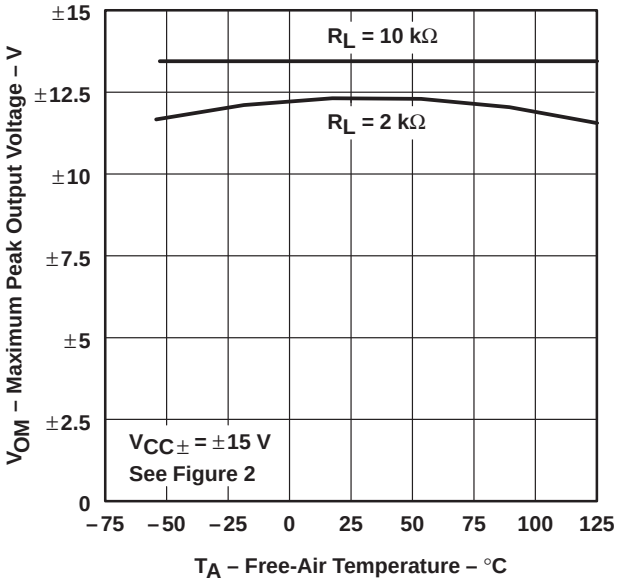


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

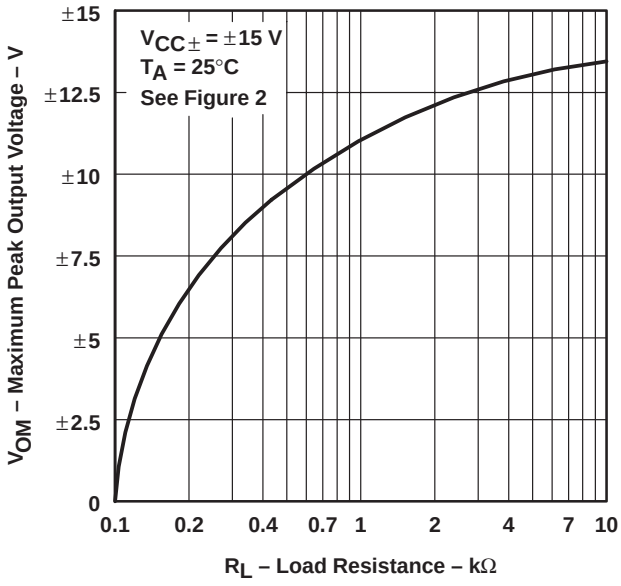


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

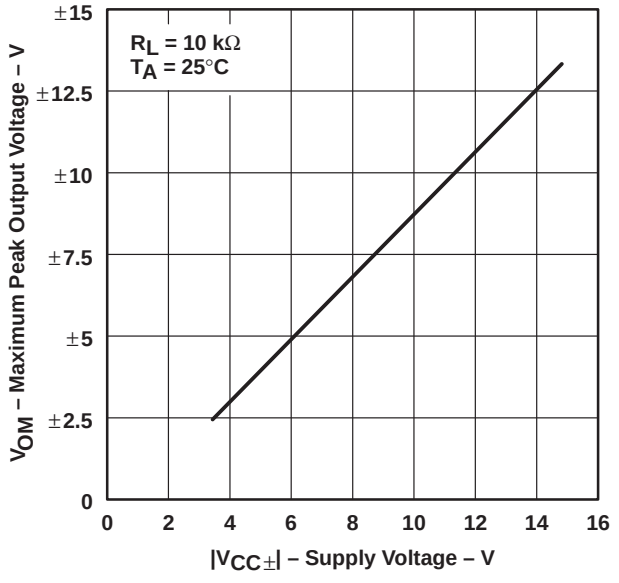


Figure 10

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

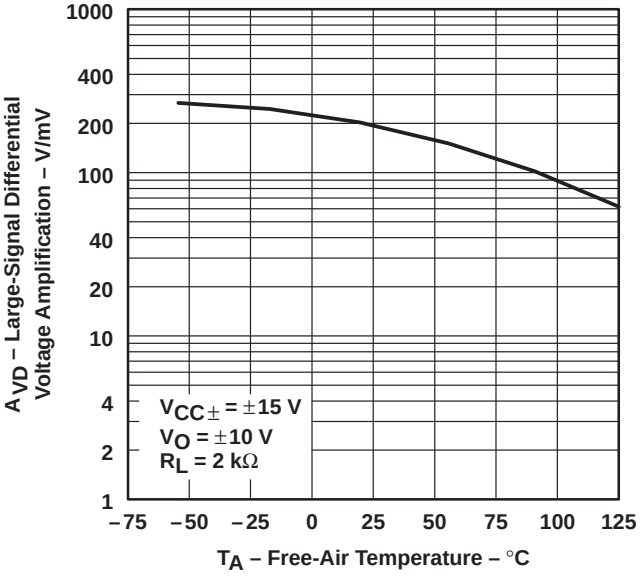


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

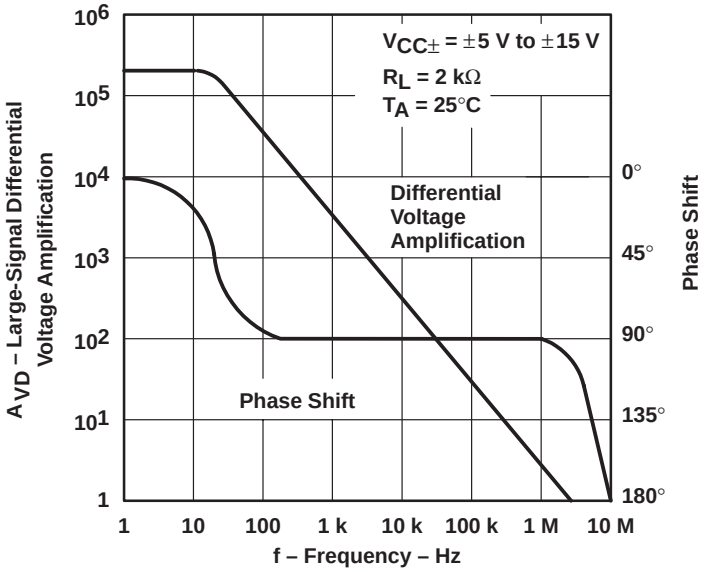


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

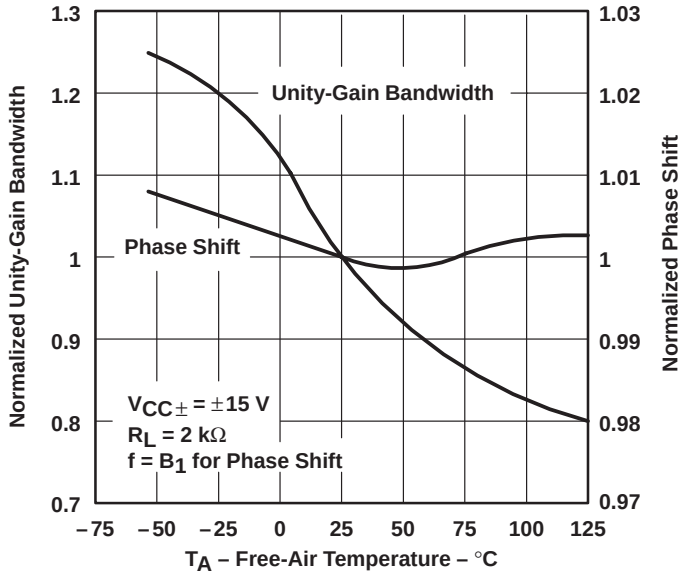


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

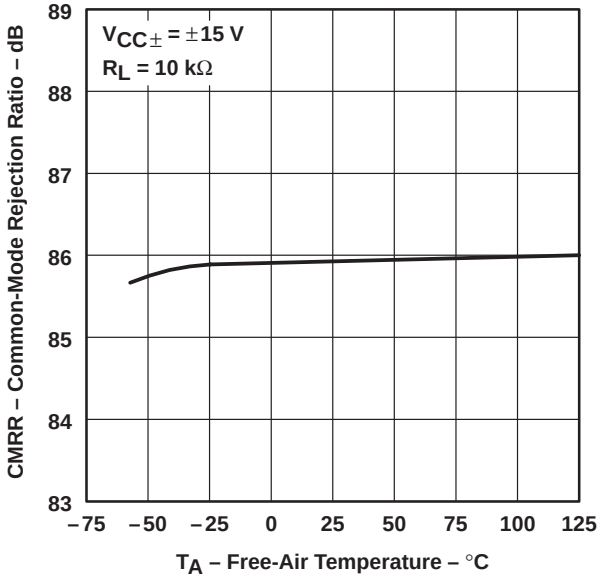


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

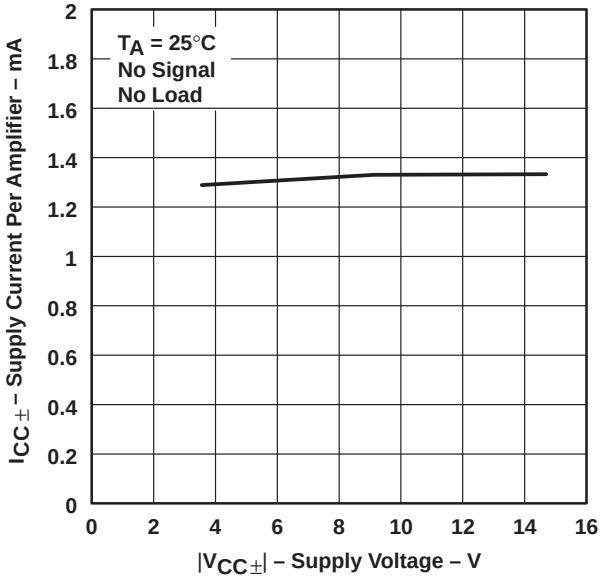


Figure 15

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

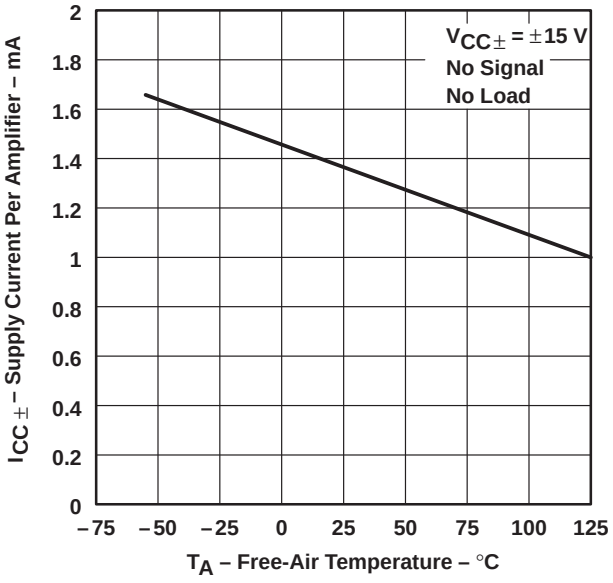


Figure 16

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

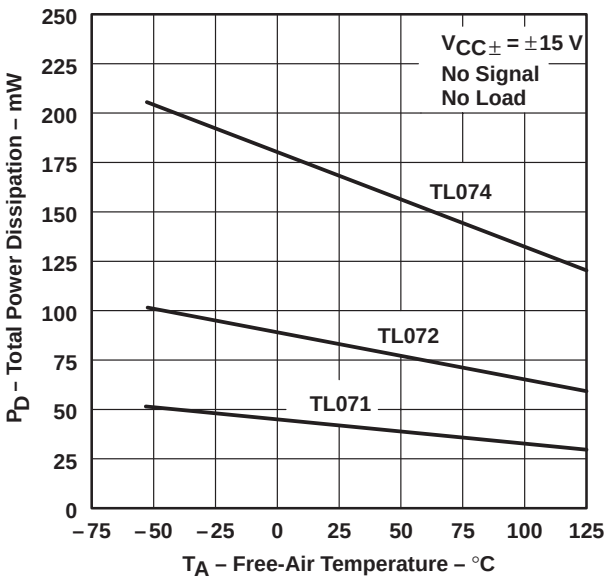


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

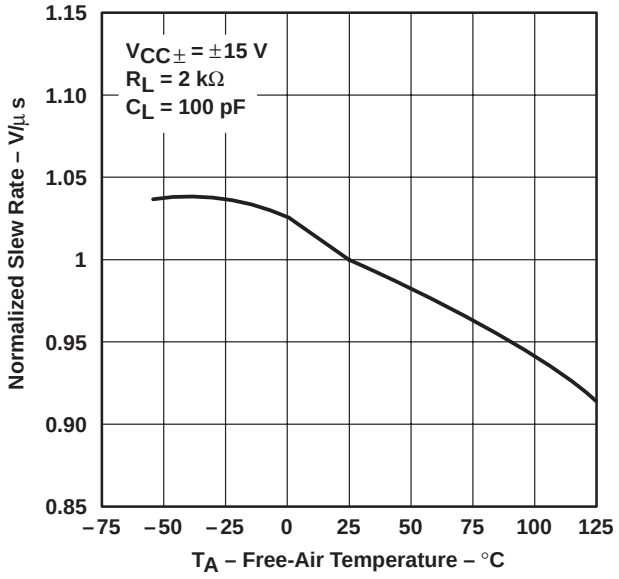


Figure 18

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

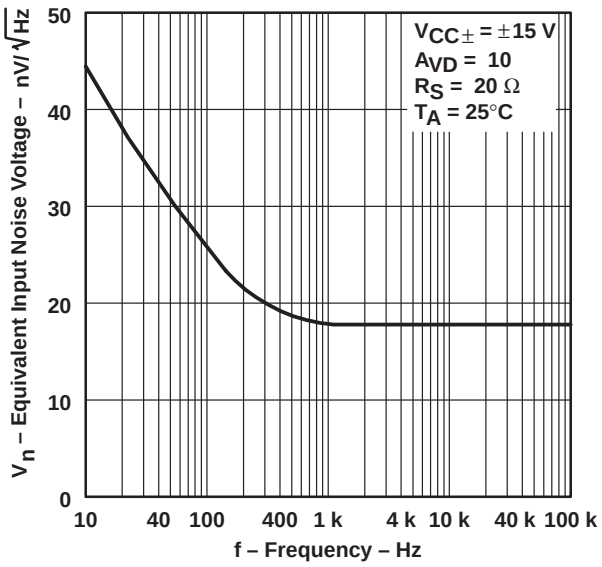


Figure 19

TOTAL HARMONIC DISTORTION vs FREQUENCY

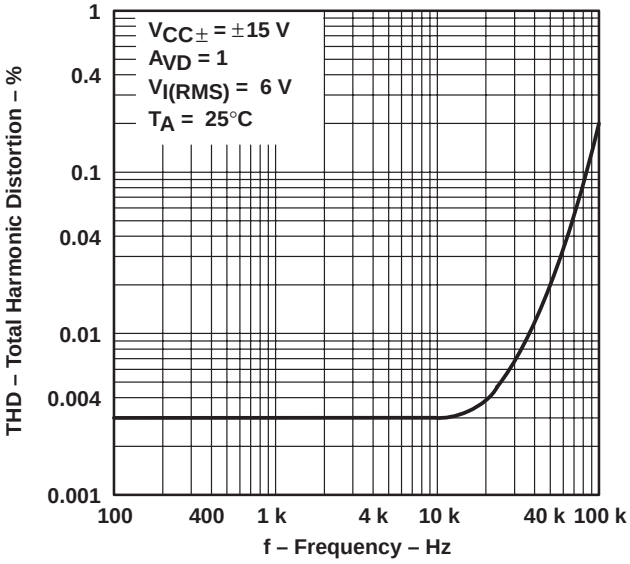


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

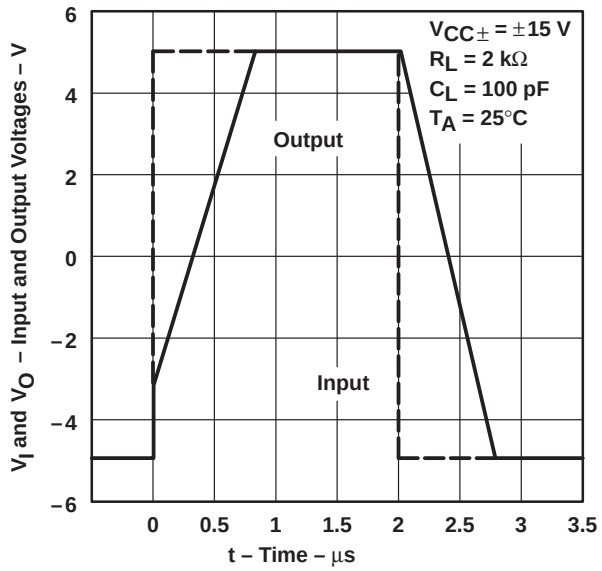


Figure 21

TYPICAL CHARACTERISTICS

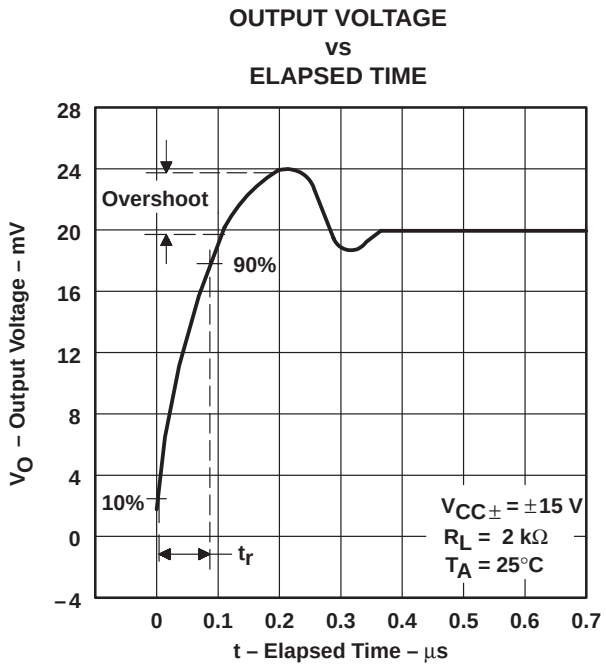


Figure 22

Order this document by MC1496/D

MOTOROLA

MC1496, B

Balanced Modulators/ Demodulators

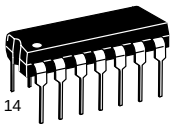
These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN531 for additional design information.

- Excellent Carrier Suppression –65 dB typ @ 0.5 MHz
  –50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection –85 dB typical

This device contains 8 active transistors.

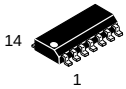
BALANCED MODULATORS/DEMODULATORS

SEMICONDUCTOR TECHNICAL DATA

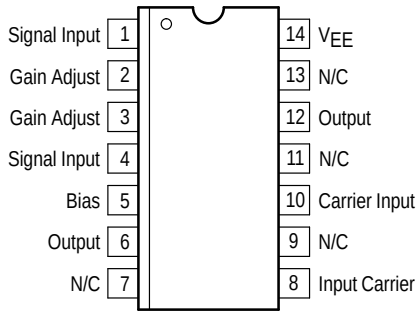


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



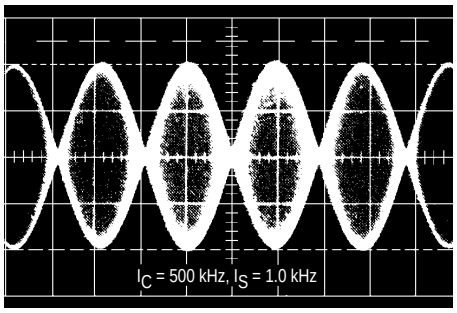


Figure 1. Suppressed Carrier Output Waveform

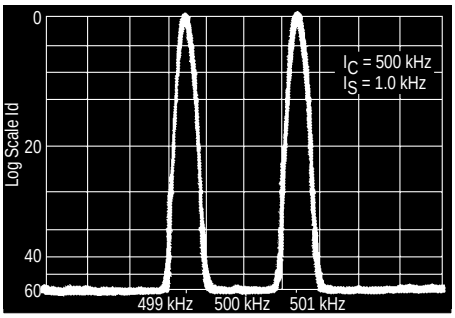


Figure 2. Suppressed Carrier Spectrum

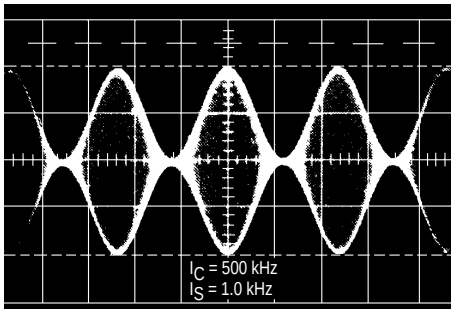
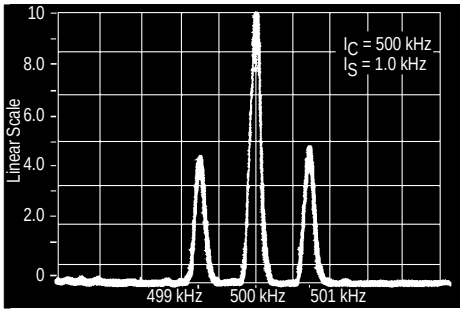


Figure 3. Amplitude Modulation Output Waveform

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1496D	T_A = 0°C to +70°C	SO–14
MC1496P		Plastic DIP
MC1496BP	T_A = –40°C to +125°C	Plastic DIP

Figure 4. Amplitude–Modulation Spectrum



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V6 – V8, V10 – V1, V12 – V8, V12 – V10, V8 – V4, V8 – V1, V10 – V4, V6 – V10, V2 – V5, V3 – V5)	ΔV	30	Vdc
Differential Input Signal	V8 – V10 V4 – V1	+5.0 ±(5+I5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction–to–Air Plastic Dual In–Line Package	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{EE} = –8.0 Vdc, I5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = T_{low} to T_{high}, all input and output characteristics are single–ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Carrier Feedthrough	5	1	V_{CFT}				μVrms
V_C = 60 mVrms sine wave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVpp square wave:							mVrms
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	5	2	V_{CS}				dB
f_S = 10 kHz, 300 mVrms							
f_C = 500 kHz, 60 mVrms sine wave				40	65	–	
f_C = 10 MHz, 60 mVrms sine wave				–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 Ω)	8	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mVrms sine wave				–	300	–	
f_S = 1.0 kHz, 300 mVrms sine wave							
Signal Input Port, V_S = 300 mVrms sine wave				–	80	–	
$\lvert V_C \rvert$ = 0.5 Vdc							
Signal Gain (V_S = 100 mVrms, f = 1.0 kHz; $\lvert V_C \rvert$= 0.5 Vdc)	10	3	A_{VS}	2.5	3.5	–	V/V
Single–Ended Input Impedance, Signal Port, f = 5.0 MHz	6	–					
Parallel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single–Ended Output Impedance, f = 10 MHz	6	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{oo}	–	5.0	–	pF
Input Bias Current	7	–					μA
$I_{bS} = \frac{I1 + I4}{2}$; $I_{bC} = \frac{I8 + I10}{2}$			I_{bS} I_{bC}	– –	12 12	30 30	
Input Offset Current	7	–					μA
I_{ioS} = I1–I4; I_{ioC} = I8–I10			$\lvert I_{ioS} \rvert$ $I_{ioC} \rvert$	– –	0.7 0.7	7.0 7.0	
Average Temperature Coefficient of Input Offset Current (T_A = –55°C to +125°C)	7	–	$\lvert TC_{Iio} \rvert$	–	2.0	–	nA/°C
Output Offset Current (I6–I9)	7	–	$\lvert I_{oo} \rvert$	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = –55°C to +125°C)	7	–	$\lvert TC_{Ioo} \rvert$	–	90	–	nA/°C
Common–Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	Vpp
Common–Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$= 0.5 Vdc	9	–	ACM	–	–85	–	dB
Common–Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_{out}	–	8.0	–	Vpp
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	Vpp
Power Supply Current I6 +I12	7	6	I_{CC}	–	2.0	4.0	mAdc
I14			I_{EE}	–	3.0	5.0	
DC Power Dissipation	7	5	P_D	–	33	–	mW

GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal–input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input–signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single–ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I5(\text{mA})}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors “on” and two transistors “off” (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I5.

$$V_S \leq I5\ R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common–mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage–current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, $P_D = 2\ I5\ (V6 - V14) + I5)\ V5 - V14$ where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$I5 = I6 = I12,$$
$$I_B << I_C \text{ for all transistors}$$

then :

$$R5 = \frac{V - -\phi}{I5} - 500\ \Omega$$

where: R5 is the resistor between Pin 5 and ground
ϕ = 0.75 at T_A = +25°C

The MC1496 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common–Mode Quiescent Output Voltage

$$V6 = V12 = V+ - I5\ R_L$$

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector–base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V6, V12) - (V8, V10)] \geq 2 \text{ Vdc}$$
$$30 \text{ Vdc} \geq [(V8, V10) - (V1, V4)] \geq 2.7 \text{ Vdc}$$
$$30 \text{ Vdc} \geq [(V1, V4) - (V5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V6 = V12,\ V8 = V10,\ V1 = V4$$

Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21C = \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \Bigg| V_o = 0$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21S = \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \Bigg| V_c = 0.5 \text{ Vdc},\ V_o = 0$$

Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

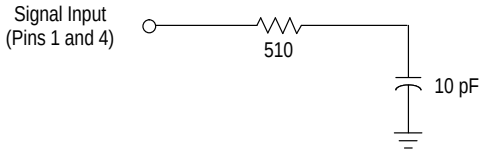
The output signal is taken from Pins 6 and 12 either balanced or single–ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single–ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source–tuned circuits that cause the oscillation.



An alternate method for low–frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

Figure 5. Carrier Rejection and Suppression

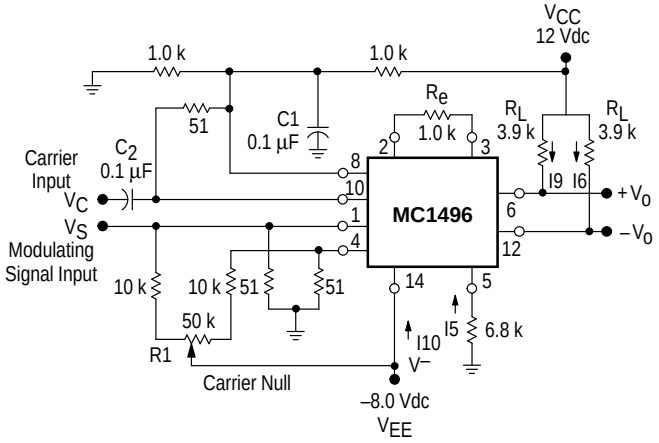
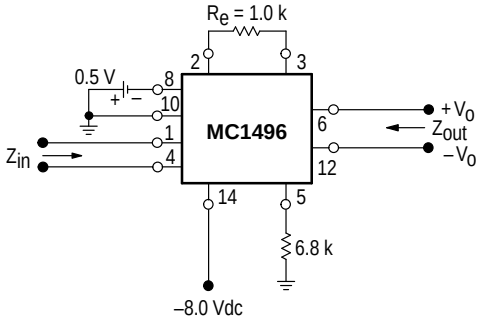


Figure 6. Input–Output Impedance



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

Figure 7. Bias and Offset Currents

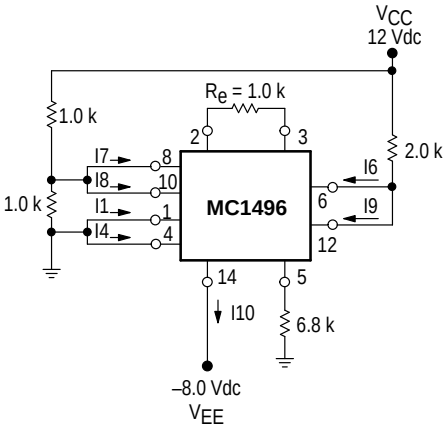


Figure 8. Transconductance Bandwidth

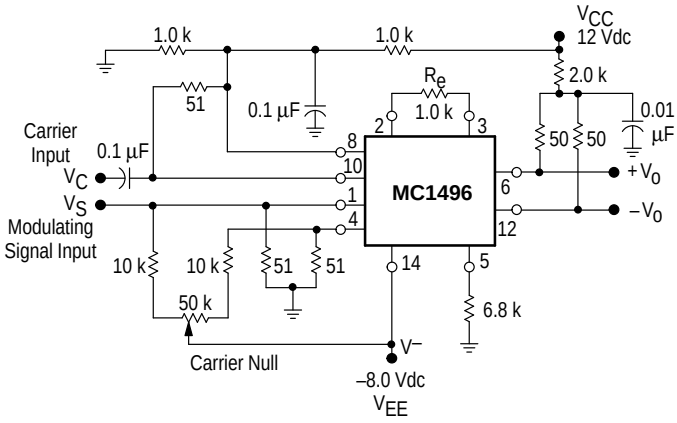


Figure 9. Common Mode Gain

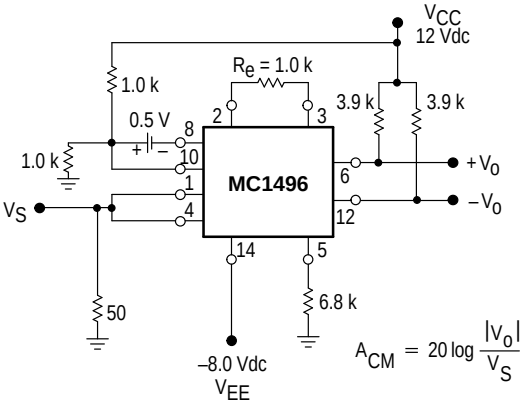
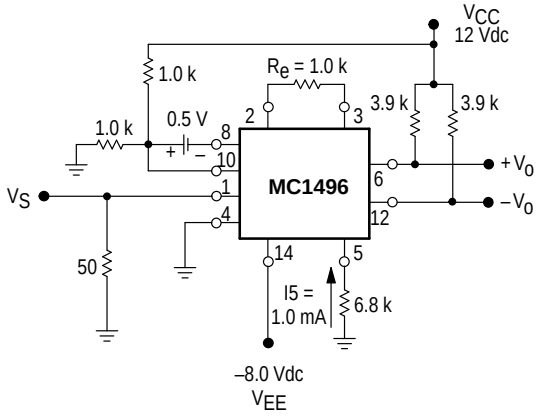


Figure 10. Signal Gain and Output Swing



TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

Figure 11. Sideband Output versus Carrier Levels

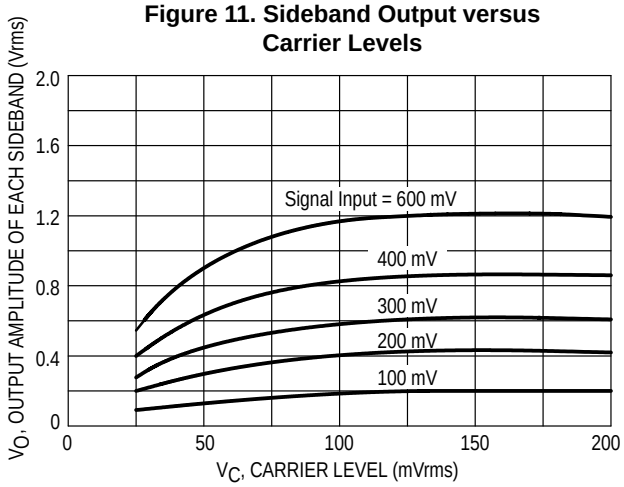


Figure 12. Signal–Port Parallel–Equivalent Input Resistance versus Frequency

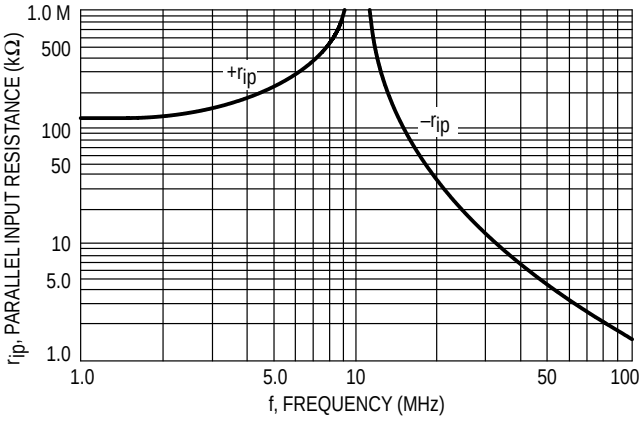


Figure 13. Signal–Port Parallel–Equivalent Input Capacitance versus Frequency

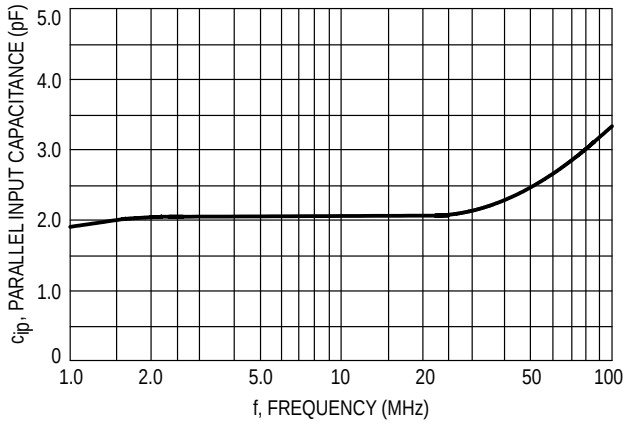
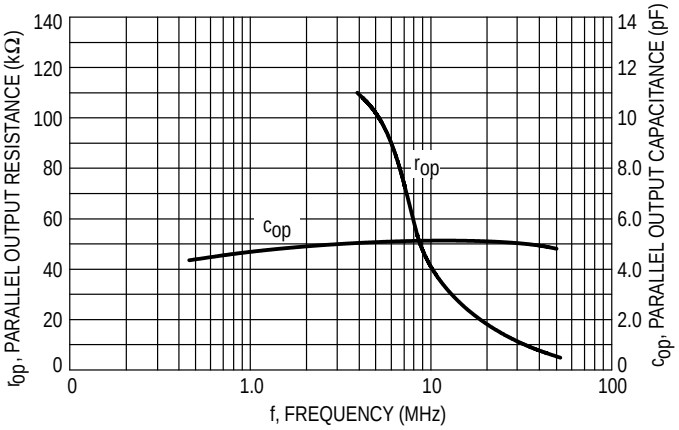


Figure 14. Single–Ended Output Impedance versus Frequency



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

Figure 15. Sideband and Signal Port Transadmittances versus Frequency

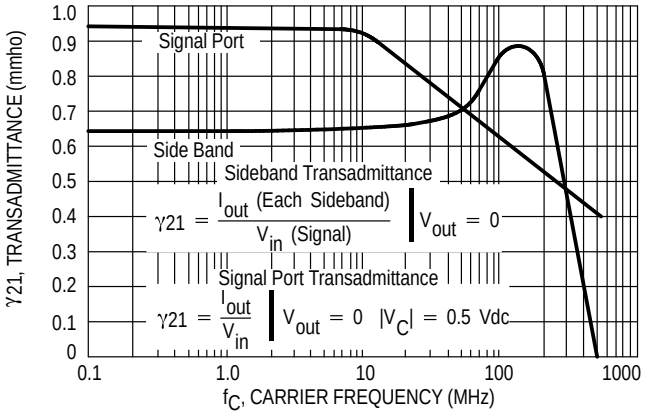


Figure 16. Carrier Suppression versus Temperature

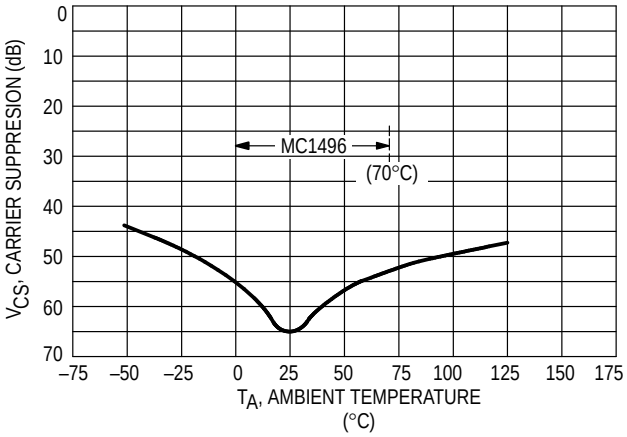


Figure 17. Signal–Port Frequency Response

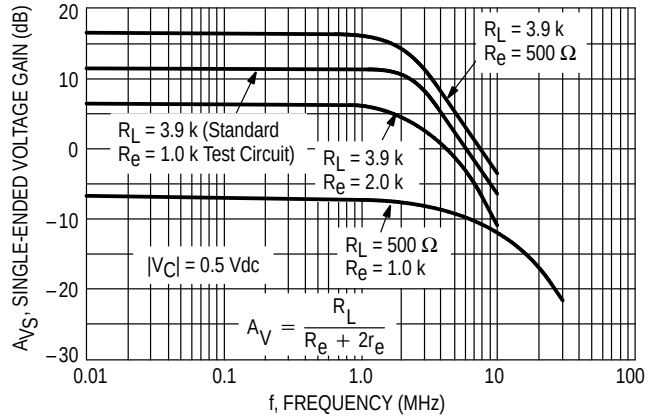


Figure 18. Carrier Suppression versus Frequency

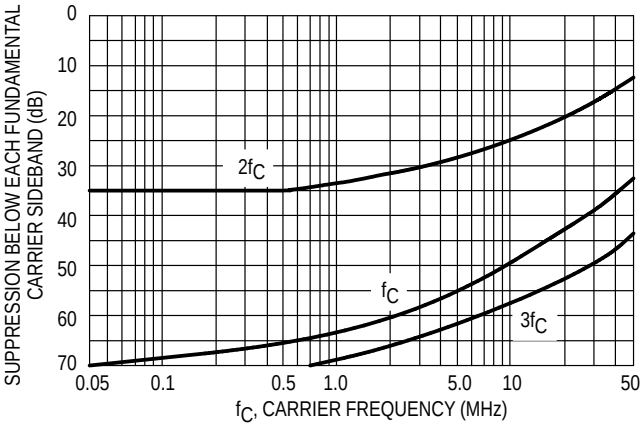


Figure 19. Carrier Feedthrough versus Frequency

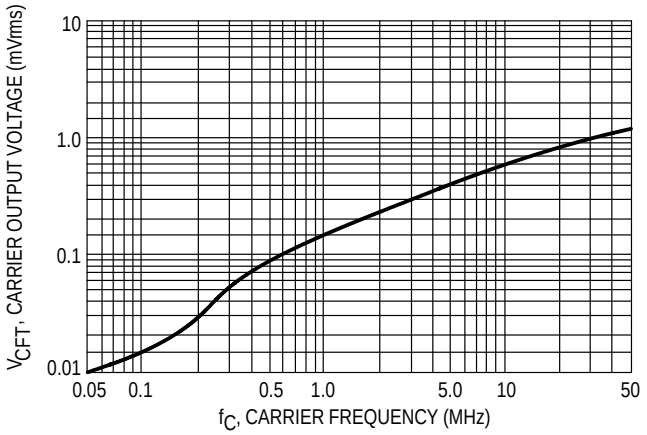


Figure 20. Sideband Harmonic Suppression versus Input Signal Level

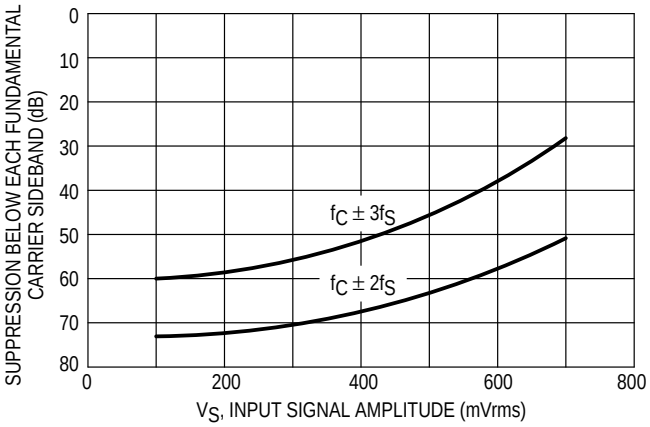


Figure 21. Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

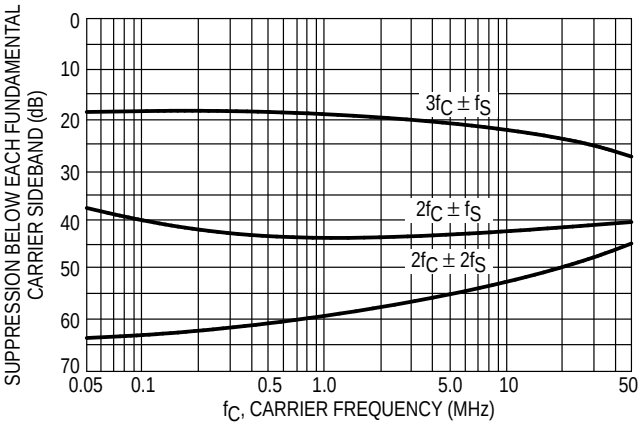
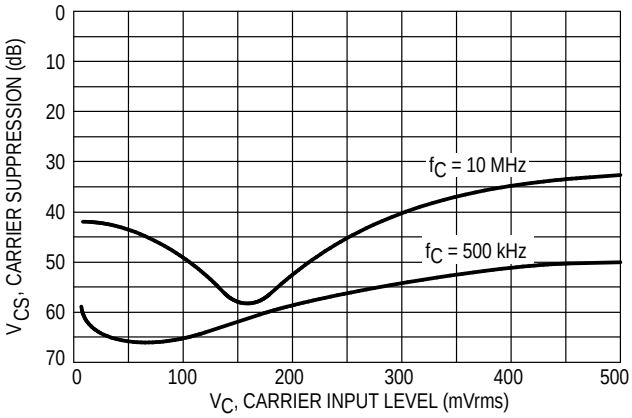


Figure 22. Carrier Suppression versus Carrier Input Level



OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross–coupled so that full–wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low–level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high–level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I5)\ (R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

Figure 23. Circuit Schematic

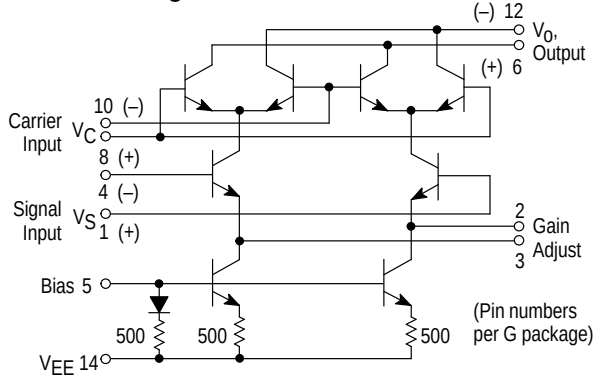


Figure 24. Typical Modulator Circuit

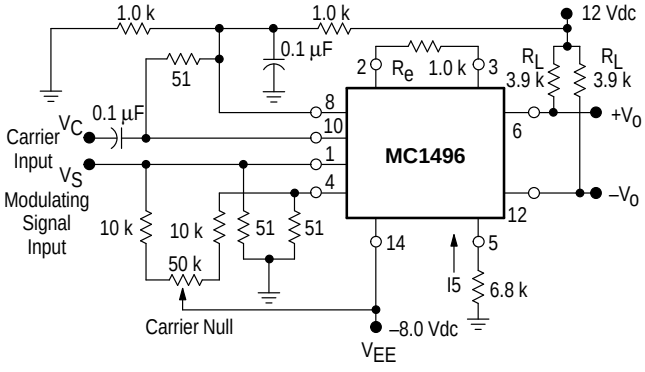


Figure 25. Voltage Gain and Output Frequencies

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low–level dc	$\frac{R_L\ V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High–level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low–level ac	$\frac{R_L\ V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High–level ac	$\frac{0.637\ R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

NOTES: 1. Low–level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single–ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between Pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at 25°C;

$$re \approx \frac{26\ mV}{I_5\ (mA)}$$

7. K = Boltzmann′s Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ mV\ at\ room\ temperature$$

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low–level modulating signal input and the following carrier input conditions:

1) Low–level dc
2) High–level dc
3) Low–level ac
4) High–level ac

These gains are summarized in Figure 25, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on Pins 8 and 10 should be increased to 1.0 μF. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential

amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1496 will function as a phase detector. High–level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

Figure 26. Balanced Modulator (12 Vdc Single Supply)

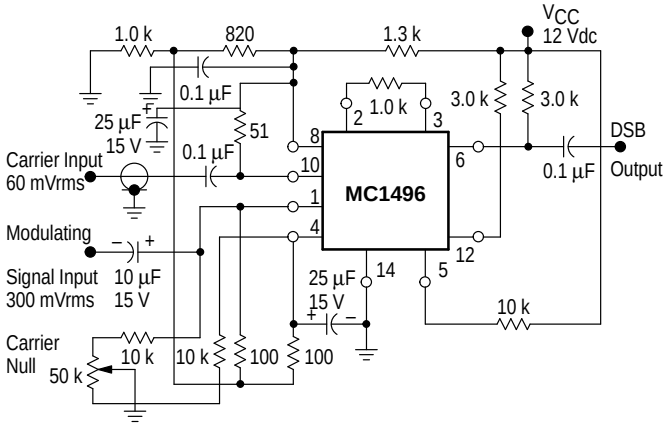


Figure 27. Balanced Modulator–Demodulator

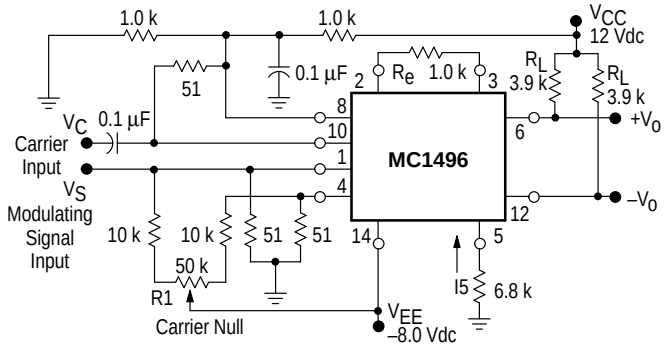


Figure 28. AM Modulator Circuit

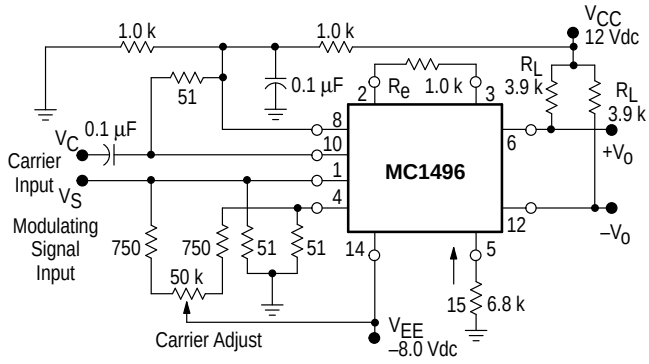


Figure 29. Product Detector (12 Vdc Single Supply)

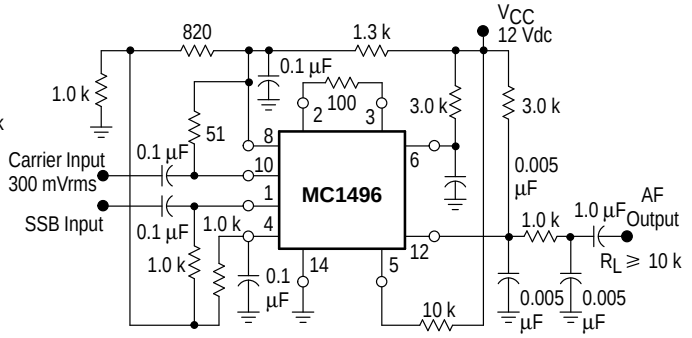
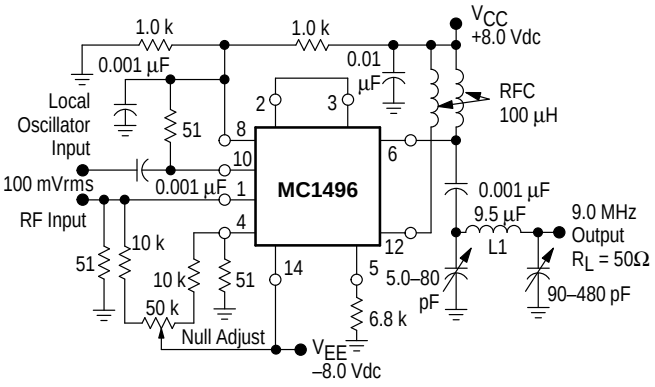


Figure 30. Doubly Balanced Mixer (Broadband Inputs, 9.0 MHz Tuned Output)



L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44–6 Toroid Core.

Figure 31. Low–Frequency Doubler

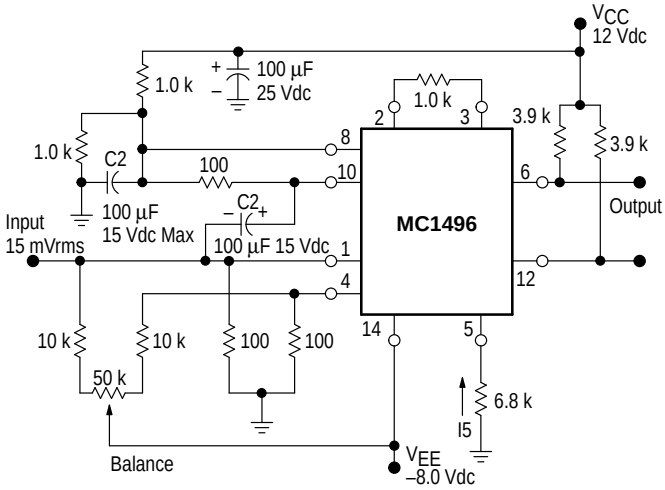
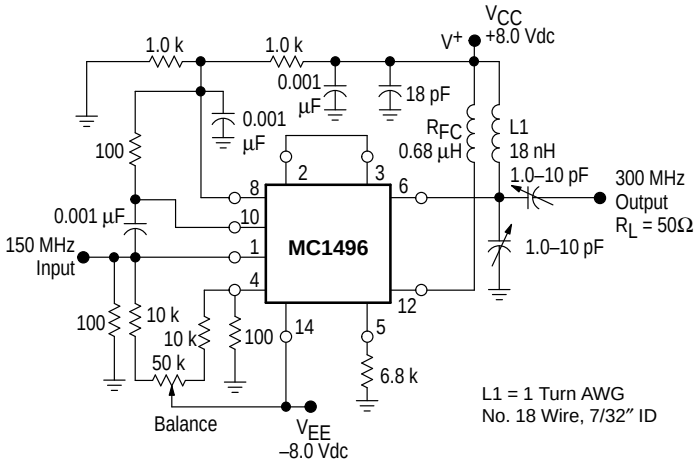
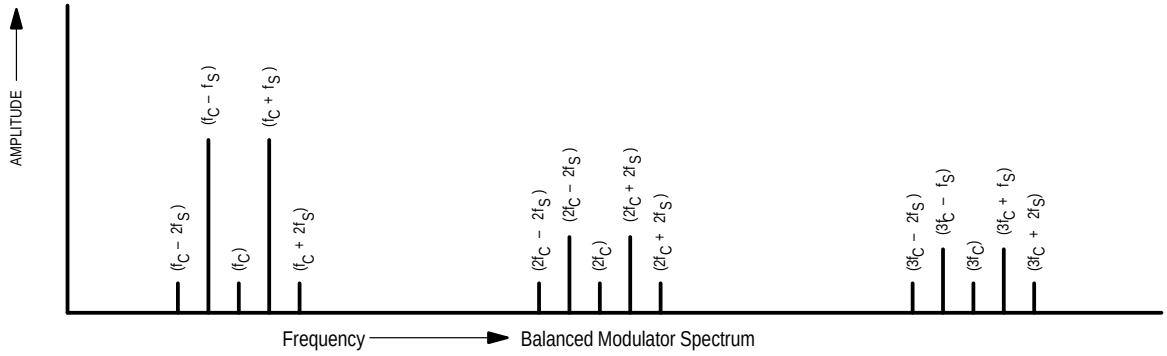


Figure 32. 150 to 300 MHz Doubler



L1 = 1 Turn AWG No. 18 Wire, 7/32″ ID



DEFINITIONS

f_C	Carrier Fundamental	$f_C \pm nf_S$	Fundamental Carrier Sideband Harmonics
f_S	Modulating Signal	nf_C	Carrier Harmonics
$f_C \pm f_S$	Fundamental Carrier Sidebands	$nf_C \pm nf_S$	Carrier Harmonic Sidebands