1 Supply Modelling Basics for High-Speed IC Design

The purpose of this text is to provide a basic representation of power supply networks in a way that is useful for circuit design. With the intuition obtained from this representation, the reader should be able to make informed decisions with respect to the decoupling strategy. These concepts can be applied at all stages of the design, starting with individual circuit blocks on the IC itself, adjacent on-die power grids, package-level supply networks, and also board-level traces, planes, capactiors, etc. leading all the way to back to the regulators.

1.1 First-Order On-Die Supply Network Model

To avoid paralysis from an overwhelmingly large number of possible supply network configurations, it is best to start with a simple first-order model (Fig. 1):

- Ideal short between all $VDDx$/VSS package pins on the PCB side.
- Ideal short between all $VDDx$/VSS pins on the die side.
- Ideal voltage supply feeding $VDDx$/VSS package pins on the PCB side.
- Purely inductive package characteristics between the pins located on the PCB interface, and those on the wafer (die) pads.

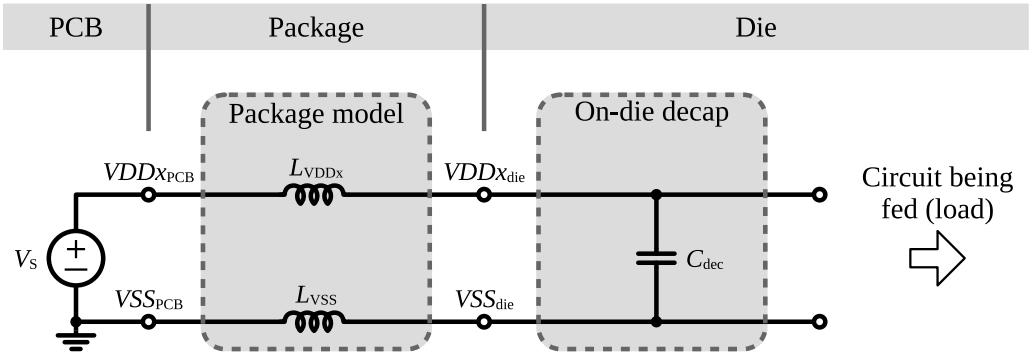

Figure 1: First-order supply model with on-die decoupling.

Note that we can lump together $L_{\mathrm{pkg}} = L_{\mathrm{VDD}} + L_{\mathrm{VSS}}$ while still maintaining the correct I–V relationships between $VDDx_{\mathrm{die}}$ & VSS_{die} (Fig. 2). In fact, the 2-port network representation of the package model remains unchanged by this transformation.

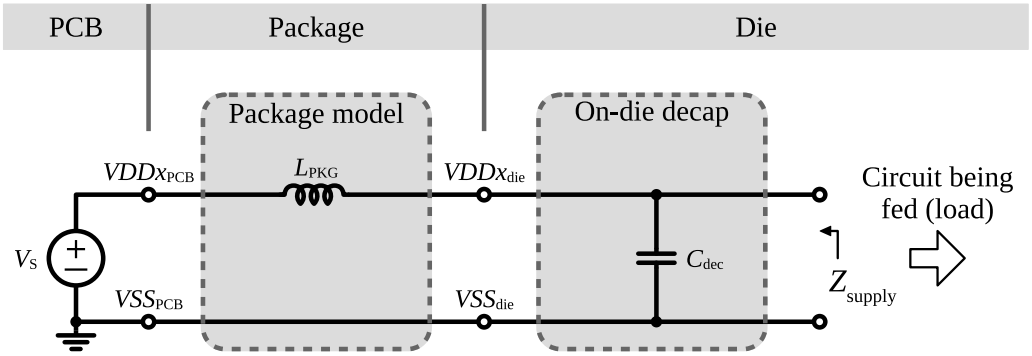

Figure 2: *Simplified* first-order supply model (L_{pkg}) with on-die decoupling.

The principal advantage of this L_{pkg} reduction is that simulators typically have less difficulty computing complex circuit responses when circuits are connected directly to node 0 (ground). It also visually simplifies the supply model a bit. Admittedly, applying such a simplification to a *4-port representation* of the package would hide certain non-critical supply

behaviours (most notably VDD_{die}–VSS_{die} common-mode bounce). In other words, the main drawback to using a single effective L_{pkg} is to lose sight of the VSS_{die} supply bounce relative to VSS_{PCB} (which people often imagine represents the "real" ground).

1.2 Supply Output Impedance, Z_{supply}

A good way to visualize supply network characteristics is through the supply impedance observed looking in from its connection to the load circuit. Ideally, the supply should exhibit little voltage variation when the load circuit draws current. This is the reason designers are interested in the $I \Rightarrow V$ (or impedance) relationship at the load.
By selecting reasonable parameters for the model in Fig. 2, the supply impedance profile in Fig. 3 is obtained:

- $L_{\text{pkg}} = 250\,\text{pH}$.
- $C_{\text{dec}} = 10\,\text{nF}$.

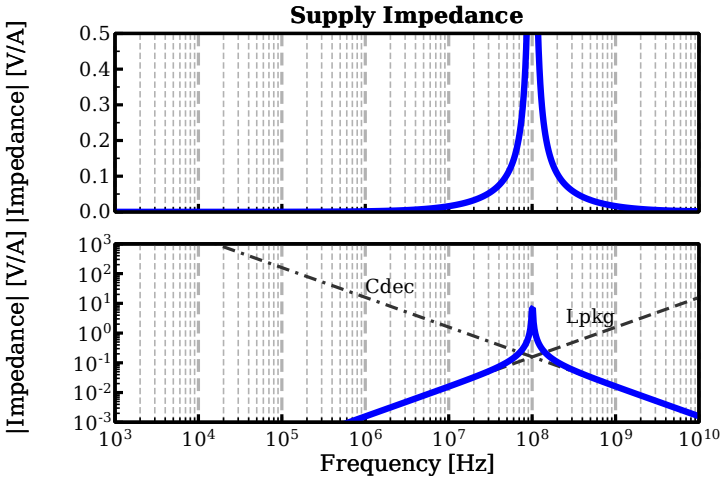

Figure 3: Supply impedance of first order model in Fig. 2.

Those familiar with supply decoupling solutions will notice Fig. 3 exhibits significant resonance at $100\,\text{MHz}$. This effect is undesireable.

1.3 Adressing the High-Q Resonance

To reduce the resonant effect observed in Fig. 3, one must de-Q the supply at $100\,\text{MHz}$. A simple way to achieve this is to add a shunt resistor, R_{damp}, in parallel with C_{dec}. Unfortunately, this solution would draw an unacceptable amount of power from the supplies. To circumvent this issue, a large DC-blocking capacitor, C_{damp}, is added in series with the damping resistor, as illustrated in Fig. 4.

A practical design point for this damped solution is to target a value of $Q = 1$. If we ignore the DC-blocking C_{damp}, it is straightforward to find a reasonable value for R_{damp} given that:

$$Q \triangleq \left| \frac{\text{Im}\{Y\}}{\text{Re}\{Y\}} \right| \tag{1}$$

Substituting in our parallel decoupling impedance, $Y = 1/R_{\text{damp}} + j\omega C_{\text{dec}}$, we get:

$$Q_{\text{damp}} = \frac{\omega_{\text{res}} C_{\text{dec}}}{1/R_{\text{damp}}} \tag{2}$$

The target value for our damping resistor is therefore obtained directly by letting $Q = 1$:

$$R_{\text{damp}} = \frac{1}{2\pi f_{\text{res}} C_{\text{dec}}} \tag{3}$$

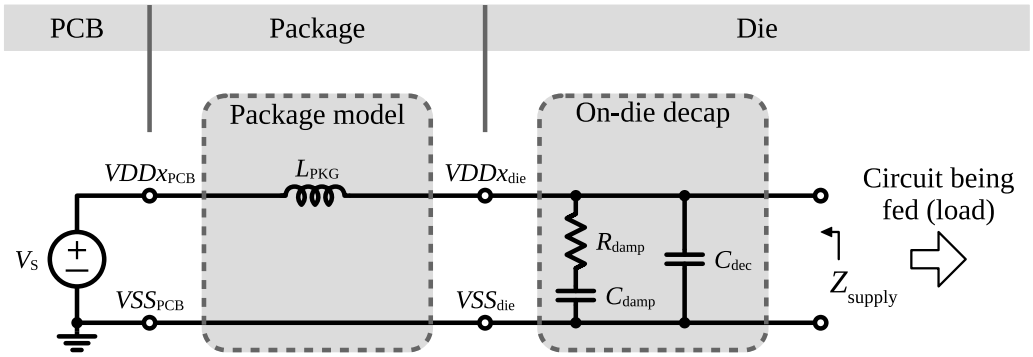

Figure 4: First-order supply model with *damped* on-die decoupling (C_{damp}).

Finally, to ensure the R_{damp}–C_{damp} branch is dominated by R_{damp} @ f_{res}, we simply need to select a value of $C_{\mathrm{damp}} \gg C_{\mathrm{dec}}$ (a factor of 5 seems reasonable). Thus, we obtain the following new component parameters for our decoupling solution:

- $R_{\mathrm{damp}} = 0.159\,\Omega$.
- $C_{\mathrm{damp}} = 5C_{\mathrm{dec}} = 50\,\mathrm{nF}$.

The impedance profile for this newly damped supply response is given in Fig. 5.

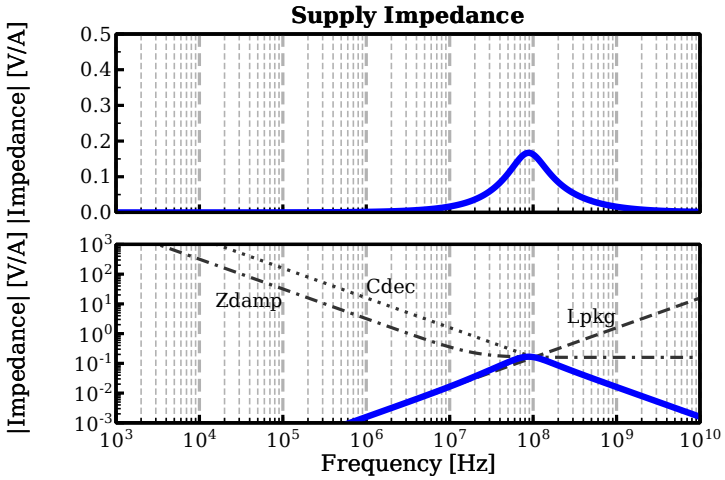

Figure 5: Supply impedance of the (damped) first order model in Fig. 4.

2 Discrpancies in First-Order Capacitor Model

Experienced supply designers might be wary of a certain feature missing from the impedance profile in Fig. 5: Typical impedance profiles for discrete decoupling capacitors tend to rise with increasing f. This is due to the physical length of the capacitor, resulting in a corresponding parasitic (effective) series inductance (ESL). The first-order RLC model in Fig. 6 captures this effect with L_{ESL}. The net impedance profile for this first-order model exhibits the characteristic ”V” shape observed in discrete capacitors.

To compensate for parasitic L_{ESL}, supply networks typically resort to adding multiple discrete bypass (decoupling) capacitors for each chip on the PCB. Bypass capacitors with staggered frequency responses tend to be selected in a way that maintains a low impedance profile at the chip pins (Fig. 7).

Ideally, on-chip capacitors should be located *very* close to the load circuit to ensure negligible values of L_{ESL}. It therefore follows that our models for on-die decoupling capacitors need not exhibit the characteristic ”V” impedance profile (at least not to a first-order).

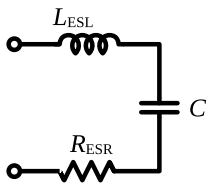

Figure 6: First order model of a discrete decoupling capacitor component.

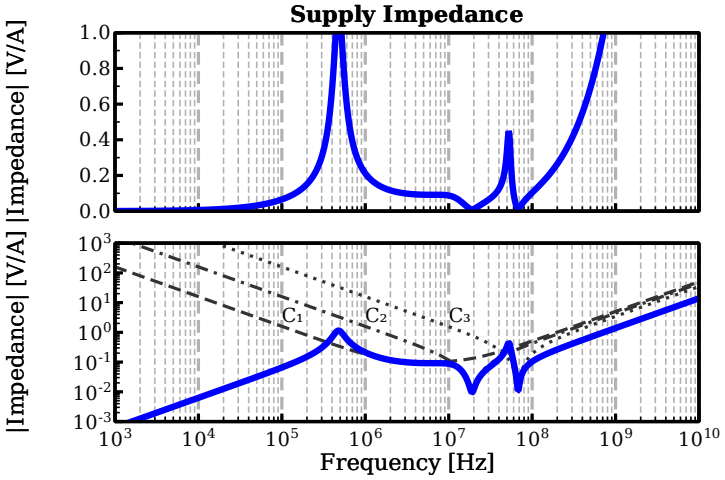

Figure 7: PCB-level supply impedance profile (incl. discrete decoupling capacitors).

3 An Intuition for Supply Transients

A good way to build up an intuition for supply transients is to experiment with realistic transient current profiles generated by actual circuits. You don't need fancy 2.5D/3D models of the power supply networks to get userful results. Even the simple first-order model from Fig. 4 can be very insightful. Note that, to minimize the complexity of your simulation, it is often sufficient to supply the circuits with an ideal voltage source. The resulting current profiles should remain representative of the actual draw on the supply newtwork. A rough schematic for such a simulation testbench is provided in Fig. 8.

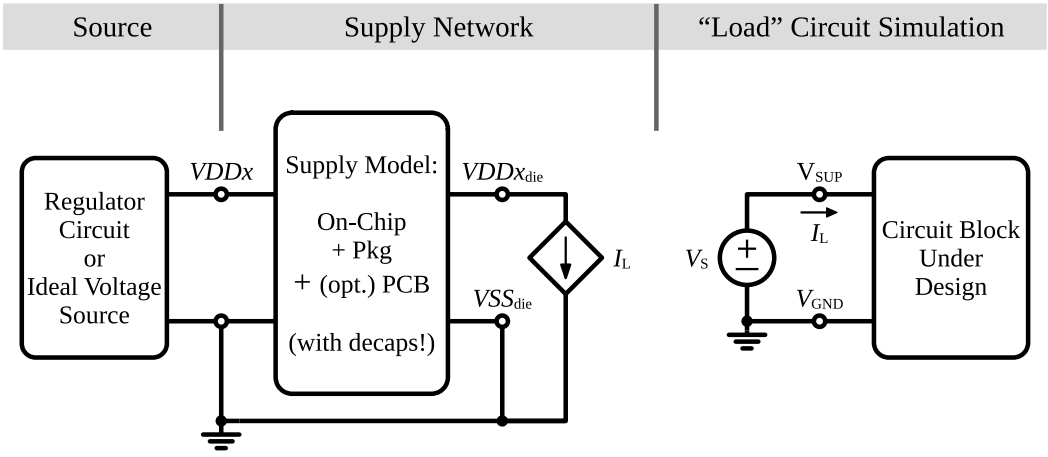

Figure 8: Testbench for supply transients using realistic current profiles.

For reference, Fig. 9 includes simulation results for a trivial circuit toggling a $400\,\mathrm{fF}$ load through $50\,\Omega$ pull-up/down resistors. Note that the VDD–VSS supply exhibits quite a bit of peak-to-peak bounce since it is relies on a little on-die

decoupling ($C_{\text{dec}} = 1\,\text{pF}$). In fact, a small value of C_{dec} was specifically chosen to ensure the resultant supply bounce was clearly visible.

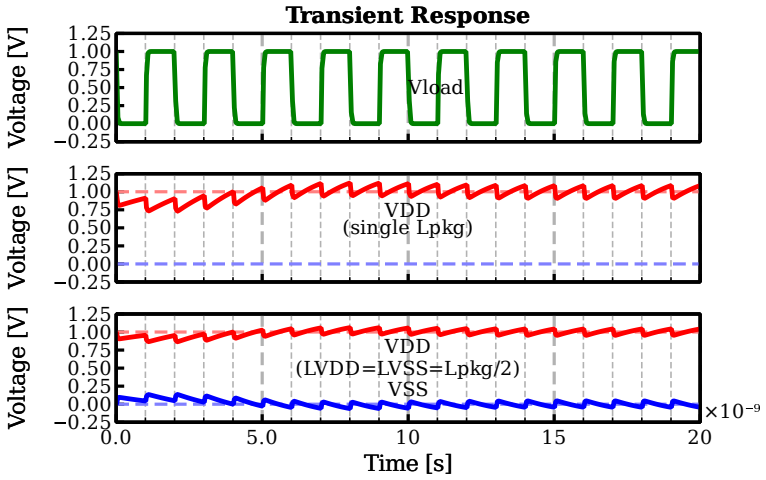

Figure 9: Supply transients for 1 ns–periodic toggle of a 400 pF load through 50 Ω pull-up/down resistors.

For completeness, the supply response generated by leaving modelled package inductances in their respective VDD & VSS paths is included in the bottom-most graph of Fig. 9 (assumes $L_{\text{VDD}} = L_{\text{VSS}} = L_{\text{pkg}}/2$). As might be expected, this model shows how supply bounce is actually shared between the two supply nets, while nonetheless exhibiting the same differential $VDD - VSS$ signature computed for the combined–L_{pkg} simplification.

4 Co-design Strategy: A 3-Step Process

It is normally bad practice to wait until top-level chip assembly to start adding components like decoupling capacitors. When tapeout approaches, designers are already busy scrambling to tie up other loose ends. Having an effective means of integrating a decoupling solution during the design stage of individual circuit blocks would be much more productive.

4.1 Critical assumption: f_{res} is known

Typically, little is known about the power supply network during the block-level design stage. A reasonable starting point is therefore to assume the value of f_{res} is known. Since many practical designs appear to exhibit a $100 - 250\,\text{MHz}$ resonance between the on-die decoupling capacitance & the series supply inductance (f_{res}), it seems reasonable to start designing for something like:

$$f_{\text{res}} = 100\,\text{MHz} \tag{4}$$

With a reasonable value of f_{res} in hand, designers can assign a certain amount of decoupling to each individual circuit block ($C_{\text{dec}}^{\text{blk}}$), then compute the package inductance "allocated" to those same blocks ($L_{\text{pkg}}^{\text{blk}}$). Similarly, a shunt damping resistor ($R_{\text{damp}}^{\text{blk}}$) can be computed, along with its DC-blocking capacitance. The relevant model equations are provided below for reference:

$$L_{\text{pkg}}^{\text{blk}} = \frac{1}{(2\pi f_{\text{res}})^2 C_{\text{dec}}^{\text{blk}}} \tag{5}$$

$$R_{\text{damp}}^{\text{blk}} = \frac{1}{2\pi f_{\text{res}} C_{\text{dec}}^{\text{blk}}} \tag{6}$$

$$C_{\text{damp}}^{\text{blk}} = 5C_{\text{dec}}^{\text{blk}} \tag{7}$$

4.2 The 3-Step Decoupling Strategy

The co-design strategy proposed in this text requires adding decoupling capacitors during the block-level simulation & layout steps. Specifically, the following 3 steps should be applied for each designed block:

1. Pick an arbitrary initial value of $C_{\mathrm{dec}}^{\mathrm{blk}} = 1\,\mathrm{pF}$, and co-simulate the supply signature corresponding to the operation of said circuit (Apply testbench described in Fig. 8 with first-order package model from Fig. 4).
2. Determine the scaling factor, k, that reduces supply bounce to within acceptable limits.
3. Add high-Q decoupling capacitors to meet this $C_{\mathrm{dec}}^{\mathrm{blk}} = k \times 1\,\mathrm{pF}$ requirement *inside* the block-level layout (do not wait for top-level assembly).

4.3 Placement of On-Die Decoupling Capacitors

To ensure optimum effectiveness of the high-Q decoupling capacitors supplying higher-frequency transient currents, all devices associated with $C_{\mathrm{dec}}^{\mathrm{blk}}$ should be located right next to the supplied blocks. Associated supply metalization should also be generous and short in order to minimize both series inductance and resistance.

On the other hand, damping capacitors C_{damp} (and assoicated R_{damp}) can be located further away, provided the distance does not result in excessive levels of parasitic inductance (ESL). In other words, parasitic series inductance must not degrade the ability of damping resistors/capacitors to de-Q the package–C_{dec} resonator.

5 Designing Outwards: IC⇒PCB⇒Regulator

To generate more accurate representations of impedance profiles and supply transients, the basic process outlined in this text can be repeated with the following refinements:

- 1st order PCB supply model + decoupling devices.
- 2.5D/3D package parasitics (+ decoupling, if present).
- 2.5D/3D PCB supply model + decoupling devices.
- Schematic model of the regulator block.

6 Supplemental Reading Material

Suggested reading:
[1][2] [3][4][5] [6]

References

[1] B. Carter, “How (not) to decouple high-speed operational amplifiers,” Texas Instruments, Application Report, September 2001, SLOA069.

[2] A. Martin, “Decoupling: Basics,” AVX Corporation, Technical Paper, S-DB2.5M1194-C.

[3] “Decoupling techniques,” Analog Devices, Tutorial, 2009, MT-101.

[4] H. Zumbahlen, “Staying well grounded,” Analog Devices, Tech. Rep., June 2012, Analog Dialogue 46-06.

[5] W. Kester, “Grounding and decoupling: Learn basics now and save yourself much grief later! (Part 2: Decoupling),” Analog Devices, Tech. Rep., April 2017, Analog Dialogue 51-04.

[6] “Choosing and using bypass capacitors,” Renesas, Application Note, October 2011, AN1325.