

Group 8 - 500Hz PWM

ECE 4901 – CMOS Fundamentals
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Project Overview

The task for this group project was to create a PWM controller with 500Hz clock and 5% to 95% duty cycle control. This project aims to utilize the WPI666 CMOS replacement of the LM555 timer to create and simulate the parameters of a PWM controller operating at 500Hz. The controller will adjust the input's duty cycle to vary from 5% to 95%. Each section of this PWM (Oscillator, PWM) will have their parameters reported along with their test benches. The full modulator, its layout, and its test bench is also showcased.

Design Approach

Work began with hand calculations supported by the reference calculators linked in the assignment overview. These tools provided starting values for the timing network, which we then cross-checked against typical 555 operating limits and component ranges. Baseline resistor and capacitor values were selected to keep charge and discharge currents moderate, as to avoid excessively large capacitors that slow recovery. With provisional values established, the design was prepared for parametric sweeps, but only after the operating behavior of the device was reviewed to ensure that later adjustments would be done in the correct timing relationships.

The 555 timer operates using two internal thresholds at one third and two thirds of the supply voltage, a pair of comparators, an SR latch, and a discharge transistor. Its behavior is commonly used in two modes. In monostable mode, a negative trigger pulse sets the output high and allows the timing capacitor to charge through a resistor until the upper threshold is reached. The latch then resets, the output returns low, and the discharge transistor rapidly empties the capacitor, establishing a single, well-defined pulse width. In astable mode, the capacitor alternately charges and discharges between the lower and upper thresholds through a two-resistor network. The charge path uses the series sum of the resistors, and the discharge path uses the

lower resistor and the internal discharge transistor. This produces a continuous square wave whose frequency and duty cycle depend on the chosen resistor and capacitor values.

Guided by these operating characteristics, we used a monostable operation to size the timing network for the PWM one-shot, giving a fixed pulse width set by a resistor R and capacitor C. For the free-running clock, we used an astable operation to generate the required oscillation frequency and duty cycle. This partition lets us tune pulse width and carrier frequency independently during parametric analysis and layout.

Design proceeded under the following assumptions and requirements:

1. The PWM output must span 5% to 95% duty cycle.
2. The carrier frequency is 500 Hz.
3. The oscillator is solely responsible for generating this 500 Hz waveform from a constant DC supply, with no external pulsed or function-generator sources in simulation.
4. All frequency generation occurs within the 555 block so the output does not depend on any stimulus outside the design.

With these targets set, development was broken into two modules: a free-running oscillator and the PWM stage. Each module received its own testbench. For the PWM testbench, the oscillator output was abstracted as an ideal 500 Hz square wave at 66% duty to exercise the comparator thresholds and one-shot behavior. For the oscillator testbench, only DC rails were applied and the expected outcome was a self-sustained output near 500 Hz. This structure enabled focused verification of timing relationships and simplified fault isolation.

The separation also supported parallel work. Two team members ran parametric sweeps on each module to determine resistor and capacitor values and to set the control and compensation voltages. In parallel, two others advanced the layout of each block. The fixed 500 Hz in the PWM bench allowed the schematic designer to debug the modulator without the effects from an evolving oscillator. The oscillator team could then confirm start-up, frequency stability, and amplitude independently, ensuring that the integrated WPI666 met specification.

Simulation results matched expectations. The oscillator produced approximately 500 Hz within a $\pm 10\%$ tolerance. A compensation voltage of 2.03 V was selected based on parametric sweeps and on prior optimization of the differential pair from the operational-amplifier lab. The oscillator duty cycle was not treated as a critical parameter because the PWM stage regulates effective duty via the control-voltage pin. The oscillator was therefore tuned for frequency accuracy and reliable start-up, while the PWM stage was tuned to optimize the full 5% to 95% duty-cycle range.

Simulation and Results

Pre layout - Simulations and Schematics

In the pre-layout of the oscillator, each parameter was measured using a 50 millisecond transient sweep of the schematic. The power was found utilizing the browser tab of the resulting figures. The frequency of the output can be found by putting vertical markers from the falling edge of the first signal to the falling edge of the next, before taking that period and inverting the value. The oscillator should provide the signal, whose duty cycle is altered by the control voltage of the modulator. Two bits are implemented here as a proof of concept, although additional D-Flip Flops (DFF) could be added should the need arise. In order to achieve the 50 width-length ratio, NMOS transistor M2 has a width of 2.5 μ and a length of 500 nano at 10 fingers, achieving the desired size. The PMOS transistor M1 has a width of 2.5 μ and a length of 2 μ at 10 fingers for a width-length ratio of 25.

For the full scale schematic, which involved combining the oscillator and pulse width modulator blocks(block meaning the separate WPI666 timers and their supporting resistors, capacitors, and sources required for correct operation), the main task was to ensure a correct output from the oscillator and to test voltage range input into the control pin of the PWM block, which would dictate the duty cycle of our PWM output. Because of the relatively low-frequency nature of our specified 500Hz oscillator we were able to use the direct output of the oscillator block without any need for the frequency divider pins.

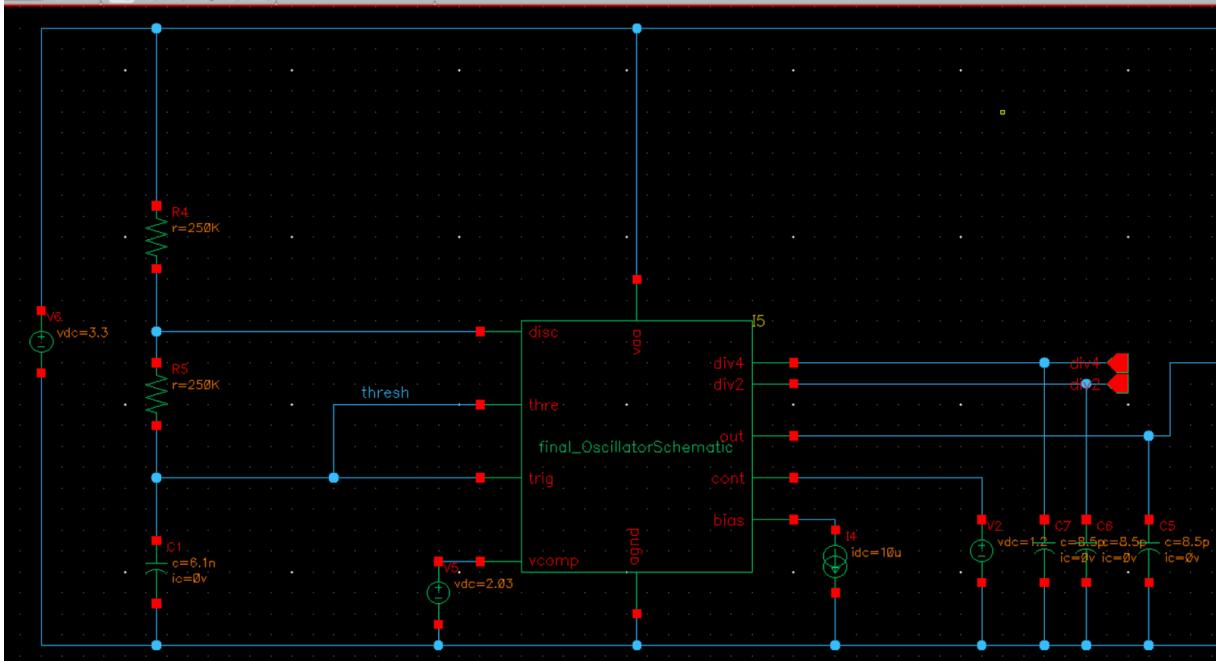


Figure 1: Testbench Schematic setup for Oscillator block

Values for R4 and R5 were chosen arbitrarily, while C1 was calculated using the provided calculators, before later being tuned to be as close as possible to 500Hz. Our biasing voltage of 2.03 V was decided as mentioned earlier by use of parametric sweep, while our biasing current was as recommended in the project proposal document.

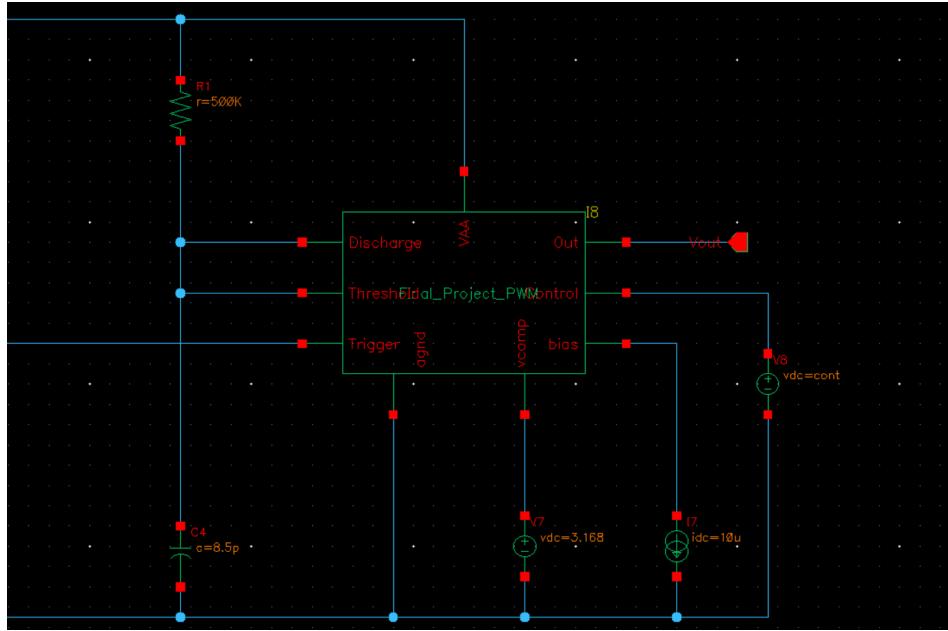


Figure 2: Testbench Schematic setup for PWM block

Again, parametric sweeps were used to find ideal biasing voltage at VComp, as well as voltage range for the control pin, which will subsequently control the pulse width of our system.

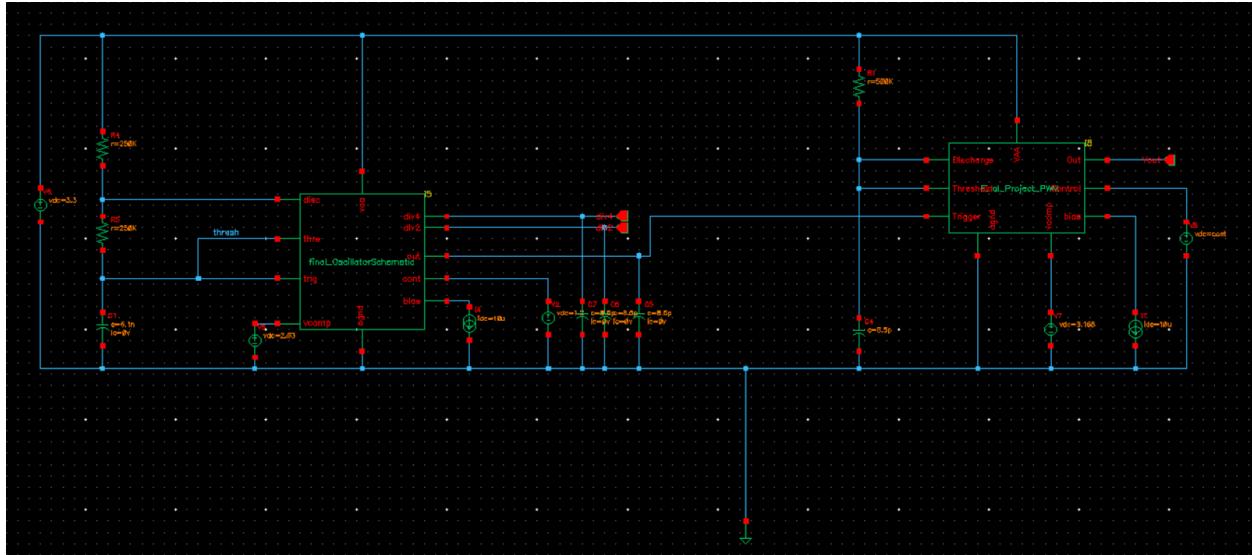


Figure 3: Full Testbench Schematic

Connected, the two make up our full testbench schematic which was used for both pre-and post layout simulation.

Layout - Theory

The WPI666 layout integrated the previously constructed operational amplifier with the digital control and passive elements. The floorplan comprised matched PMOS and NMOS transistor arrays, an SR latch, a chain of D flip-flops (DFFs), and bias resistors. All physical design work was performed in Cadence Virtuoso Layout Suite XL. The objective was a common-centroid arrangement with symmetry about both axes to support matching, predictable parasitics, and straightforward power distribution.

Dummy transistors were placed at the edges of each array to equalize proximity effects, improve current balance, and reduce fringe-field parasitics. Guard rings and well ties were inserted to provide substrate isolation and a low-impedance return for noise. Routing prioritized short, orthogonal paths between matched pairs and consistent layer usage for corresponding nets to limit systematic variation. Power and ground rails were implemented primarily on metal-1, with vertical and horizontal segregation used to control coupling and ease pin access.

As shown in Figure 1, the timer core was laid out on one side and mirrored across the centerline, producing a balanced composition. The block measures 30.84 μm in width and 89.205 μm in length for a total area of 2 751.0822 μm^2 . Bias resistors were placed along the lower edge for clean access to global rails and to maintain spacing from sensitive analog nodes. The operational amplifier sits laterally, which simplified symmetry across the center while reserving the interior for timing and control logic.

The SR latch was constructed from the library's NOR221 cells (Figure 2) and abutted to minimize internal interconnect. A divider sub-block was created for the DFF chain (Figure 3). This hierarchical block provides a divide-by-four function for the present design and remains modular, allowing additional stages to be appended if alternative division ratios are required. The modular approach also streamlined concurrent work on schematic refinement and physical layout, since the divider could be verified and placed as a unit.

Figures 1 through 3 compose the full PWM layout shown in Figure 4. The integrated block was exercised with the assignment testbench to confirm connectivity, pin orientation, and expected signal flow prior to sign-off checks. Symmetry about the centroid was preserved through even finger counts in matched devices, mirrored placement of digital cells, and consistent diffusion and poly enclosure. This produced a compact, balanced layout that is prepared for final verification and export.

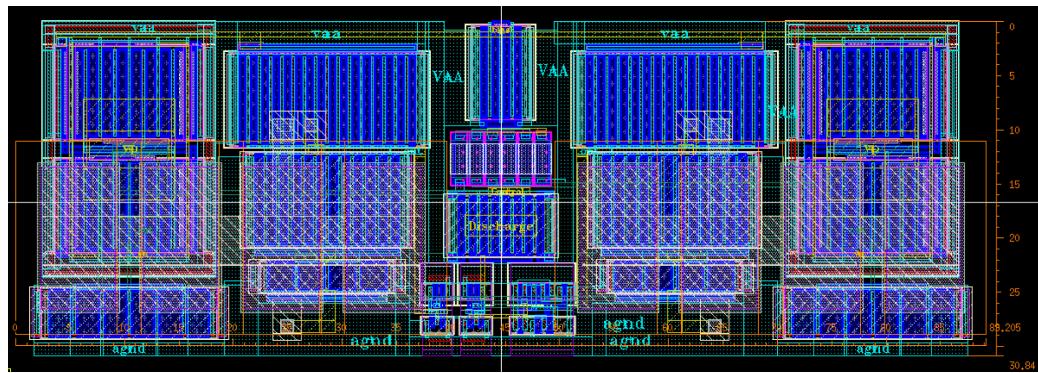


Figure 1: Layout of the WPI666 Timer

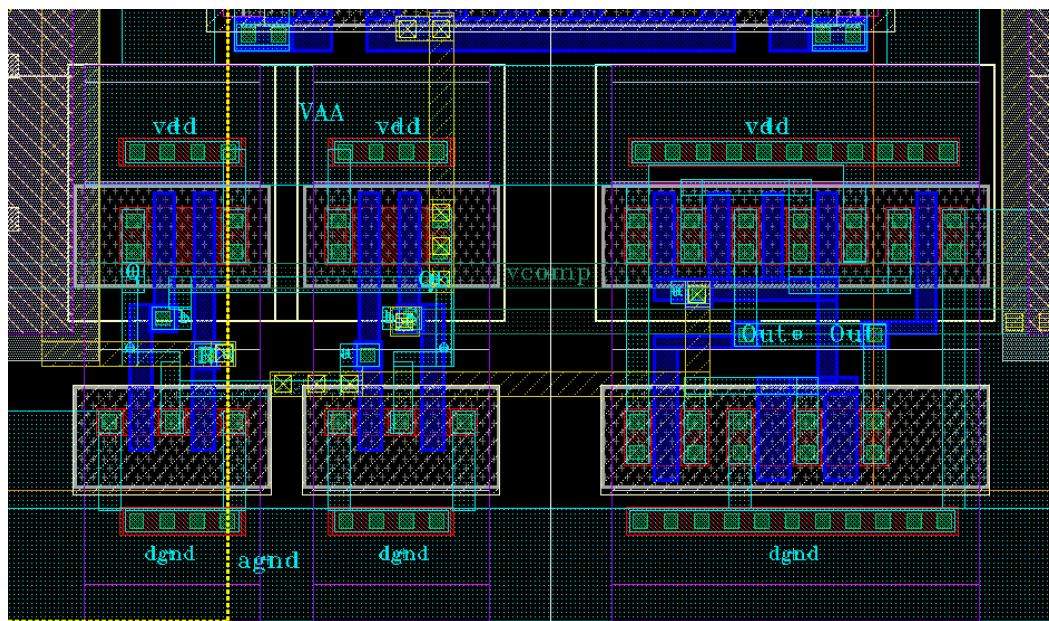


Figure 2. SR Latch Layout

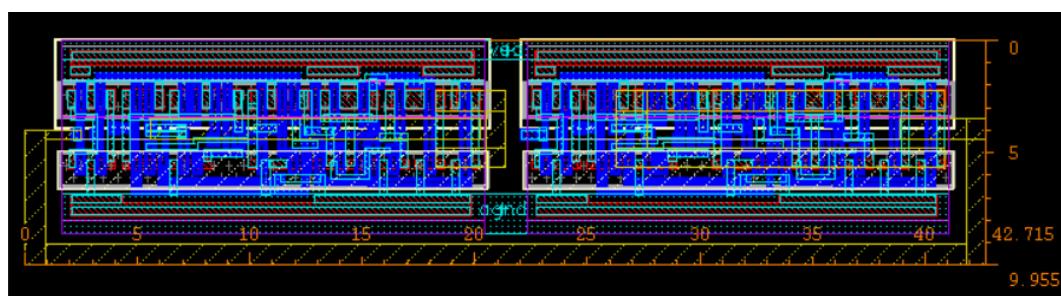


Figure 3: Divider Layout

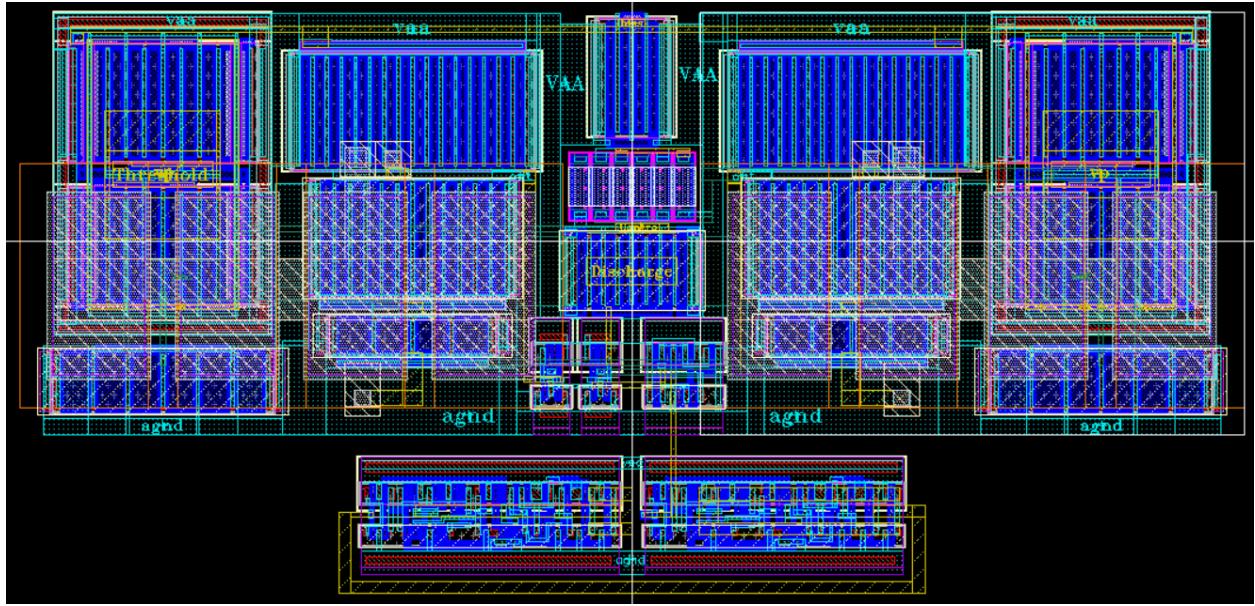


Figure 4: Full PWM Layout

Layout - Result and Alterations to pass DRC / LVS

Design Rule Checks (DRC) were run throughout the WPI666 block layout rather than reserved for the final stage. Continuous verification identified spacing, width, enclosure, minimum-area, and density issues at the point of introduction, which reduced redesign effort. Route widths were standardized, paths were aligned to the routing grid, and via arrays with the required diffusion and poly enclosure were applied. Where clearance was constrained, bends were widened, short jogs were trimmed or patched to meet minimum area, and selected segments were moved to higher metal to increase separation.

The operational-amplifier output stage required the most attention. Contact arrays were centered on source and drain regions, diffusion enclosure was matched across all fingers, and placements were aligned with the principal current path to limit series resistance. Device symmetry was maintained to protect gain and linearity. After each major modification, DRC was re-run and results documented, which kept the layout compliant and ensured consistent connectivity across the block, streamlining the entire process. Initially, the output was made with minimal tolerance between metal 1 regions.

Post Layout - Simulations

Following layout, the testbench used in the pre-layout simulations was recycled and used again in post-layout. Having obtained the biasing and other operating characteristics in the pre-layout simulation, a series of transient simulations was run using a parametric sweep to confirm the behavior of the PWM circuit, with another small transient simulation being run to reevaluate the frequency of the PWM circuit. As done in lab 3, the “Calibre” parameter was added to the environment of the analysis so that ADE L would pull the Calibre files to use during simulation. These Calibre files contain the information from PEX, including the parasitic

capacitors and resistors. It was expected that the parasitics would slightly change the behavior of the final circuit post layout.

Pre Layout Results

Pre layout results showed a promising ability to modulate the pulse width. We were able to achieve a frequency of 501.8 Hz, which we decided at a .36% rate of error was acceptable to continue with, as well as full 0% to 100% duty range at values of 2.7 to 2.95 volts.

Post Layout Results

Post layout, the frequency increased by around 10%, but the PWM characteristics remained largely the same. The intended frequency was 500 Hz, the resulting frequency was 555 Hz. As for PWM, we were able to achieve a full range of 95% to 5% duty cycle, however this occurred between voltages of 2.7 and 2.95. For further control, the R and C values should be modified to better suit the frequency. The R and C values for the time constant of the oscillator or the voltage control for the oscillator could also be changed to retune the frequency to achieve the target frequency and PWM behavior more closely.

Experimental Setup

Using Cadence Virtuoso and TSMC180nm parameters for the transistors and layout models, the WPI666 was created inside the large suite. It was determined based on the specifications of the project that the W/L ratio of M2 should be greater than 50, netting a greater gain between the capacitor's discharge voltage and the SR latch. Running 50 millisecond sweeps on output and the divisions, the oscillator portion used resistor values of $125\text{k}\Omega$ and 7.7nF , as seen in Appendix B, Figure 1. In order to verify the layout, we utilized Calibre and Electronic Design Automation (EDA) tools such as DRC, Layout Versus Schematic (LVS), and Parasitic EXtraction (PEX). After altering the layout to pass both DRC and LVS, the post-layout results will be simulated and denoted in the performance parameters and result tables below.

Oscillator Output Frequency

Open loop measurements were made to evaluate the performance of the designed IC modules. This involved a series of transient measurements because the circuits created involved entirely time-domain performance parameters. The first of these parameters was the output of the oscillator circuit. This was measured by performing a transient simulation for a short period of a couple of milliseconds, in order to capture a reasonable number of periods to view the frequency and the duty cycle of the oscillator, which was targeting 500 Hz.

PWM Duty Cycle Control

The other parameter of interest was related to the other module, specifically the PWM performance. This was not able to be determined with a single number, but rather was a range determined by the input on the control pin of the 555 timer. By applying the appropriate voltages, it is possible to vary the PWM duty cycle which was measured in the time domain by using a transient simulation of a few milliseconds to capture enough periods to observe the behavior of the output waveform. The desired performance target was a PWM variation of between 5% and 95%.

Obtaining the performance characteristics for PWM was more tedious to obtain due to needing to use a parametric analysis to obtain the results. One potential improvement to the process could be to use a time-variant single sweep analysis, but with the limited functionality of the Cadence server at the time, it was easier to just perform a parametric analysis.

Results Summary

The section below indicates the results observed from the completed pulse-width modulator pre-layout and post-layout. These parameters were obtained by running a transient simulation and observing the resulting waveforms, as well as clicking the browser tab, which then yielded the power consumption and voltage gain. We found that by most metrics, - both in pre-layout and post-layout - we were able to complete the goals set by the project requirements. Our PWM circuit operated almost exactly at or within reason for frequency, pulse width, power consumption and layout size goals. We prioritized the 500Hz 95%-5% pulse width, but also found that our power consumption and layout size were both within reason.

Table 1: Summary of Final Transistor Sizes

Transistor	Size	Function
M1	1.0m/50nm	differential input, positive terminal
666 PMOS	32um/500nm	Bias opamps
666 NMOS	40um / 500nm	Bias Discharge

Table 2: Summary of Final Design Specifications

Power consumption is the total static current supplied through VAA times VAA (V).

Total Size goal should be approximated by combining total area of the transistors (A1) and capacitors (A2). Estimate the transistor layout area by using $A1=10*(\text{sum of } [W_s * L_s])$. Area of the capacitance can be approximated by using $A2=\text{sum of } (C_{\text{used}}/5fF)$

Conclusions

Our project overall was successful given the circumstances that we were given to work

Parameter	Goal	Results (schematic)	Goal Achieved?
Oscillation Frequency	500 Hz	501.8 Hz	Yes
PWM 95%-5%	0-3.3V	2.7-2.95V	Partially
Power Consumption	Small, within reason	2.875E-3 W	Yes
Total Layout Size	Small, within reason	N/A	Yes
Parameter	Goal	Results (layout)	Goal Achieved?
Oscillation Frequency	500 Hz	555	Partially
PWM 95%-5%	0-3.3V	2.7-2.93V	Partially
Power Consumption	Small, within reason	2.873E-3 W	Yes
Total Layout Size	Small, within reason	2751 um^2	Yes

under. With limited time and resources and an underpowered server to work on, we made the most out of the project. While not fully meeting specification post-layout, our final product comes very close and with a little bit more tuning, should be 99% accurate to the design.

Project Analysis

This project was insightful into learning how the entire process of CMOS manufacturing from product inception to final layout design occurs. The experience of learning how to function as a team, from processing equations to performing layout and then validation afterwards mirrors that of similar processes done in a real workplace setting. The course as a whole sets up the environment in a similar manner, encouraging the product development process naturally by introducing concepts in the order that they are performed in.

Some critiques of the experience are that there were many shortcomings with the performance of the tools that we were using. While in other classes, software based tools are generally well performing and reliable, the Cadence server that we were given was underperformant at best and absolutely unusable at its worst. In a company setting, this would be extremely costly as engineers experience downtime and therefore their time is wasted. As students trying to learn the software while completing a project such as this one, it was extremely discouraging and a generally negative experience. Additionally, the component of design was never covered thoroughly during the class, and going from just copying schematics to designing your own circuit was not an intuitive transition. Had there been more guidance or a larger set of recommended resources, it may have been more enjoyable and straightforward to complete this project.

The project requirements itself, however, seemed logical and realistic. The presentation requirement was a good method of ensuring that not only do engineers need to understand their circuit, they have to be able to explain it to others as well. Having this as part of the assignment really added to the experience and solidified our understanding of our circuit and the process overall. Such a presentation would be a good analog to a presentation in front of an engineering management or project management team in which the systems engineers or business management get involved, and the skill of explaining to a layperson becomes critical.

Appendix A Schematics

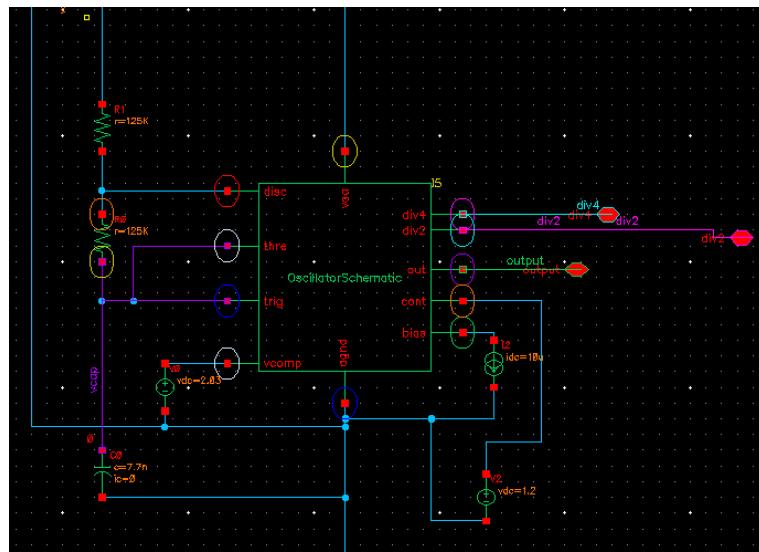


Figure 1. Oscillator Schematic

Appendix B Hand Calculations

Choose Configuration

Astable Monostable

R ₁ Resistor Value	R ₂ Resistor Value		
125	kΩ	125	kΩ

C₁ Capacitance Value

0.0077 μF

Formula

$$T_h = 0.693(R_1 + R_2)C_1 \quad T_l = 0.693R_2C_1$$

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

Time High Time Low

1.3 ms 0.6670 ms

Frequency

499 Hz

The 555 timer circuit is configured as an astable multivibrator. It consists of a 555 timer IC (labeled 8-pin component), two resistors (R1 and R2, both 125 kΩ), and one capacitor (C1, 0.0077 μF). The timer is connected with its pins 7 (DIS), 6 (THR), and 2 (TRIG) tied together and connected to ground. Pin 8 (VCC) is connected to a power source, and pin 1 (GND) is connected to ground. The output signal (OUT) is shown as a square wave with a frequency of 499 Hz. The waveform is labeled "TIME HIGH" for the 1.3 ms period and "TIME LOW" for the 0.6670 ms period.

Figure 1. Resistor and capacitor values

Appendix C

Schematics and Simulation Outputs

Pre Layout - Oscillator Measures (1)

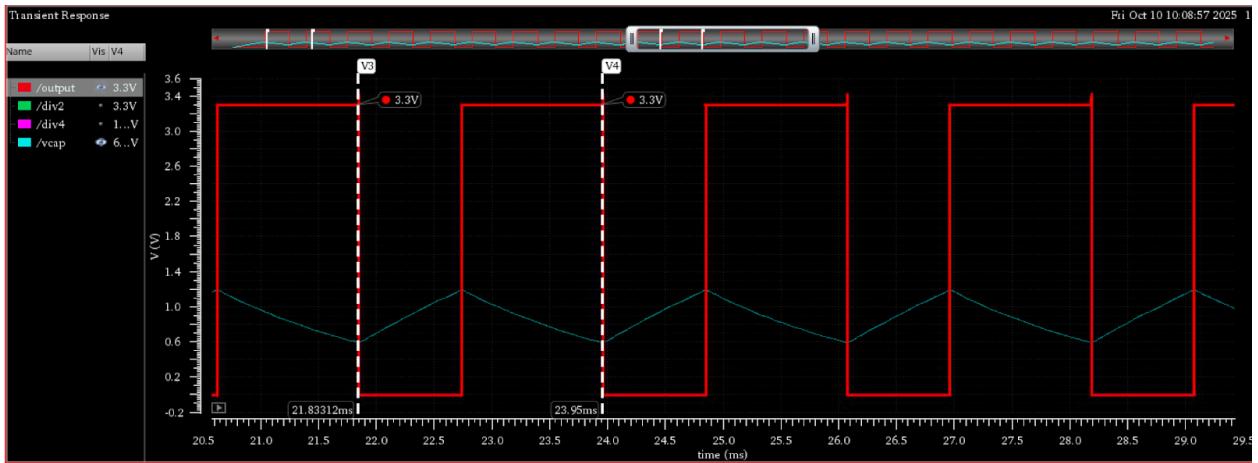


Figure 1a. Oscillator Output - 471.69Hz.

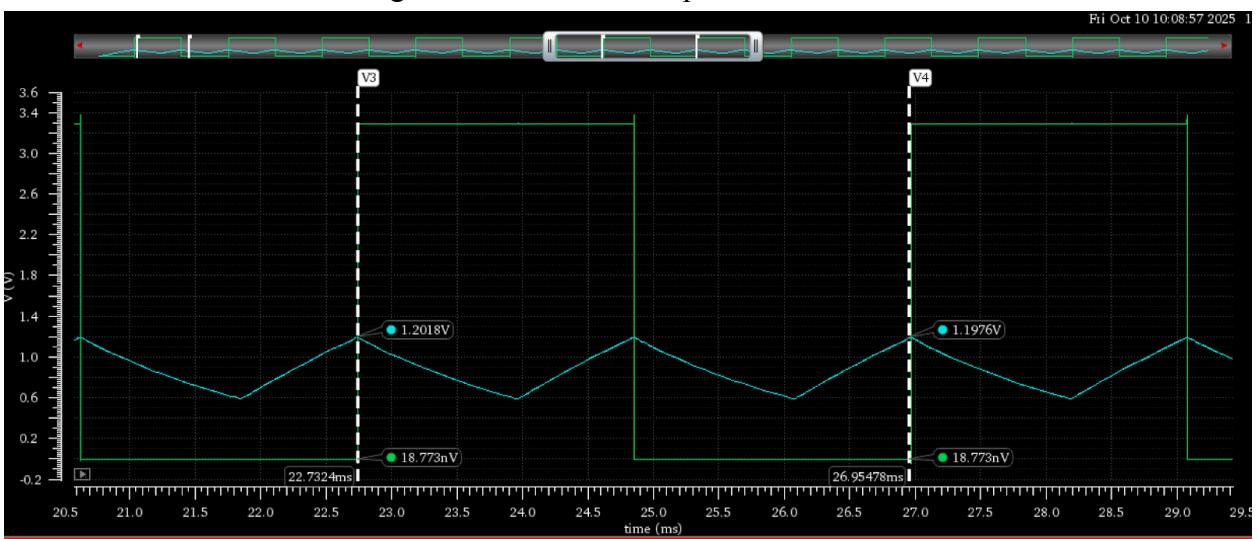


Figure 1b. Output - Frequency divided by two

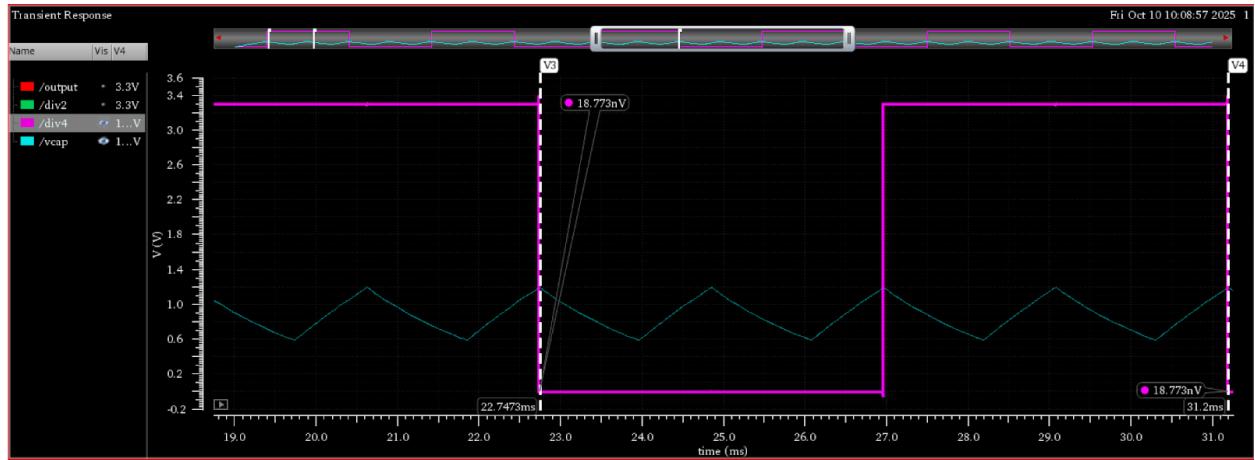


Figure 1c. Output - Frequency divided by two

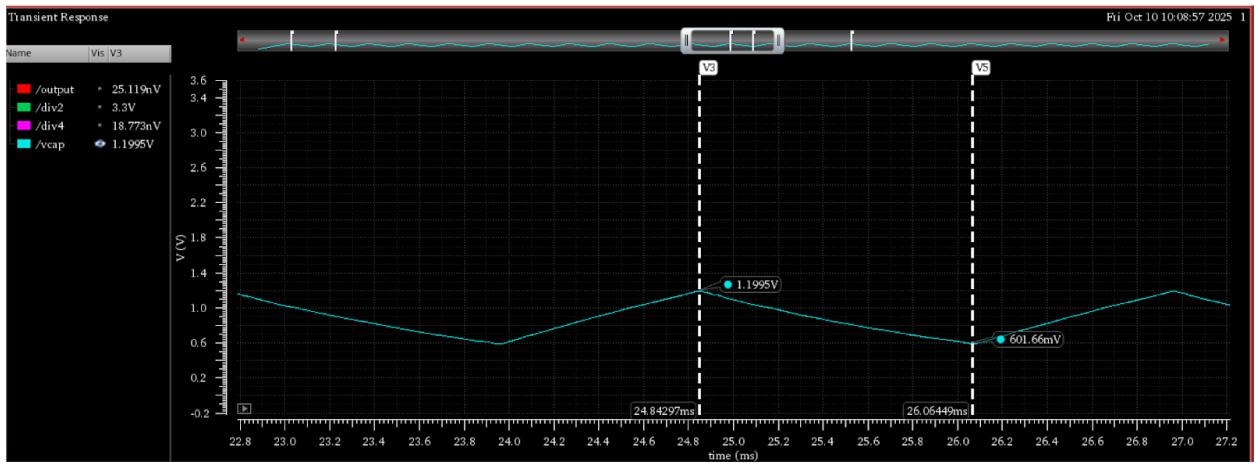


Figure 1d. Capacitor charging and discharging

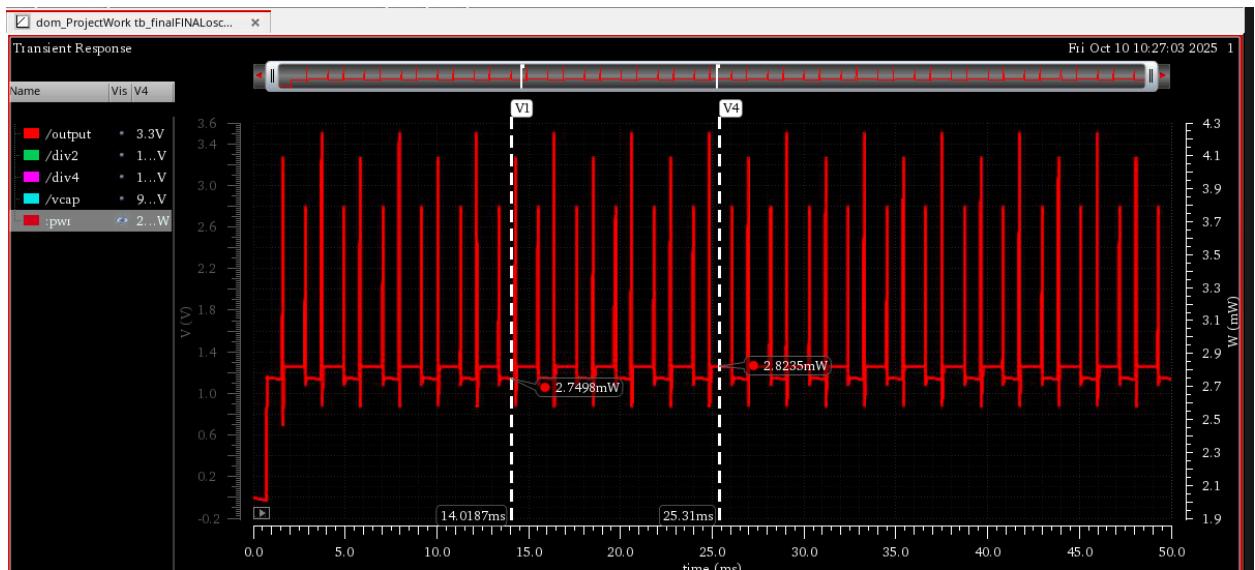


Figure 1e. Oscillator power usage

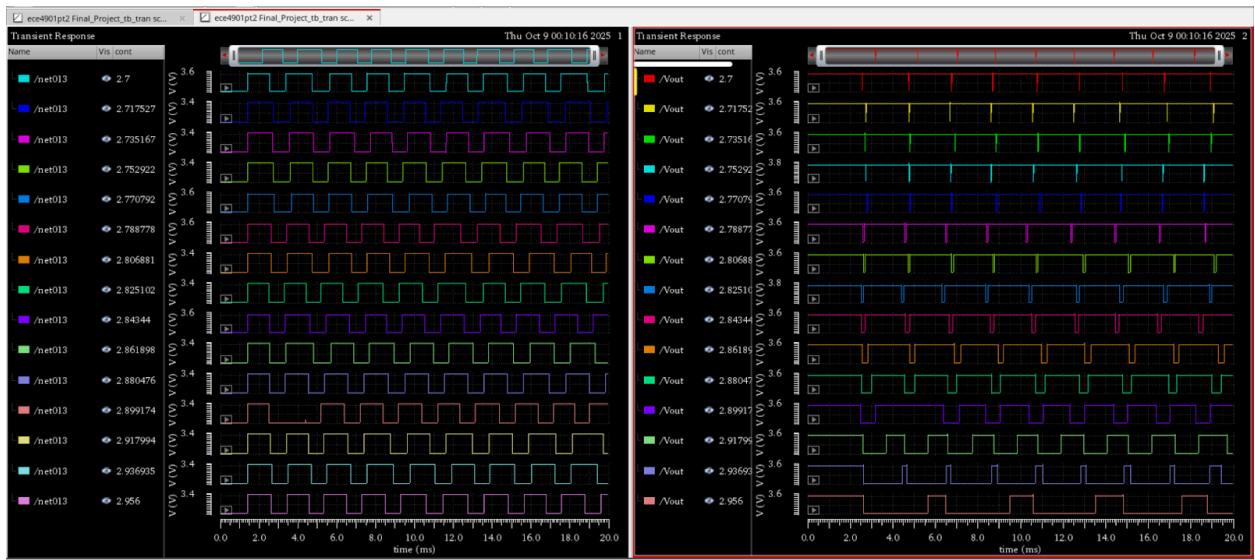


Figure 1f. PWM performance

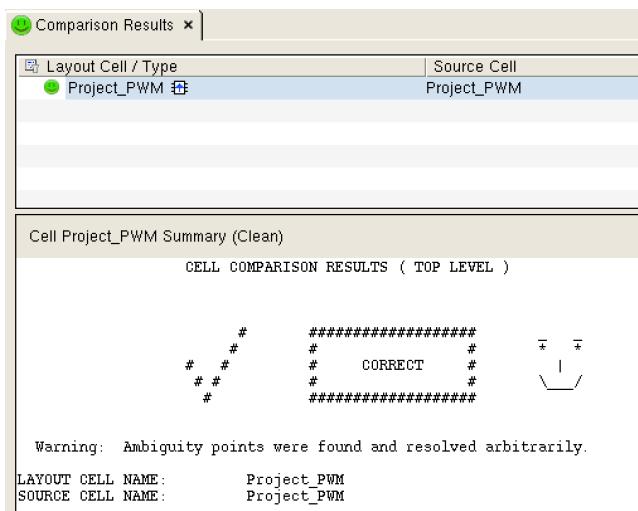


Figure 2a. LVS pass for modulator

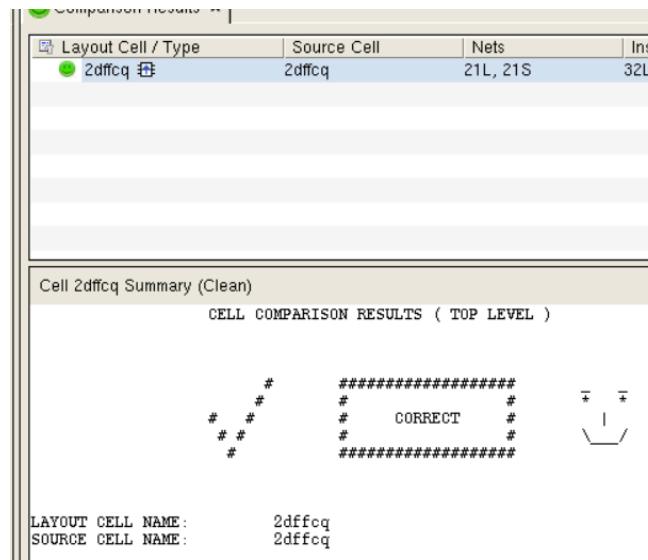


Figure 2b. LVS pass for Divider

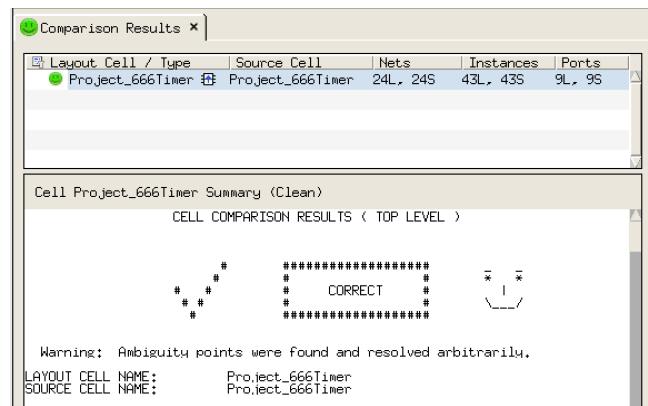


Figure 2c. LVS pass for full project

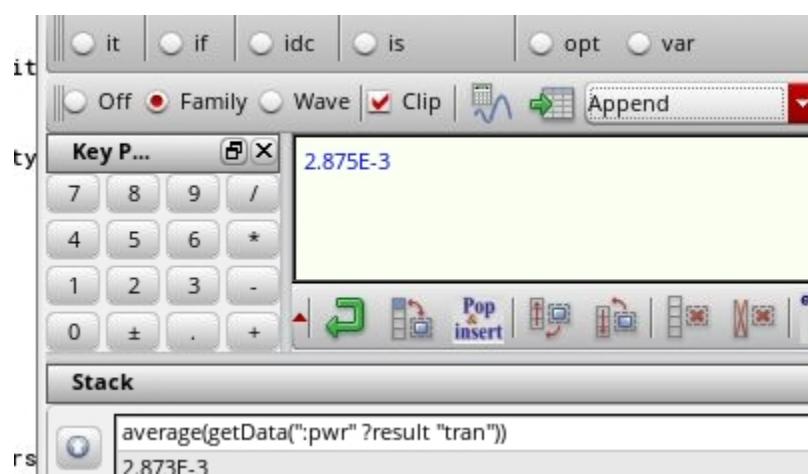


Figure 2d. Power analysis for full schematic pre layout

Post Layout - Oscillator Measure

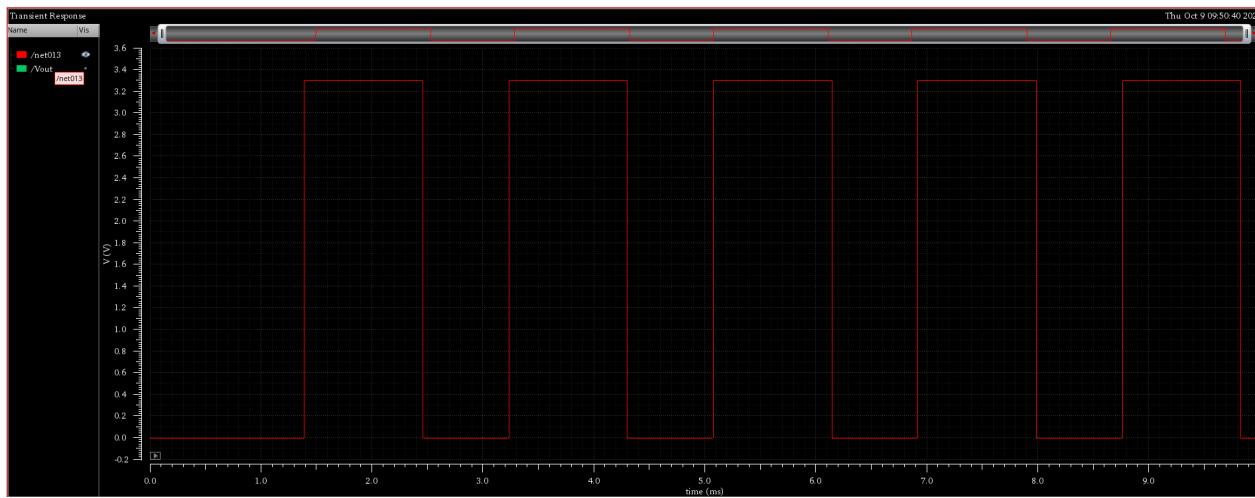


Figure 1. Post layout oscillator - Frequency of 555Hz

Post Layout - PWM Measures (1)

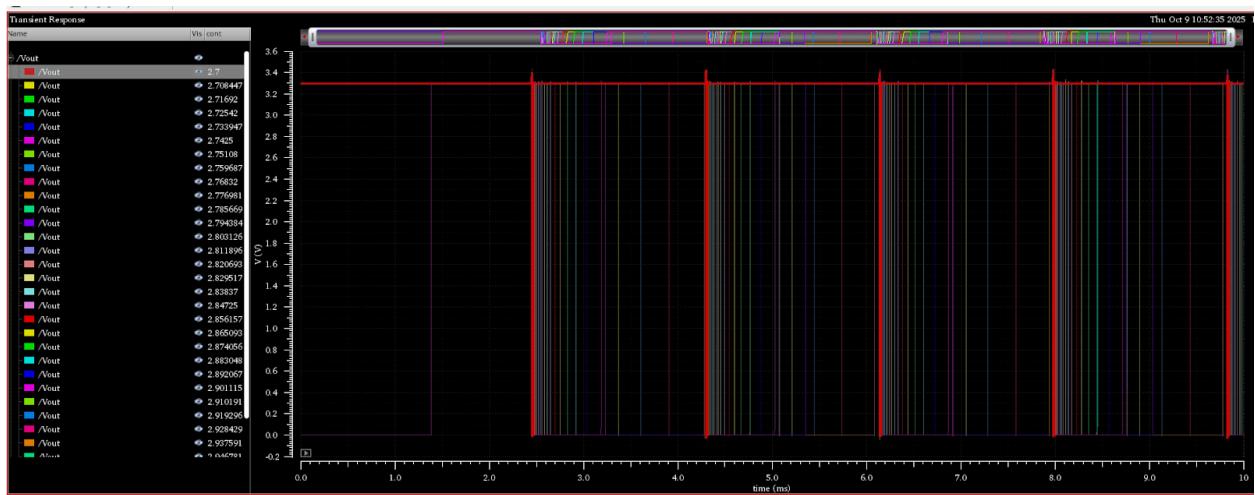


Figure 2. Post layout PWM - Duty cycle of 99% at 2.7 Volts

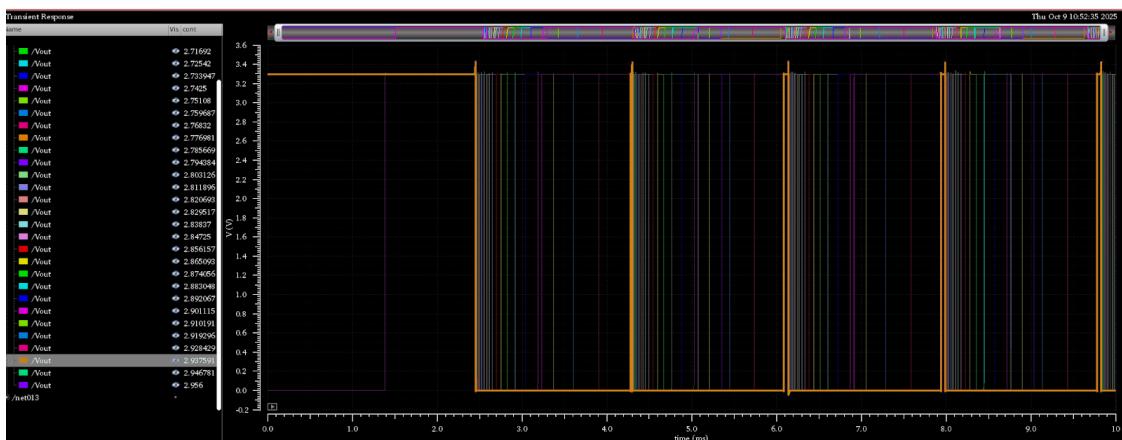


Figure 3. Post layout PWM - Duty cycle of 5% at 2.93 Volts