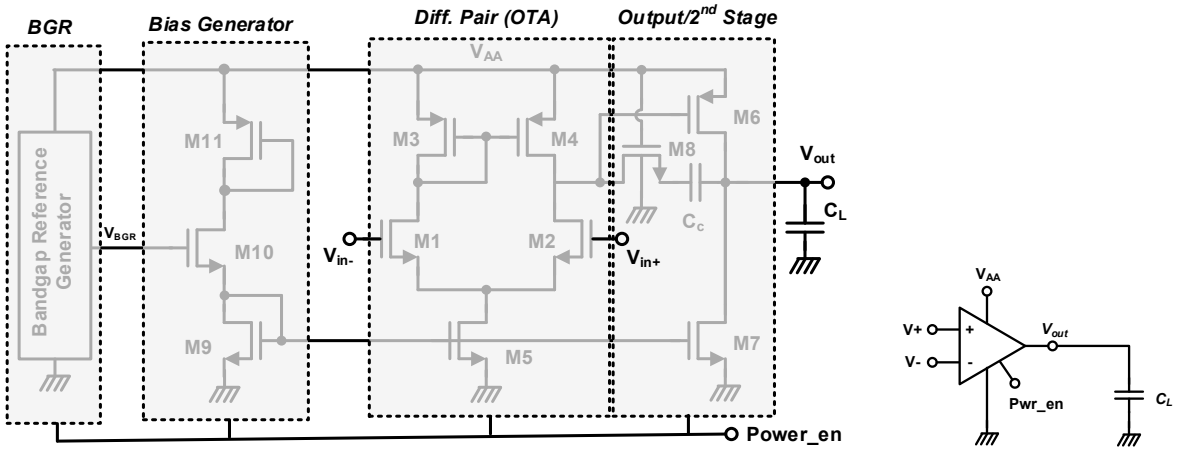
ECE 4902 – Analog IC Design

Term Project

Design and simulate two-stage, Miller-compensated CMOS Operational Amplifier (OPAMP) with on chip bias/reference generator and power down capability. *Shown schematic below is reference purpose only*. You can use other circuit techniques (such as cascoding) to improve gain or other parameters of circuits or devices (like M8). Reference and bias generator circuits could also be different. However, it should have specified V_{BGR} output voltage and complete set of circuits in it (i.e. including startup circuits). Power enable (power_en) input can be used as startup signal to BGR and powering down the whole OPAMP. Use TSMC 180nm process for your design.



Design Specifications

(post layout performance for all temperature and process corners)

Open Loop Gain (Av)	≥ 75 dB
Phase Margin (PM)	≥ 60°
Unity gain frequency (UGBW) (f_u)	≥ 25MHz
Slew Rate (SR)	≥ 20V/μsec
Input common more range (ICMR)	≥2.0V (>0.8V up to 3.3V, V_{AA}=3.3V) (Rail-2-Rail is desirable!)
Bandgap Voltage (V_{BGR})	+1.0 Volt (@ T=25C°)
TC_F of Bandgap Voltage	<100 ppm
Settling Time (T_{settle})	< 250ns (to 8-bit resolution on 1.0V step input, between 1.2V and 2.2V)
Power Consumption	< 1.5mW (DC, ON, Power_en=V_{AA}) <1μW (DC, OFF, Power_en=0)
Supply Voltage (V_{AA})	+3.3 Volt (from 3.0V to 3.6V)
Load Capacitance (C_L)	≤ 20pF
Temperature Range	0C°/ +70C°

Reporting and Submission Requirements

1. Use project report template available on class web site.
2. Design the layout not including the load capacitor C_L.
3. Describe the function of each block and transistors in your design.
4. Explain how you chose the device sizes/circuit topologies/etc. , write up your design strategy, design procedure, trade-offs, calculations, etc.
5. Show your DC and small signal analysis of the circuits,
6. Report pre- and post-layout simulation results for each performance parameters of your design at PVT corners. Report only the corner simulation results including; supply voltage of (V_{AA}) 3.0V, 3.3V (nominal), and 3.6V; room temperature (T=25C), minimum and maximum temperatures (T=0C and T=70C) and at different process corners including all 5 corners TT(default), SS, SF, FS, and FF.
7. Report nominal (T=25C,V_{AA}=3.3V, TT corner), best and worst-case performance of your design comparing to the target specifications. Mark if the target spec is "met" or "not met" on the table for all parameters and corners. Make sure worst-case performance meets the target specifications. Also make sure that your design meets all (or as many as possible) target specifications.
8. Report power consumption and layout size (in μm^2) for each block. Cycle power couple times and show & report the total power consumption for ON and OFF states clearly.
9. Include legible schematics (both circuit blocks and simulation testbenches), simulation results, and layouts (mark each block and device using the names from schematics) in your report.
10. Include any code you wrote or used (Matlab, Python, C, etc.) for your design as appendix to your report.

Team PRESENTATIONS:

December 11, 2025, Thursday, 1:00- 2:50pm EST
(3 students/team, 11 teams, 10 minutes presentation)

Report DEADLINE:

December 12, 2025, Friday, 5.00pm EST