

Lab 3

Bulk Driven Amplifier - Redesign

ECE4901

Introduction

In this lab report, a redesign of the bulk-driven amplifier will be proposed and laid out. The same schematic will be adjusted in order to yield the best symmetry and to quell the issues outlined in the previous lab report. Afterwards, this layout will go through Electronic Design Automation (EDA) tools to ensure proper adherence to the rules outlined by the tsmc 180nm processes. Lastly, this layout will be tested within a similar setup as homework one.

Redesign - Bulk Amplifier

Partitioning

In this redesign, the critiques offered in the last report are implemented. For each odd-fingered transistor in this layout, the number of their fingers will be doubled and their width halved to account for this increase. This allows for a symmetric design about the centroid, ensuring balanced parasitics and current flow on both sides. Furthermore, transistors' m4 and m6 will be lumped into one current mirror. By combining the two transistors into one block, this will allow for the width of the total design to be smaller. Following a similar principle, transistors' m0, m1, and m2 will be combined into one larger current mirror, as lumping them into one block will cut down on the redundancy of making each transistor an individual connection.

Regarding the current mirror formed by m0 to m2, the strategy here is to use a design similar to a weighted unit-capacitor network. This configuration of unit transistors with the same length and halved widths will allow for the most optimal grouping of these transistors. As the software recognizes which transistors should be matched with their respective blocks. So long as the drain and source connections are consistent with Figure 1, this will enable us to create a design with far more symmetry than one long transistor block.

Another point of discussion are the dummies indicated within the corners of the transistor block in the middle of Figure 2. The dummies will be implemented by planting another transistor of two fingers and the same physical dimensions, with their connections exactly the same as m0.

This will result in a design that is symmetric and dense, rather than an open and wasteful alternative. This strategy enables larger networks to be created without sacrificing compactness.

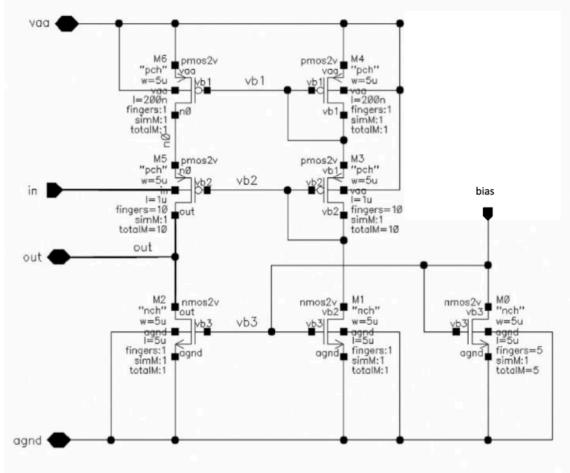


Figure 1: Schematic

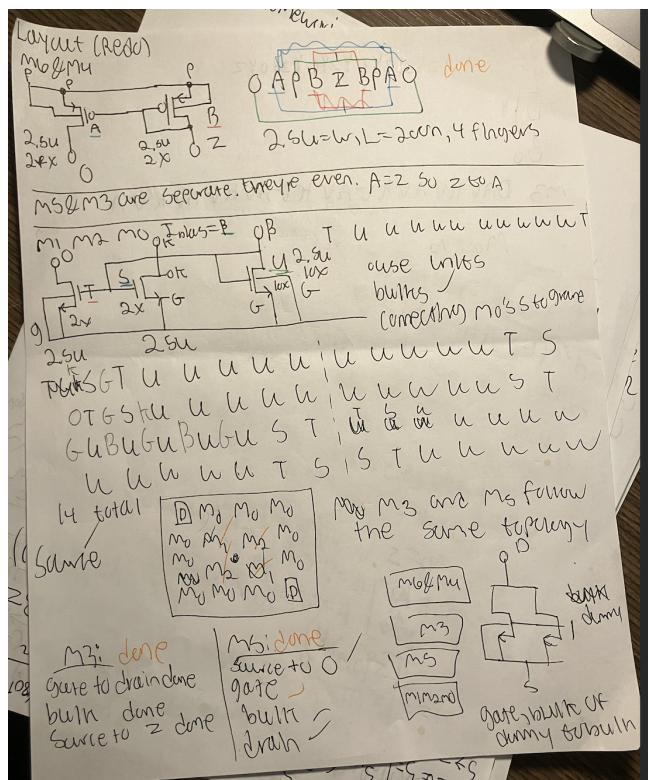


Figure 2: Scratch work for layout

Layout

Below is the final layout and the individual poly and metal layers. Discussion can be found after the pictures.

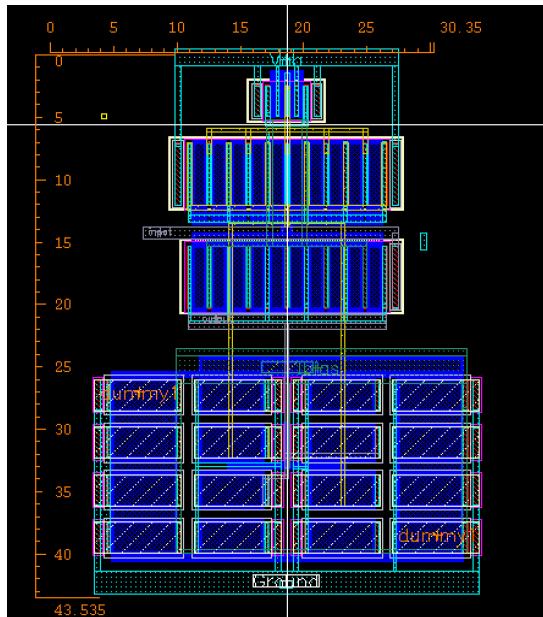


Figure 1: Completed layout

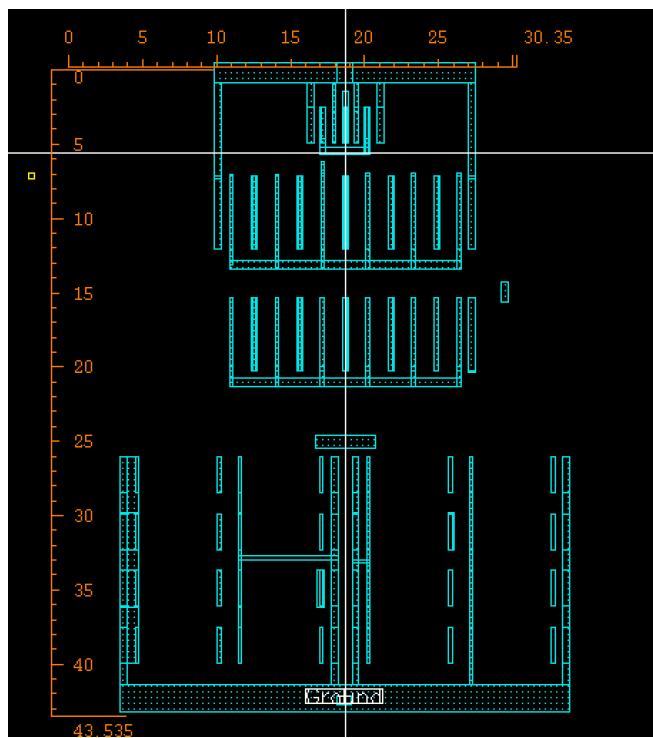


Figure 2: Metal 1 layer

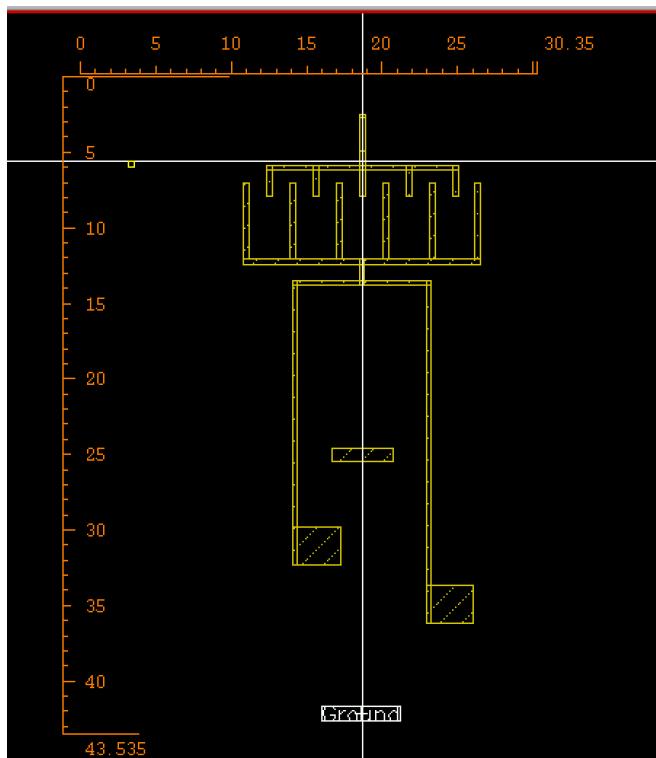


Figure 3: Metal 2 layer

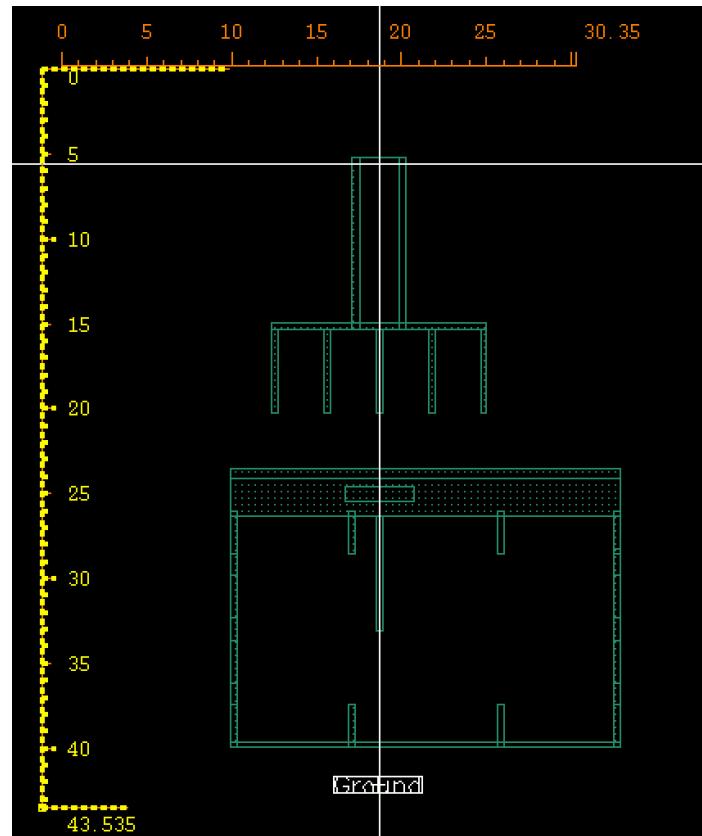


Figure 4: Metal 3 layer

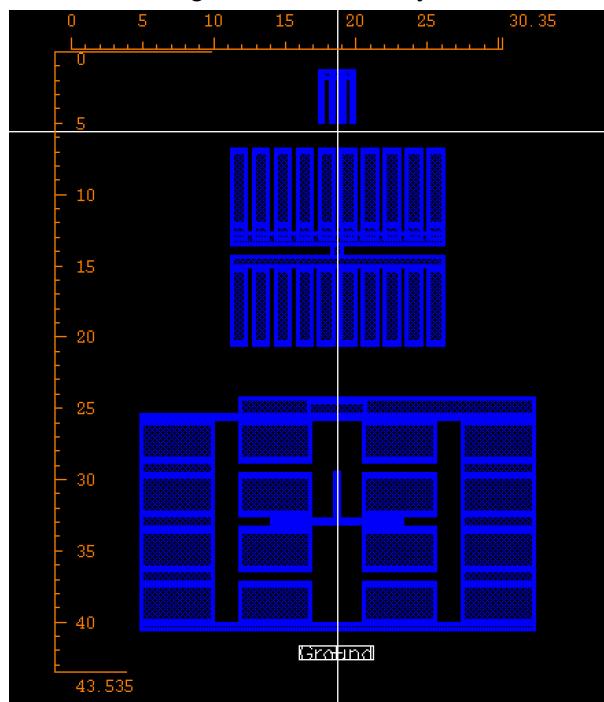


Figure 5: Poly layer

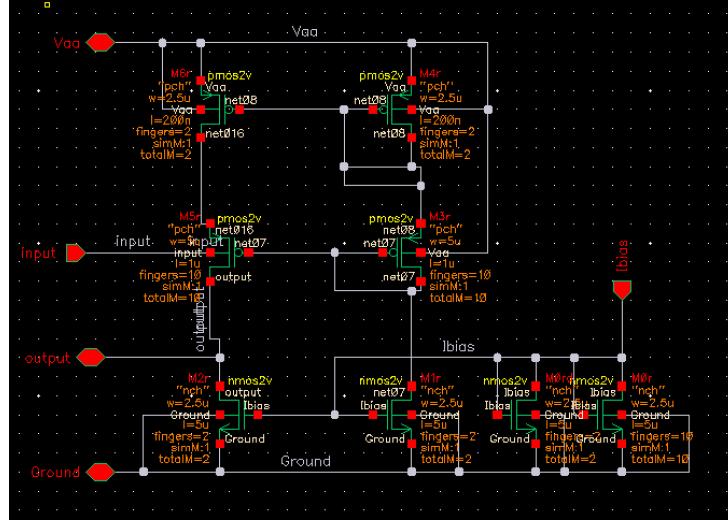


Figure 6: Schematic

Discussion

As observed, this layout takes up an area of 30.35um by 43.535, as indicated in Figure 1. The dummy transistor placed in Figure 6 represents the draft layout as discussed in the previous section. After the layout, DRC, LVS, and PEX were run to correct this design and clear up any violations. LVS ensured that this layout was accurate relative to the schematic for this bulk driven amplifier. These reports and summaries are attached to this report as separate files.

Simulations

As this amplifier is completed, it will be tested in a manner reminiscent of homework 1. Figure 1 indicates the schematic utilized along with the newly laid out amplifier. Here, we will run simulations to compare with the pre-layout simulations.

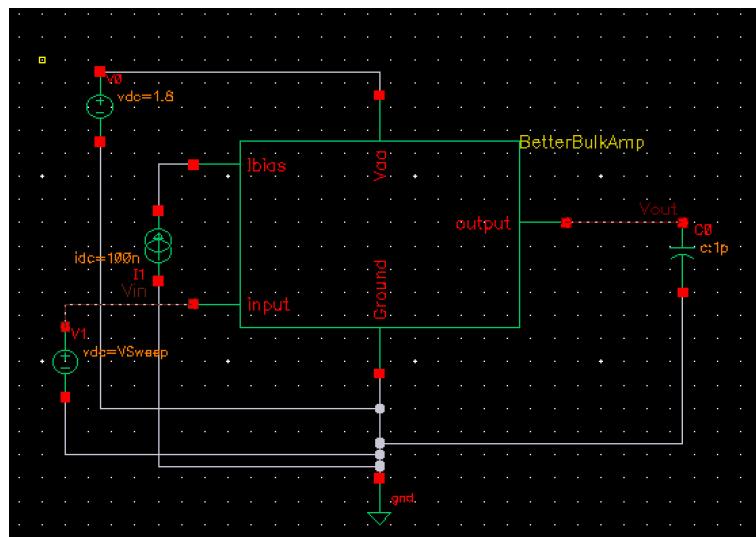


Figure 1 : New schematic for CMOSBlockAmplifier

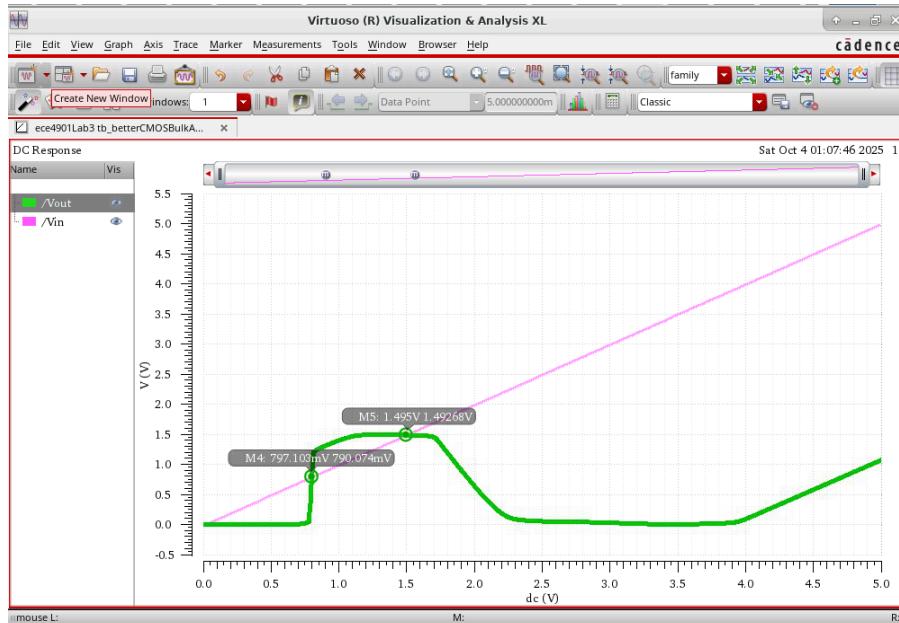


Figure 1: DC Voltage Sweep



Figure 2: Low frequency gain (32.5dB at ~24Hz)

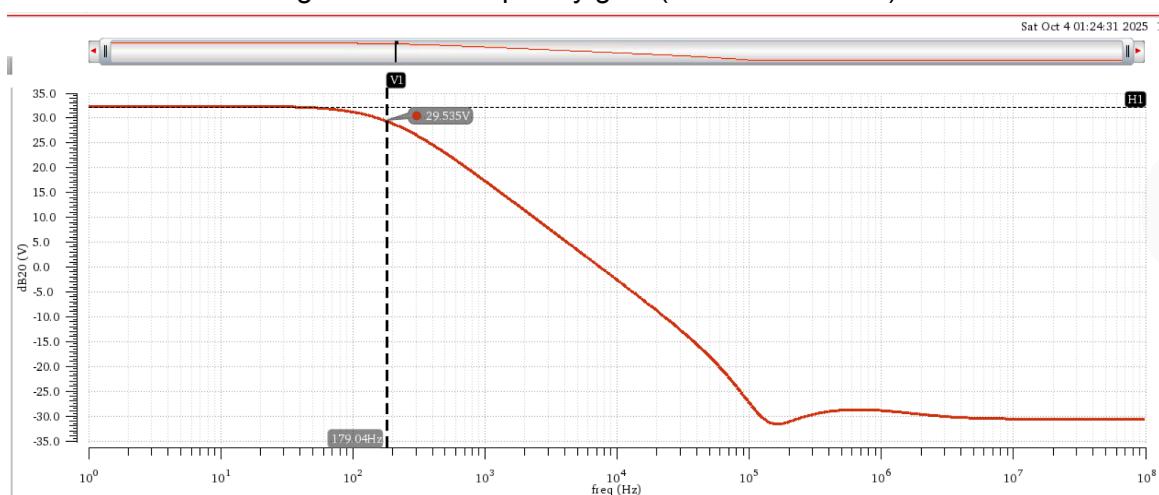


Figure 3: Bandwidth frequency (-3dB of max gain; frequency of 179.04)

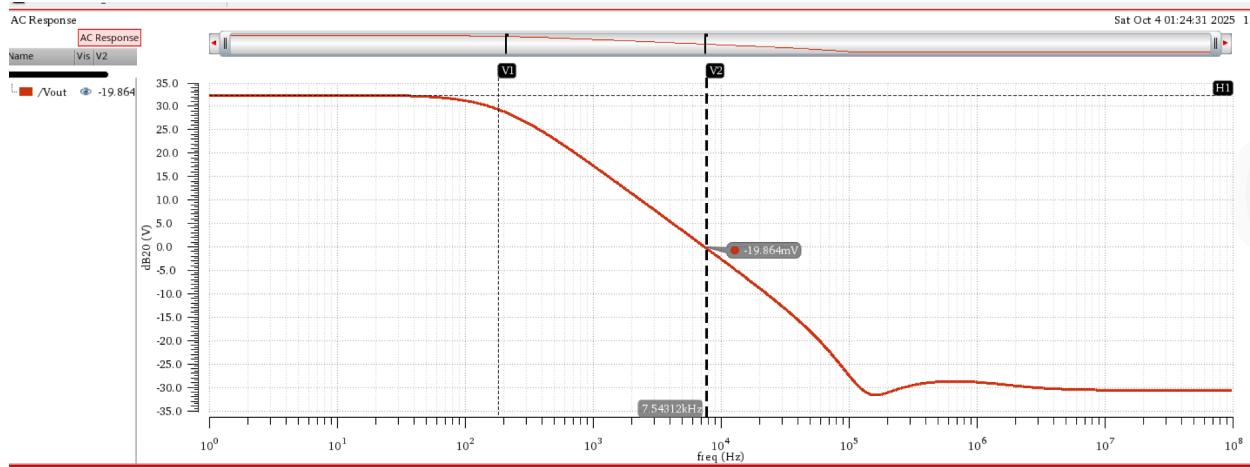


Figure 4: Unity Gain bandwidth

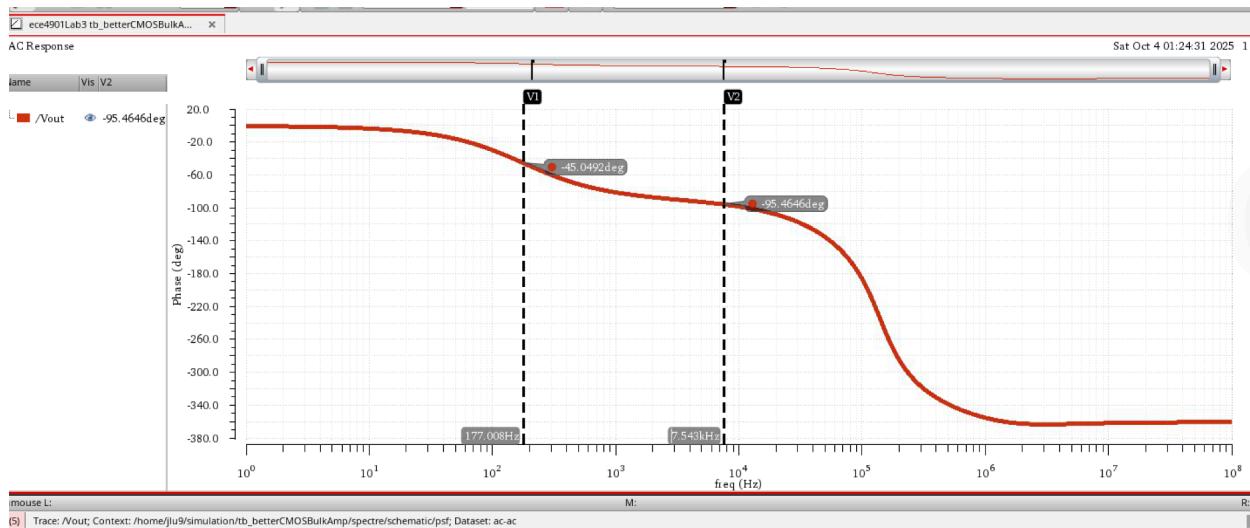


Figure 5: Phase at bandwidth and UGBW

Values

The homework one / pre-layout results can be found in the addendum underneath the conclusion. While the pre-layout result had a gain of 32.7dB, this post-layout design has a gain of 32.5dB, although this could be chalked up to a slight difference in measurement. Similarly, the maximizing voltage can be found at 0.79 volts with the layout instead of the 0.78 volts before the layout. The post-layout -3dB bandwidth point can be found at 177Hz and the unity gain bandwidth can be found at 7.543kHz. Compared to homework one's 210Hz and 8.21kHz, this is a non-negligible difference that could be attributed a lower resistance than the model used in the simulation. Lastly, the phase charts are nearly identical, with no significant differences.

Conclusion

In this lab session, the bulk driven amplifier has been laid out using TSMC180nm processes and simulated using Virtuoso. The changes suggested in the previous report have been implemented and this device successfully amplifies the signal with functional behaviour.

Addendum: Homework one / Pre-layout figures



Figure 1: Small signal gain

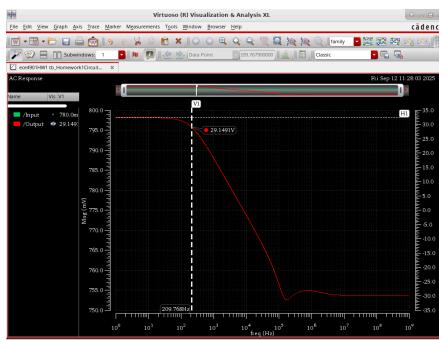


Figure 2: -3dB on bode plot

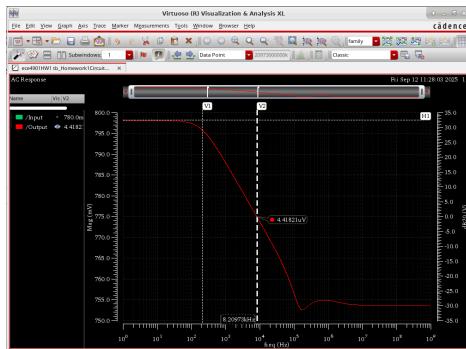


Figure 3: Unity gain bandwidth at 8.2kHz

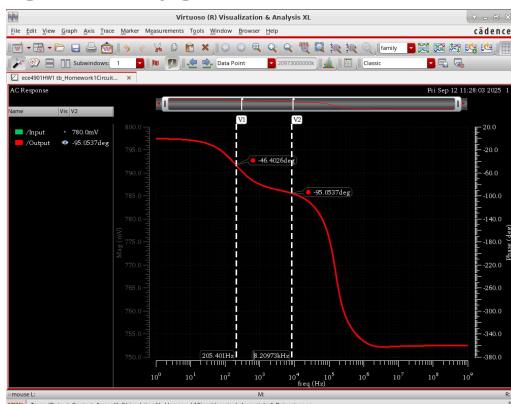


Figure 4: Phase graph at 1pF