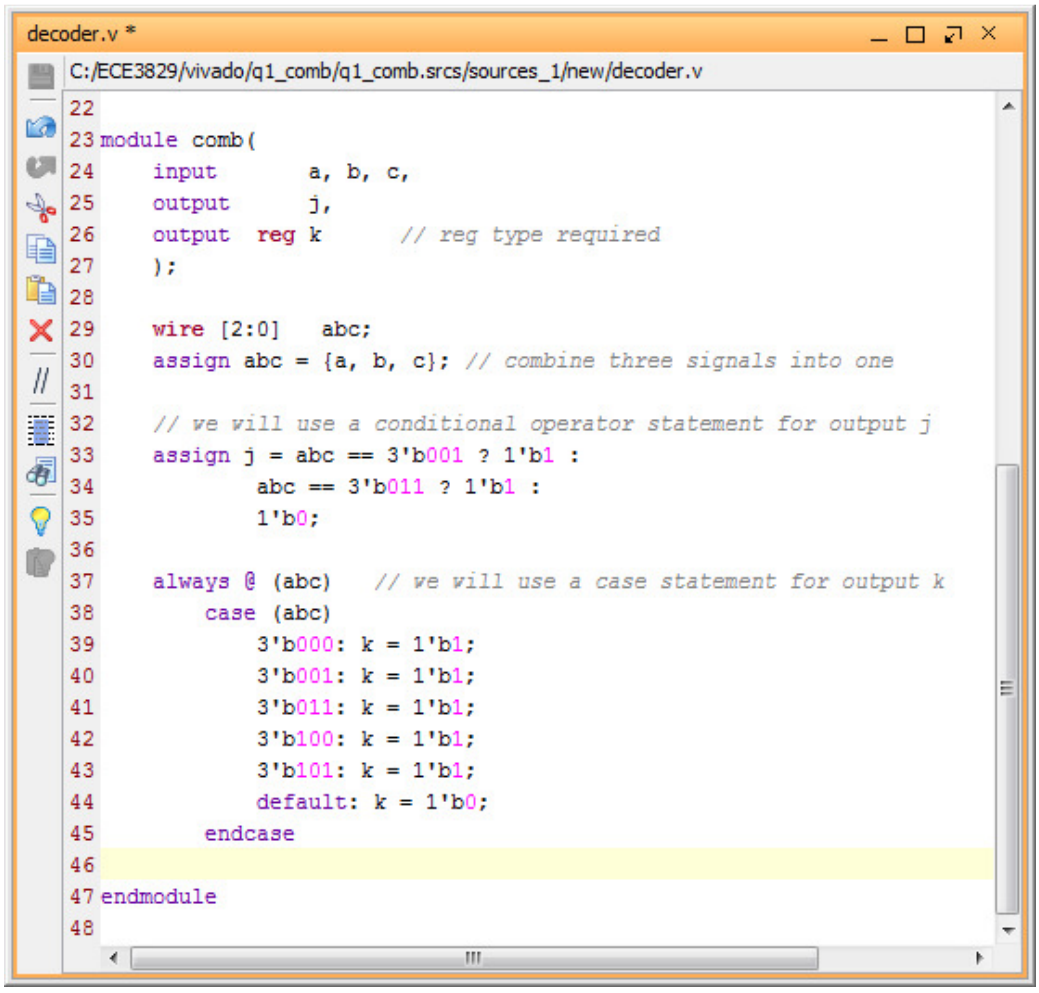
Using Vivado to create a simple Test Fixture in Verilog

In this tutorial we will create a simple combinational circuit and then create a test fixture (test bench) to simulate and test the correct operation of the circuit.

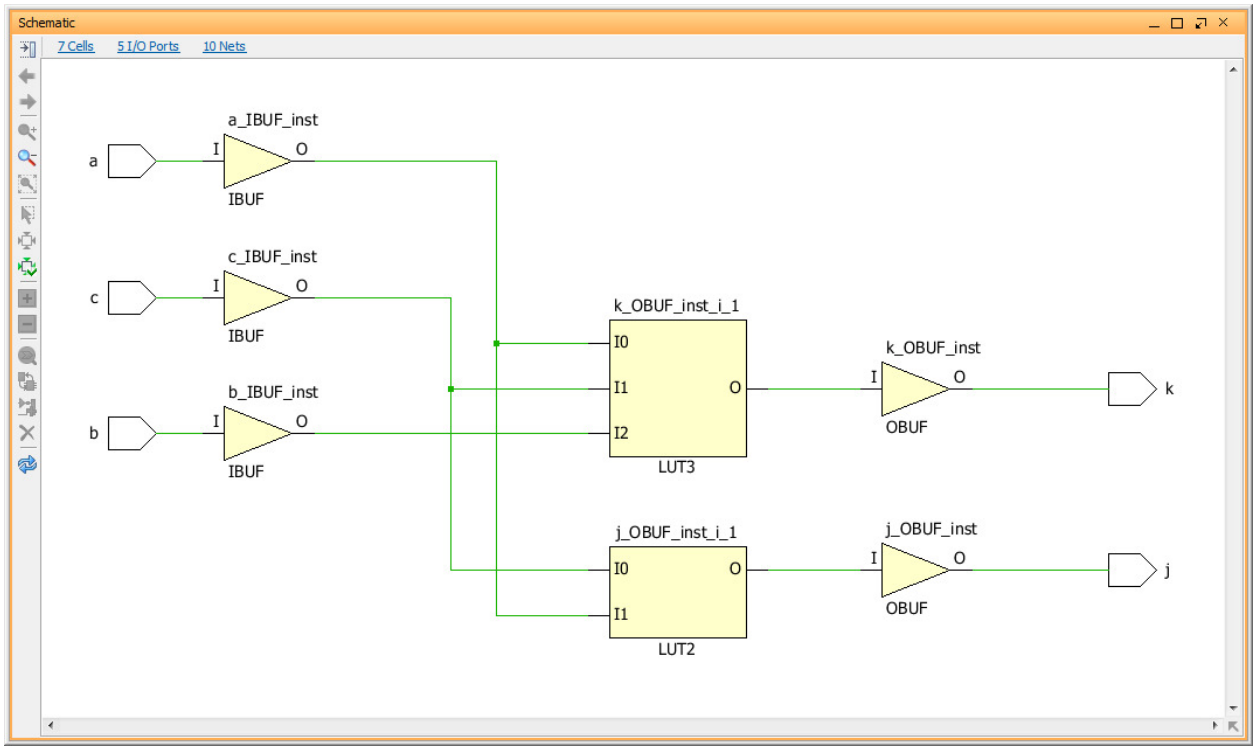
Truth table of simple combinational circuit (A, b, and c are inputs. J and k are outputs)

a	b	c	j	k
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

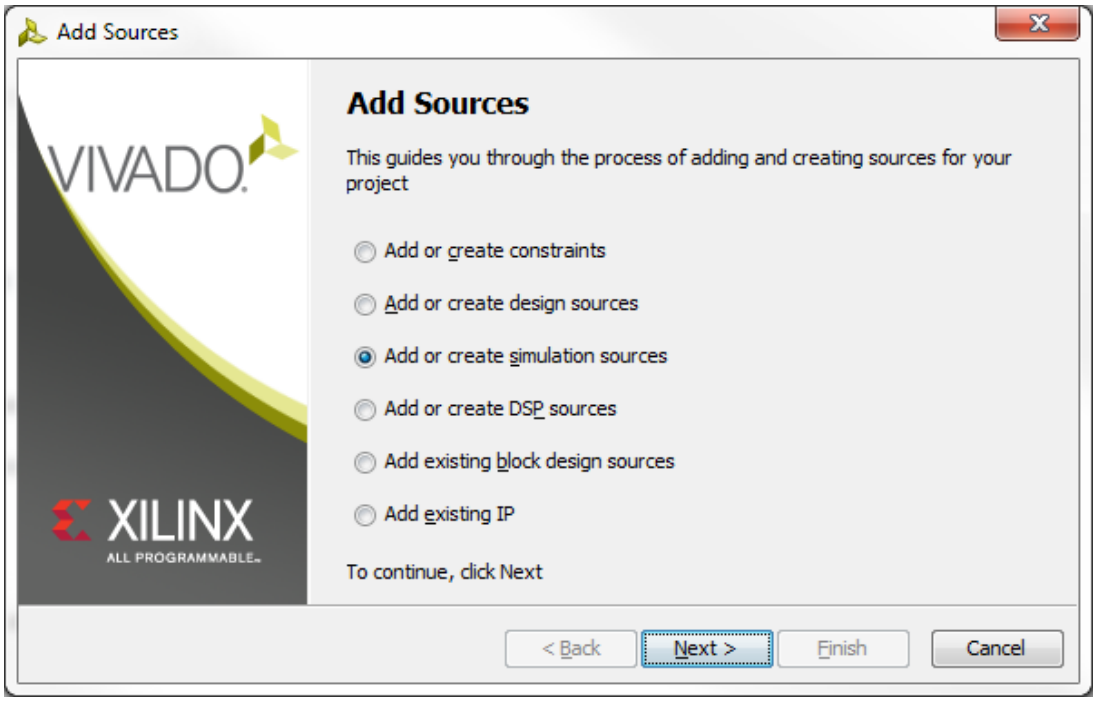
Create a new project and create a Verilog source file describing the behavior of this circuit. For example:



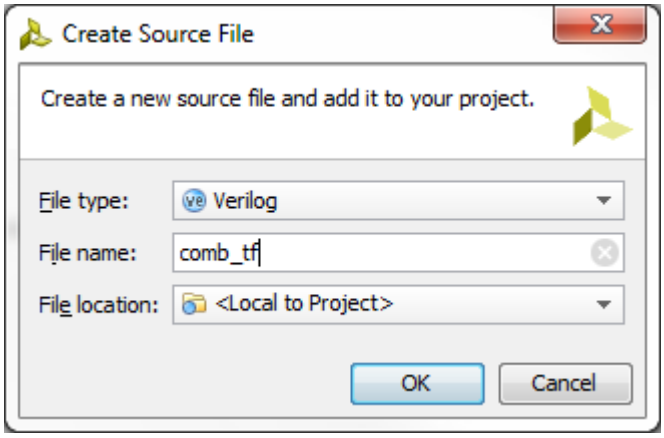
Note: In the Flow Navigator, under Open Synthesized Design you can view a schematic representation of the design:



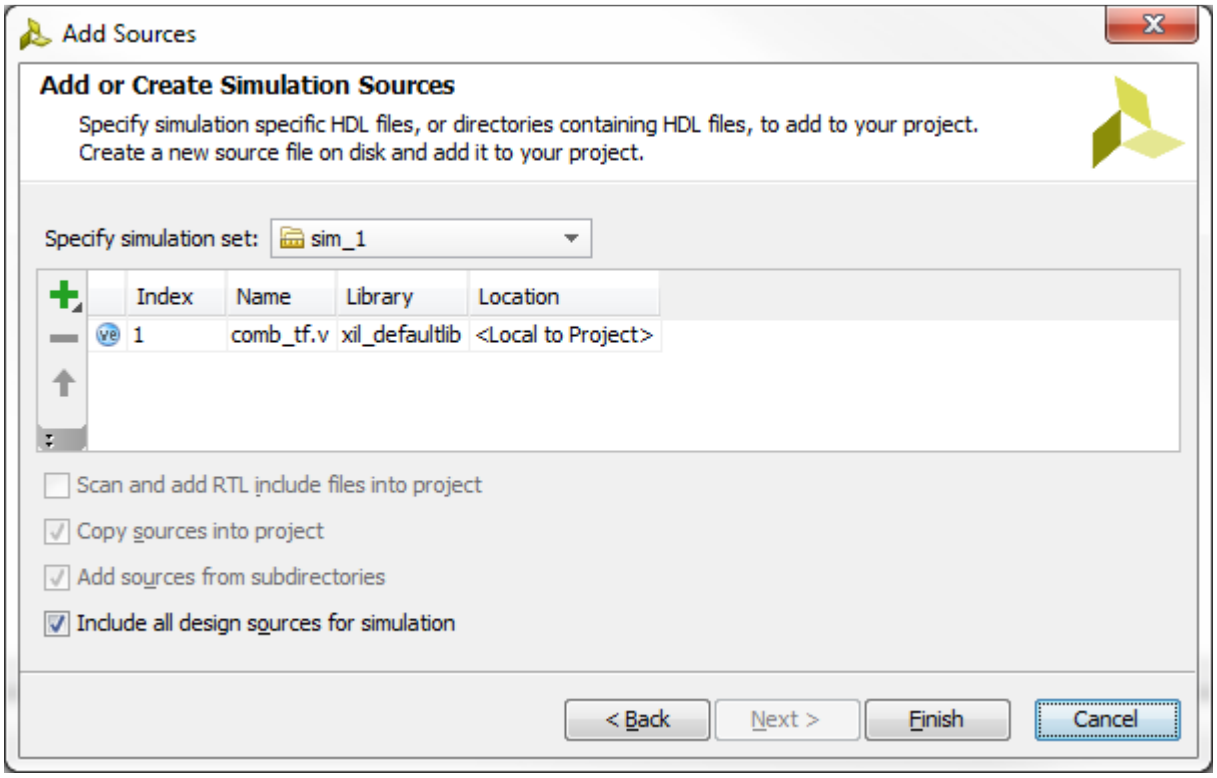
We will now create a simple test bench to test the operation of this combinational circuit. Create a simulation source:



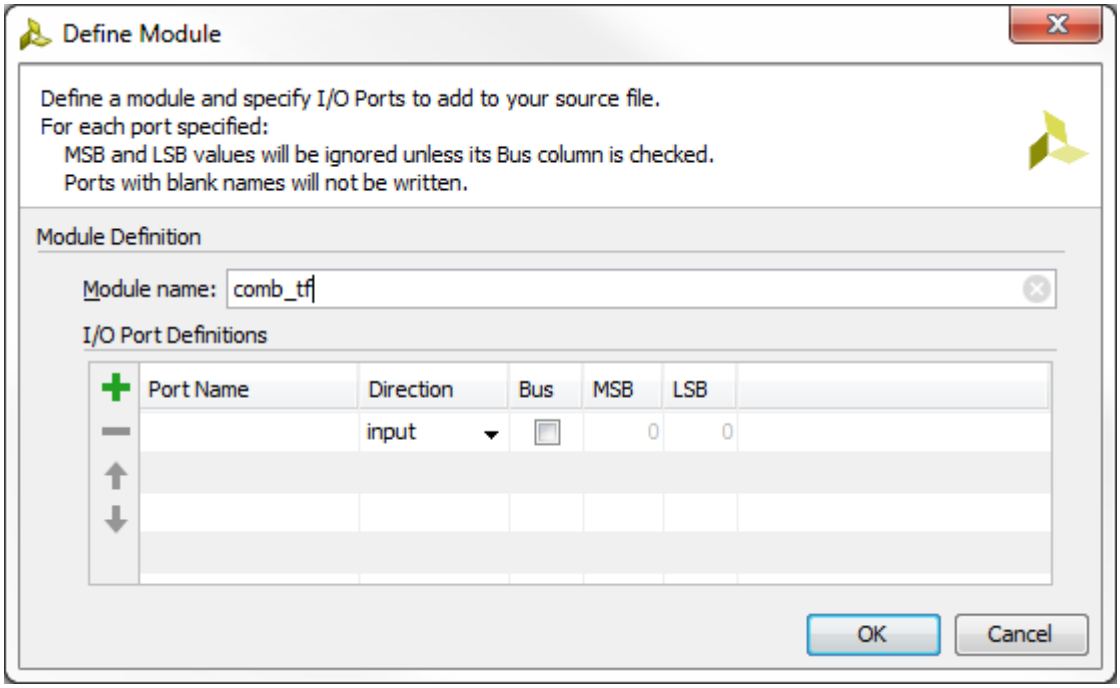
Create a new source file – called comb_tf:



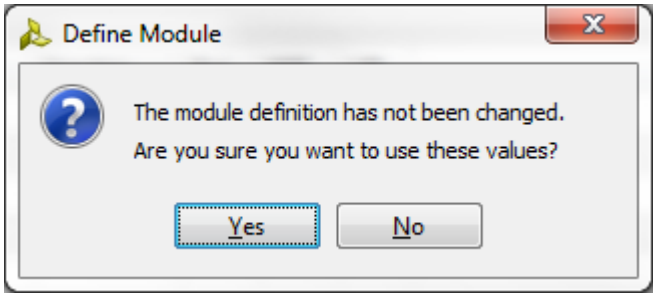
Click **OK**



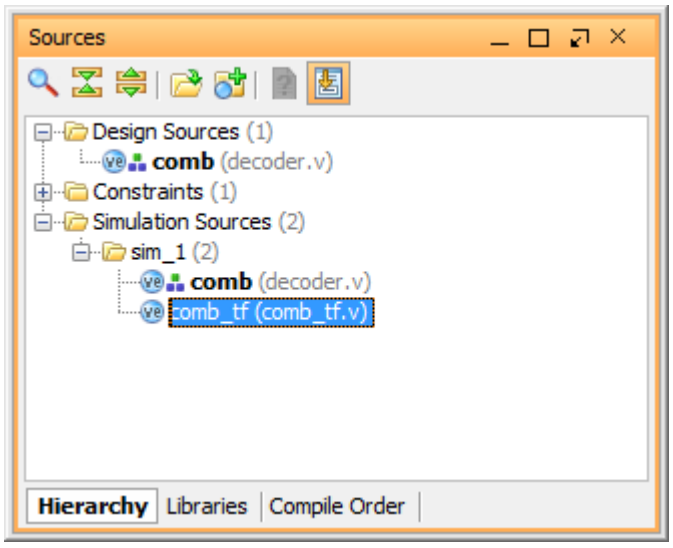
Click **Finish**



A Test Fixture does not need any inputs and outputs so just click OK.



Click **Yes,** the text fixture file is added to the simulation sources:



Open up the nearly created *comb.tf* file and add the following Verilog statements to instantiate a copy of the *comb* module and create a simple test fixture:

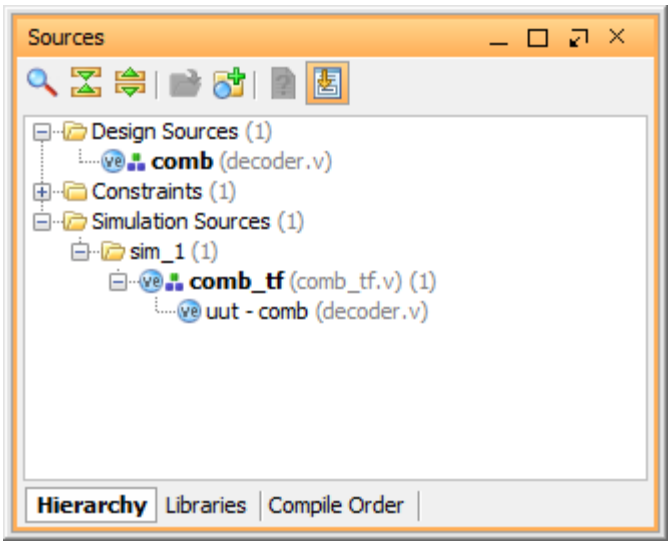
comb_tf.v

C:/ECE3829/vivado/q1_comb/q1_comb.srcs/sim_1/new/comb_tf.v

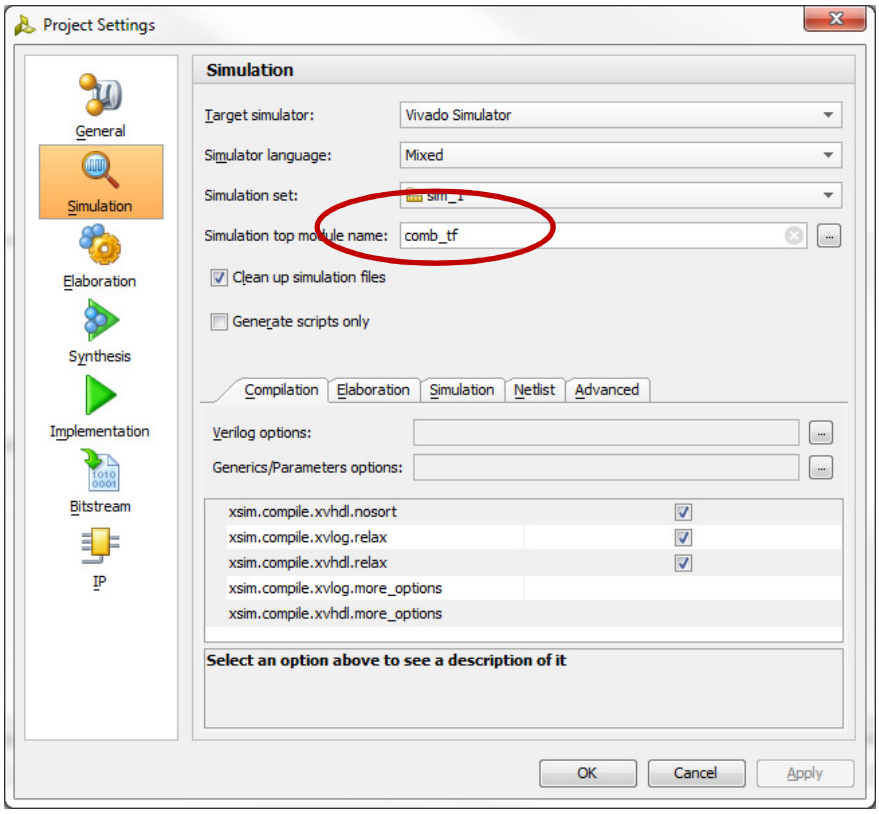
Read-only: C:/ECE3829/vivado/q1_comb/q1

```
22
23 module comb_tf(
24     );
25
26     // Inputs (combine into one bus)
27     reg [2:0]   abc;
28     // Outputs
29     wire    j, k;
30
31     // Instantiate the unit under test and connect inputs and outputs
32     comb uut (
33         .a(abc[2]),
34         .b(abc[1]),
35         .c(abc[0]),
36         .j(j),
37         .k(k)
38     );
39
40     // apply input stimulus, check all combinations
41     initial begin
42         abc = 3'b000;
43         #100;   // wait 100ns
44         abc = 3'b001;
45         #100;
46         abc = 3'b010;
47         #100;
48         abc = 3'b011;
49         #100;
50         abc = 3'b100;
51         #100;
52         abc = 3'b101;
53         #100;
54         abc = 3'b110;
55         #100;
56         abc = 3'b111;
57     end
58
59 endmodule
60
```

Click **save** and you will the Simulation Sources hierarchy is now updated:



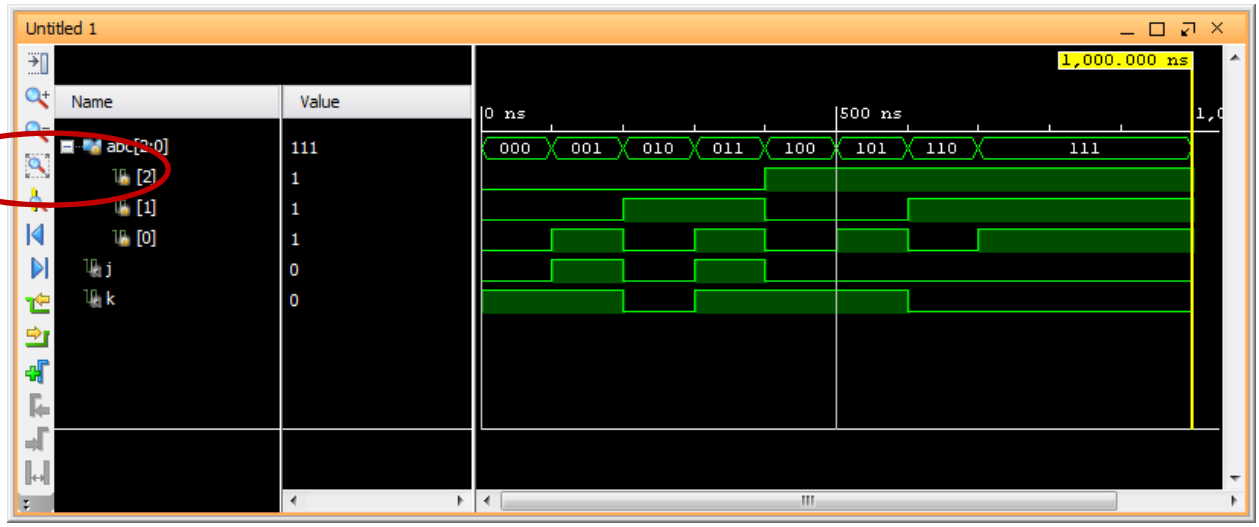
In the Flow navigator select Simulation Settings and verify the Simulation top module name is comb_tf:



In the Flow Navigator select Run Simulation => Run Behavioral Simulation

A simulation window will open.

Select the Zoom Fit option on the left and you will see the simulation results:



You can visually check the j and k outputs and verify they match the truth table.