## Using Vivado to create a simple Test Fixture in Verilog

In this tutorial we will create a simple combinational circuit and then create a test fixture (test bench) to simulate and test the correct operation of the circuit.

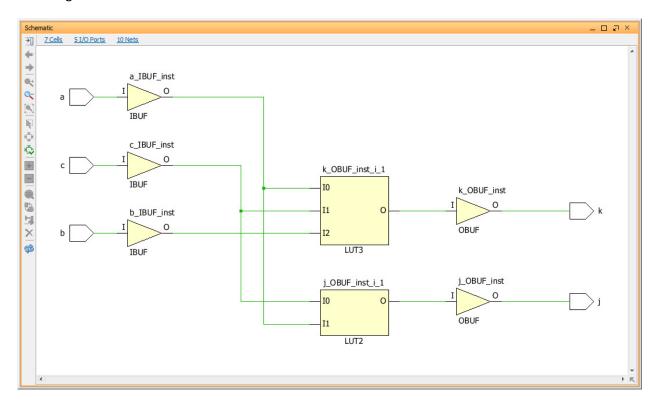
Truth table of simple combinational circuit (A, b, and c are inputs. J and k are outputs)

а	b	С	j	k
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

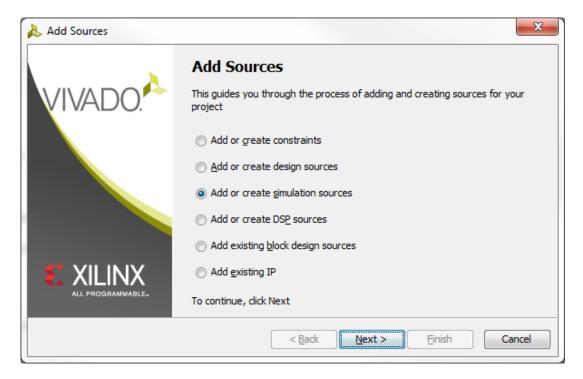
Create a new project and create a Verilog source file describing the behavior of this circuit. For example:

```
decoder.v *
                                                                _ 🗆 🗗 ×
C:/ECE3829/vivado/q1_comb/q1_comb.srcs/sources_1/new/decoder.v
   22
23 module comb (
24
         input
                     a, b, c,
25
         output
                     j,
   26
         output reg k
                          // reg type required
27
         );
28
X 29
        wire [2:0]
                      abc;
   30
         assign abc = {a, b, c}; // combine three signals into one
//
   31
32
       // we will use a conditional operator statement for output j
   33
         assign j = abc == 3'b001 ? 1'b1 :
æ.
   34
                 abc == 3'b011 ? 1'b1 :
  35
V
                 1'b0;
   36
   37
         always @ (abc) // we will use a case statement for output k
   38
             case (abc)
                 3'b0000: k = 1'b1;
   39
                 3'b001: k = 1'b1;
   40
                 3'b011: k = 1'b1;
   41
                 3'b100: k = 1'b1;
   42
                 3'b101: k = 1'b1;
   43
   44
                 default: k = 1'b0;
   45
             endcase
   46
   47 endmodule
   48
      4
                                 III
```

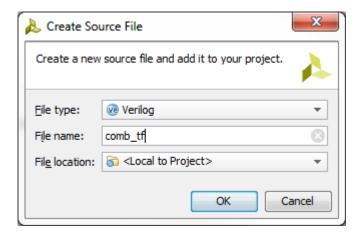
Note: In the Flow Navigator, under Open Synthesized Design you can view a schematic representation of the design:



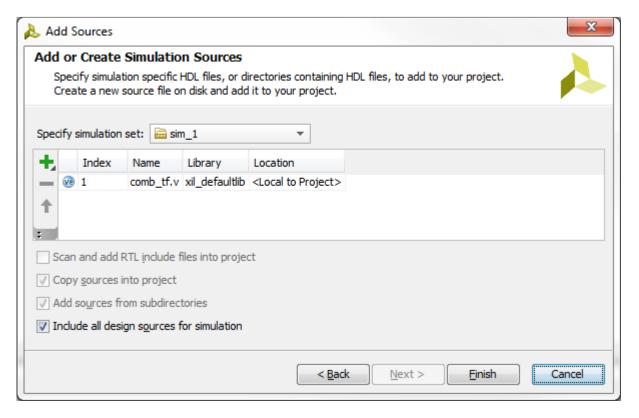
We will now create a simple test bench to test the operation of this combinational circuit. Create a simulation source:



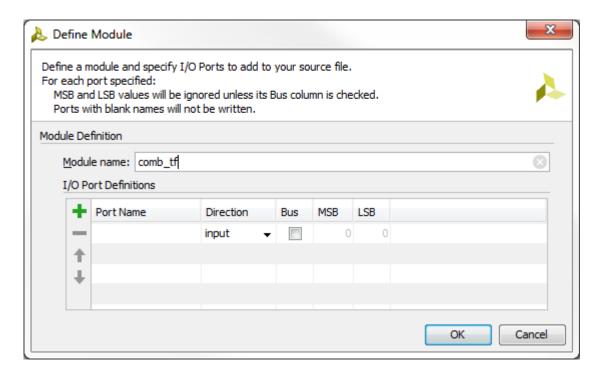
Create a new source file – called comb\_tf:



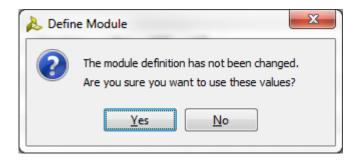
Click OK



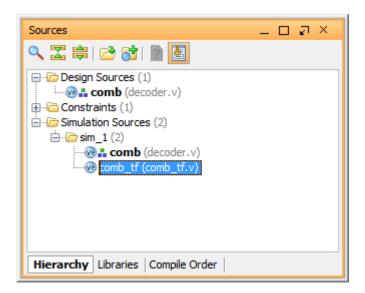
Click Finish



A Test Fixture does not need any inputs and outputs so just click OK.



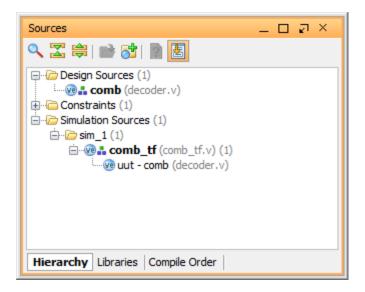
Click **Yes**, the text fixture file is added to the simulation sources:



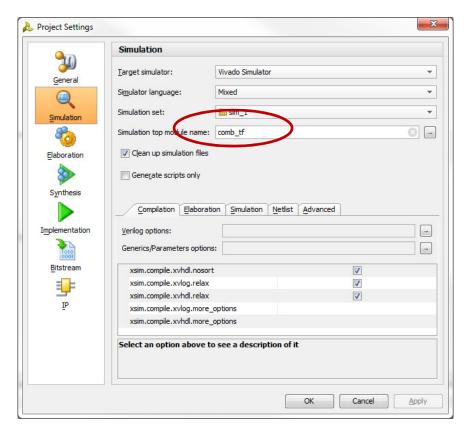
Open up the nearly created *comb.tf* file and add the following Verilog statements to instantiate a copy of the *comb* module and create a simple test fixture:

```
comb_tf.v
                                                                        _ 🗆 🗗 ×
C:/ECE3829/vivado/q1_comb/q1_comb.srcs/sim_1/new/comb_tf.v
   22
                                                   Read-only: C:/ECE3829/vivado/q1_comb/q1
   23 module comb_tf(
24
         );
25
   26
         // Inputs (combine into one bus)
27
         reg [2:0]
                      abc;
28
          // Outputs
X 29
         wire
                  j, k;
   30
//
   31
         // Instantiate the unit under test and connect inputs and outputs
32
         comb uut (
33
              .a(abc[2]),
   34
              .b(abc[1]),
   35
              .c(abc[0]),
   36
              .j(j),
   37
              .k(k)
   38
         );
   39
         // apply input stimulus, check all combinations
   40
   41
         initial begin
   42
             abc = 3'b000;
              #100; // wait 100ns
   43
   44
              abc = 3'b001;
              #100;
   45
              abc = 3'b010;
   46
   47
              #100;
   48
              abc = 3'b011;
   49
              #100;
   50
             abc = 3'b100;
   51
              #100;
   52
              abc = 3'b101;
              #100;
   53
   54
              abc = 3'b110;
   55
              #100;
   56
              abc = 3'b111;
   57
          end
   58
   59 endmodule
   60
      4
```

Click **save** and you will the Simulation Sources hierarchy is now updated:



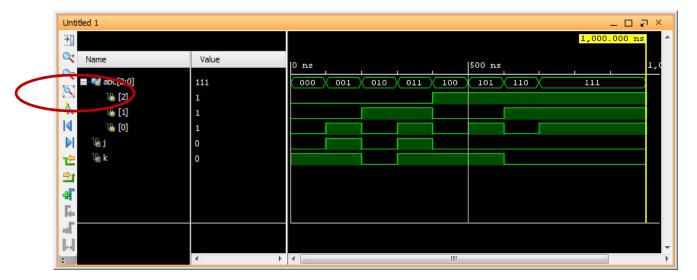
In the Flow navigator select Simulation Settings and verify the Simulation top module name is comb\_tf:



In the Flow Navigator select Run Simulation => Run Behavioral Simulation

A simulation window will open.

Select the Zoom Fit option on the left and you will see the simulation results:



You can visually check the j and k outputs and verify they match the truth table.