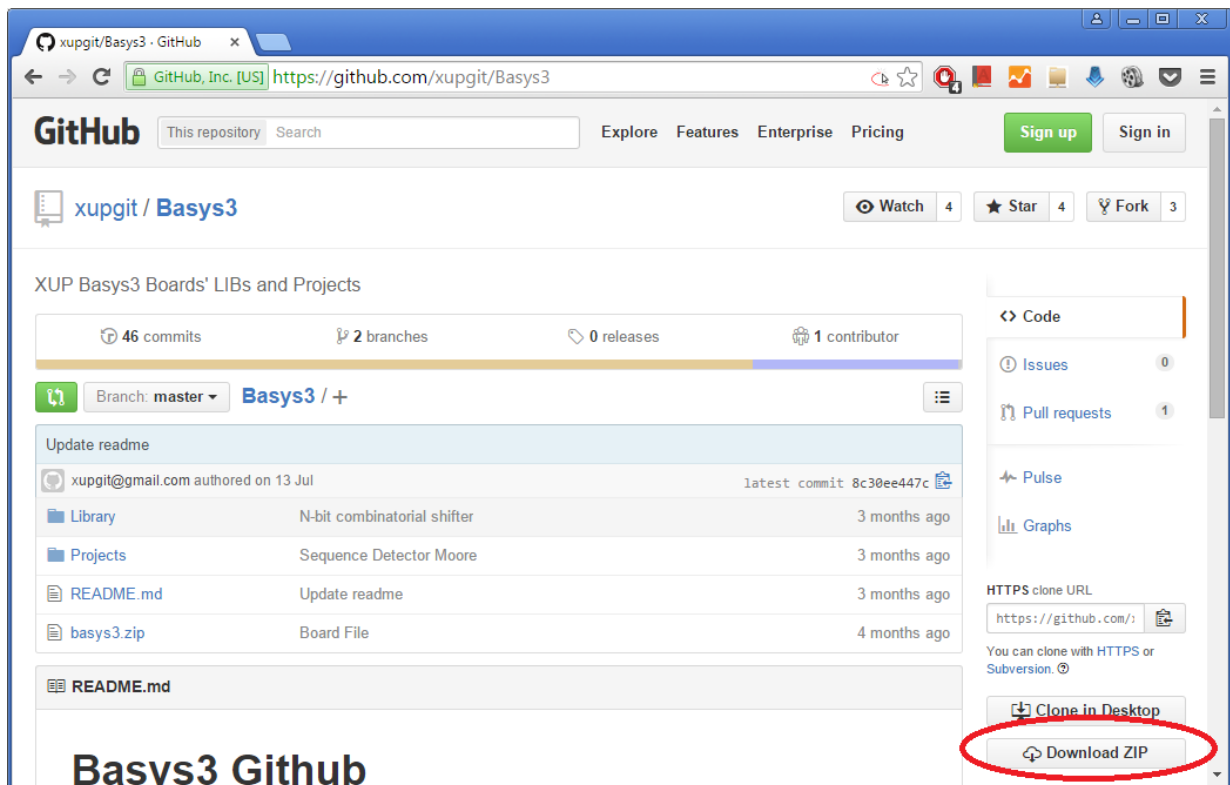


Basys 3 Github quick start guide

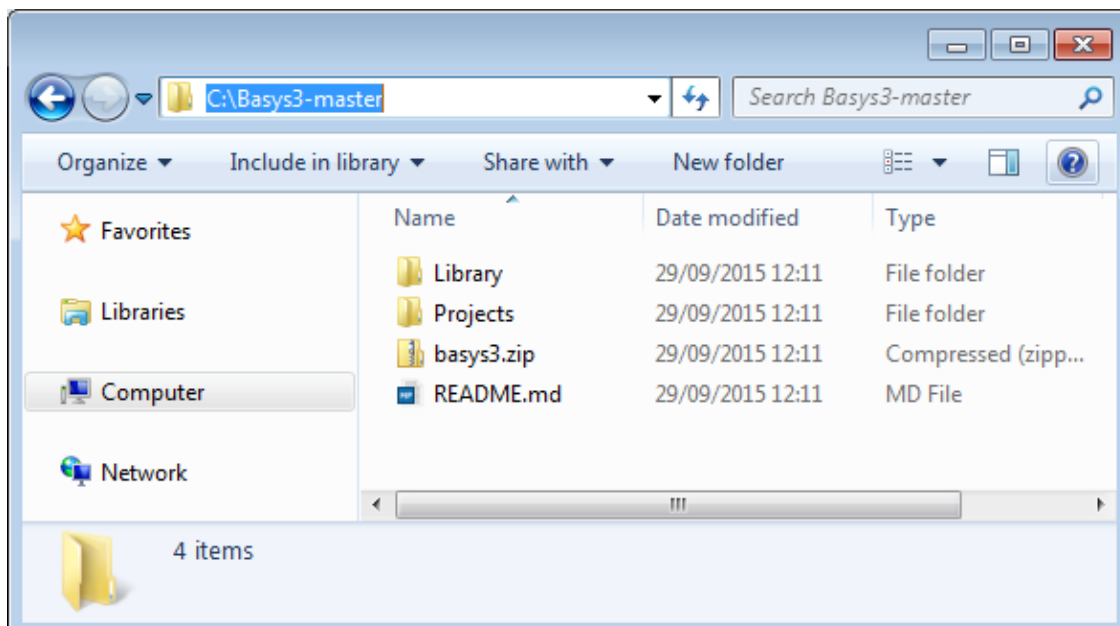
Using the basic libraries

This guide shows how to use the Basys 3 GitHub repository with Vivado IP integrator. For questions, please contact xup@xilinx.com

- Download a ZIP of the whole project archive (you can also clone the GitHub project):

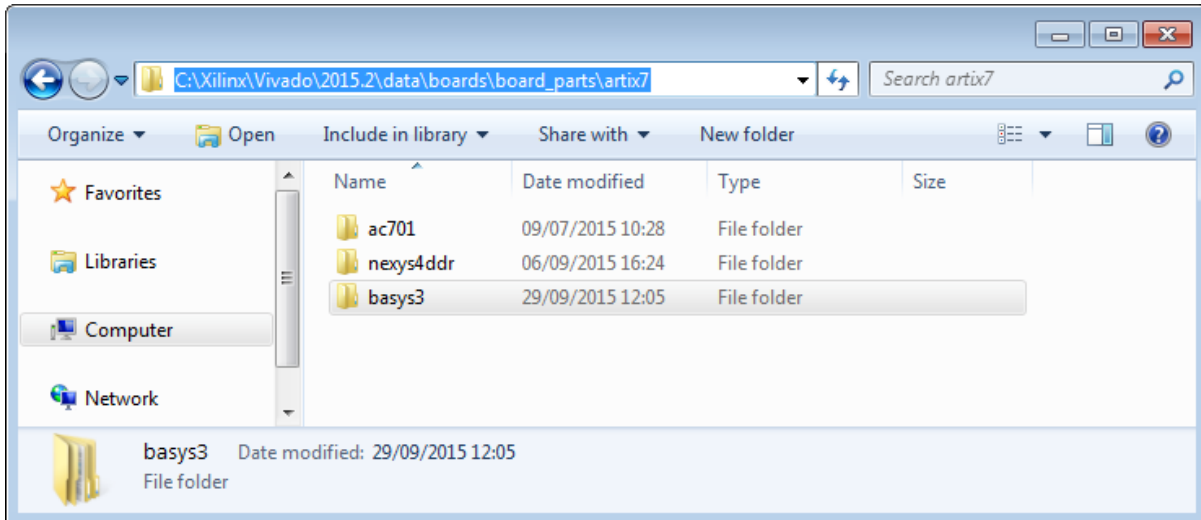


- Extract the archive, in this case to C:\

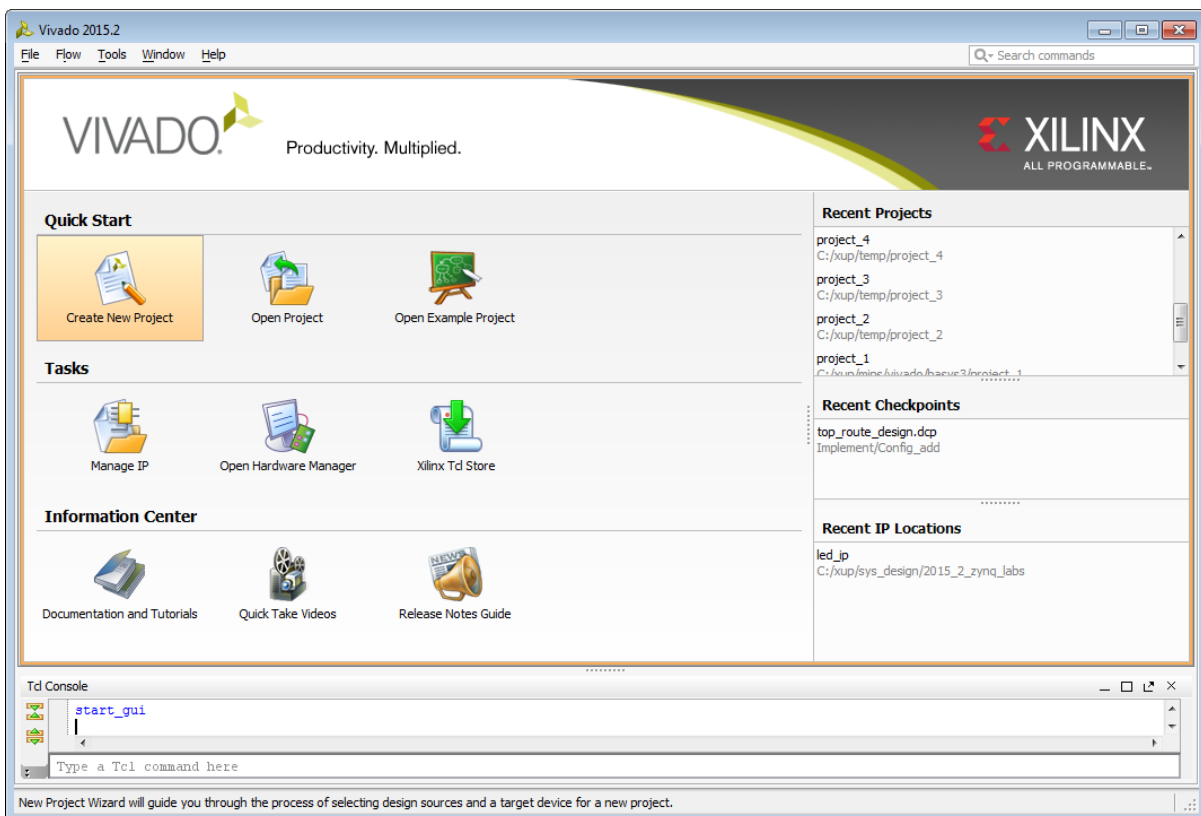


- Extract **basys3.zip**, and copy the extract the *basys3* folder to your Vivado installation.

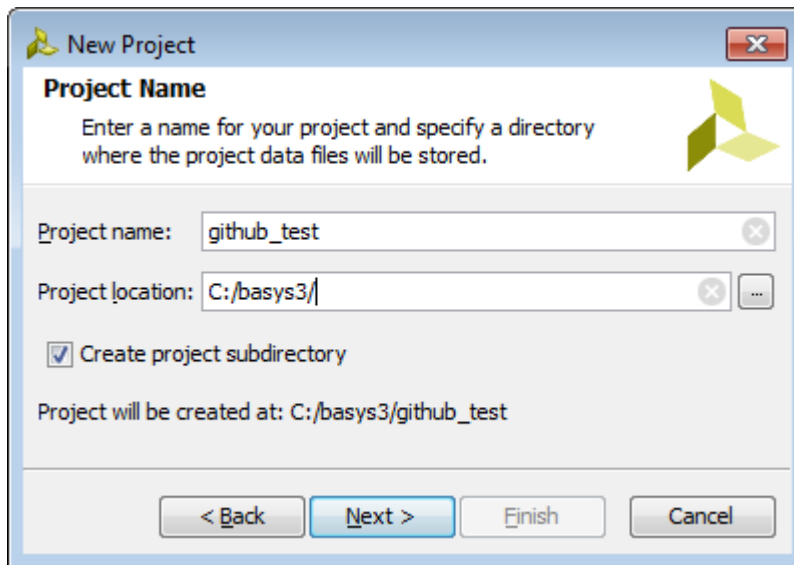
E.g. C:\Xilinx\Vivado\2015.2\data\boards\board_parts\artix7



- Open Vivado, and *Create a New Project*:



- Choose a project name and location



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

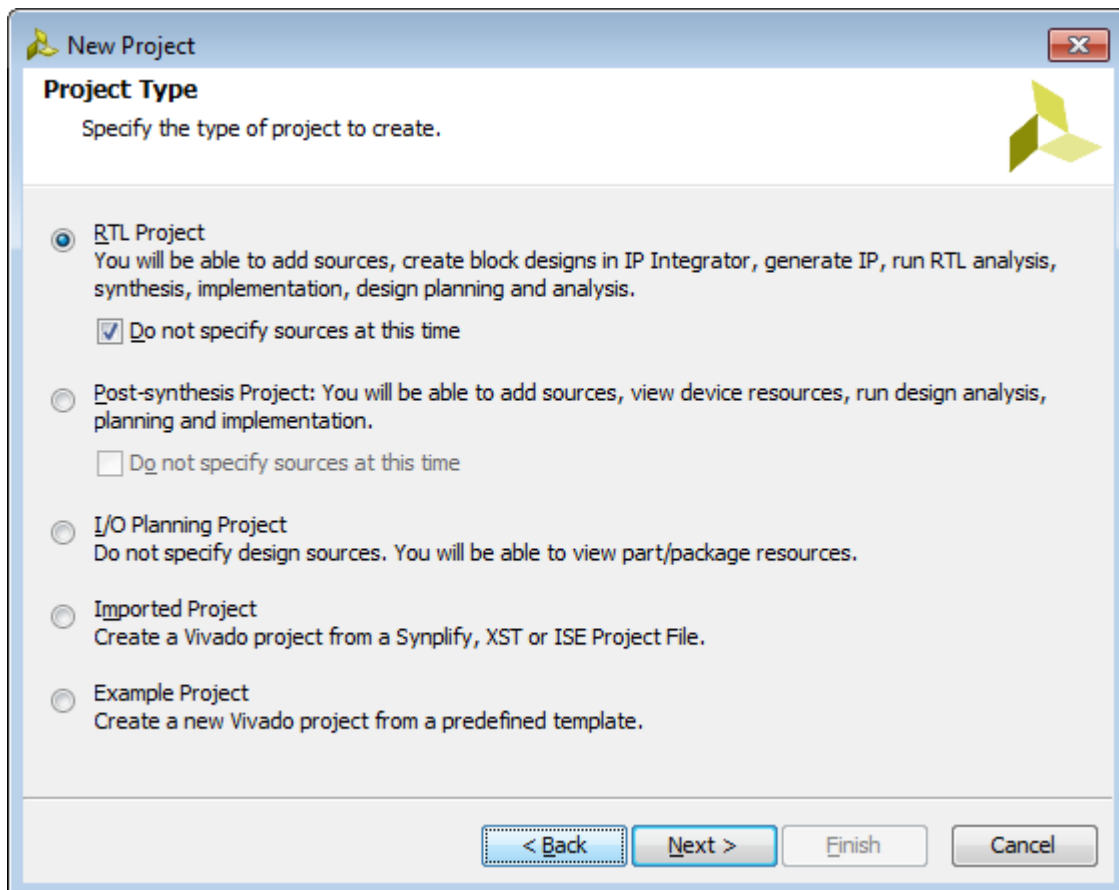
Project location:

☒ Create project subdirectory

Project will be created at: C:/basys3/github_test

< Back Next > Finish Cancel

- Choose *RTL project*, and check *Do not specify sources at this time*



New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time

☐ **Post-synthesis Project:** You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

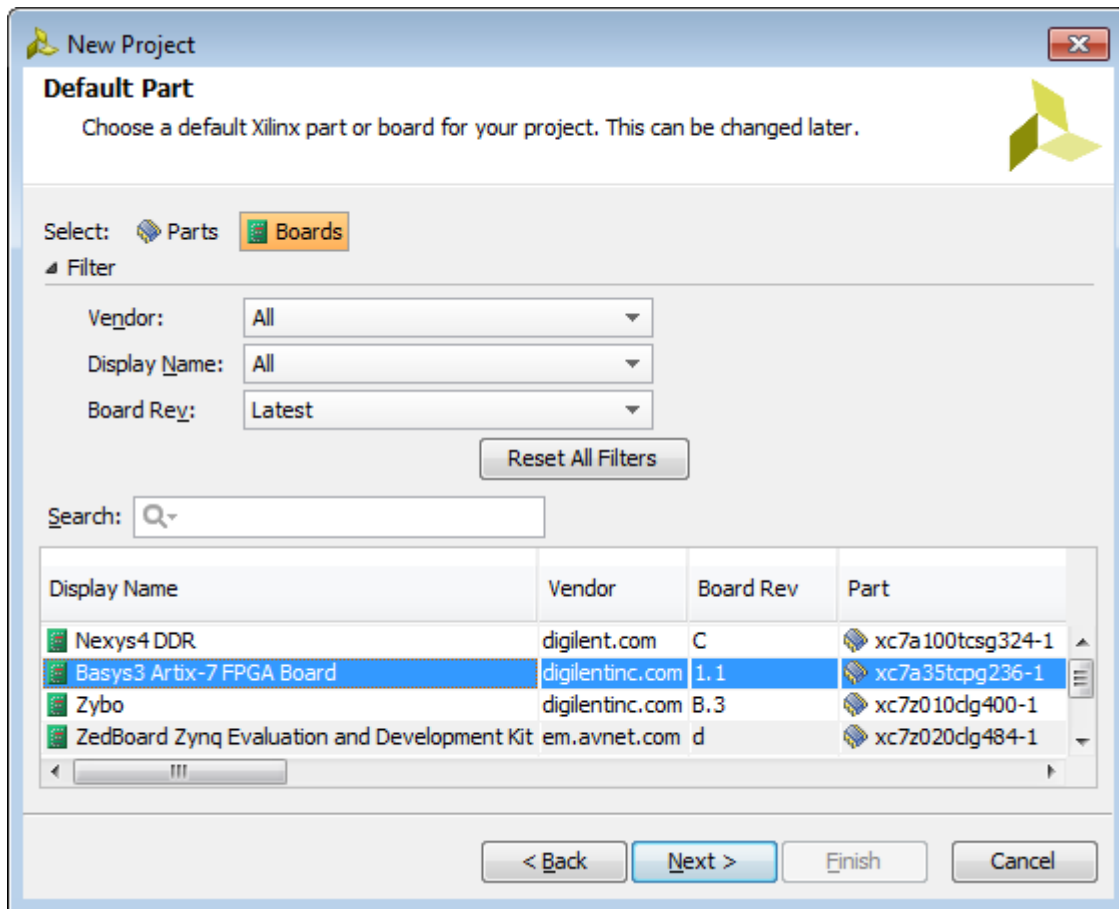
☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

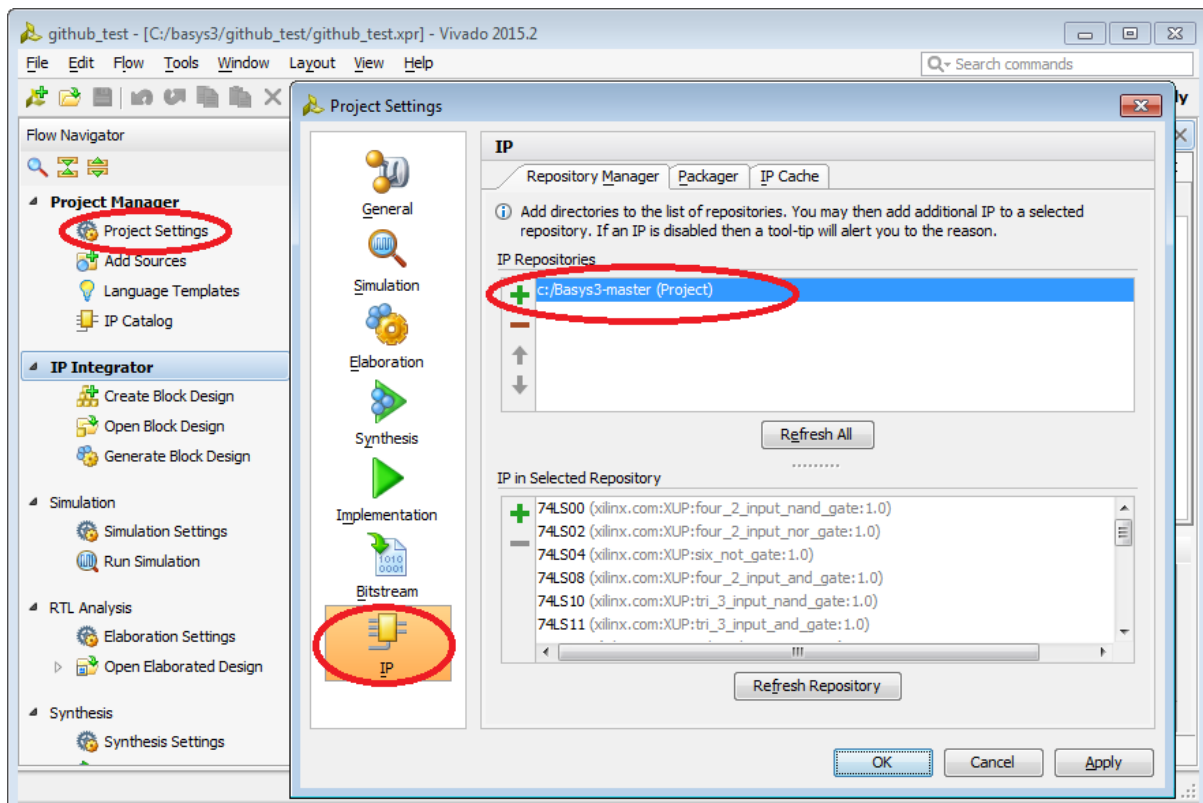
☐ **Example Project**
Create a new Vivado project from a predefined template.

< Back Next > Finish Cancel

- Click *Board*, and select the **Basys3**

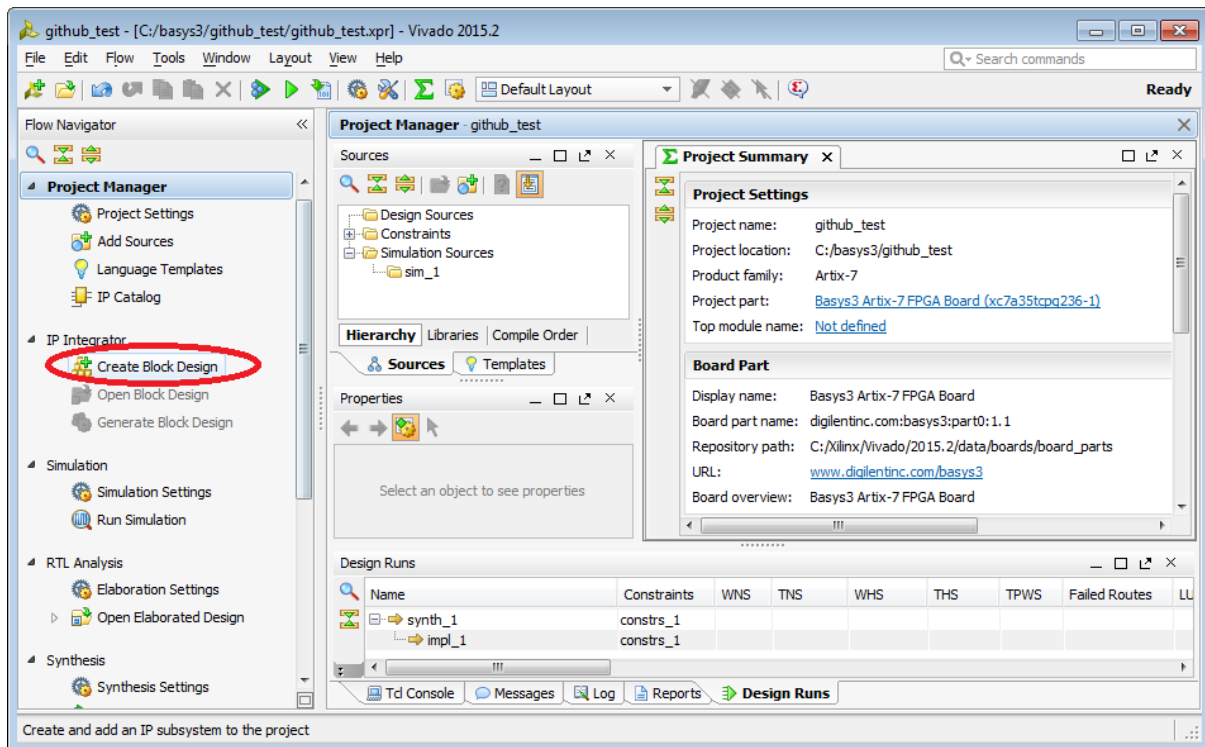


- Click *Project settings*, select *IP*, click on the *Add Icon* and browse to the extracted archive:



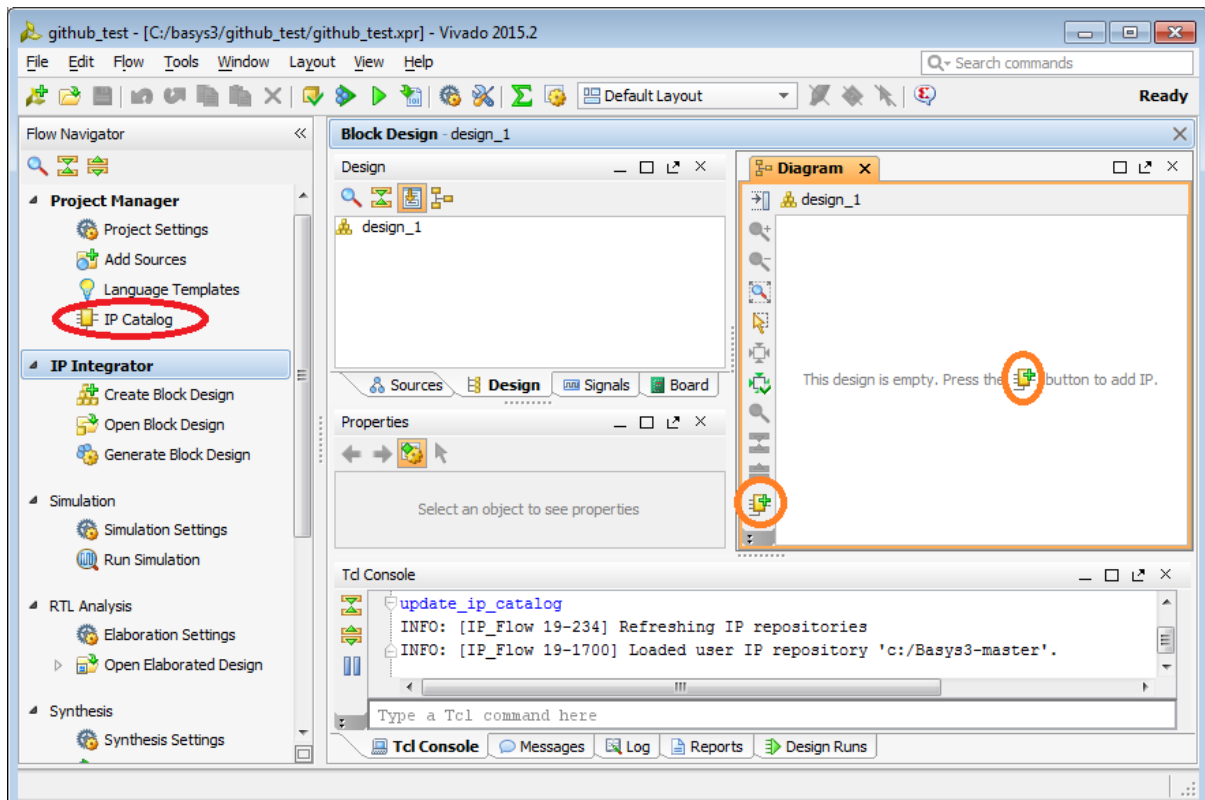
Notice the list of *IP in Selected Repository*. This is the IP that has been found in the directory.

- Create a new IP Integrator *Block Design*



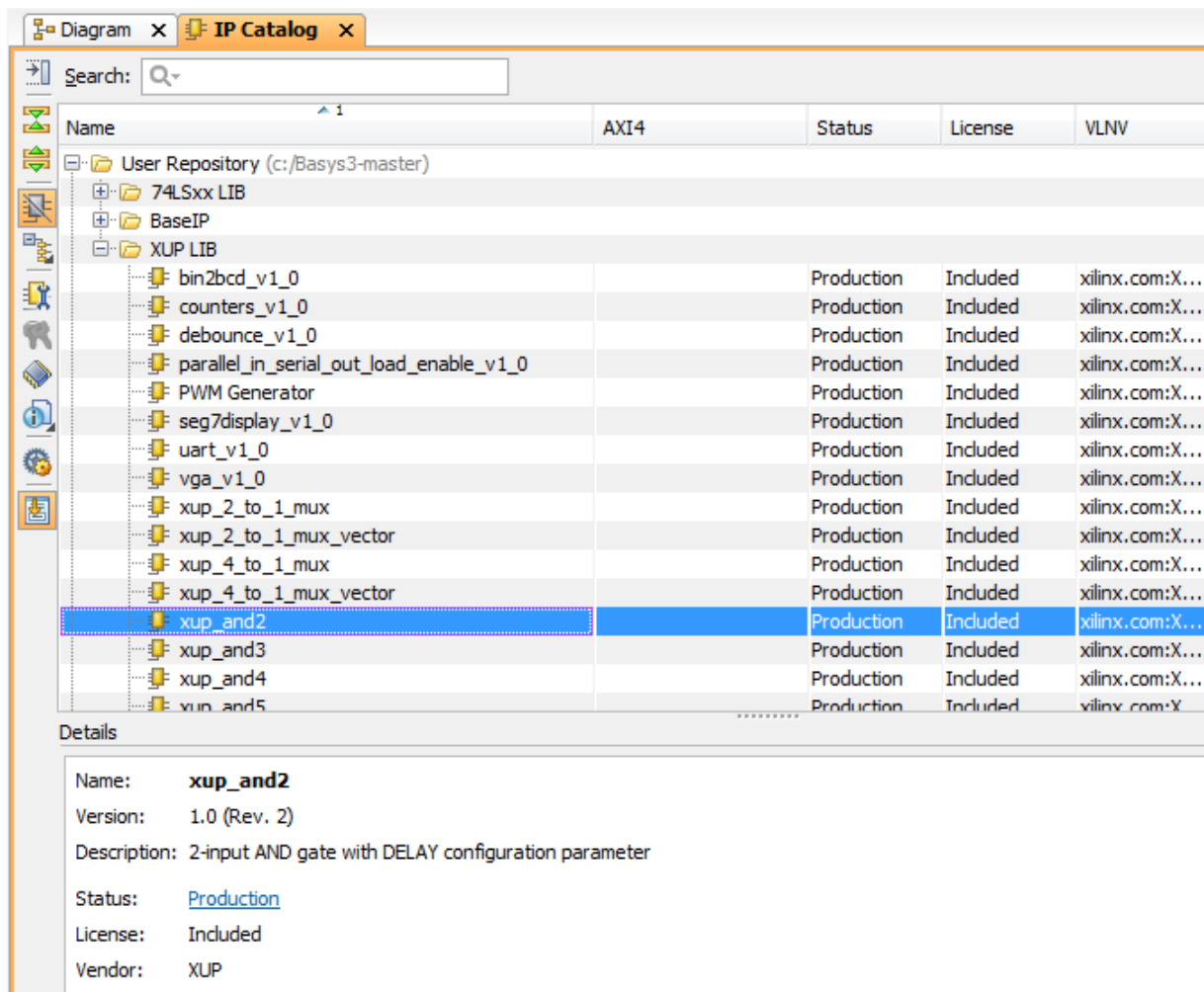
You can click on the *Add IP* icon. (You can also right click and select *Add IP*, or press Ctrl + I.) You can also add IP from the Catalog.

- Click on *IP Catalog* on the left



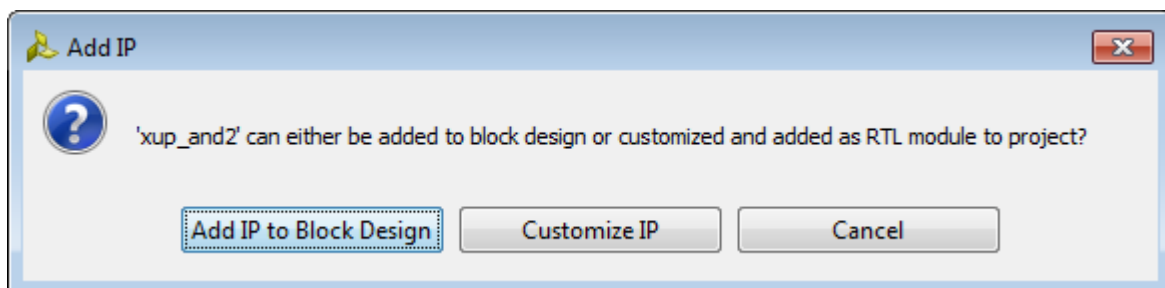
You can browse and search the Catalog. The XUP IP has been included under the *User Repository* folder.

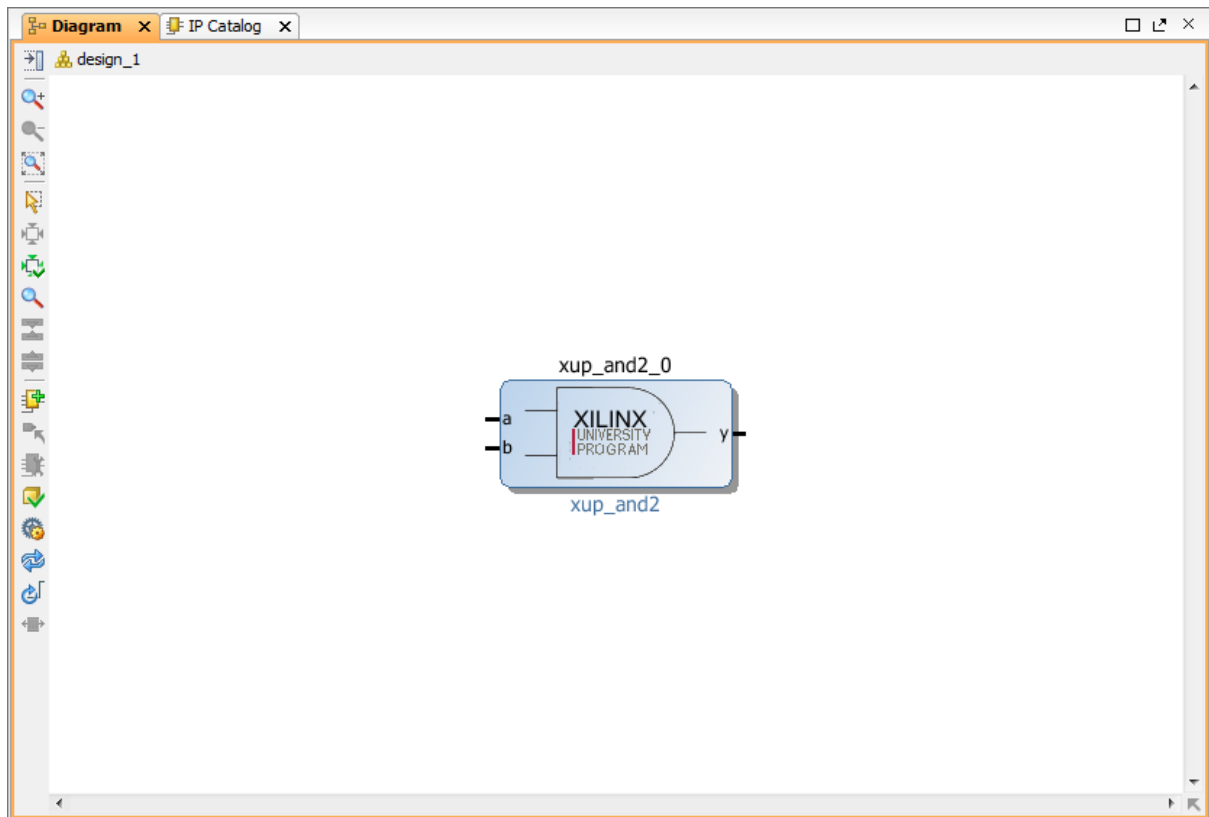
- Expand XUP LIB, and double click on *xup_and2*



From the Catalog, you will have the option to *Add IP to Block Design* (IP Integrator flow), or to *Customize IP* (non-IP Integrator flow). *Customize IP* will generate the HLD instantiation files for using in a standard HDL flow, outside an IP Integrator block diagram.

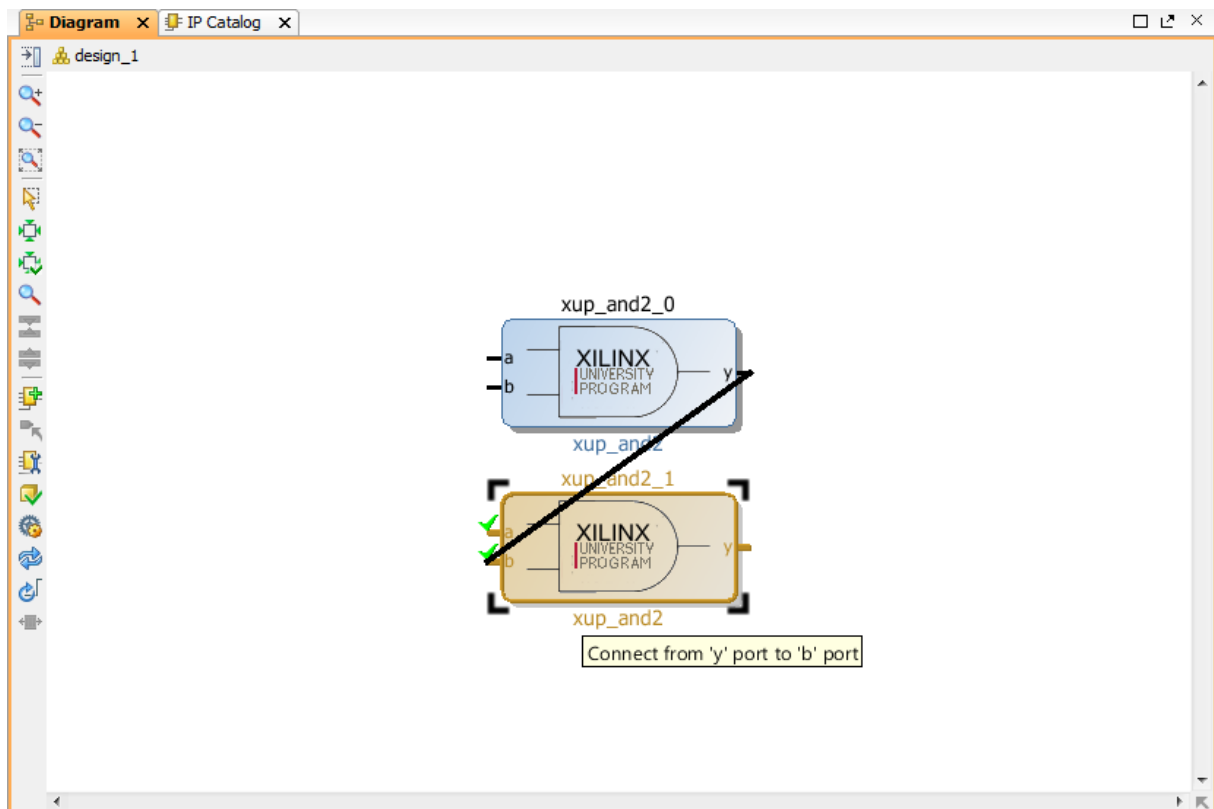
- Click Add IP to Block Design



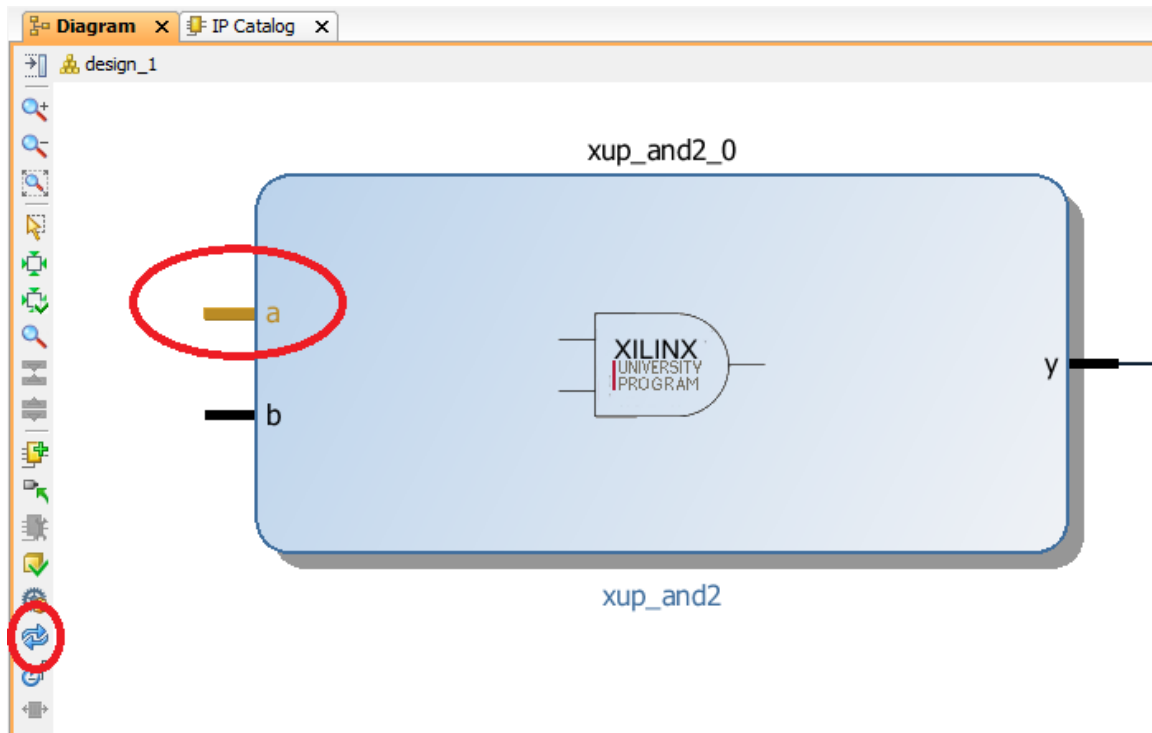


You can then copy or add more IP blocks to your design.

Ports can be connected by clicking and dragging.

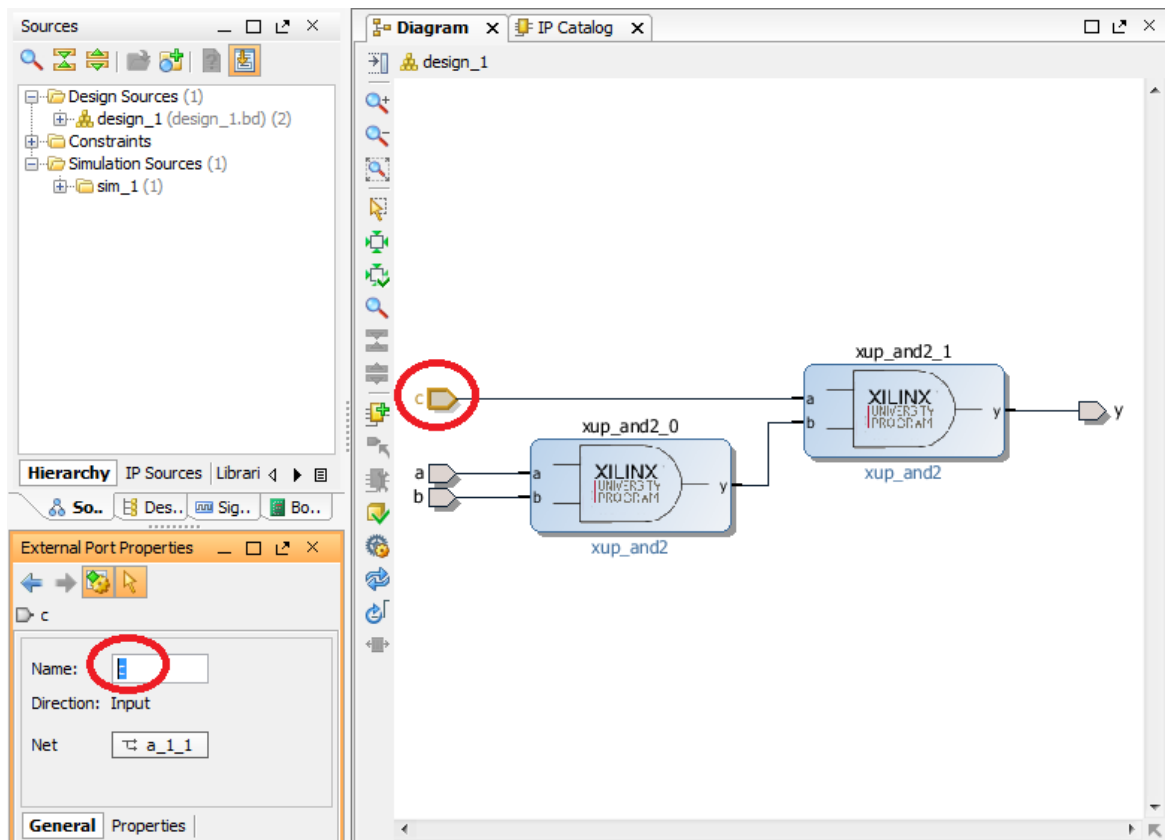


- To connect make a port external (to allow it to connect to an FPGA pin), click on a port to select it, right click and select *Make External* (Ctrl + T)



You can also click on the redraw button to automatically redraw the whole design.

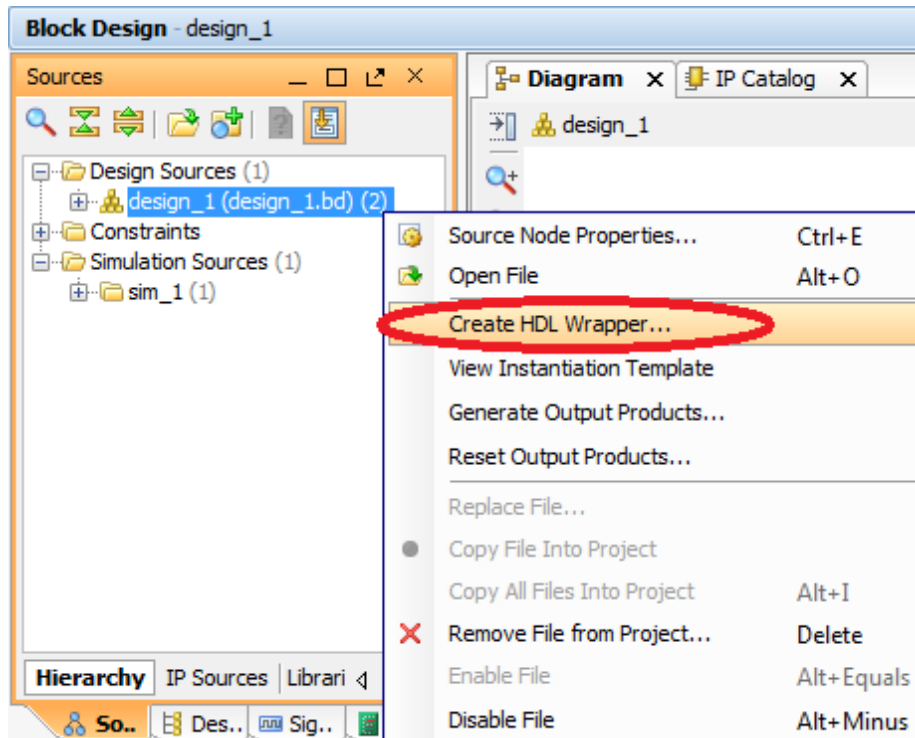
You can change a port name by clicking on the port in the block diagram, and changing its name in the *Properties* tab:



You can run a design rule check by pressing F6 to check for any errors.

Before building the design a HDL wrapper must be generated.

- Right click on the block design file in the sources panel, and select *Create HDL Wrapper*.



You can add you own HDL to the project, and instantiate this block in your code.

You can also choose to allow Vivado to automatically update this HDL file. This means that when you make a change to the block design, the HDL file will be automatically updated. If you want to modify this HDL file, choose the option to *copy*.

You may need to add pin constraints to your design. After doing this, the bitstream for this design can now be generated.

For questions, please contact xup@xilinx.com

Using the projects

- Go to the project directory and follow the readme file:

e.g. C:\Basys3-master\Projects\Logic_Design\CN_Design\array_multiplier\

- Start Vivado, and change to the `src` directory (you can also do this from the Vivado tcl prompt)

```
cd {C:\Basys3-master\Projects\Logic_Design\CN_Design\array_multiplier\src}
```

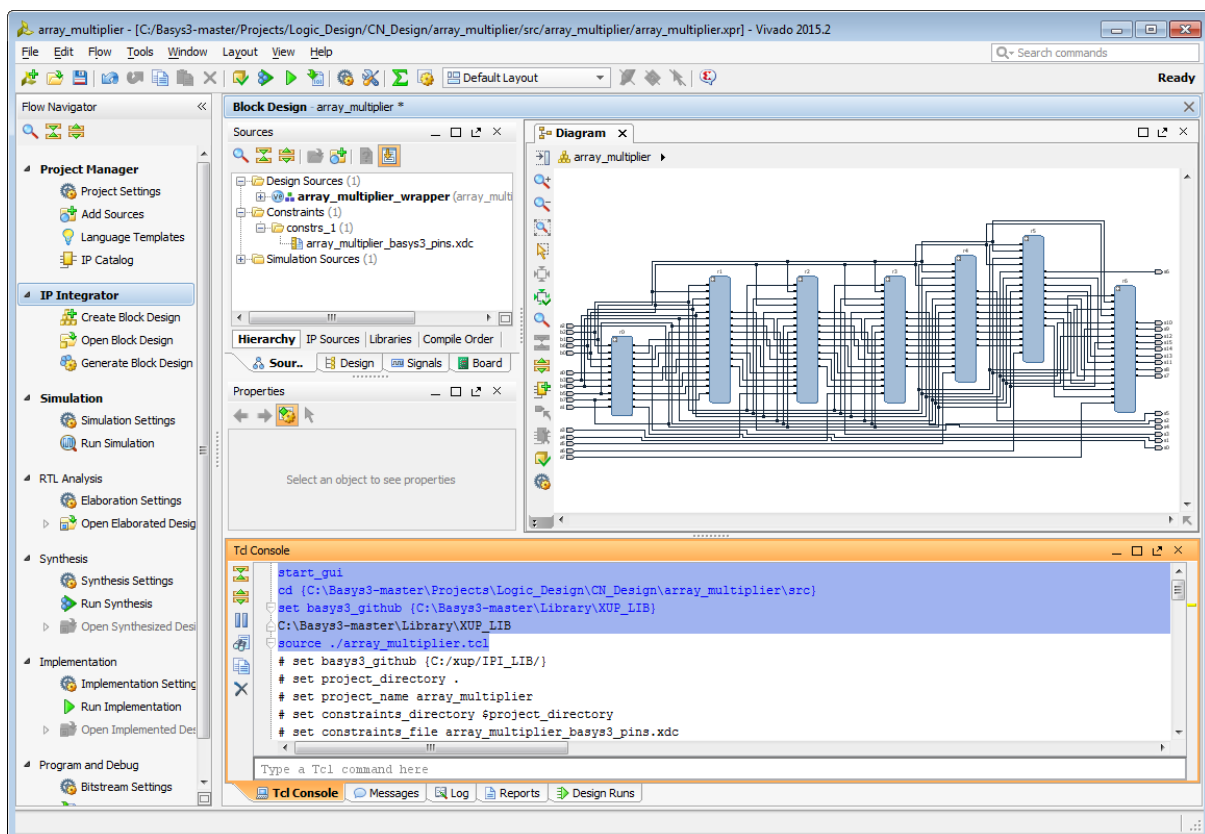
- As instructed in the readme file, set the `basys3_github` path

```
set basys3_github {C:\Basys3-master\Library\XUP_LIB}
```

- Source the tcl script

```
source ./array_multiplier.tcl
```

The project will automatically build. You can then run simulation, or generate the bitstream to test on the board.



For questions, please contact xup@xilinx.com