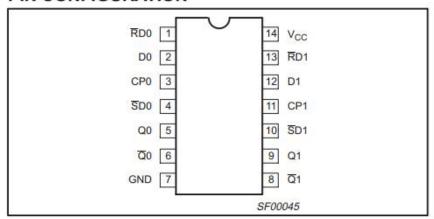
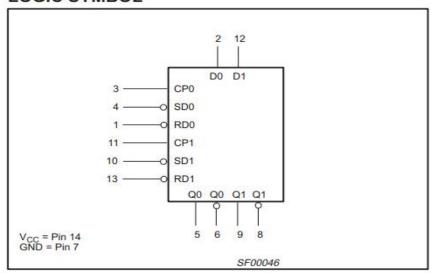
# **Dual D-type flip-flop**

## 74F74

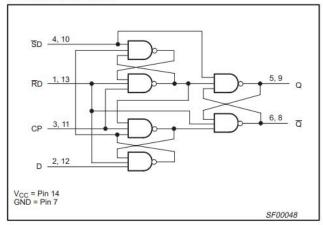
### PIN CONFIGURATION



#### LOGIC SYMBOL



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

INPUTS				OUTPUTS		OPERATING
SD	RD	CP	D	Q	Q	MODE
L	Н	Х	X	Н	L	Asynchronous set
Н	L	X	Х	L	Н	Asynchronous reset
L	L	Х	X	Н	н	Undetermined*
Н	Н	1	h	Н	L	Load "1"
Н	Н	1	1	L	Н	Load "0"
Н	Н	1	X	NC	NC	Hold

#### NOTES:

H = High voltage level

h = High voltage level one setup time prior to low-to-high clock transition

= Low voltage level one setup time prior to low-to-high clock transition

NC= No change from the previous setup

X = Don't care

↑ = Low-to-biol = Low-to-high clock transition

Not low-to-high clock transition
 This setup is unstable and will of

= This setup is unstable and will change when either set or reset return to the high level.