IMPLEMENTATION OF MAXIDISCAP-SPECIFIC FUNCTIONS ON THE SIRAMATRIX BOARD

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POWER CONVERTERS IN CERN

A power converter is a device that takes energy from the electrical grid and transforms it to control the flow of energy supplied to a specific load.

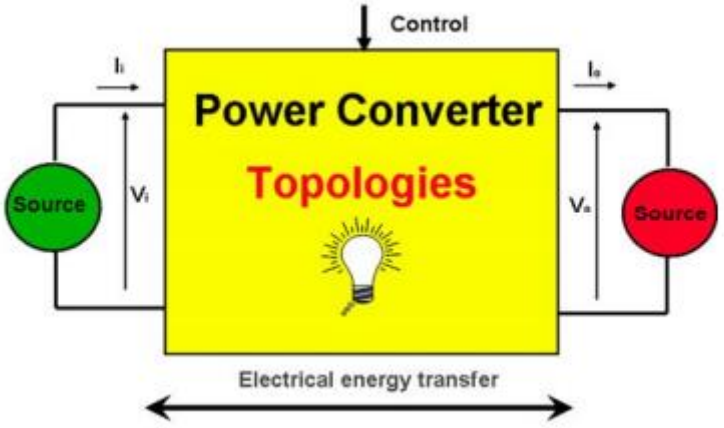


Figure 1 Power Converter Definition [1]

Particle accelerators are complex machines which consume a lot of electricity. About 70% to 90% of the total energy needed in a particle accelerator is consumed by the magnets and the radio-frequency (RF) systems. Furthermore, these loads have very particular requirements, so that the power converters necessary for this applications fall outside the range of classical industrial products. [2]

The work of this project gravitated around fast pulsed power converters used to supply magnet loads in various accelerators in the CERN complex. In CERN, fast pulsed power converters are understood to be switching power converters with pulsed lengths of 100µs to few ms.

The different magnet types in the accelerator complex are used for crucial tasks involving the control of the beam. In synchrotron machines, for example, dipole magnets are used to bend the particle beam. The beam energy in this type of accelerators is proportional to the magnetic field of the dipole magnets, and the magnetic field is in turn generated by the current circulating in the magnet coils. It follows that, to control the beam, the operators need to be able to control the current through the magnets with high precision.

However, in a magnet, the relation between the current and the magnetic field is not linear due to magnetic hysteresis of the core and eddy currents. This is one of the main difficulties that must be tackled when designing power converters which must provide precision control of the current output. Furthermore, when the power converters in the accelerators receive a current reference from the control room, it must be executed with precise timing throughout the whole accelerator, giving way to yet another sensitive design consideration. [2]

The goal of this project was to write and/or update the converter-specific modules to be implemented in the Spartan6 FPGA found in the SIRAMATRIX regulation board, for the MAXIDISCAP fast-pulsed power converter. This board is used to implement converter specific functions.

THE MAXIDISCAP

The Maxidiscap is designed to produce trapezoidal current waveforms with high precision flat-top for different magnet loads, mostly quadrupoles. These converters use a high power *insulated-gate bipolar transistor* (IGBT) module in its ohmic region to perform output current regulation.

The system is based on the use of a DC voltage source to ramp the output current and a linear stage to control the current during flat-top. The DC voltage source is formed by a large capacitor bank *C* that is first charged and then discharged during the pulse. [3]

The MAXIDISCAP is designed to meet following basic specifications:

- Maximum output current: 350 A
- Maximum output voltage: 1000 V
- Maximum flat-top duration: From 300us to 10ms
- Maximum repetition rate: 5 Hz
- *Im* precision during flat-top: 1000ppm
- Input from the mains: 230 V

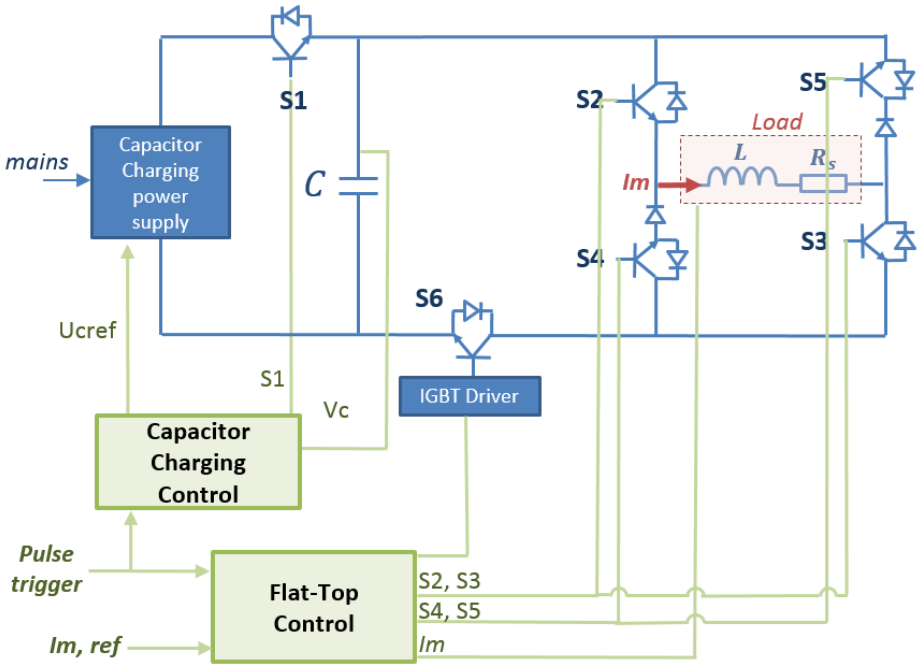


Figure 2 MAXIDISCAP converter topology

Observe in figure 2 that the magnet load is modelled as an inductance *Lm* in series with a resistor *Rm.* For a simple explanation of the converter operation it is sufficient to view the IGBT modules S1 through S2 as switches.

The operation of the converter can be divided into four main phases:

- Phase 1: Capacitor Charging
- Phase 2: Ramp Up
- Phase 3: Flat-top
- Phase 4: Ramp Down

During phase 1, S1 is on, whereas the rest of the IGBT modules are off, and the capacitor bank is given time to charge. See figure 3.

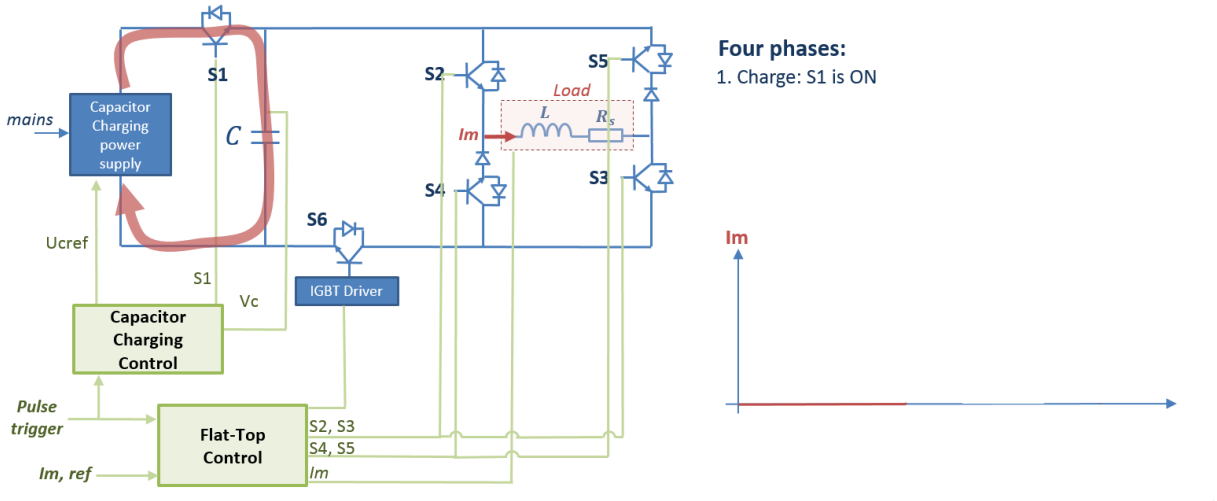


Figure 3 Capacitor Charge.

During Phase 2, *S2* and *S3* are switched on. *S6*, the high power IGBT module, is in saturation mode. See figure below. The output current *Im* ramps with a slope given by *Vm/L* if the resistive part of the load is neglected.

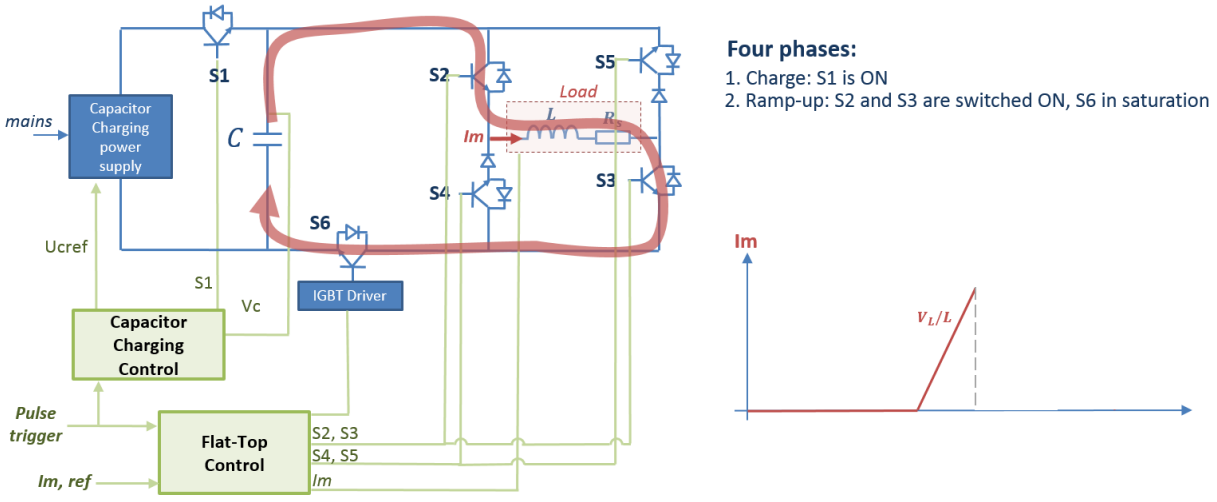


Figure 4 Ramp up of the current.

When the magnet current reaches its reference value *Iref,* which is set by control, *S5* is operated in its active region. Regulation of the current takes place during the flat-top. The output current of the converter is then regulated by controlling the Vce voltage of S6.

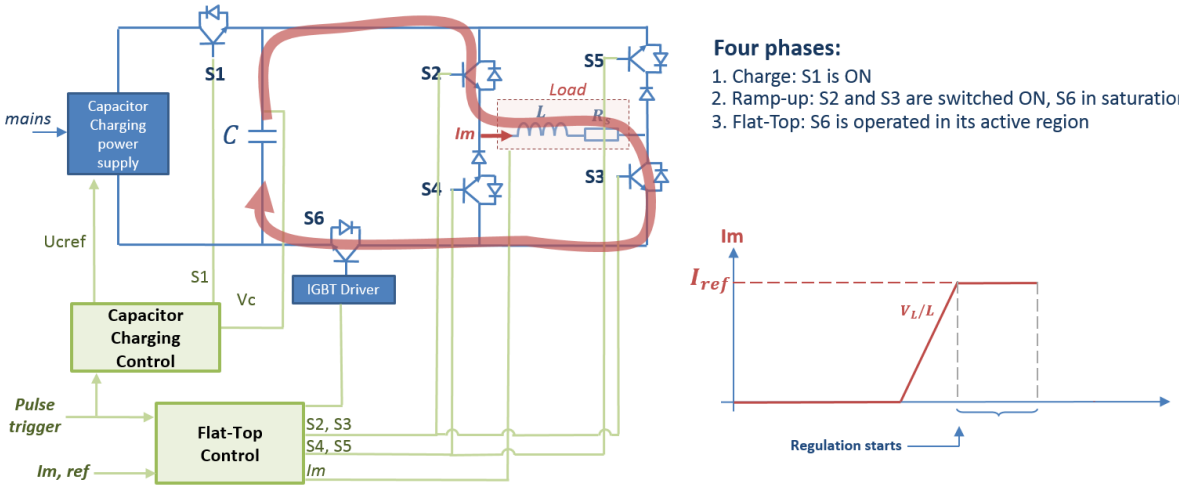


Figure 5 Flat-top.

After reaching the target duration of the flat-top, *S2* and *S3* are switched off while *S4* and *S5* are switched on. The current flows through the antiparallel diode of *S5* and the energy stored in the magnet load is recovered in the capacitor bank *C*. When the output current reaches zero, the diodes in series with *S4* and *S5* are switched off and the pulse is terminated. [4]

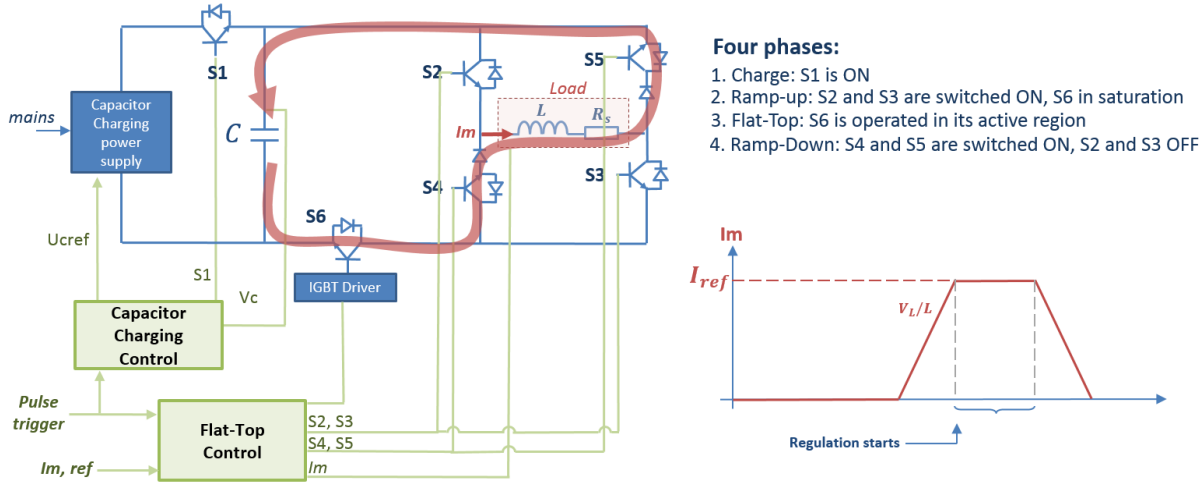


Figure 5 Ramp-down.

THE SIRAMATRIX AND THE CONTROL SYSTEM OF THE MAXIDISCAP

A Function Generator Controler (called FGC) is the main board in the control systems used in CERN to control the various power converters. Three different generations of the FGC have been developed at CERN, the FGC1, FGC2 and the FGC3. Currently, a radiation tolerant version of the FGC called the FGCLite is under development in the CCE section.

The RegFGC3 is a system which expands the capabilities of the FGC3. The FGC3 alone is capable of controlling a small power converter, however, the available I/Os are very limited. The RegFGC3 is in fact nothing more than the FGC3 connected to various cards which provide expanded functionality, and all these cards feature FPGAs unto which common communication modules, timing modules and safety chains are programmed. The SIRAMATRIX board is one such card.

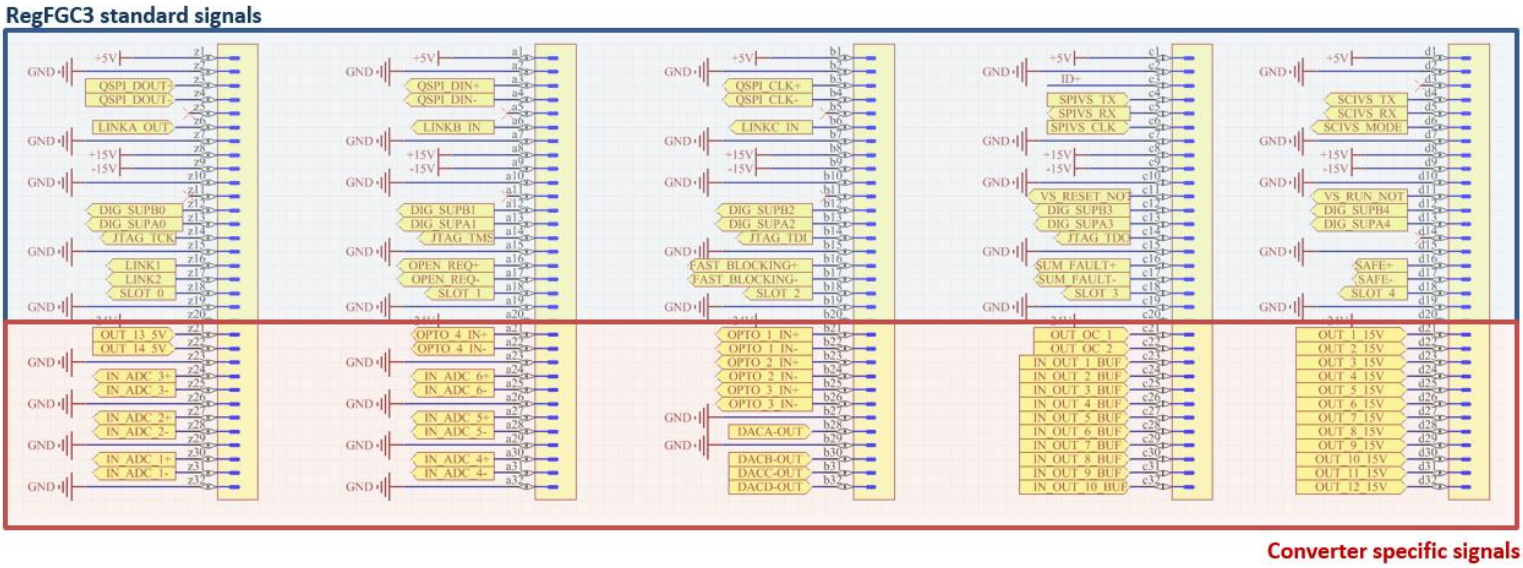
A list of the RegFGC3 standard modules, which are shared among all cards, and a short description of the functionality in regards to the SIRAMATRIX follows below.

- SPI Communication: Transmission of reference values from FGC3 to SIRAMATRIX
- SCI Communication: Transmission of regulation parameters from FGC3 to SIRAMATRIX
- QSPI Communication: Diagnostic interface module, transmission of faults from SIRAMATRIX to FGC3
- Timing: Timing signals SUPB/SUPA are timing signals from the State Control of the FGC3 to the SIRAMATRIX
- Daisy chains: OPEN Request, Fast Blocking, Sum Fault, Safe. If any of the chains are opened it means one of the cards in the RegFGC3 has discovered a fault and actions will be taken either to protect the converter or shut it down completely.

The main functionalities of the SIRAMATRIX are the following:

- Pulse Control / Synchronization
- Regulation Algorithm Execution
- Interaction with the REGFGC3 environment

In the next figure, the pinout from the backplane of the card is shown. It shows which pins are dedicated to RegFGC3 functionality and which are specific to the converter.



The converter specific signals correspond to 6 ADC channels, 4 DAC channels and various GPIO.

ADC Channels

ADC Channel	ADC	Conditioning	Description	Throughput
CH 1	AD7621	G = 0.2 - BP = 1.5MHz	16bits,Bipolar,Parallel	3 MSPS
CH 2	AD7621	G = 0.2 - BP = 1.5MHz	16bits,Bipolar,Parallel	3 MSPS
CH 3	AD7621	G = 0.2 - BP = 0.5MHz	16bits,Bipolar,Serial	1 MSPS
CH 4	AD7621	G = 0.4 - BP = 0.5MHz	16bits,Unipolar,Serial, Precision	1 MSPS
CH 5	AD7621	G = 0.2 - BP = 0.5MHz	16bits,Bipolar,Serial	1 MSPS
CH 6	TLV2541	G = 0.2 - BP = 0.5MHz	12bits,Bipolar,Serial, Low speed	200 KSPS

DAC Channels

DAC Channel	ADC	Output range	Description	Max throughput
DACA	DAC904	+/-10V	14bits, Fast DAC	160MSPS
DACB	LTC2641	+/-10V	16bits, Slow DAC	3MSPS
DACC	LTC2641	+/-10V	16bits, Slow DAC	3MSPS
DACD	LTC2641	+/-10V	16bits, Slow DAC	3MSPS

GPIOs

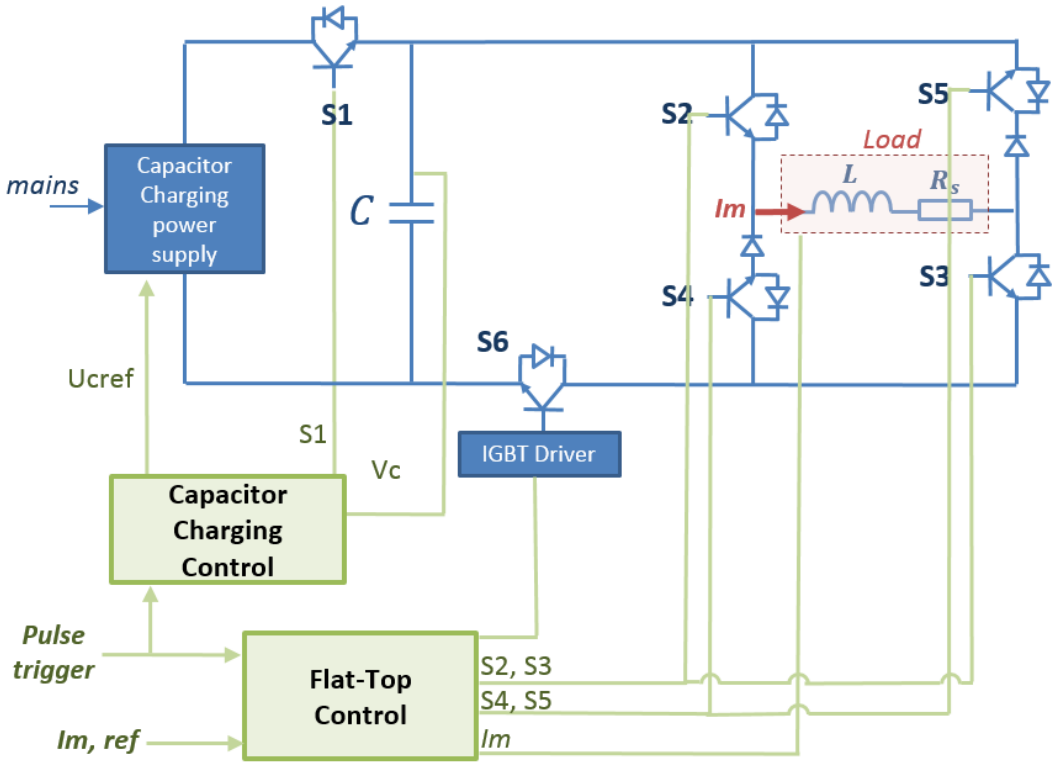
Name	Number	Direction	Type
OUT_X_15V	1 .. 12	OUT	MOS driver output (15V)
IN_OUT_X_BUF	1 .. 10	IN/ OUT	LSTTL
OUT_OC_X	1 .. 2	OUT	Open Drain
OPTO_X_IN+/-	1 .. 4	IN	Opto (Differential)
OUT_X_5V	13 .. 14	OUT	LSTTL

ADC CONFIGURATION AND OPERATION

The SIRAMATRIX board features 6 ADC channels, which can be used to read information from the state of the power converter. In the MAXIDISCAP, only ADC channels 2 through 4 are used.

Channel	Signal	Mode	ADC Type	Input	Digital Output
2	Uigbt	bipolar	AD7621	+/-10V	8000=-2000V / 7FFF=2000V
3	Uc	bipolar	AD7621	+/-10V	8000=-2000V / 7FFF=2000V
4	Im	unipolar	AD7621	0-10V	8000=0 / 7FFF=Inominal

These signals correspond to voltage over S6, voltage over C and Im in the figure below, which was also used in section 1.2.2.1 to explain the operation of the converter.



The characteristics of the ADCs are shown below.

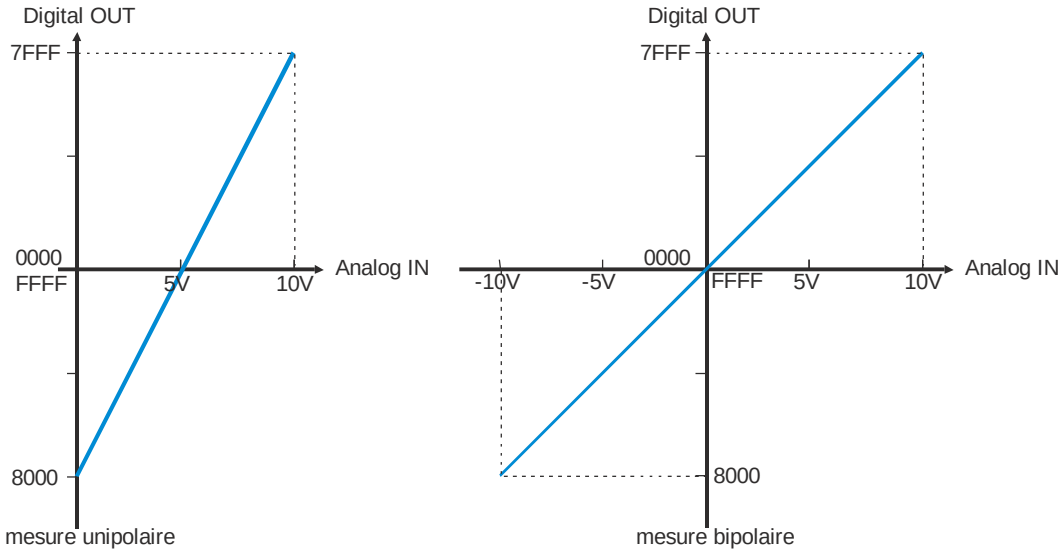


Figure 6 Characteristics of the ADCs.

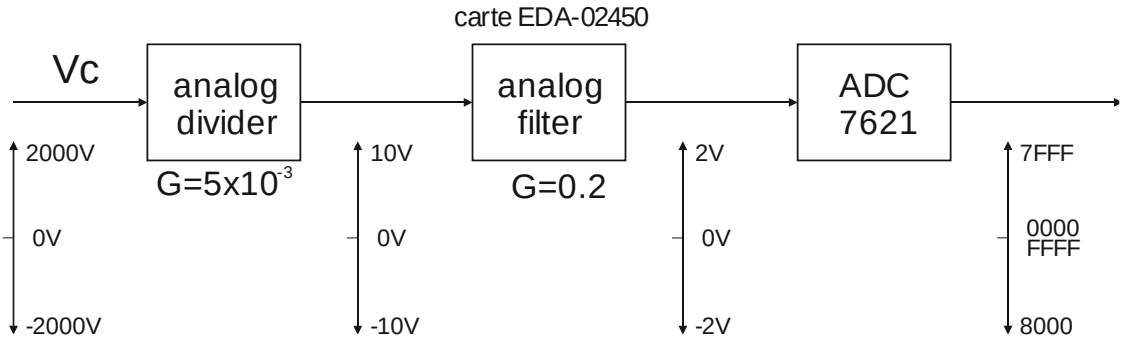


Figure 7 ADC Input path.

DAC CONFIGURATION AND OPERATION

Channel	Signal	Mode	DAC Type	Digital Input	Analog Output
A	IGBT cmd	Bipolar	LTC2641-16	0000=-10V / 3FFF=+10V	+/-10V
B	Ucref	Bipolar	LTC2641-16	0000=-10V / 7FFF=+10V	0 – 10V → 0V – 1000V

The characteristic of the DACs is shown below

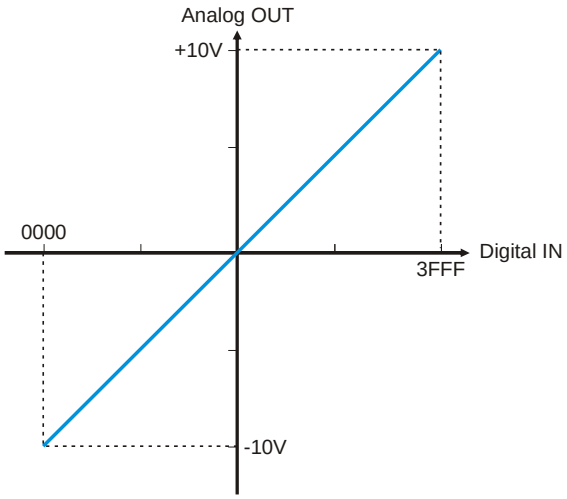


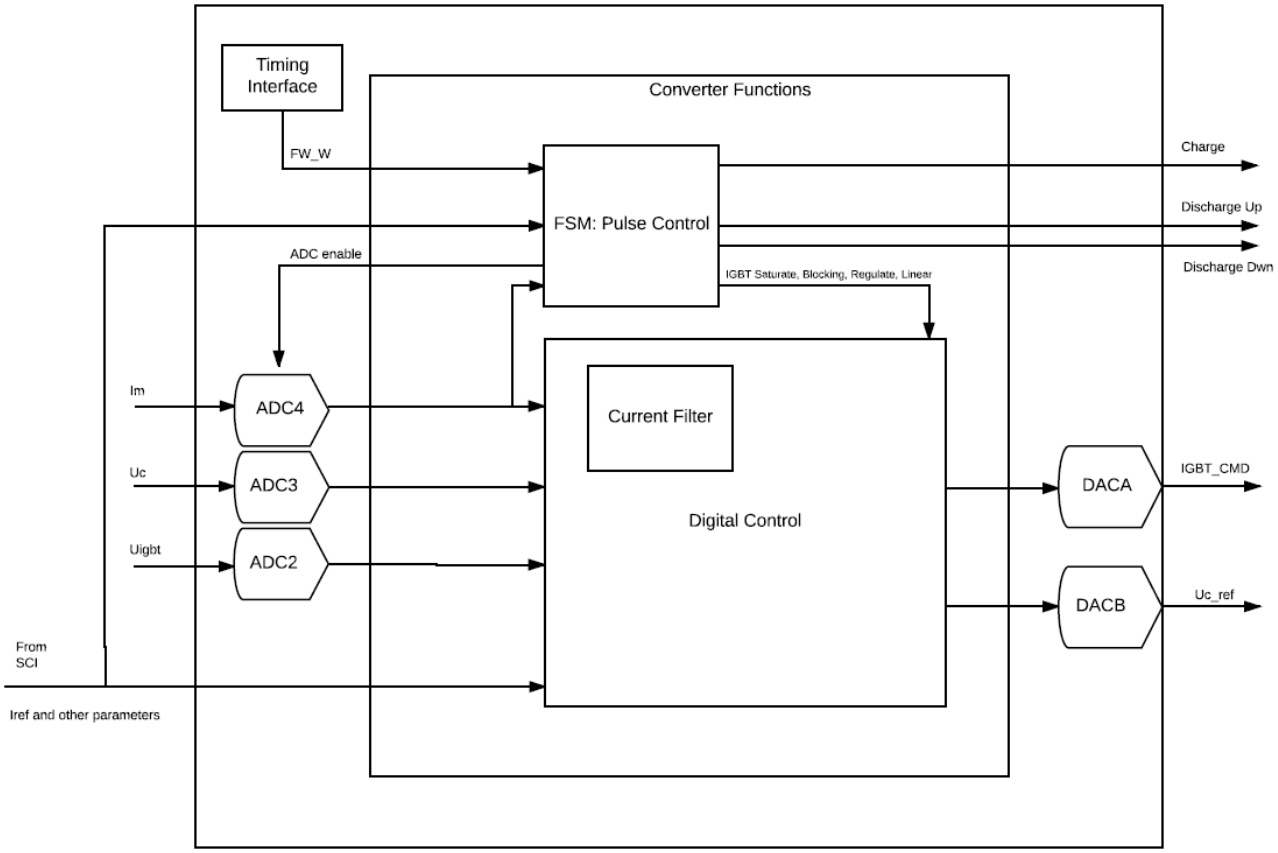
Figure 8 Characteristic of the DACs.

$Vout_{DAC}$ = (Vdigital/65535)x5V

and $Vout_{board}$ = ($Vout_{DAC}$x4)-10V = (Vdigital/65535)x20-10V

FPGA BLOCK DIAGRAM FOR CONVERTER SPECIFIC BLOCKS

The block diagram below depicts only the blocks concerned with the operation of the MAXIDISCAP specifically, for ease of understanding.



1.1 PULSE CONTROL

This block describes the finite state machine that controls which phase of the pulse the converter is in.

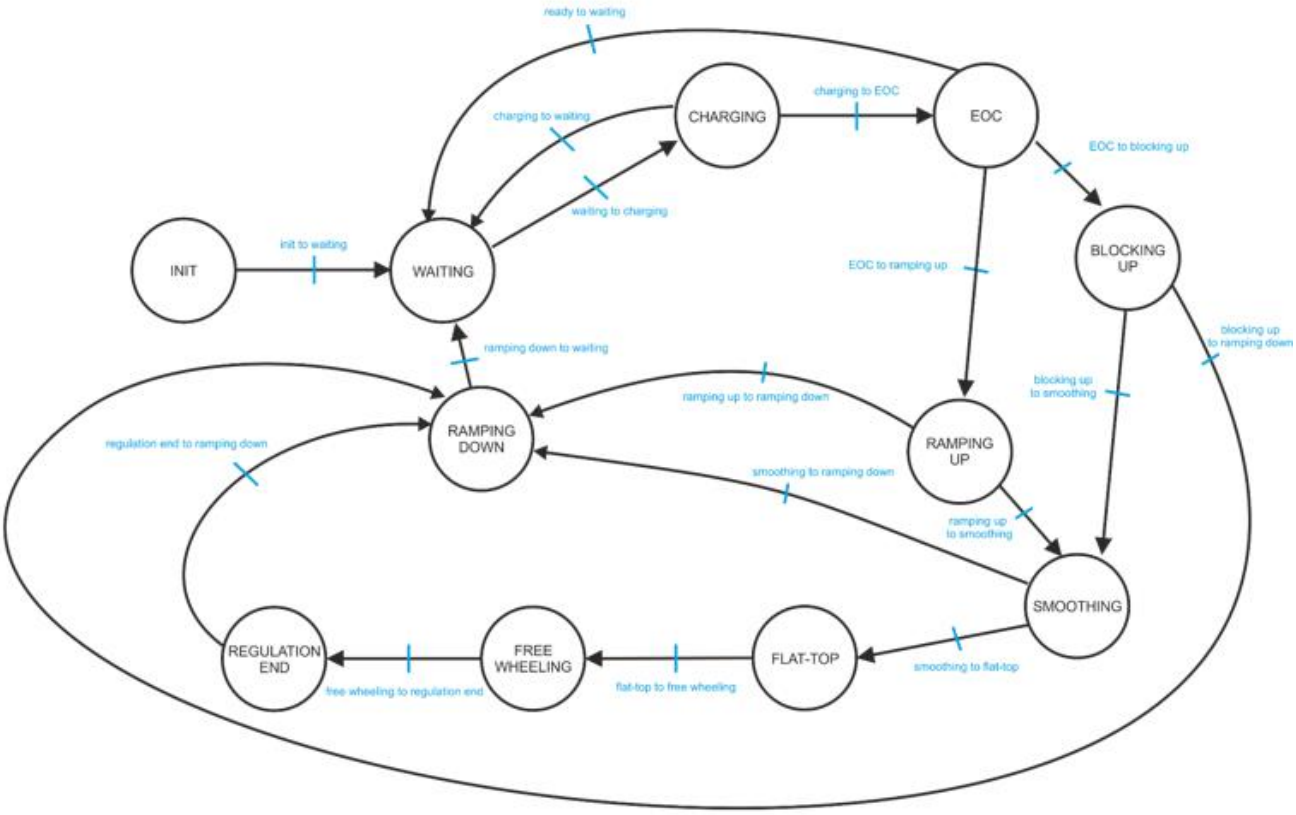


Figure 9 Finite State Machine State Diagram.

Descriptions of the various states, their outputs and the transition sentitivity requirements follow bellow.

1.1.1 INIT

This is the initialization state. In this state, all the ADCs are powered down and no information is streaming in from the converter. The capacitor is prevented from charging and the IGBT is blocked. It is not desirable for the ADCs to be continuously on during the operation of the power converter due to power dissipation caused by the discrete components involved in the input stage of the ADCs, so they are only powered during the flat-top of the current.

1.1.1.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=0	Disable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=1	Power down ADC2
output	PD3_o=1	Power down ADC3
output	PD4_o=1	Power down ADC4
output	IGBT_Saturate_o = 0	IGBT is not saturated
output	IGBT_Blocking _o=1	IGBT is blocked
internal	wait 100ms	

1.1.1.2 Transition: Init to Waiting

Sensitivity
The initialization counter must reach 100ms.

Comment
Exit init state after 100ms delay.

Equation
Init_Counter=100ms

1.1.2 WAITING

In this state, the FSM waits for the FW timing pulse that indicates that operation should start.

1.1.2.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=0	Disable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=1	Power down ADC2
output	PD3_o=1	Power down ADC3
output	PD4_o=1	Power down ADC4
output	IGBT_Saturate_o = 0	IGBT is not saturated
output	IGBT_Blocking _o=1	IGBT is blocked

1.1.2.2 Transition: Waiting to Charging

Sensitivity

Condition	Comment
Blocking_Pulse_i=0	Pulse is enabled
ON_i=1	ON command from state control
FW_W_i = rising edge	FW pulse received

Comment

System starts a pulse cycle

Equation

(Blocking_Pulse_i=0) & (ON_i=1) & (FW_W_i =↑)

1.1.3 CHARGING

During this state, the charger is enabled and the capacitor bank charges.

1.1.3.1 Actions

	Action	Comment
output	Charge_o=1	Enable charging
output	Discharge_up_o=0	Disable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=1	Power down ADC2
output	PD3_o=1	Power down ADC3
output	PD4_o=1	Power down ADC4
output	IGBT_Saturate_o = 0	IGBT is not saturated
output	IGBT_Blocking _o=1	IGBT is blocked

1.1.3.2 Transition: Charging to End of Charge

Sensitivity

Condition	Comment
Blocking_Pulse_i=0	Pulse is enabled
FW_W = falling edge + 1ms delay	Wait 1ms after FW_W falling edge (W pulse) received

Comment
Charging time ended – 1ms delay added after W pulse received

Equation
(Blocking_Pulse_i=0) & (Wait1ms_after_W=ok)

1.1.3.3 Transition: Charging to waiting

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted
Pulse enable=0	discharge pulse is not authorized

Comment
Security warning or discharge pulse not allowed

Equation
(Stop_Security=1) or (Pulse_Enable=0)

1.1.4 END OF CHARGE (EOC)

A timing pulse is received indicating that the capacitor bank is to stop charging. Notice how the ADCs become enabled in this state.

1.1.4.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=0	Disable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=0	Enable ADC2 to be ready for regulation
output	PD3_o=0	Enable ADC3 (Uc) for delay calculation
output	PD4_o=0	Enable ADC4 to be ready for regulation
output	IGBT_Saturate_o = 0	IGBT is not saturated
output	IGBT_Blocking _o=1	IGBT is blocked

1.1.4.2 Transition: EOC to Ramping Up

Sensitivity

Condition	Comment
Stop_Security=0	no security warning
Delay_Enable=0	external start operation mode
START=↑	start trigger rise edge received
regulation_mode≠’00’	regulation mode is not very low current mode

Comment

Security warning or discharge pulse not allowed

Equation

(Stop_Security=0) & (Delay_Enable=0) & (ST=↑) & (regulation_mode ≠’00’)

1.1.4.3 Transition: EOC to Blocking Up

Sensitivity

Condition	Comment
Stop_Security=0	no security warning
Delay_Enable=0	external start operation mode
START=↑	start trigger rise edge received
regulation_mode=’00’	regulation mode is very low current mode

Comment

Security warning or discharge pulse not allowed

Equation

(Stop_Security=0) & (Delay_Enable=0) & (ST=↑) & (regulation_mode =’00’)

1.1.4.4 Transition: EOC (Ready) to Waiting

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted
Pulse enable=0	discharge pulse is not authorized

Comment

Security warning or discharge pulse not allowed

Equation

(Stop_Security=1) or (Pulse_Enable=0)

1.1.5 RAMPING UP

The ouput current pulse is ramped up during this state.

1.1.5.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=1	Enable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=0	Enable ADC2 to be ready for regulation
output	PD3_o=0	Enable ADC3 (Uc) for delay calculation
output	PD4_o=0	Enable ADC4 to be ready for regulation
output	IGBT_Saturate_o=1	IGBT is saturated
output	IGBT_Blocking _o=0	IGBT is not blocked
internal	start and increment ramp_up_max counter	monitor maximum ramp up duration

1.1.5.2 Transition: Ramping up to Smoothing

Sensitivity

Condition	Comment
Im=Iref-Ipredetect	flat-top is approaching

Comment
Flat-top detection is approaching, smoothing mode asserted.

Equation
Im=Iref-Ipredetect

Transition: Ramping Up to Ramping Down

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted
ramp_up_counter_flag=1	ramping up max duration is exceded

Comment
Security warning or flat-top not attained in allowed time

Equation
(Stop_Security=1) or (ramp_up_counter_flag=1)

1.1.6 BLOCKING UP

Polarize linear IGBT before low current pulse.

1.1.6.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=1	Enable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=0	Enable ADC2 to be ready for regulation
output	PD3_o=0	Enable ADC3 (Uc) for delay calculation
output	PD4_o=0	Enable ADC4 to be ready for regulation
output	IGBT_Saturate_o=0	IGBT is not saturated
output	IGBT_Blocking _o=1	IGBT is blocked
internal	start and increment BlockUp_time_max counter	monitor maximum blocking up duration

1.1.6.2 Transition: Blocking Up to Ramping Down

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted

Comment
Maximum blocking up time is detected

Equation
(Blocking_Up timeout=1)

1.1.6.3 Transition: Blocking Up to Smoothing

Sensitivity

Condition	Comment
Stop_Security=0	security warning asserted
Blocking_up timeout='1'	maximum blocking up time is detected

Comment
Maximum blocking up time is detected

Equation
(Blocking_Up timeout=1)

1.1.7 SMOOTHING

Predetection of the flat-top to smooth the transient during the flat-top.

1.1.7.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=1	Enable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=0	Enable ADC2 to be ready for regulation
output	PD3_o=0	Enable ADC3 (Uc) for delay calculation
output	PD4_o=0	Enable ADC4 to be ready for regulation
output	IGBT_Saturate_o=1	IGBT is in linear mode with fixed value
output	IGBT_Blocking _o=1	IGBT is in linear mode with fixed value
internal	increment Smooth_time_max counter	monitor maximum smoothing duration

1.1.7.2 Transition: Smoothing to Ramping Down

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted

Comment

Security warning

Equation

(Stop_Security=1)

1.1.7.3 Transition: Smoothing to Flat-Top

Sensitivity

Condition	Comment
Im=Iref	flat-top is detected
smoothing_timeout='1'	Maximum smoothing time is detected

Comment

Flat-top is detected or maximum smoothing time is detected

Equation

(Im=Iref) or (maximum smoothing time = '1')

1.1.8 FLAT-TOP

Flat-topping the output current pulse. Here is where regulation takes place.

1.1.8.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=1	Enable ramping up
output	Discharge_down_o=0	Disable ramping down
output	Regulation_OFF_o=0	Enable control system operation
output	PADC_PD2_o=0	Enable ADC2 for regulation
output	PD3_o=0	Enable ADC3 (Uc) for regulation
output	PD4_o=0	Enable ADC4 for regulation
output	IGBT_Saturate_o=0	IGBT is in linear mode with regulation
output	IGBT_Blocking _o=0	IGBT is in linear mode with regulation
internal	start and increment flat-top counter	monitor maximum flat-top duration

1.1.8.2 Transition: Flat-top to Free Wheeling

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted
Flat top end =’1’	flat-top duration attained

Comment

Security warning or flat-top timeout detected

Equation

(Stop_Security=1) or (Flat-top_end =’1’)

1.1.9 FREE WHEELING

Free-wheeling the magnet current with H-bridge.

1.1.9.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=1	Enable ramping up (free wheel)
output	Discharge_down_o=1	Enable ramping down (free wheel)
output	Regulation_OFF_o=0	Enable control system operation
output	PADC_PD2_o=0	Enable ADC2 for regulation
output	PD3_o=0	Enable ADC3 (Uc) for regulation
output	PD4_o=0	Enable ADC4 for regulation
output	IGBT_Saturate_o=0	IGBT is in linear mode with regulation
output	IGBT_Blocking _o=0	IGBT is in linear mode with regulation
internal	start and increment free wheeling counter	fixed time duration

1.1.9.2 Transition: Free Wheeling to Regulation End

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted
DeadTime_counter='1'	20us freewheeling achieved

Comment

Security warning or 20us freewheeling state duration achieved

Equation

(Stop_Security=1) or (DeadTime_counter ='1')

1.1.10 REGULATION END

Stop regulation and start ramping down the current.

1.1.10.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=0	Disable ramping up
output	Discharge_down_o=1	Enable ramping down
output	Regulation_OFF_o=0	Enable control system operation
output	PADC_PD2_o=0	Enable ADC2 for regulation
output	PD3_o=0	Enable ADC3 (Uc) for regulation
output	PD4_o=0	Enable ADC4 for regulation
output	IGBT_Saturate_o=0	IGBT is in linear mode with regulation
output	IGBT_Blocking _o=0	IGBT is in linear mode with regulation
internal	start and increment regulation end counter	fixed time duration

1.1.10.2 Transition: Regulation End to Ramping Down

Sensitivity

Condition	Comment
Stop_Security=1	security warning asserted
Regulation_end_counter='1'	150us regulation end achieved

Comment

Security warning or 20us 150us regulation end achieved

Equation

(Stop_Security=1) or (Regulation_end_counter ='1')

1.1.11 RAMPING DOWN

Ramping down the output current pulse.

1.1.11.1 Actions

	Action	Comment
output	Charge_o=0	Disable charging
output	Discharge_up_o=0	Disable ramping up
output	Discharge_down_o=1	Enable ramping down
output	Regulation_OFF_o=1	Disable control system operation
output	PADC_PD2_o=1	Disable ADC2
output	PD3_o=0	Disable ADC3
output	PD4_o=0	Disable ADC4
output	IGBT_Saturate_o=0	IGBT is blocked
output	IGBT_Blocking _o=1	IGBT is blocked
internal	start and increment regulation dwn counter	monitor max ramp down duration

1.1.11.2 Transition: Ramping down to Waiting

Sensitivity

Condition	Comment
ramp_dwn_counter_flag=1	ramping down is achieved

Comment
Flat-top is finished

Equation
(ramp_dwn_counter_flag=1)

1.2 DIGITAL CONTROL

This block describes the current control regulation taking place during the flat-top of the pulse as seen in figure (4). It is a digital PI current regulator following the equations:

$$E(k) = Iref(k) - Iacq(k)$$

$$512Y(k) = Mult1 \times E(k) - Mult2 \times E(k-1) + 512Y(k-1)$$

The multipliers are parameters that can be set from the gateway using the SCI communication protocol, and in the code correspond to the ports

$$Y(k) = \frac{1}{512}(Mult1 \times E(k) - Mult2 \times E(k-1) + 512Y(k-1))$$

We also have a feedforward loop with the capacitor bank voltage:

$$Y'(k) = Y(k) + 2Uc(k)$$

In the VHDL code, Uc(k) corresponds to the port-level signal VC_Measurement_i.

Furthermore, we have to calculate an initial value for the PI regulator, since we cannot initialize the equation with y(k-1)=0 as the current is not zero when the regulator starts to operate. We do this using the following equation:

$$Y(k-1) = Iref \times Init\_Cond\_Iref\_Mult\_HC/2048 + Init\_Cond\_Iref\_Offset\_HC$$

The coefficients for the equation are also set as parameter inputs to the module.

The output of the regulation block is the command of the IGBT in linear mode. This signal depends on the state machine found in the pulse control block. The control signals are:

Blocking = 0	Saturate = 0	Regulation Mode	Actuation = $Y'(k)$
Blocking = 0	Saturate = 1	Saturation Mode	Actuation = '0000'
Blocking = 1	Saturate = 0	Saturation Mode	Actuation = '3FFF'
Blocking = 1	Saturate = 1	Invalid State	Not defined

Where "Blocking" corresponds to the port input *Blocking_IGBT_i* and "Saturate" corresponds to the port *Saturate_IGBT_i*.

1.2.1 CURRENT FILTERING

In order to remove noise from the input current measurement, a second-order low-pass filter was deviced that implemets following equations:

$$R(K) = F1 * u(k) + F2 * u(k-1) + F3 * u(k-2) + \frac{1}{1024} * (F4 * Y(K-1) - F5 * Y(k-2))$$

$$Y(K) = \frac{R(K)}{1024}$$

Where *Y(K)* is the output filtered current, *u(k)* is the input current measurement, and F1 through F3 are parameter coefficients that can be set remotely from the gateway.

The code structure is based on the diagram below, which also shows the minimum requirement for the length of the vectors involved in the calculation.

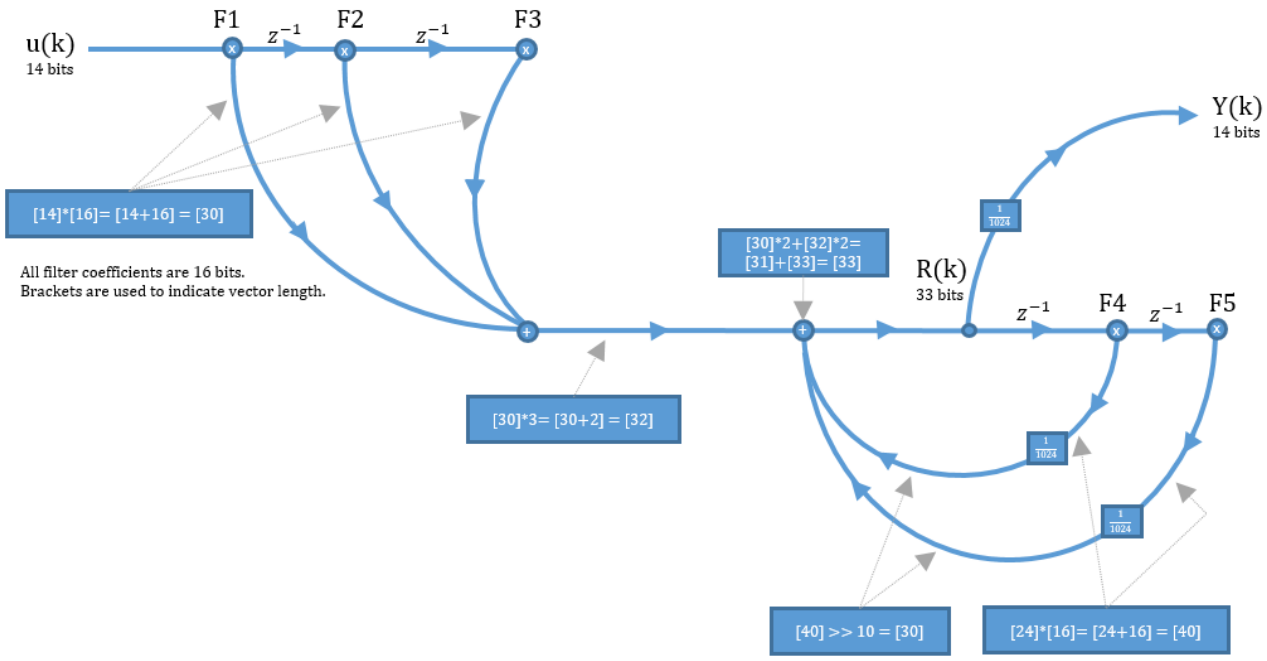


Figure 10 Filter Calculation Structure.

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