Application Report
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nFBGA Packaging

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ABSTRACT

This application report provides technical background on nFBGA packages and explains how to use them to build advanced board layouts.

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1 Introduction

The parallel pursuit of cost reduction and miniaturization in recent years has increased emphasis on very small integrated circuit (IC) package solutions. This is particularly evident in consumer-based end equipment using digital signal processor (DSP) solutions such as wireless telephones, laptop computers, and hard-disk drives. Despite the formal definition, packages with an area similar in size to the IC they encapsulate are loosely referred to as chip scale packages (CSPs). Figure 1 illustrates this trend.

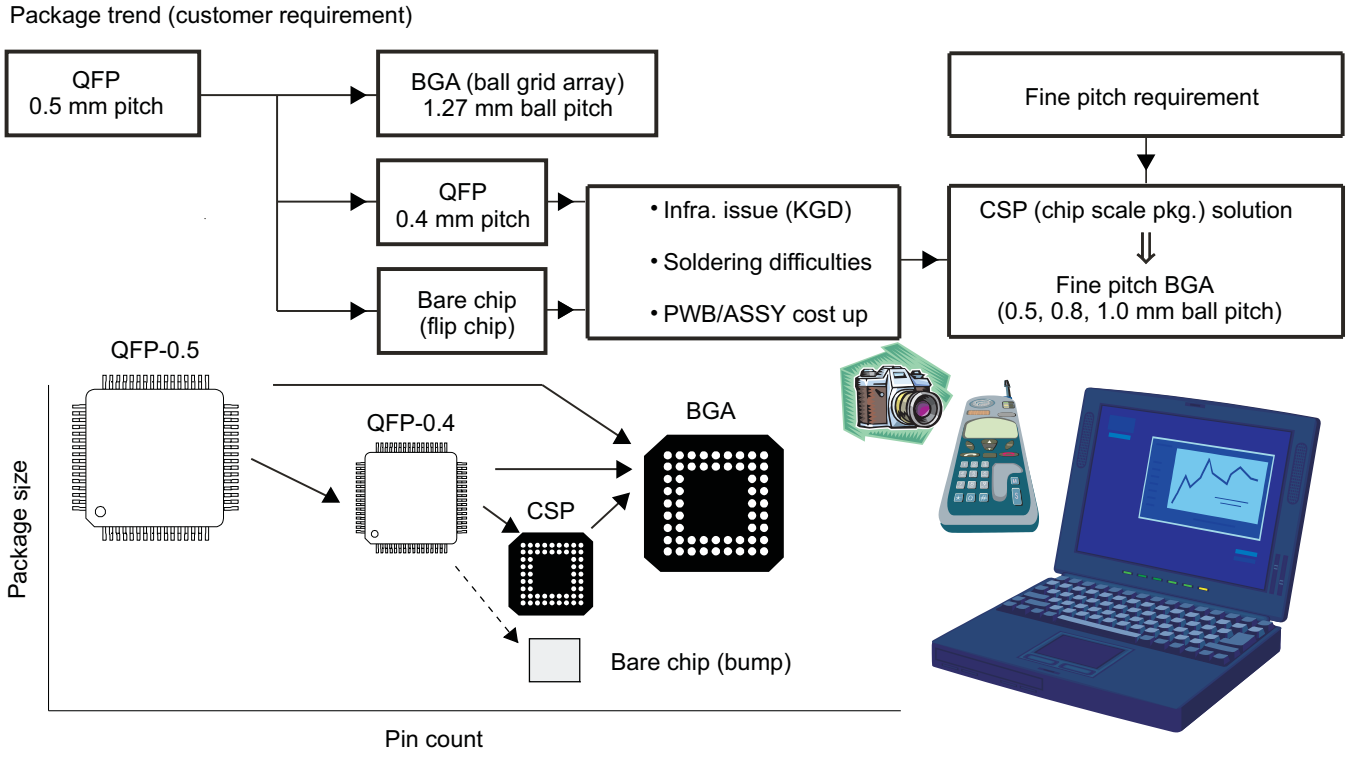


Figure 1. Packaging Trends

CSPs are in many ways an ideal solution to the cost reduction and miniaturization requirements. They offer enormous area reductions compared to quad flat packages (QFPs) and have increasing potential to do so without adding to system-level cost. In the best case, CSPs compete today on a cost-per-terminal basis with QFPs. Various CSPs from Texas Instruments (TI) are now available at cost parity with thin QFPs.

Texas Instruments produces a laminate-based family of CSPs known as New Fine Pitch Ball Grid Array packages (also referred to as nFBGA packages). Like most other CSPs, nFBGA packages use solder alloy balls as the interconnect between the package substrate and the board on which the package is soldered. The nFBGA family comes in a range of solder ball pitch, and can accommodate various stacked die configurations, with as many as three die housed in each package. Figure 2 shows the structure of TI's nFBGA package.

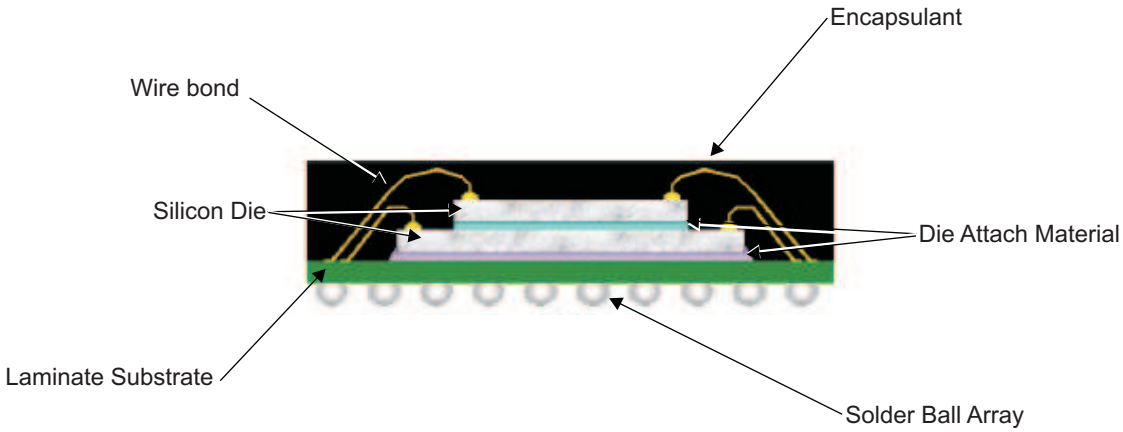


Figure 2. Structure of TI's nFBGA Package

Texas Instruments addressed several key issues in package assembly to produce a CSP that is not only physically and mechanically stable but cost-effective for a wide variety of applications. Figure 3 shows a general flow used to produce TI nFBGA packages.

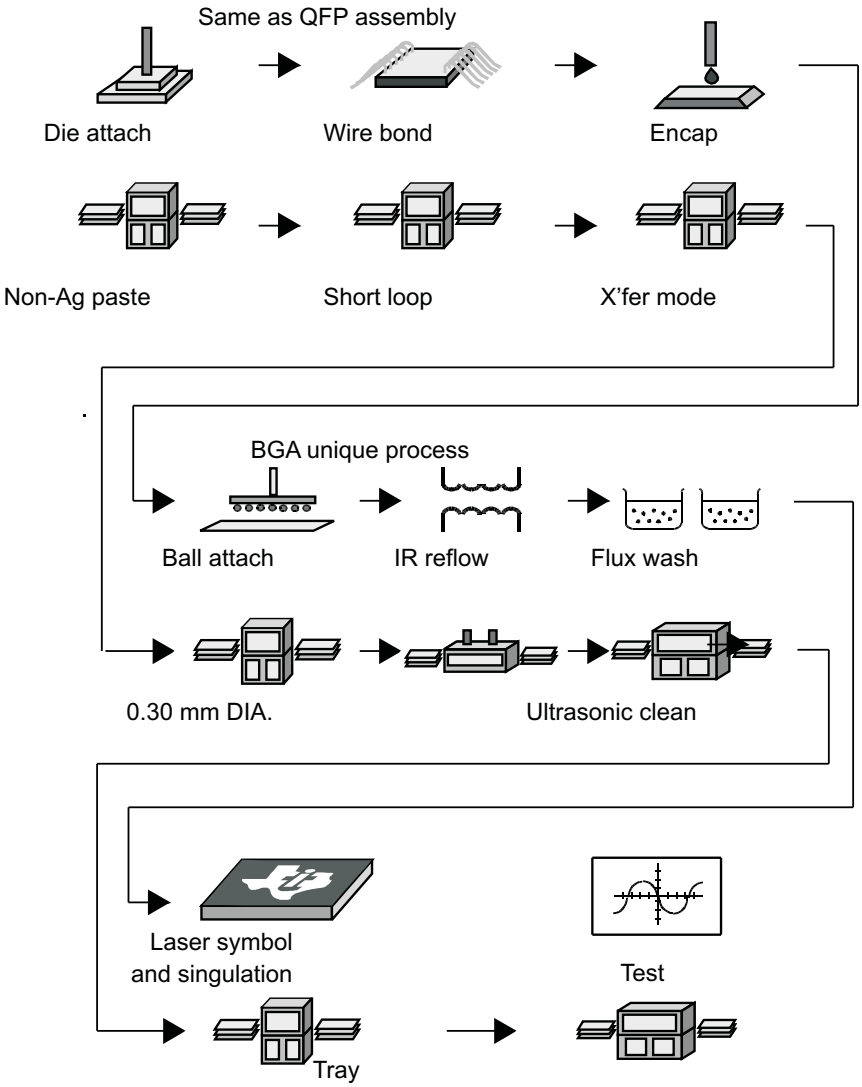


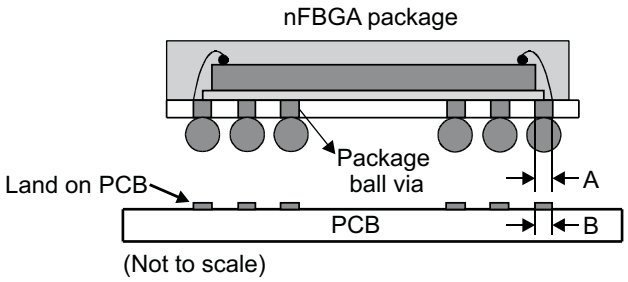
Figure 3. nFBGA Package Assembly Flow

The nFBGA package has been fully qualified in numerous applications and is being used extensively in mobile phones, laptops, modems, handheld devices, and office environment equipment. For more information on using reliable and cost-effective nFBGA packaging in your application, contact your local TI field sales office.

2 PCB Design Considerations

2.1 Solder Land Areas

Designs of both the nFBGA package itself and the printed circuit board (PCB) are important in achieving good manufacturability and optimum reliability. In particular, the diameters of the package vias and the board lands are critical. While the actual sizes of these dimensions are important, their ratio is more critical. Figure 4 illustrates the package via-to-PCB configuration and Figure 5 illustrates why this ratio is critical.



A = Via diameter on package
B = Land diameter on PCB

Ratio A/B should equal 1.0 for optimum reliability.

Figure 4. Package Via to Board Land Area Configuration

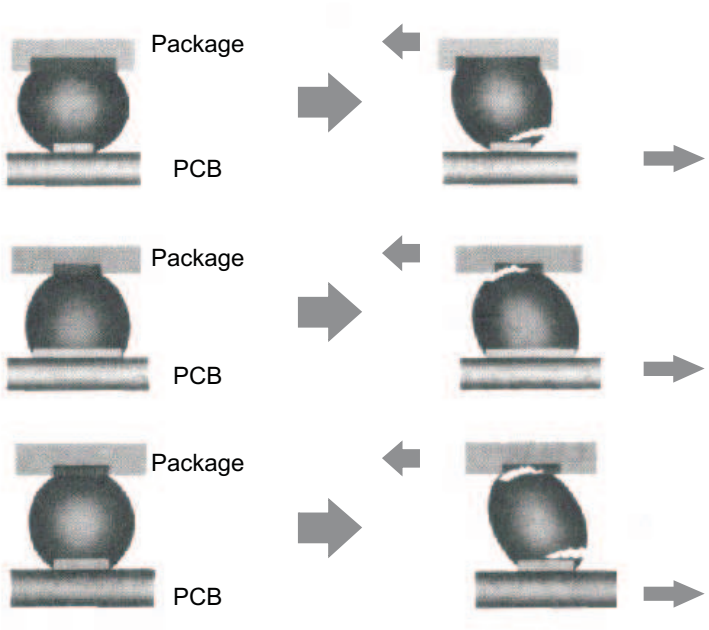


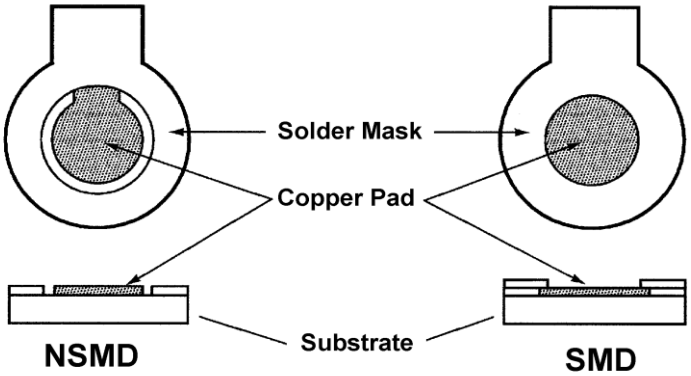
Figure 5. Effects of Via-to-Land Ratios

In the top view of Figure 5, the package via is larger than the PCB via, and the solder ball is prone to crack prematurely at the PCB interface. In the middle view, the PCB via is larger than the package via, which leads to cracks at the package surface. In the bottom view, where the ratio is almost 1:1, the stresses are equalized and neither site is more susceptible to cracking than the other.

Solder lands on the PCB are generally simple round pads. Solder lands are either solder-mask-defined or non-solder-mask-defined.

- *Solder-mask-defined (SMD) land.* With this method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Better size control is the result of photo imaging the stencils for masks. The chief disadvantage of this method is that the larger copper spot can make routing more difficult.
- *Non-solder-mask-defined (NSMD) land.* Here, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the solder mask method, the overall pattern registration is dependent on copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size.

For an example of optimum land diameters and configurations for a common nFBGA pitch, see Table 1.



A  It is not recommended to use "U" shape PCB land because of trapping void during reflow.

Figure 6. Optimum Land Configurations

Table 1. Optimum Land Configurations

All Measurements in mm		Ball Size, SMO, Pad Size and Apertures are Shown in Diameters				
		PCB Design		Stencil Design		
Ball Pitch	Solder Mask Type	SMO	Pad Size	Thickness	Aperture	Area Aspect Ratio
0.4	SMD	0.225	0.300	0.076	0.250	0.82
	NSMD	0.300	0.225			
0.5	SMD	0.300	0.400	0.100	0.300	0.75
	NSMD	0.400	0.300			
0.65	SMD	0.350	0.450	0.127	0.350	0.69
	NSMD	0.450	0.350			
0.8	SMD	0.400	0.500	0.152	0.400	0.66
	NSMD	0.500	0.400			
1	SMD	0.450	0.550	0.152	0.450	0.74
	NSMD	0.550	0.450			

- Area Ratio = Area of Aperture / Area of Aperture Wall
- For optimal release of solder paste, Area Ratio ≥ 0.66 is recommended.

2.2 Conductor Width/Spacing

Figure 7 presents some design considerations based on commonly used PCB design rules. Conventionally, the pads are connected by wide copper traces to other devices or to plated through holes (PTH). As a rule, the mounting pads must be isolated from the PTH. Placing the PTH interstitially to the land pads often achieves this.

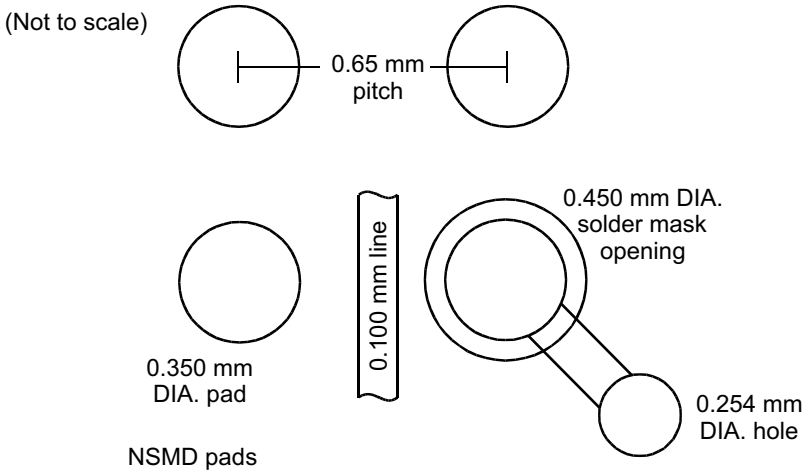


Figure 7. PCB Design Considerations (Conventional)

2.3 High-Density Routing Techniques

A challenge when designing with CSP packages is that as available space contracts, the space available for signal fanout also decreases. Routing of nFBGA packages can be especially challenging because of the tight ball pitch and a full array of solder balls that most packages have. By using a few high-density routing techniques, the PCB designer can minimize many of these design and manufacturing challenges.

2.4 Via Density

Via density, as mentioned earlier, can be a limiting factor when designing high-density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia, shown in Figure 8, has solved many of the problems associated with via density.

Figure 8. Microvia Structure

Microvias are often created using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4-mil-thick dielectric layer, creating the 4 µm microvia shown in Figure 8. The layout designer can now route to the first internal board layer. Two layers (each 4 mils thick) can be laser-drilled, creating a 200 µm microvia diameter. In this case, routing to the first two internal layers is possible.

2.5 Conventional PCB Design

The relatively large via density on the package periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce or eliminate the via density problem on the periphery of the package, designers can build the PCB vertically from the BGA pad through the internal layers of the board, as shown in Figure 9. By working vertically and mechanically drilling 250 µm vias between the pads on the board and the internal layers, designers can create a “pick-and-choose” method. They can pick the layer and choose the route. A “dog bone” method is used to connect the through-hole via and the pad. This reduces the risk of trapped voids that can reduce the board mount process margin.

This method requires a very small mechanical drill to create the necessary number of vias for one package. Although this method is the least expensive, a disadvantage is that the vias go through the board, creating a matrix of vias on the bottom side of the board, which may limit the use of using the back side for routing.

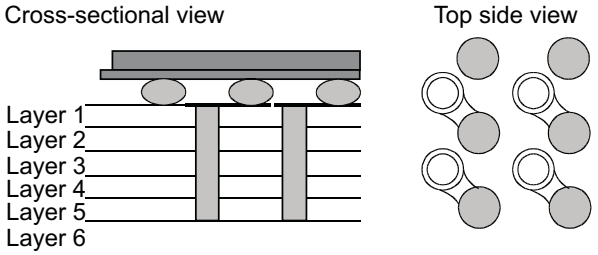


Figure 9. "Dog Bone" Via Structure

2.6 Advanced Design Methods

Another option is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers. Buried vias usually connect only the inner layers. Figure 10 illustrates this method using 4-mil laser-drilled microvias in the center of the pads and burying the dog bone on layer 2.

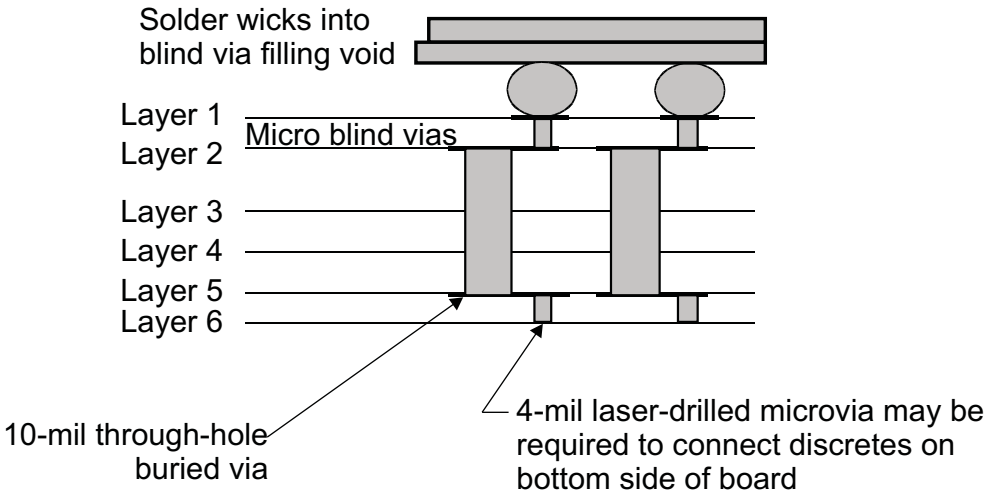


Figure 10. Buried Vias

Since the buried via does not extend through the underside of the board, the designer can use another set of laser-drilled blind microvias, if needed, to connect the bypass capacitors and other discrete components to the bottom side.

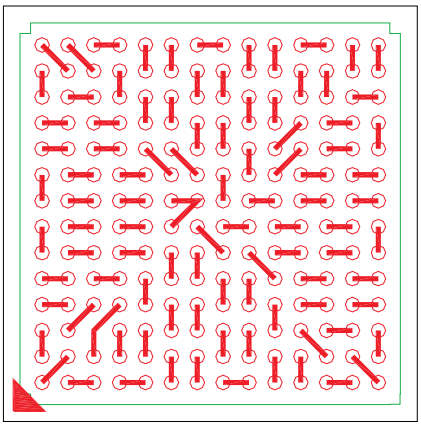
More information on these advanced techniques is available by contacting your local TI field sales office.

3 Reliability

3.1 Daisy-Chained Units

Daisy-chained units are used to gain experience in the handling and mounting of CSPs for board-reliability testing, to check PCB electrical layouts, and to confirm the accuracy of the mounting equipment. To facilitate this, Texas Instruments offers daisy-chained units in all production nFBGA packages.

Each daisy-chained pinout differs slightly depending on package layout. An example is shown in Figure 11. Daisy-chained packages are wired to provide a continuous path through the package for easy testing. TI issues a net list for each package, which correlates each ball position with a corresponding wire pad number. Examples of package net lists for production packages are included in Appendix B.



BALL No.	BALL No.	BALL No.
A1	B2	
B1	C1	
C2	D4	
D2	D3	
D1	E1	
E2	E3	
E4	E5	
F5	F6	
F3	F4	
F1	F2	
G1	G2	
G3	G4	
G5	G6	
G7	H6	
H4	H5	
H2	H3	
H1	J1	
J2	J3	
J4	J5	
K3	K4	
K1	K2	
L1	L2	
L3	M2	
M1	N1	
N2	P1	

BALL No.	BALL No.	BALL No.
P2	P3	
M3	N3	
L4	M4	
N4	P4	
N5	P5	
L5	M5	
J6	K5	
K6	L6	
M6	N6	
P6	P7	
M7	N7	
K7	L7	
H7	J7	
J8	K8	
L8	M8	
N8	P8	
N9	P9	
L9	M9	
K9	L10	
M10	N10	
P10	P11	
M11	N11	
N12	P12	
P13	P14	
N13	N14	

BALL No.	BALL No.	BALL No.
M12	M13	
L14	M14	
L12	L13	
K10	L11	
K11	K12	
K13	K14	
J13	J14	
J11	J12	
J10	J9	
H8	H9	
H10	H11	
H12	H13	
G14	H14	
G12	G13	
G10	G11	
F10	G9	
F11	F12	
F13	F14	
E13	E14	
E11	E12	
D12	D13	
C14	D14	
B14	C13	
A14	B13	
A12	A13	

BALL No.	BALL No.	BALL No.
B12	C12	
C11	D11	
A11	B11	
A10	B10	
C10	D10	
E10	F9	
D9	E9	
B9	C9	
A8	A9	
B8	C8	
D8	E8	
F7	F8	G8
D7	E7	
B7	C7	
A6	A7	
B6	C6	
D6	E6	
C5	D5	
A5	B5	
A4	B4	
B3	C4	
A2	A3	

Figure 11. Daisy-Chained Pinout List (195ZWV nFBGA Package)

Figure 12 shows a PCB layout for an 80 GQE daisy-chained package. When a daisy-chained package is assembled on the PCB, a complete circuit is formed, which allows continuity testing. The circuit includes the solder balls, the metal pattern on the die, the bond wires, and the PCB traces. The entire package or only a quadrant can be interconnected and tested. A diagram of the test configuration is shown in Figure 13.

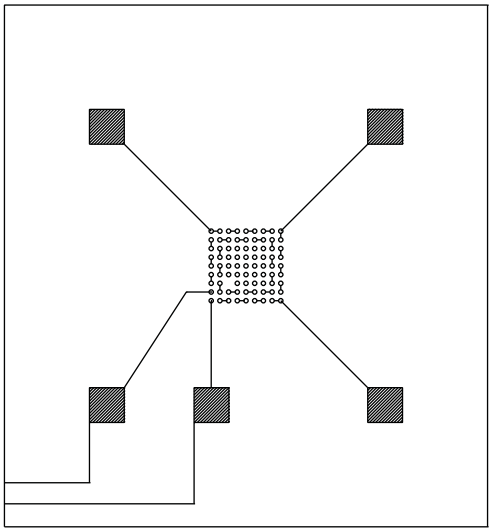


Figure 12. PCB Layout for Daisy-Chained Unit

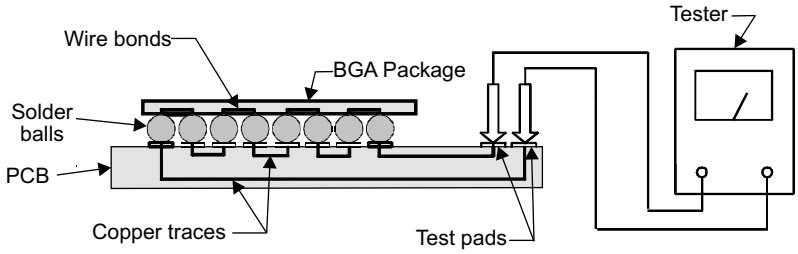


Figure 13. Daisy-Chain Test Configuration

Reliability is one of the first questions designers ask about any new packaging technology. They want to know how well the package will survive handling and assembly operation, and how long it will last on the board. The elements of package reliability and system reliability, while related, focus on different material properties and characteristics and are tested by different methods.

Package reliability focuses on materials of construction, thermal flows, material adherence/delamination issues, resistance to high temperatures, moisture resistance and ball/stitch bond reliability. Thorough engineering of the package is performed to prevent delamination caused by the interaction of the substrate material and the mold compound.

TI subjects each nFBGA to rigorous qualification testing before the package is released to production. These tests are summarized in Table 2. All samples used in these tests are preconditioned according to guidelines of the Joint Electronic Device Committee (JEDEC) A113 at various levels. Typical data is presented in Table 3. The nFBGA packages have proven robust and reliable.

Table 2. Package-Level Reliability Tests

Test Environments	Conditions	Read Points
HAST	85RH/85°C	600 hrs., 1000 hrs.
Temp. Cycle	-55/125°C	500 cycles, 750 cycles, 1000 cycles
Thermal Shock	-55/125°C	200 cycles, 500 cycles, 750 cycles, 1000 cycles
HTOL	125°C, Op. voltage	500 hrs., 600 hrs., 1000 hrs.
HTOL(1)	140°C, Op. voltage	500 hrs.
HTOL(1)	140°C, Op. voltage	500 hrs.
Bake(1)	150°C, 170°C	600 hrs., 1000 hrs., 420 hrs.
HAST(1)	170°C	96 hrs.

(1) Optional tests. One or more of them may be added to meet customer requirements.

Table 3. Package-Level Reliability Test Results

		Package Types		
	Leads	113ZVD	289ZVL	289ZWE
	Body (mm)	8x8	12x12	13x13
	Die (mm)	4.2 × 4.2	5.8 × 5.7	10.6 × 8.2 (Die 1) 8.1 × 7.7 (Die 2)
	Level	3	3	3
Test Environment				
T/C, -55/125°C	(500 cycles) (1000 cycles)	0/78 0/78	0/83 0/83	0/246 0/245
T/S, -55/125°C	(500 cycles) (1000 cycles)		0/77 0/77	0/77 0/77
HAST, 85°C/85%RH	(600 cycles) (1000 cycles)	0/78 0/78	0/78 0/78	0/77 0/77
150°C Storage	(600 cycles) (1000 cycles)	0/45 0/45	0/77 0/77	0/77 0/77
HTOL	(1000 hrs.)	0/120		

Board-level reliability (BLR) issues generally focus on the complex interaction of various materials under the influence of heat generated by the operation of electronic devices. Not only is there a complex thermal situation caused by multiple heat sources, but there are cyclical strains due to expansion mismatches, warping and transient conditions, non-linear material properties, and solder fatigue behavior influenced by geometry, metallurgy, stress relaxation phenomenon, and cycle conditions. In addition to material issues, board and package design can influence reliability. Thermal management from a system level is critical for optimum reliability, and thermal cycling tests are generally used to predict behavior and reliability. Many of these are used in conjunction with solder fatigue life models using a modified Coffin-Manson strain range-fatigue life plots (number of cycles to failure has an inverse exponential relationship with the thermal cycle temperature range).

In addition to device/package testing, board-level reliability testing has been extensively performed on the nFBGA packages. Various types of daisy-chained packages were assembled to special boards, with electrical measurements made in the initial state and then at intervals after temperature cycles were run. Table 4 shows a summary of a wide range of board-level reliability.

Table 4. Board-Level Reliability Summary

Conditions (With Solder Paste)						Failures/Sample Size						
						Requirements			Extended Range			
Package	TI Mfg Site	Body	Pitch	Die	Temp.	500	800	1000	1500	2000	2500	3000
	Test Site	(mm)	(mm)	(mm)	Cycle (°C)	(Cycles)			(Cycles)			
ZVD 113 balls	TI Hiji	8×8	0.65	5x5	-40/125	0/36	0/36	0/36	0/36	0/36	0/36	0/36
ZVD 113 balls	TI Hiji	8×8	0.65	4.2x4.2	-40/125	0/48	0/48	0/48	0/48	0/48	0/48	4/43
ZVD 289 balls	TI Hiji	12×12	0.50	9x9	-40/125	0/95	0/95	0/95	0/95	0/95	0/94	0/94
ZVD 289 balls	TI Hiji	12×12	0.50	6.5x6.5	-40/125	0/36	0/36	0/36	0/36	0/36	0/36	1/36

Table 5 summarizes conclusions from the testing. Two important conclusions are that the PCB pad size needs to match the via size, and that solder paste is needed for attachment to give optimal reliability.

Table 5. Summary of Significant BLR Improvements

Condition	Improved BLR →		
Die size	Larger	→	Smaller
Die edge	Over balls	→	Within ball matrix
Ball count	Smaller	→	Larger
Ball size	Smaller	→	Larger
PCB pad size	Over/undersized	→	Matches package via (for NSMD ~90% of via)
Solder paste	None or insufficient	→	Thickness 0.10 nom. (type matches reflow)

3.2 Reliability Calculations

Another important aspect of predicting how a package will perform in any given application is reliability modeling. Thermal, electrical, and thermomechanical modeling, verified by experimental results, provide insight into system behavior, shorten package development time, predict system lifetimes, and provide an important analytical tool. In applications such as BGAs, where the interconnections are made through solder balls, the useful life of the package is, in most cases, dependent on the useful life of the solder itself. This is an area that has been studied extensively, and very accurate models for predicting both solder behavior and interpreting accelerated life testing exist.

The current methodology employed at Texas Instruments includes both extensive model refinement and constant experimental verification. For a given package, a detailed 2D finite element model (FEM) is constructed. This model is used to carry out 2D plain strain elastoplastic analysis to predict areas of high stress. These models also account for the thermal variation of material properties, such as modulus of elasticity, coefficient of thermal expansion, and Poisson's Ratio as a function of temperature. These allow the FEM to calculate the thermomechanical plastic strains in the solder joints for a given thermal loading.

The combination of finite element analysis (FEA), accurate thermal property information, and advanced statistical methods allows prediction of the number of cycles to failure for various probability levels. Using the assumption that cyclic fatigue lifetime follows a Weibull distribution, various probability levels can be calculated. For these calculations, the Weibull shape parameter used is $\beta = 4$, which is based on experimental data calibration. It is also consistent with available experimental data found in the literature for leadless packages. This then results in the following equation: $Nf(\times\%) = Nf(50\%)[\ln(1-0.01\times)/\ln(0.5)]1/\beta$.

Using this equation, and using the plastic strain ξp in combination with the S–N curves, the data below is an example of the accuracy possible with this method:

Sample Finite Element Simulation and Life Prediction:

144 GGU @ T/C: -40/125°C

{Model}→ ξp = 0.353% on the outmost joint → Nf(50%)= 4434 cycles

→ Nf(1%) = 1539 cycles

{BLR Testing}→ -40/125°C (10 min/10 min)

→ Nf(1%) = 1657 cycles

Modeling is most useful in exploring changes in materials, designs, and process parameters without the need to build experimental units. For example, modeling was used to study the effects of changes in board thickness and pad size. Table 6 shows the simulated effects of pad size and board thickness on the fatigue life of a 144-GGU package.

Table 6. Effects of Pad Size and Board Thickness on Fatigue Life

Example1: Effects of pad size on fatigue life • Package: 144 GGU • Die: 8.8 x 8.8 x 0.279 mm • Board: FR-4 board 52 mils thick	**Pad Dia. (mils)**	**Pad Standoff (mm)**	**Solder Center Dia. (mm)**	**Plastic Strain (%)**	**Nf (1%) (cycles to failure)**	**Difference**
	12	0.3847	0.4908	0.4400	998	0.88x
	13	0.3689	0.4951	0.4127	1134	1
	14	0.3523	0.5005	0.3908	1263	1.11x
	15	0.3350	0.5060	0.3741	1377	1.21x
Example 2: Effects of board thickness on fatigue life • Package: 144 GGU • Die: 8.8 x 8.8 x 0.279 mm • Board: FR-4 • Pad Size: 13 mils	**Board Thickness (mils)**	**Plastic Strain (%)**	**Nf (1%) (cycles to failure)**	**Difference**		
	50	0.4095	1152	1		
	31	0.4095	1249	1.08x		

3.3 Package Characteristics

Texas Instruments has extensive package characterization capabilities, including an electrical measurements lab with TDR/LRC (Time Domain Reflectometer/inductance resistance capacitance) and network analysis capabilities, a thermal measurements lab with JEDEC standard test conditions up to 1000 watts, and extensive electrical, thermal, and mechanical modeling capability. Modeling was implemented at TI starting in 1984. Stress analysis is done with the Ansys Analysis tool, which provides full linear, nonlinear, 2D and 3D capabilities for solder reliability, package warpage, and stress analysis studies. An internally developed tool (PACED™) is used for electrical modeling that gives 2.5D and full 3D capability for LRC models, transmission lines, lossy dielectrics, and SPICE deck outputs. The thermal modeling tool was also internally developed (ThermCAL™) and it provides full 3D automatic mesh generation for most packages.

Complex geometries, transient analysis, and anisotropic materials can be modeled with it. With these capabilities, a full range of modeling from device level through system level can be provided. Package modeling is used to predict package performance at the design stage, to provide a package development tool, to aid qualification by similarity, and as a failure analysis tool.

3.4 Thermal Modeling

Figure 14 outlines the thermal modeling process. Thermal modeling data for sample nFBGA packages can be found in Appendix C.

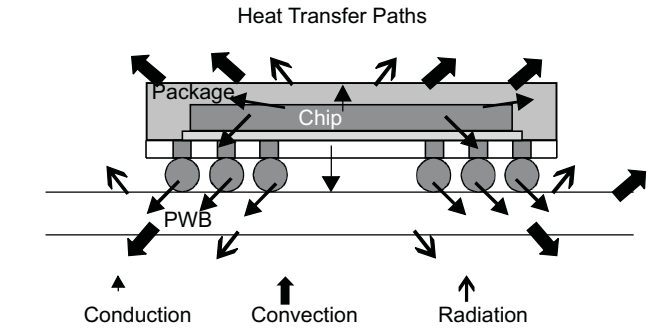


Figure 14. Thermal Modeling Process

4 Surface-Mounting nFBGA Packages

Surface-mount technology (SMT) has evolved over the past decade from an art into a science with the development of design guidelines and rules. While these guidelines are specific enough to incorporate many shared conclusions, they are general enough to allow flexibility in board layouts, solder pastes, stencils, fixturing, and reflow profiles. From experience, most assembly operations have found nFBGA packages to be robust, manufacturing-friendly packages that fit easily within existing processes and profiles. In addition, they do not require special handling. However, as ball pitch becomes smaller, layout methodology and placement accuracy become more critical. Below is a review of the more important aspects of surface-mounted CSPs. The suggestions provided may aid in efficient, cost-effective production.

4.1 Design for Manufacturability (DFM)

A well-designed board that follows the basic surface-mount technology considerations greatly improves the cost, cycle time, and quality of the end product. Board designers should comprehend the SMT-automated equipment used for assembly, including minimum and maximum dimensional limits and placement accuracy. Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. While odd-shaped or small boards can be assembled, they require panelization or special tooling to process in-line. The more irregular the board — non-rectangular with no cutouts — the more expensive the assembly cost.

Fiducials (the optical alignment targets that align the module to the automated equipment) should allow vision-assisted equipment to accommodate the shrink and stretch of the raw board during processing. They also define the coordinate system for all automated equipment, such as printing and pick-and-place.

The following guidelines may be helpful:

- Automated equipment requires a minimum of two and preferably three fiducials.
- A wide range of fiducial shapes and sizes can be used. Among the most useful is a circle 1.6 mm in diameter with an annulus of 3.175/3.71 mm. The outer ring is optional, but no other feature may be within 0.76 mm of the fiducial.
- The most useful placement for the fiducials is an L configuration, which is orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0,0).
- All components should be within 101.6 mm of a fiducial to assure placement accuracy. For large boards or panels, a fourth fiducial should be added.

If the edges of the boards are to be used for conveyer transfer, a cleared zone of at least 3.17 mm should be allowed. Normally, the longest edges of the board are used for this purpose, and the actual width is dependent on equipment capability. While no component lands or fiducials can be in this area, breakaway tabs may be.

Interpackage spacing is a key aspect of DFM, and the question of how close you can safely put components to each other is a critical one. The following component layout considerations are recommendations based on TI experience:

- There should be a minimum of 0.508 mm between land areas of adjacent components to reduce the risk of shorting.
- The recommended minimum spacing between SMD discrete component bodies is equal to the height of the tallest component. This allows for a 45° soldering angle in case manual work is needed.
- Polarization symbols need to be provided for discrete SMDs (diodes, capacitors, and so forth.) next to the positive pin.
- Pin-1 indicators or features are necessary to determine the keying of SMD components.
- Space between lands (under components) on the backside discrete components should be a minimum of 0.33 mm. No open vias may be in this space.
- The direction of backside discretes for wave solder should be perpendicular to the direction through the wave.
- Do not put SMT components on the bottom side that exceed 200 grams per square inch of contact area with the board.
- If space permits, symbolize all reference designators within the land pattern of the respective components.
- It is preferable to have all components oriented in well-ordered columns and rows.
- Group similar components together whenever possible.
- Room for testing must be allowed.

4.2 Solder Paste

TI recommends the use of paste when mounting nFBGAs. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- It helps compensate for minor variations in the planarity of the solder balls.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted component. Most assembly operations have found that no changes in existing pastes are required by the addition of nFBGA, but due to the large variety of board designs and tolerances, it is not possible to say this will be true for any specific application.

Nearly as critical as paste selection is stencil design. A proactive approach to stencil design can pay large dividends in assembly yields and lower costs. In general, nFBGA packages are special cases of BGA packages, and the general design guidelines for BGA package assembly applies to them as well. There are some excellent papers on BGA assembly, so only a brief overview of issues especially important to nFBGA packages is presented here.

The typical stencil hole diameter should be the same size as the land area, and 100-120-µm-thick stencils have been found to give the best results. Good release and a consistent amount of solder paste and shapes are critical, especially as ball pitches decrease. The use of metal squeegee blades, or at the very least, high durometer polyblades, is important in achieving this. Paste viscosity and consistency during screening are some variables that require close control.

4.3 Solder Ball Collapse

To produce the optimum solder joint, it is important to understand the amount of collapse of the solder balls, and the overall shape of the joint. These are a function of:

- The diameter of the package solder ball via.
- The volume and type of paste screened onto the PCB.
- The diameter of the PCB land.
- The board assembly reflow conditions.
- The weight of the package.

The original ball height on the package for a typical 0.5-mm-pitch package is 0.20 mm. After the package is mounted, this typically drops to 0.15 mm, as illustrated in Figure 15.

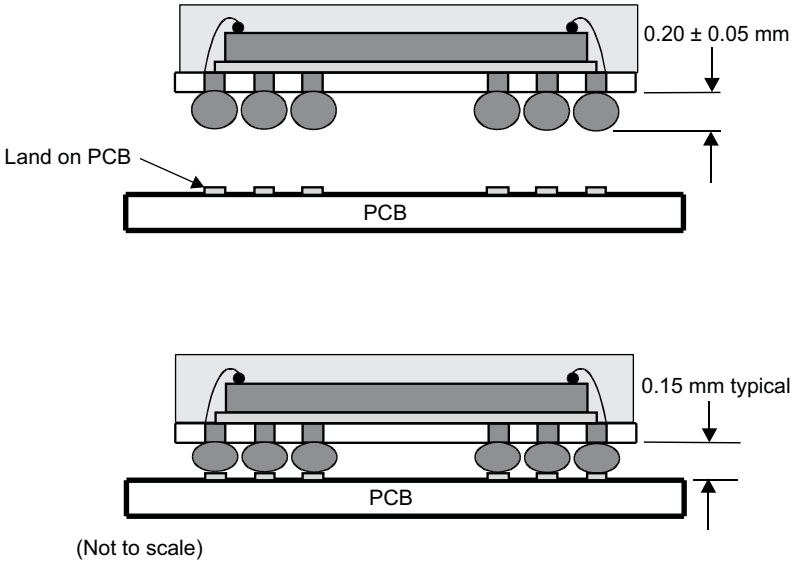


Figure 15. Solder Ball Collapse

Controlling the collapse, and thus defining the package standoff, is critical to obtaining the optimum joint reliability. Generally, a larger standoff gives better solder joint fatigue strength, but this should not be achieved by reducing the board land diameter. Reducing the land diameter will increase the standoff, but will also reduce the minimum cross-section area of the joint. This, in turn, will increase the maximum shear force at the PCB side of the solder joint. Therefore, a reduction of land diameter will normally result in a worse fatigue life, and should be avoided unless all the consequences are well understood.

4.4 Reflow

Solder reflow conditions are the next critical step in the mounting process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the surfaces takes place by wicking of molten solder, the solder balls collapse, and finally solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with small or no voids and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven joint thickness, discontinuities, and insufficient fillet can occur. While the exact cycle used depends on the reflow system and paste composition, there are several key points all successful cycles have in common.

The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat or a bake, or, more commonly, a hold in the cycle at evaporation temperatures. If there is less solvent in the paste (such as in a high-viscosity, high-metal-content paste), then the hold can be shorter. However, when the hold is not long enough to get all of the solvent out or too fast to allow it to evaporate, many negative things happen. These range from solder-particle splatter to trapped gases, which can cause voids and embrittlement. A significant number of reliability problems with solder joints can be solved with the warm-up step, so it needs careful attention.

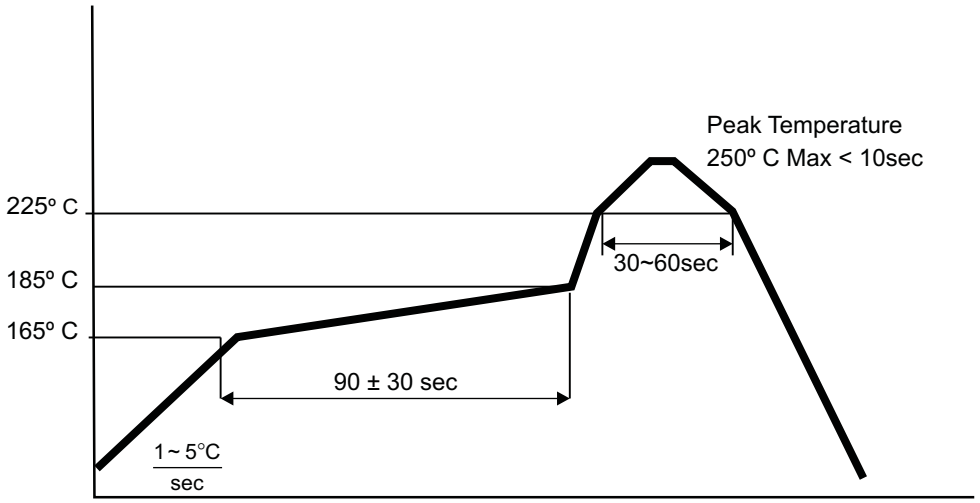
The second key point that successful reflow cycles have in common is uniform heating across the package and the board. Uneven solder thickness and non-uniform solder joints may be an indicator that the profile needs adjustment. There can also be a problem when different sized components are reflowed at the same time. Care needs to be taken when profiling an oven to be sure that the indicated temperatures are representative of what the most difficult to reflow parts are seeing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow, than with others, such as forced hot-air convection.

Finally, successful reflow cycles strike a balance among temperature, timing, and length of cycle. Mistiming may lead to excessive fluxing activation, oxidation, excessive voiding, or even damage to the package. Heating the paste too hot, too quickly before it melts can also dry the paste, which leads to poor wetting. Process development is needed to optimize reflow profiles for each solder paste/flux combination.

The profile shown in Figure 16 is an ideal one for use on a Pb-Free nFBGA package in a forced-air-convection furnace, which is the most highly recommended type. The best results have been found in a nitrogen atmosphere. The corresponding optimal reflow profile for an nFBGA package exhibiting eutectic SnPb solder balls is shown in Figure 17.

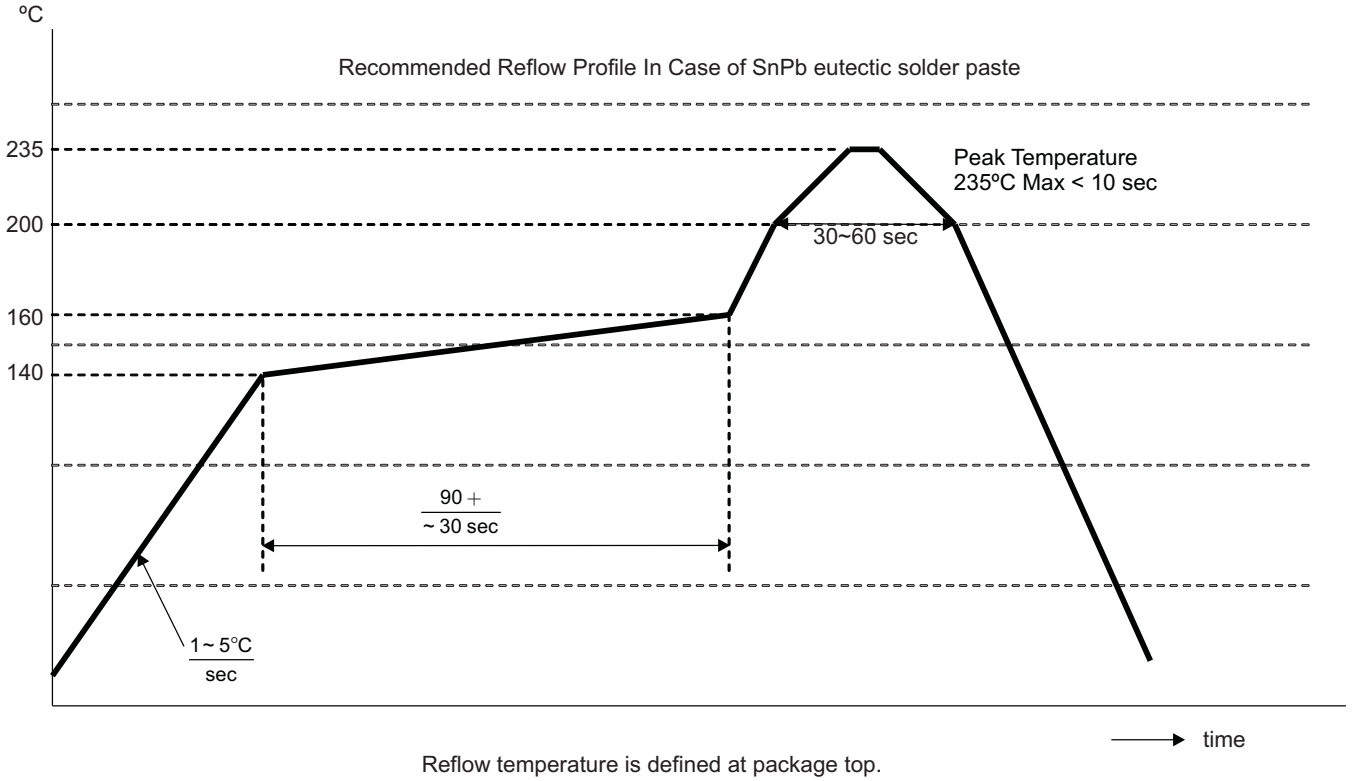
The guidelines upon which these profiles are based are general. Modification to the ideal reflow profile will be driven by the interplay of solder-paste particle size and flux percentage with process variables such as heating rates, peak temperatures, board construction factors, and atmosphere. These modifications are dependent on specific applications.

It should be noted that while they are more rugged than most CSP-type packages, many nFBGA packages are still slightly moisture-sensitive at the time of publishing this application report. The time out of a dry environment should be controlled according to the label on the packing material. This will prevent moisture absorption problems with the package such as “popcorning,” or delamination.



RT to 150 ± 10C	1~5°C / sec
175 ± 10C	90 ± 30 sec
225°C	30 ~ 60 sec
245 ~ 250°C peek	10 sec

Figure 16. Recommended Reflow Profile of Pb-Free nFBGA Package



Reflow temperature is defined at package top.

Figure 17. Recommended Reflow Profile of Eutectic SnPb nFBGA Package

Other concerns with BGA packages are those caused by a PCB bowing or twisting during reflow. As PCBs get thinner, these problems will become more significant. Potential problems from these effects will show up as open pins, hourglass solder joints, or solder discontinuities. Proper support of the PCB through the furnace, balancing the tab attachments to a panel, and, in worst cases, using a weight to stiffen the PCB can help prevent this. In general, the small size of CSPs create fewer problems than standard BGAs. It is also true that BGAs generally have fewer problems than leaded components.

4.5 Inspection

The nFBGA packages have been designed to be consistent with very high-yield assembly processes. Because of their relatively light weight, nFBGA packages tend to self-align during reflow. Since the pitch of the ball pattern is large compared to that of fine-pitch leaded packages, solder bridging is rarely encountered. It is recommended that a high-quality solder joint assembly process be developed using the various inspection and analytical techniques, such as cross-sectioning. Once a quality process has been developed, detailed inspection should not be necessary. Visual methods, while obviously limited, can offer valuable clues to the general stability of the process. Electrical checks can confirm interconnection. Both transmission X-rays and laminographic X-rays have proven to be useful nondestructive tools, if desired.

5 Packing and Shipping

The nFBGA packages are shipped in either of two packing methods:

- Trays
- Tape and Reel

5.1 Tray Packing Method

Thermally resistant plastic trays are one of two methods currently used to ship these packages. Each family of pats with the same package outline has its own individually designed tray. The trays are designed to be used with pick-and-place machines. Figure 18 gives typical tray details, and Table 7 shows the number of units per tray.

The steps following Table 7 illustrate the packing method used to ship trays. Before the trays are sealed in the aluminum lined plastic bag, they are baked in accordance with the requirements for dry-packing at the appropriate level.

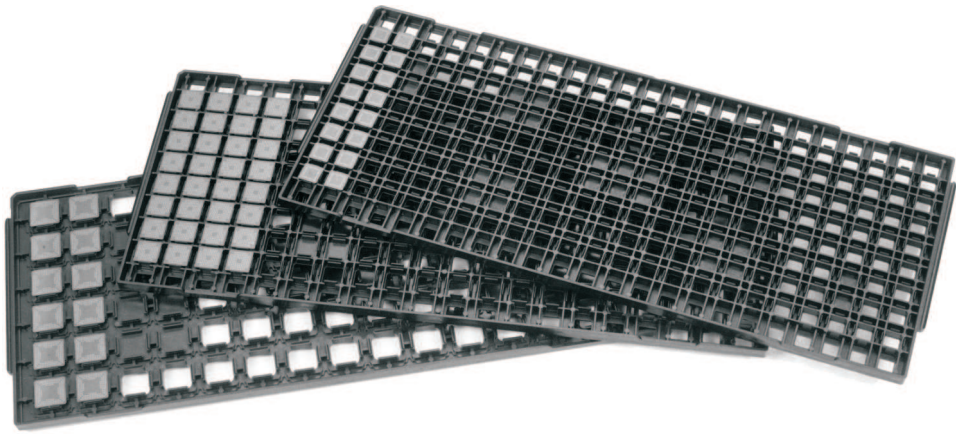
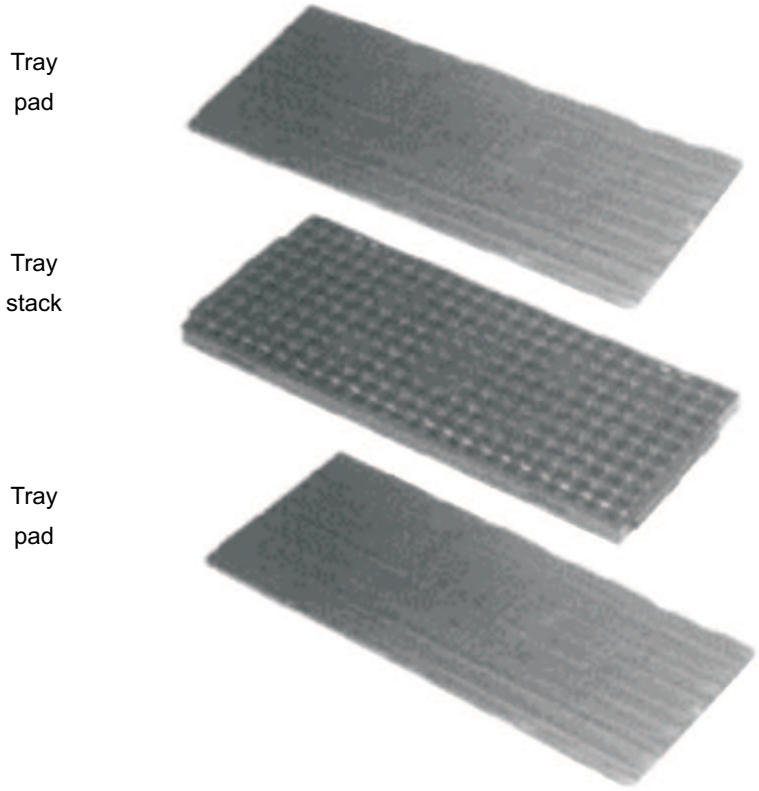


Figure 18. Shipping Tray Detail

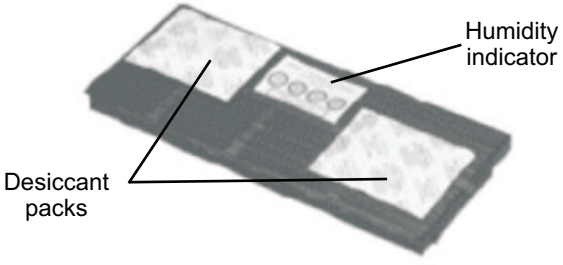
Table 7. Number of Units per Shipping Tray

Body Size (mm)	Matrix	Units/Tray	Units/Box
8 × 8	10 × 26	260	2600
10 × 10	8 × 23	184	1840
10 × 10	8 × 21	168	1680
13 × 13	8 × 20	160	1600
7 × 17	7 × 18	126	1260
14 × 14	7 × 17	126	1190
16 × 16	6 v 15	126	900

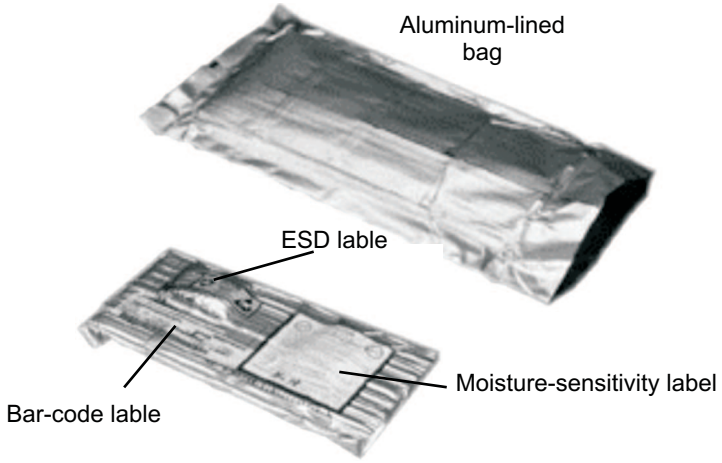
1. Arrange the stack of trays to be packed with a tray pad on the top and bottom.



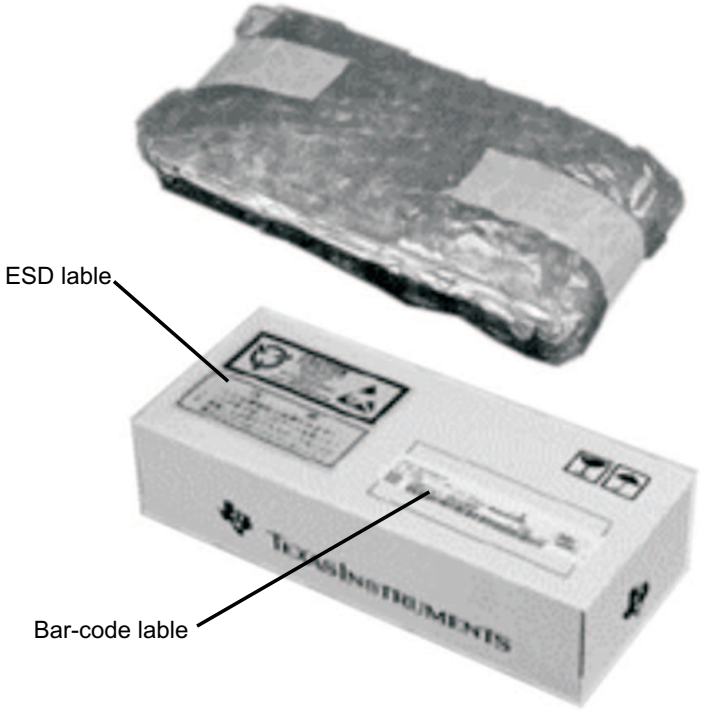
2. Strap the tray stack and pads together with four straps—three crosswise and one lengthwise. Then, place the desiccants and the humidity indicator on top.



3. Place the lot inside the aluminum-lined bag and vacuum-seal it. Place the necessary labels on the sealed bag

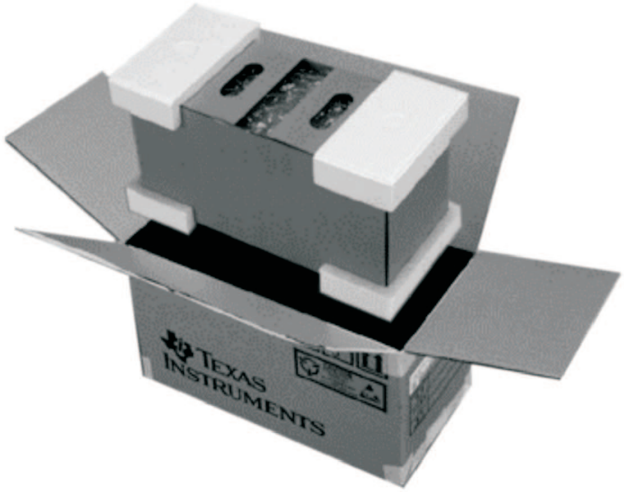


4. Wrap and tap bubble pack around the bag for a snug fit in the inner carton. Place the necessary labels on the inner carton.



5. Add bubble pack around the inner carton for a snug fit in the skidboard liner.

6. Place four foam corner spacers on the folded skidboard liner before placing it in the outer carton. An enhanced skidboard liner, which eliminates the need for foam spacers, may be used. Seal outer carton and apply necessary labels.



5.2 Tape-and-Reel Packing Method

The embossed tape-and-reel method is generally preferred by automatic pick-and-place machines, although trays remain an option for those customers who prefer them for nFBGA packages. The tape is made from an antistatic/conductive material. The cover tape, which peels back during use, is heat-sealed to the carrier tape to keep the devices in their cavities during shipping and handling. The tape-and-reel packaging used by Texas Instruments is in full compliance with EIA Standard 481-A, "*Taping of Surface-Mount Components for Automatic Placement*." The static-inhibiting materials used in the carrier-tape manufacturing provide device protection from static damage, while the rigid, dust-free polystyrene reels provide mechanical protection and clean-room compatibility with dereeling equipment currently available on most high-speed automated placement systems.

5.3 Tape Format

Typical tape format is shown in Figure 21. The variables used in Figure 19 and Table 8 are defined as follows: W is the tape width; P is the pocket pitch; A_0 is the pocket width; B_0 is the pocket length; K_0 is the pocket depth; K is the maximum tape depth; and F is the distance between the drive hole and the centerline of the pocket.

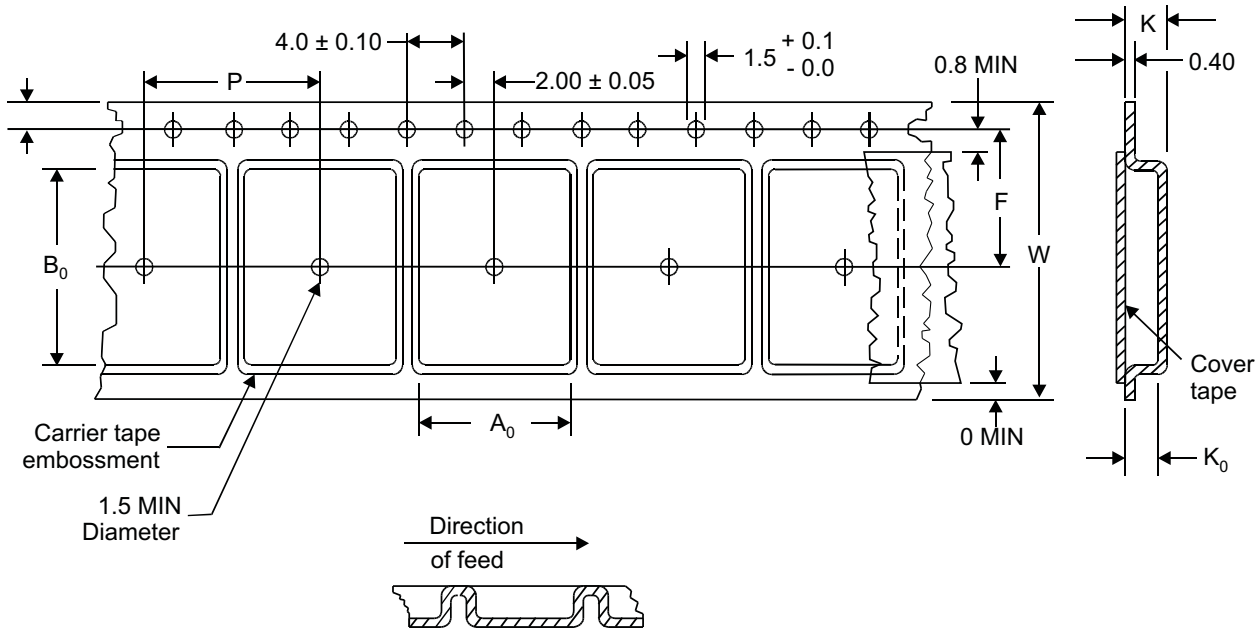


Figure 19. Single Sprocket Tape Dimension

Table 8. Tape Dimensions(1)

Tape Width (W)	Pocket Pitch (P)	Pocket Width (A_0)	Pocket Length (B_0)	Pocket Depth (K_0)	Max. Tape Depth (K)	Centerline to Drive Hole (F)	Package Size
16	8	6.3	6.3	1.35	0.75	7.5	6 × 6
16	12	8.3	8.3	1.85	1.10	7.5	8 × 8
24	16	10.3	10.3	1.90	1.10	11.5	10 × 10
24	16	12.3	12.3	2.00	1.10	11.5	12 × 12
24	16	13.3	13.3	2.00	1.30	11.50	13 × 13
24	24	14.3	14.3	1.40	0.70	11.50	14 × 14

(1) All dimensions are in millimeters.

The reels are shown in Figure 20. In this figure, G is the width of the tape, N is the diameter of the hub, and T is the total reel thickness.

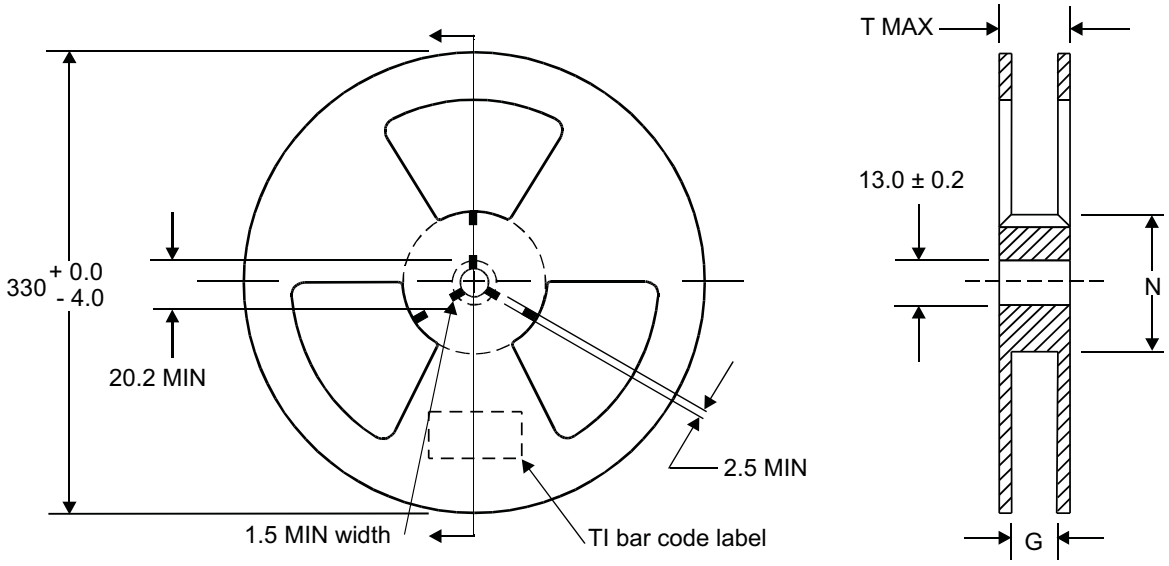


Figure 20. Reel Dimensions

Table 9. Reel Dimensions(1)

Tape Width (G)	Reel Hub Diameter (N)	Reel Total Thickness (T MAX)	Parts per Reel
16	100	16.4	2500
24	100	24.4	1000

(1) After the parts are loaded into the reel, each individual reel is packed in its own “pizza” box for shipping, as shown in Figure 21.

After the parts are loaded into the reel, each individual reel is packed in its own “pizza” box for shipping, as shown in Figure 21.

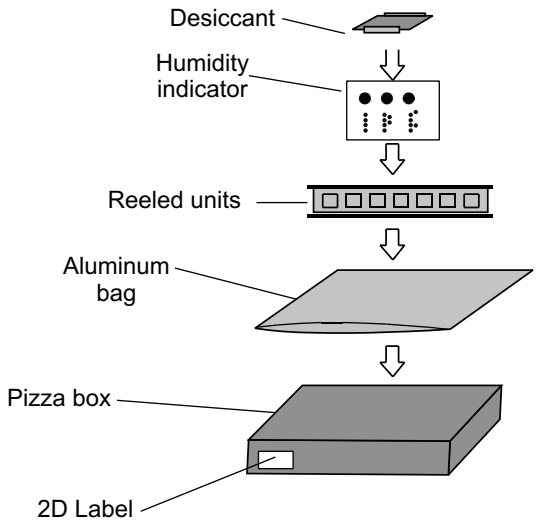


Figure 21. Tape-and-Reel Packing

5.4 Device Insertion

Devices are inserted toward the outer periphery of the tape by placing the side with the device name face up and the side with the balls attached face down. The pin-1 indicator is placed in the top left-hand corner of the pocket, next to the sprocket holes.

5.5 Packaging Method

For reels, once the taping has been completed, the end of the leader is fixed onto the reel with tape. The product name, lot number, quantity, and date code are recorded on the reel and the cardboard box used for tape delivery. Each reel is separately packed in a cardboard box for delivery.

Trays are packed with five loaded trays and one empty tray on top for support and to keep packages secure. The stack is secured with stable plastic straps and sealed in a moisture-proof bag.

Customer-specific bar code labels can be added under request or general purchasing specification.

Moisture-sensitive packages are baked before packing and are packed within 8 hours of coming out of the oven. Both the tape-and-reel and the tray moisture-proof bags are sealed and marked with appropriate labeling warning that the packages inside the bags are dry-packed and giving the level of moisture sensitivity.

6 Sockets

6.1 The Design Challenge

The fine pitch of nFBGA packages makes socketing a special challenge. Mechanical, thermal, and electrical issues must be accommodated by the socket designer. The size of a specific package within the TI nFBGA family is based on the package construction, and is independent of die size. Therefore, a range of die sizes and I/Os within a family will have the same package dimensions. Each different family has a specific I/O pitch and array. For maximum socket versatility, an adapter or “personalizer” can be customized for each application, allowing a single-socket body to be used with many packages. This feature is especially useful in the early days as the technology is being developed and adopted as well as during volume production phase to minimize socket costs.

6.2 Contacting the Ball

A number of different approaches for contacting the solder ball are shown schematically in Figure 22. The pinch style contact has been used extensively for contacting solder balls in conventional BGAs and is starting to be proposed also for the most advanced fine pitch CSP packages.

The most common methods used for contacting as small as 0.4 mm pitch CSP packages are either metal pinch (a) or metal (f). Both methods provide the most reliable solutions with less ball deformation and small socket form factor at an affordable cost. Texas Instruments Interconnect Business Unit (TI IBU) has designed both pinch and micro tuning fork (metal type) contacts that satisfy all of these requirements. Further information on the availability of these sockets can be obtained from your local TI Field Sales representative.

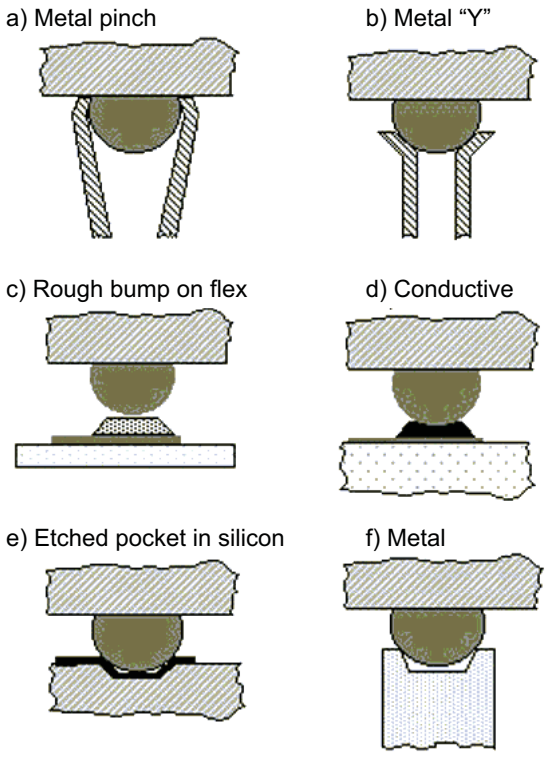


Figure 22. Approaches for Contacting the Solder Ball

6.3 Pinch Contact

The contact is designed to grip the solder ball with a pinching action. This not only provides electrical contact to the solder ball but also helps retain the package in the socket. The contact is shown in Figure 23. It was made using a beryllium copper alloy. This alloy is used for spring applications that are exposed to high stresses and temperatures because of its excellent stress relaxation performance and formability.

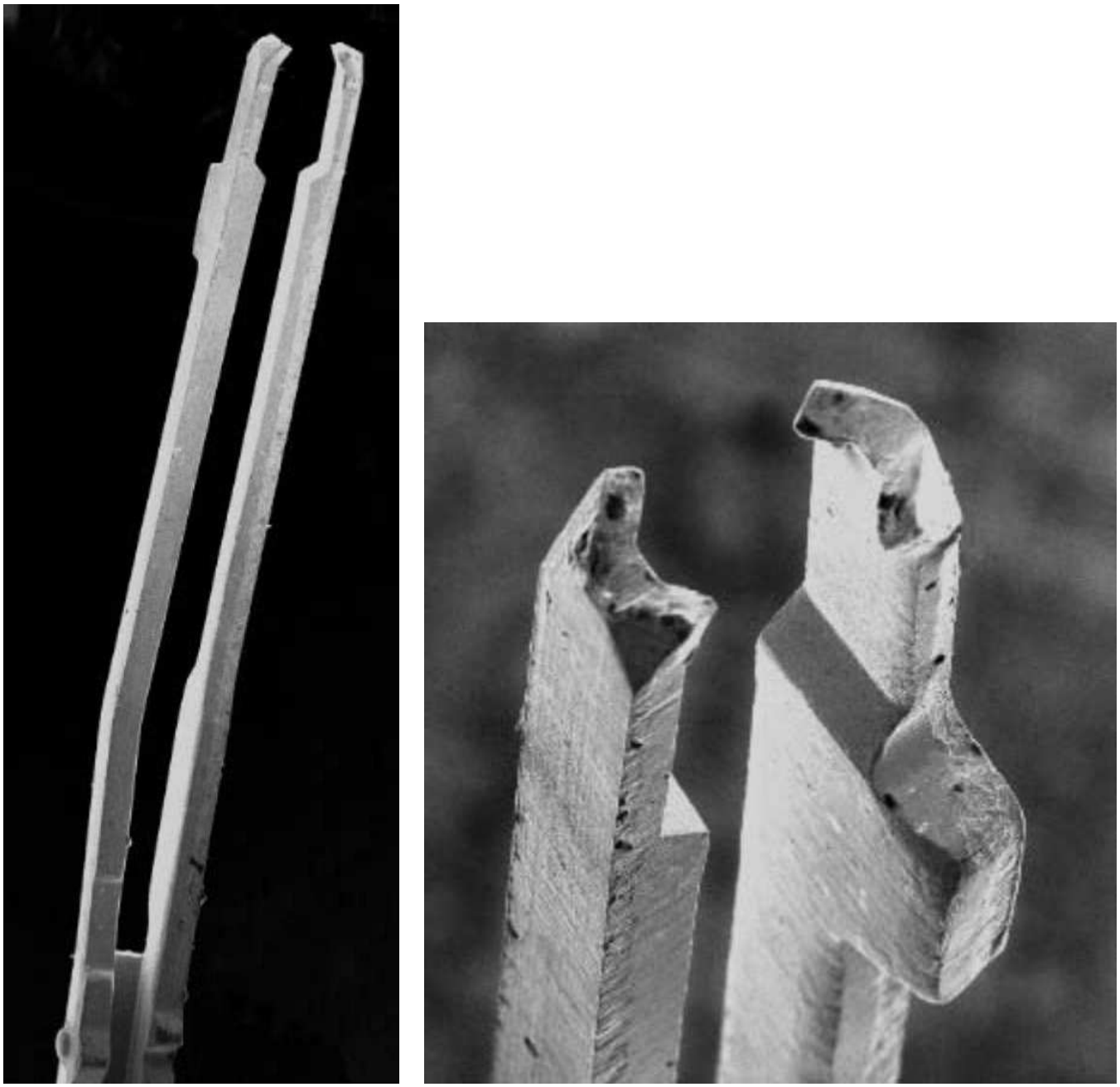


Figure 23. Pinch Contact for Solder Ball

Each contact incorporates two beams that provide an oxide-piercing interface with the sides of the balls above the central area—the equator. No contact is made on the bottom of the solder ball so the original package planarity specifications are unchanged. A photo-micrograph of the contact touching the solder balls is shown in Figure 24.

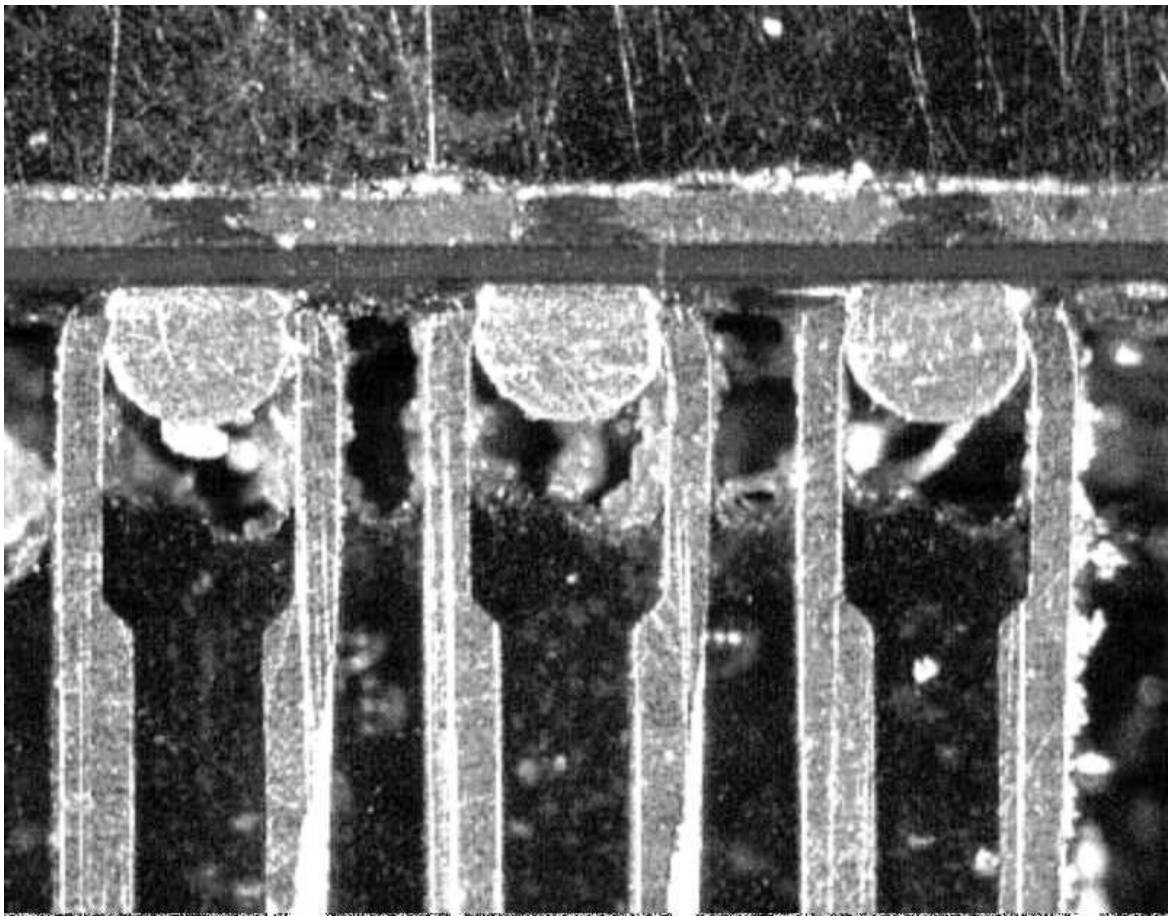


Figure 24. Contact Area on Solder Ball

The witness marks left on the solder ball from the contact are shown in Figure 25. This ball was contacted at room temperature and it is clear that there was no damage to the bottom of the ball or any witness marks from the contact above the equator.

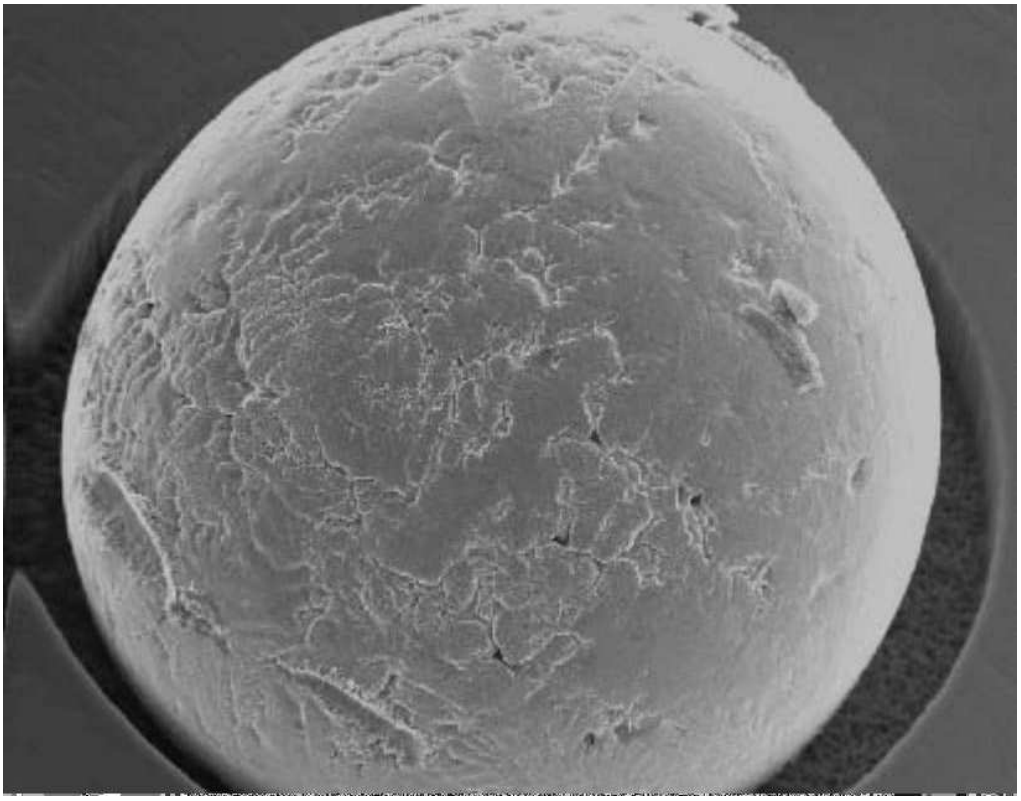


Figure 25. Witness Marks on Solder Ball

The effect of burn-in on the probe marks was examined by simulating a cycle and placing a loaded socket into an oven at 125°C for nine hours. The result is shown in Figure 26. The penetration of the contact into the solder ball due to the higher temperature is greater but is well within the acceptable range. There was no visible pickup of solder on the contact tips. The location of the contact pinch is clearly seen in this photograph.

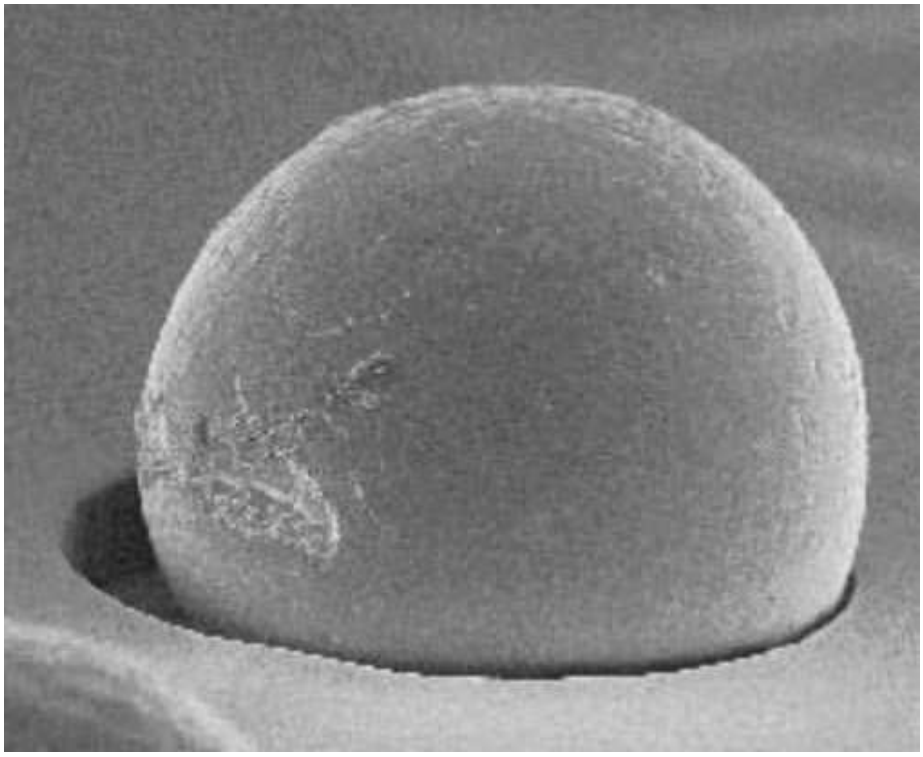


Figure 26. Effect of Bur-In on Probe Mark

6.4 Micro Tuning Fork Contact

Micro tuning fork contact system with vertical launch secures the solder balls to provide stable electrical continuity. Figure 27 shows how the micro fork contacts solder ball as well as solder witness marks after 24 hours at 150°C. There is also no contact made on the bottom of the solder ball preventing ball damage that could affect solder ball planarity specification, as illustrated in Figure 28.

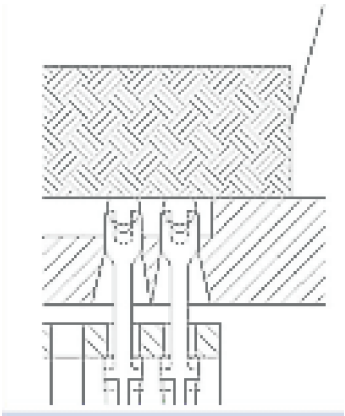


Figure 27. Micro Tuning Fork Contact for 0.5mm Pitch

Figure 28. Micro Tuning Fork Contact and Contact Marks on Solder Balls

6.5 Texas Instruments Sockets

Pictures below are showing Texas Instruments most advanced 0.8 mm and 0.5 mm pitch showing :

- Very small form factor
- Open top solution for easy automatic loading/unloading operations.

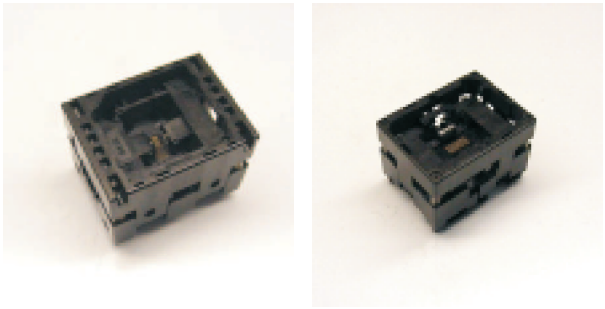


Figure 29. Socket Examples: Tuning Fork (Left) and Pinch Style (Right)

6.6 Conclusion

Some very good progress has been made during the past few years in developing fine pitch CSP packages sockets for CSP ball pitch. Sockets are now very common and proposed by most sockets manufacturers with open top or clam shell options.

Texas Instruments Interconnect Business Unit will provide you with a complete range of sockets technology for CSP package. For further information your local TI Field Sales representative can give you up-to-date information or please visit web site http://www.ti.com/snc/products/controls/burnin.htm

Frequently Asked Questions

A.1 Package Questions

Q **Do the solder balls come off during shipping?**

A No, this has never been observed. The balls are inspected for coplanarity, diameter, and other physical properties prior to packing for shipment. Because solder is used during the ball-attachment process, uniformly high ball-attachment strengths are developed. Also, the ball-attachment strength is monitored frequently in the assembly process to prevent ball loss from vibration and other shipping forces.

Q **Is package repair possible? Are tools available?**

A Yes, some limited package repair is possible, and there are some semiautomatic M/C tools available. However, TI does not specify the reliability of repaired packages.

Q **What are the leads that appear on the package edge for? Are they connected to the inner pattern?**

A Those leads are used for plating connections during the plating of Ni/Au on the copper trace during the fabrication of the substrate. Since they do have electrical connection with the inner pattern, they can be used for test probing and signal analysis. There is no reliability risk with them.

Q **Is burn-in testing possible? How about ball damage?**

A There are commercial sockets available for fine pitch package burn-in. For further information your local TI Field Sales representative can give you up-to-date information. The ball damage observed falls within specified tolerances, so the testing does not affect board mount.

Q **Is tape-and-reel shipping available?**

A Yes, tape-and-reel is an available method for shipping nFBGA packages.

Q **How does the packaging cost compare to QFPs?**

A CSPs are in many ways an ideal solution to cost reduction and miniaturization requirements. They offer enormous area reductions in comparison to QFPs and have increasing potential to do so without adding to system-level costs. In the best case, CSPs compete today on a cost-per-terminal basis with QFPs. For example, various CSPs from Texas Instruments are now available at cost parity within QFPs.

A.2 Assembly Questions

Q **What alignment accuracy is possible?**

A Alignment accuracy for the nFBGA package is dependent upon board-level pad tolerance, placement accuracy, and solder ball position tolerance. Nominal ball position tolerances are specified at ±50 µm. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q **Can the solder joints be inspected after reflow?**

A Process yields of 5-ppm (parts per million) rejects are typically seen, so no final in-line inspection is required. Some customers are achieving satisfactory results during process set-up with lamographic X-ray techniques.

Q **How do the board assembly yields of nFBGAs compare to QFPs?**

A Many customers are initially concerned about assembly yields. However, once they had nFBGA packages in production, most of them report improved process yields compared to QFPs. This is due to the elimination of bent and misoriented leads, and the ability of these packages to self-align during reflow. The collapsing solder balls also mean that the coplanarity is improved over leaded components.

Q **Are there specific recommendations for SMT processing?**

A Texas Instruments recommends alignment with the solder balls for the CSP package, although it is possible to use the package outline for alignment. Most customers have found they do not need to change their reflow profile.

Q **Can the boards be repaired?**

A Yes, there are rework and repair tools and profiles available. TI strongly recommends that removed packages be discarded.

Q **What size land diameter for these packages should I design on my board?**

A Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in this document.

Package Data Sheets

Table 10 shows TI's strategic package lineup, followed by package data sheets for many of the package families offered as standard products by Texas Instruments. As new packages are added, they will be placed on the strategic package lineup. Contact your TI field sales office for information on the most current offerings. Samples are available for all packages shown in Table 10.

Table 10. TI's Strategic Package Line-Up

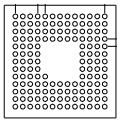
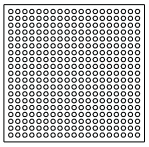
nFBGA Package Product Guide								
Pitch (mm)	Package Size (mm)							
	6×6	7×7	8×8	10×10	12×12	13×13	14×14	16×16
0.8					145ZWS 			361ZWT 
0.65			113ZVD 					

Table 10. TI's Strategic Package Line-Up (continued)

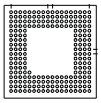
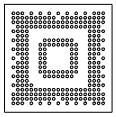
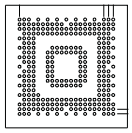
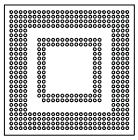
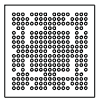
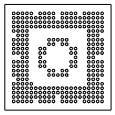
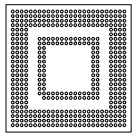
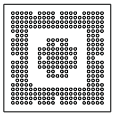
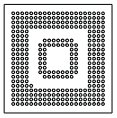
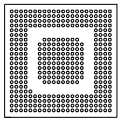
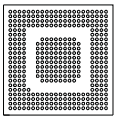
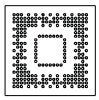
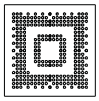
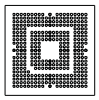
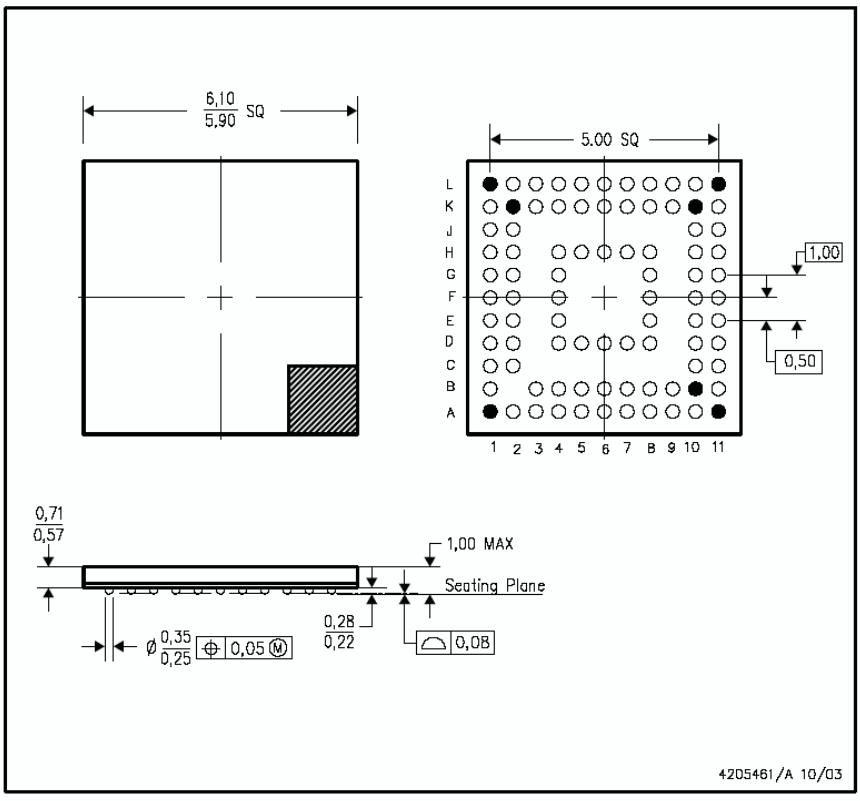
nFBGA Package Product Guide								
Pitch (mm)	Package Size (mm)							
	6×6	7×7	8×8	10×10	12×12	13×13	14×14	16×16
0.5	87ZVW 	72ZST 	195ZWV 	225ZWF 	289ZVL 	289ZWE 	447ZAC 	
	143ZWU 		241ZWG 	293ZVL 			447ZAF 	
	143ZZC 			318ZVL 				
	152ZZB 			325ZVL 				
				385ZWK 				
				385ZWM 				

Table 10. TI's Strategic Package Line-Up (continued)

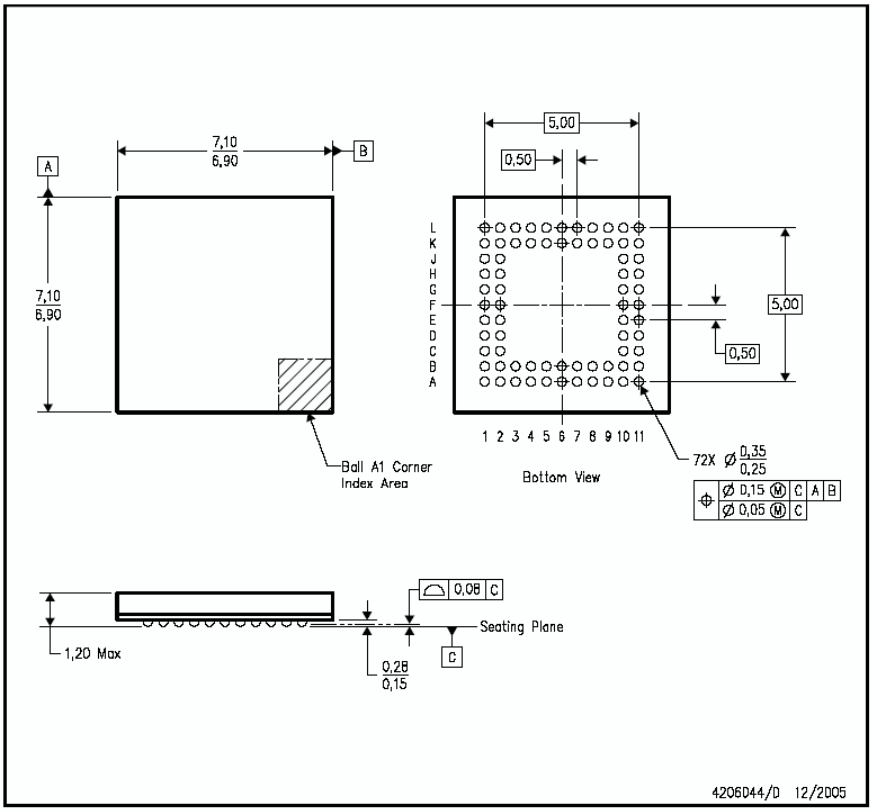
nFBGA Package Product Guide								
Pitch (mm)	Package Size (mm)							
	6×6	7×7	8×8	10×10	12×12	13×13	14×14	16×16
0.4		209ZXN 		241ZWJ 				
				289ZWJ 				
				360ZWJ 				



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration.
D. A1, A11, L1, L11, B10, K2, K10 to be dummy balls.
E. This package is lead-free.

Figure 30. 87ZVW Package Outline (6 x 6mm, 0.5mm pitch)

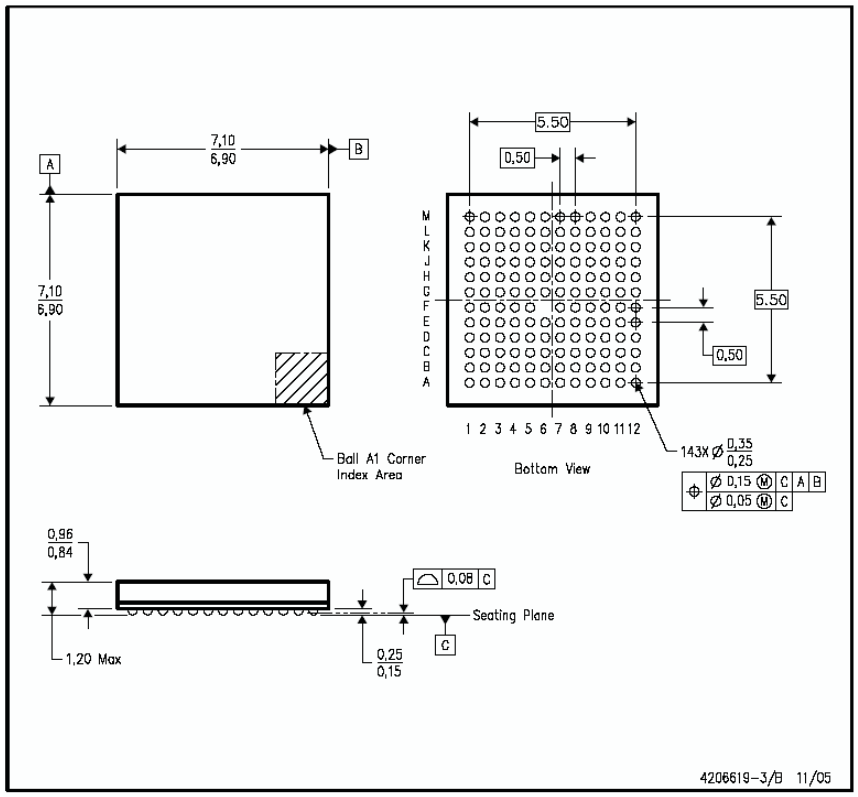
87ZVW Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO–195 variation AD (depopulated).
D. This package is lead–free. Refer to the 72 GST package (drawing 4206043) for tin–lead (SnPb).

Figure 31. 72ZST Package Outline (7 x 7mm, 0.5mm pitch)

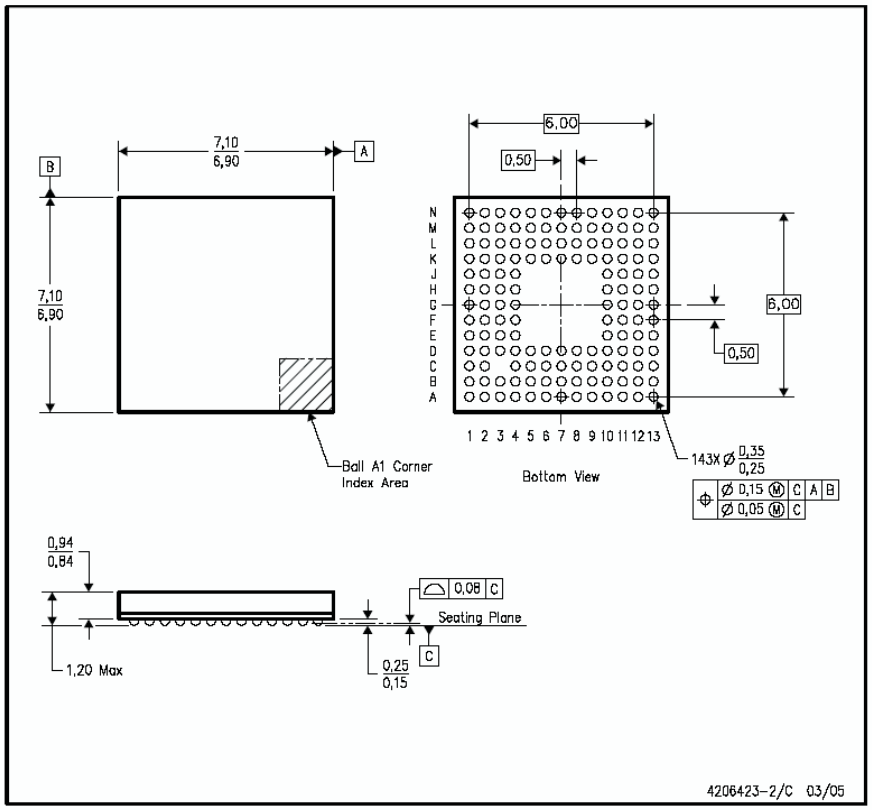
72ZST Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO-225 registration is pending.
D. This is a lead-free solder ball design.

Figure 32. 143ZZC Package Outline (7 x 7mm, 0.5mm pitch)

143ZZC Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO-225 registration is pending.
D. This package is lead-free.

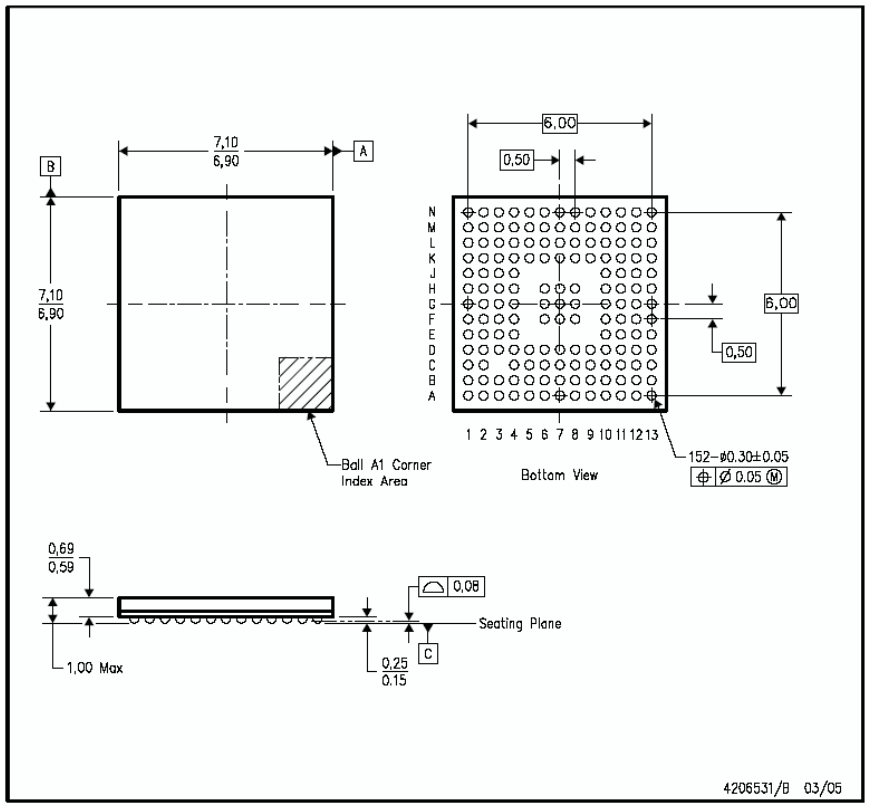
Figure 33. 143ZWU Package Outline (7 x 7mm, 0.5mm pitch)

BALL No.	BALL No.
A1	B1
C1	D1
E1	F1
G1	H1
J1	K1
L1	L2
M1	N1
A2	
B2	C2
D2	D3
E2	E3
F2	F3
G2	G3
H2	H3
J2	J3
K2	K3
M2	N2
A3	B3
L3	M3
N3	N4
A4	A5
B4	C4
D4	E4
F4	G4
H4	J4

BALL No.	BALL No.
K4	K5
L4	M4
B5	C5
D5	D6
L5	M5
N5	N6
A6	A7
B6	C6
K6	K7
L6	M6
B7	C7
D7	D8
L7	M7
N7	N8
A8	A9
B8	C8
K8	K9
L8	M8
B9	C9
D10	D9
L9	M9
N10	N9
A10	A11
B10	C10
E10	F10

BALL No.	BALL No.
G10	H10
J10	K10
L10	M10
B11	C11
D11	D12
E11	E12
F11	F12
G11	G12
H11	H12
J11	J12
K11	K12
L11	L12
M11	N11
A12	B12
C12	C13
M12	M13
N12	N13
A13	B13
D13	E13
F13	G13
H13	J13
K13	L13

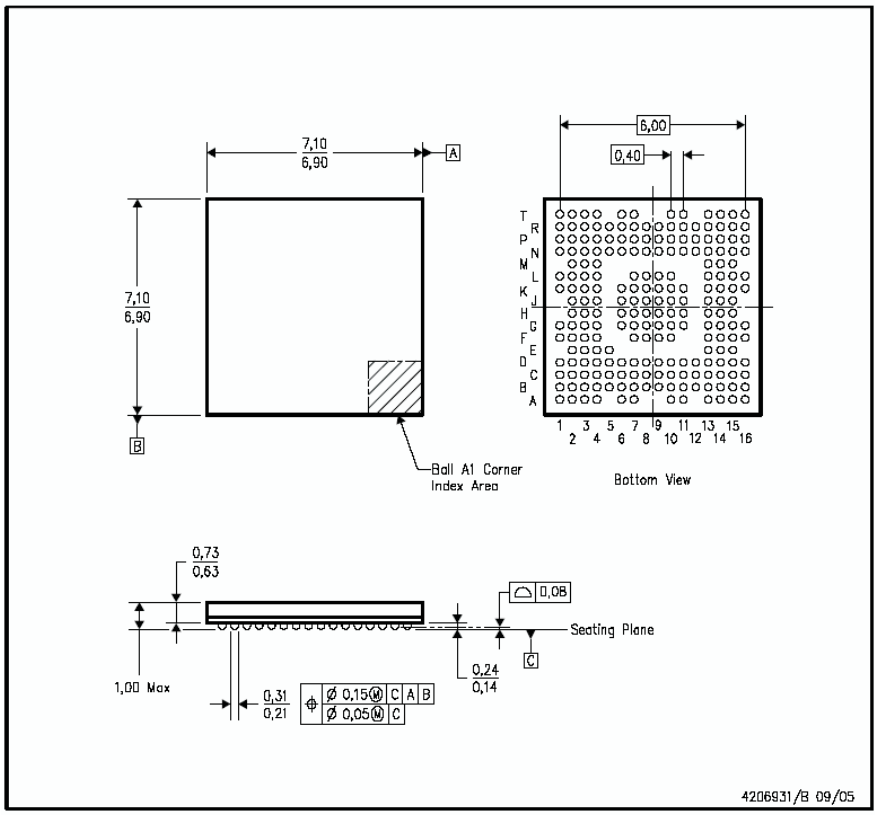
Figure 34. 143ZWU Daisy Chain Net List



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO–225 registration is pending.
D. This package is lead–free.

Figure 35. 152ZZB Package Outline (7 x 7mm, 0.5mm pitch)

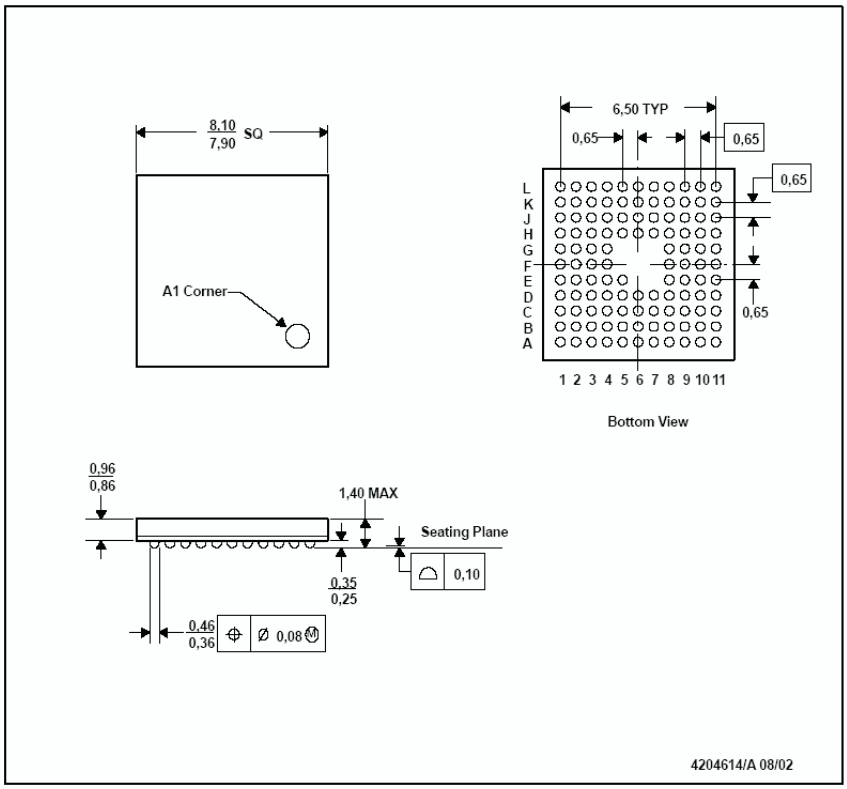
152ZZB Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–195.
D. This package is lead–free.

Figure 36. 209ZXN Package Outline (7 x 7mm, 0.4mm pitch)

209ZXN Daisy Chain Net List Not Available



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. LFBGA configuration
D. This package id lead-free.

Figure 37. 113ZVD Package Outline (8 x 8mm, 0.65mm pitch)

8x8nFBGA Daigy Chain Sample NET LIS

Ball to Ball Connection Information

Ball#	Ball#
A1	B1
C2	C1
D4, E5	D3
D2	D1
E4	E3
E2	E1
F4	F2, F3
F1	G1
G2	H1
H2	H3
H4	J1
J2	K1
J3	L1
K2	L2
K3	J4
L3	K4
L4	J5
K5	L5
J6	K6
L6	L7
K7	J7, H5
H6	L8
K8	J8, H7
H8	L9
K9	L10
J9	K10
L11	K11
J10	H9
J11	H10
H11	G8
G9	G10
G11	F9
F10	F11
E11	E10
D11	D10
E9	D9
C11	C10
F8	B11
E8	C9
B10	A11
B9	A10
D8	A9
C8	B8
A8	D7
C7	B7
A7	C6, D6
B6	A6
A5	B5
C5	D5
A4	B4
C4	A3
B3	A2
B2	C3

Figure 38. 113ZVD Daisy Chain Net List

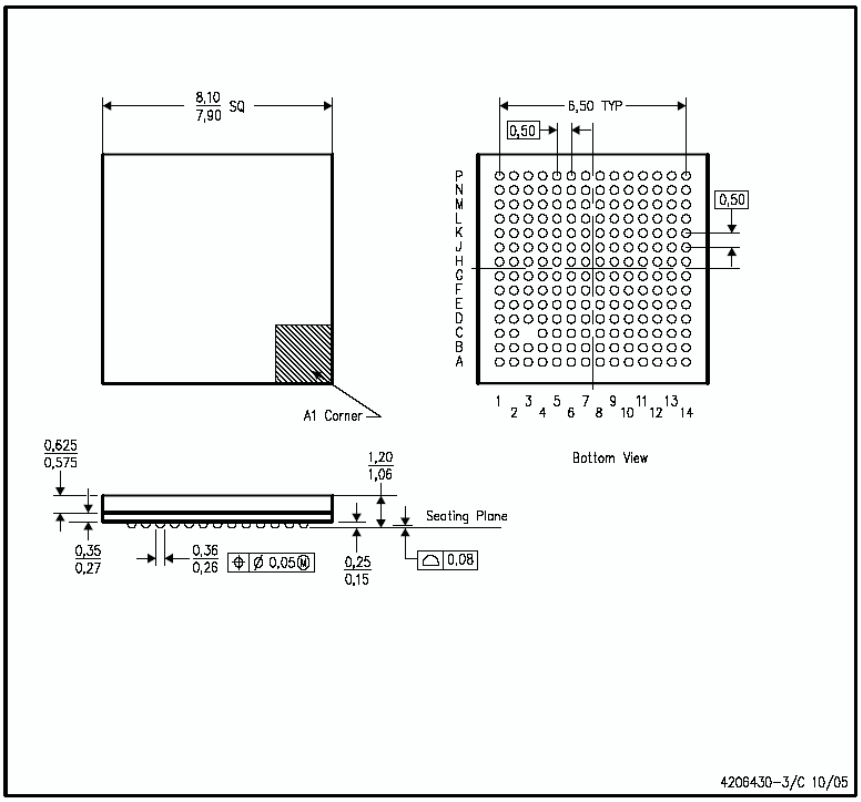


Figure 39. 195ZWV Package Outline (8 x 8mm, 0.5mm pitch)

BALL No.	BALL No.	BALL No.
A1	B2	
B1	C1	
C2	D4	
D2	D3	
D1	E1	
E2	E3	
E4	E5	
F5	F6	
F3	F4	
F1	F2	
G1	G2	
G3	G4	
G5	G6	
G7	H6	
H4	H5	
H2	H3	
H1	J1	
J2	J3	
J4	J5	
K3	K4	
K1	K2	
L1	L2	
L3	M2	
M1	N1	
N2	P1	

BALL No.	BALL No.	BALL No.
P2	P3	
M3	N3	
L4	M4	
N4	P4	
N5	P5	
L5	M5	
J6	K5	
K6	L6	
M6	N6	
P6	P7	
M7	N7	
K7	L7	
H7	J7	
J8	K8	
L8	M8	
N8	P8	
N9	P9	
L9	M9	
K9	L10	
M10	N10	
P10	P11	
M11	N11	
N12	P12	
P13	P14	
N13	N14	

BALL No.	BALL No.	BALL No.
M12	M13	
L14	M14	
L12	L13	
K10	L11	
K11	K12	
K13	K14	
J13	J14	
J11	J12	
J10	J9	
H8	H9	
H10	H11	
H12	H13	
G14	H14	
G12	G13	
G10	G11	
F10	G9	
F11	F12	
F13	F14	
E13	E14	
E11	E12	
D12	D13	
C14	D14	
B14	C13	
A14	B13	
A12	A13	

BALL No.	BALL No.	BALL No.
B12	C12	
C11	D11	
A11	B11	
A10	B10	
C10	D10	
E10	F9	
D9	E9	
B9	C9	
A8	A9	
B8	C8	
D8	E8	
F7	F8	G8
D7	E7	
B7	C7	
A6	A7	
B6	C6	
D6	E6	
C5	D5	
A5	B5	
A4	B4	
B3	C4	
A2	A3	

Figure 40. 195ZWV Daisy Chain Net List

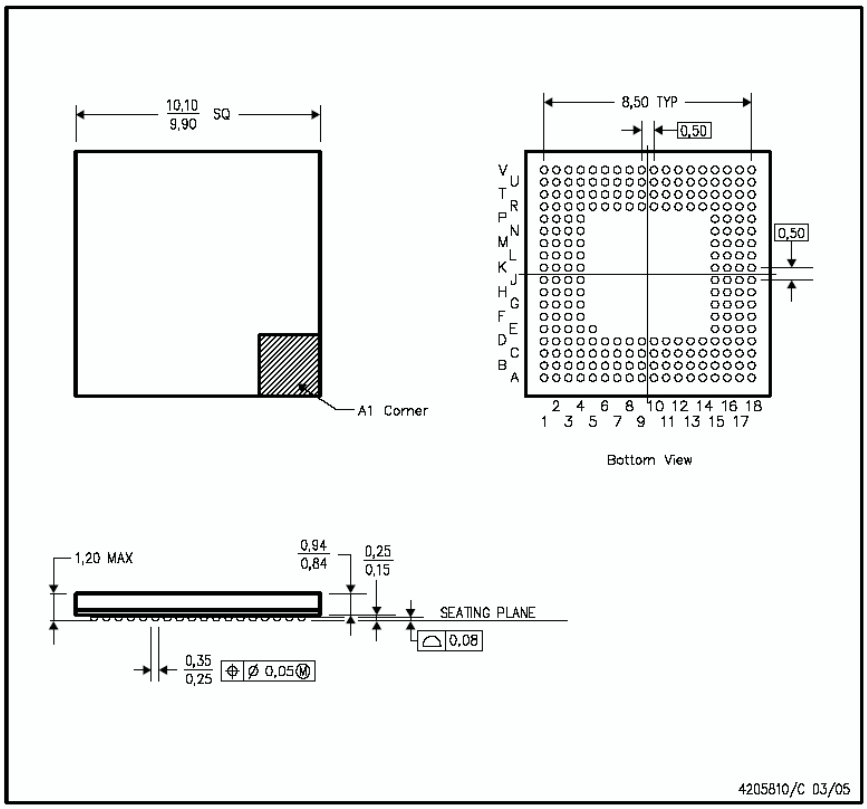
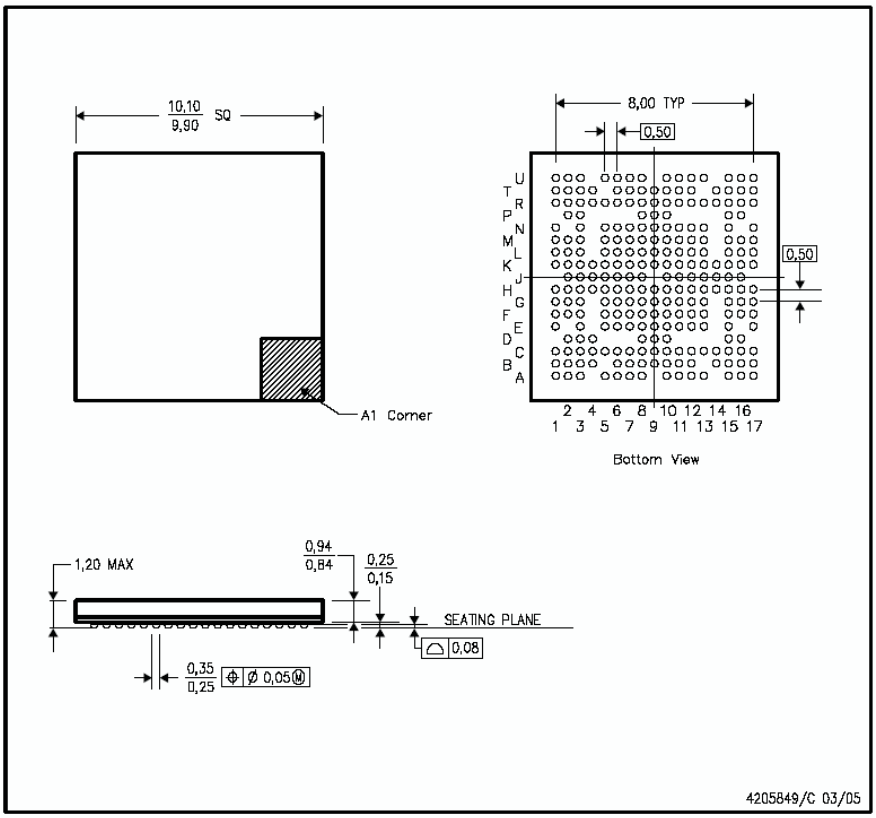


Figure 41. 225ZWF Package Outline (10 x 10mm, 0.5mm pitch)

225ZWF Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration
D. This package is lead–free.

Figure 42. 241ZWG Package Outline (10 x 10mm, 0.5mm pitch)

241ZWG Daisy Chain Net List Not Available

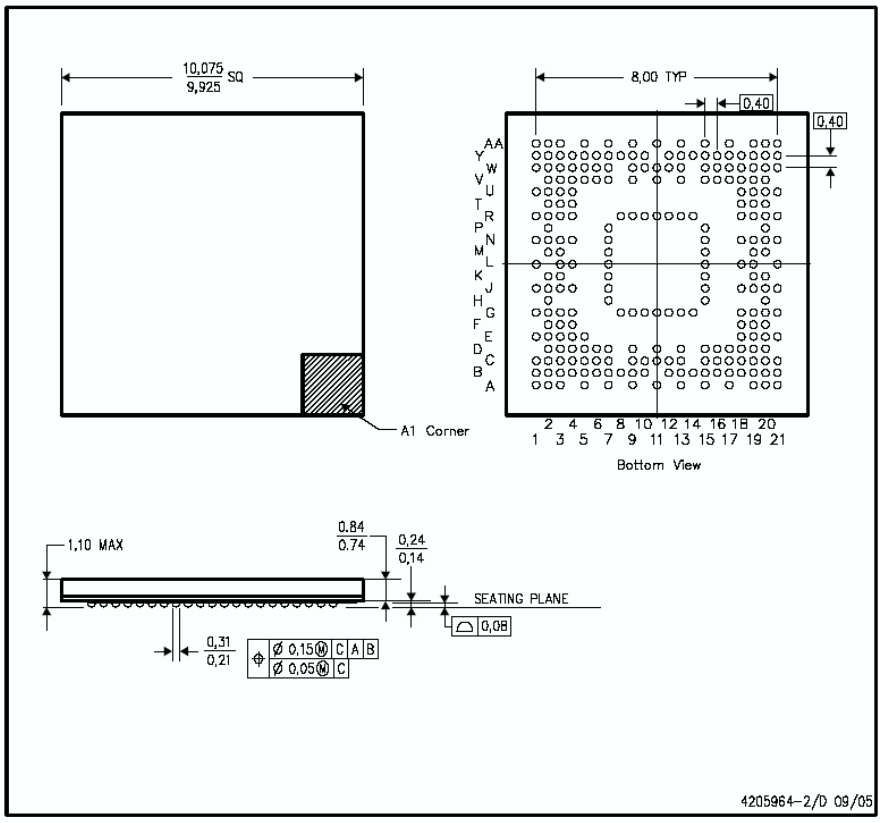


Figure 43. 241ZWJ Package Outline (10x10mm, 0.4mm pitch)

BALL No	BALL No
A1	A2
A3	A5
A7	A9
A11	A13
A15	A17
A19	A20
A21	B21
C21	E21
G21	J21
L21	N21
R21	U21
W21	Y21
AA21	AA20
AA19	AA17
AA15	AA13
AA11	AA9
AA7	AA5
AA3	AA2
AA1	Y1
W1	U1
R1	N1
L1	J1
G1	E1
C1	B1
B2	B3

BALL No	BALL No
B4	B5
B6	B7
B8	B9
B10	B12
B13	B14
B15	B16
B17	B18
B19	B20
C20	D20
E20	F20
G20	H20
J20	K20
M20	N20
P20	R20
T20	U20
V20	W20
Y20	Y19
Y18	Y17
Y16	Y15
Y14	Y13
Y12	Y10
Y9	Y8
Y7	Y6
Y5	Y4
Y3	Y2

BALL No	BALL No
W2	V2
U2	T2
R2	P2
N2	M2
K2	J2
H2	G2
F2	E2
D2	C2
C3	C4
C5	C6
C7	C9
C10	C11
C12	C13
C15	C16
C17	C18
C19	D19
E19	F19
G19	J19
K19	L19
M19	N19
R19	T19
U19	V19
W19	W18
W17	W16
W15	W13

BALL No	BALL No
W12	W11
W10	W9
W7	W6
W5	W4
W3	V3
U3	T3
R3	N3
M3	L3
K3	J3
G3	F3
E3	D3
D4	D5
D6	D7
D9	D11
D13	D15
D16	D17
D18	E18
F18	G18
J18	L18
N18	R18
T18	U18
V18	V17
V16	V15
V13	V11
V9	V7

BALL No	BALL No
V6	V5
V4	U4
T4	R4
N4	L4
J4	G4
F4	E4
E5	G8
G9	G10
G11	G12
G13	G14
H15	J15
K15	L15
M15	N15
P15	R14
R13	R12
R11	R10
R9	R8
P7	N7
M7	L7
K7	J7
H7	

Figure 44. 241ZWJ Daisy Chain Net List

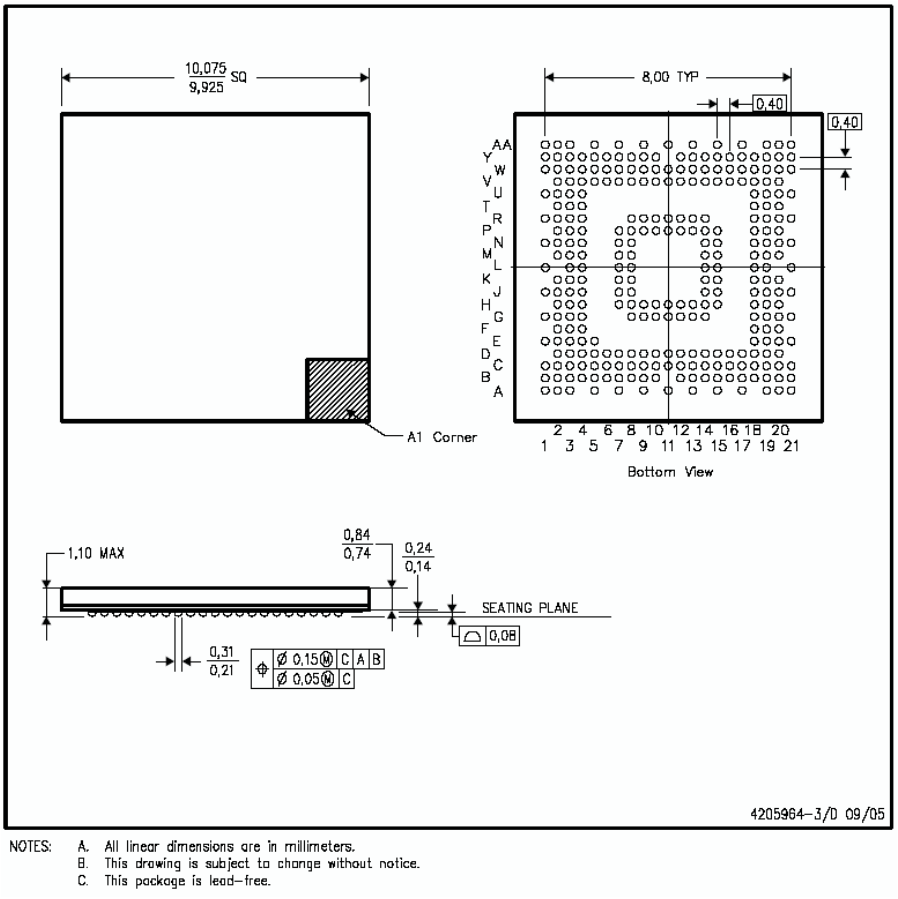


Figure 45. 289ZWJ Package Outline (10 x 10mm, 0.4mm pitch)

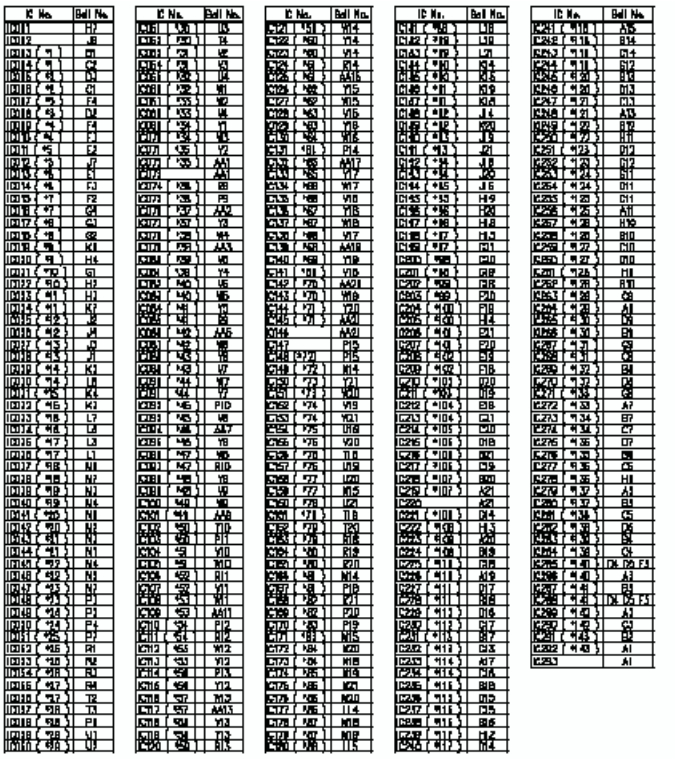


Figure 46. 289ZWJ Daisy Chain Net List

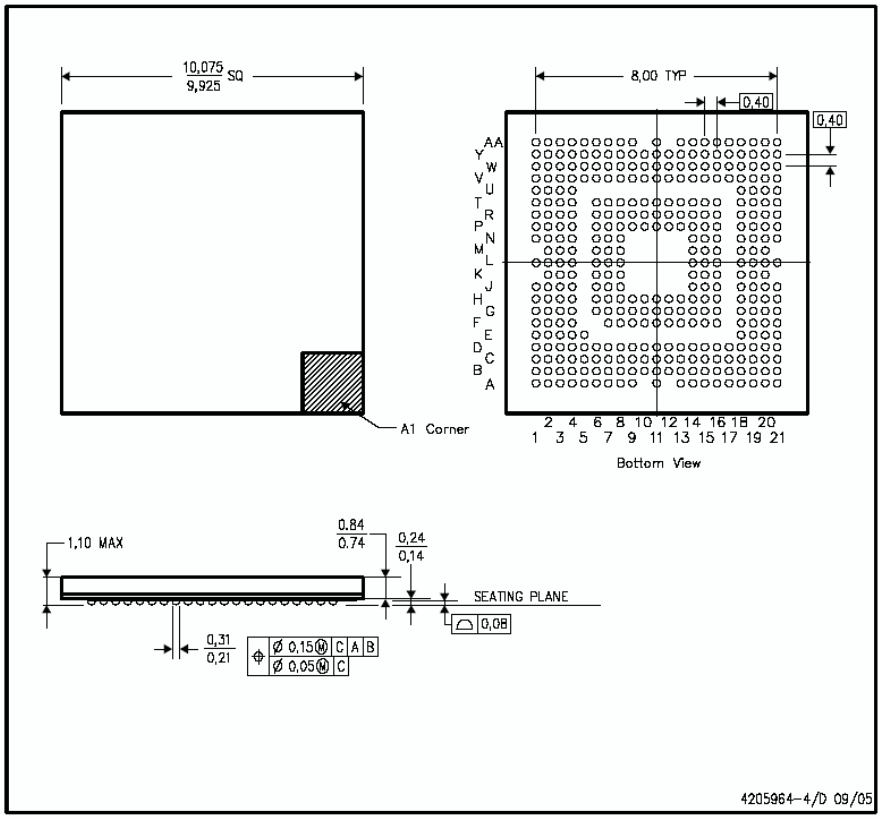


Figure 47. 360ZWJ Package Outline (10 x 10mm, 0.4mm pitch)

BALL No.	BALL No.
A1	A2
A3	A4
A5	A6
A7	A8
A9	A10
A11	A12
A13	A14
A15	A16
A17	A18
A19	A20
A21	B21
C21	D21
E21	F21
G21	H21
J21	L21
N21	P21
R21	T21
U21	V21
W21	Y21
AA21	AA20
AA19	AA18
AA17	AA16
AA15	AA14
AA13	AA11
AA9	AA8
AA7	AA6

BALL No.	BALL No.
AA5	AA4
AA3	AA2
AA1	Y1
W1	V1
U1	T1
R1	P1
N1	L1
J1	H1
G1	F1
E1	D1
C1	B1
B2	B3
B4	B5
B6	B7
B8	B9
B10	B11
B12	B13
B14	B15
B18	B17
B16	B19
B20	C20
D20	E20
F20	G20
H20	J20
K20	L20

BALL No.	BALL No.
M20	N20
P20	R20
T20	U20
V20	W20
Y20	Y19
Y18	Y17
Y16	Y15
Y14	Y13
Y12	Y11
Y10	Y9
Y8	Y7
Y6	Y5
Y4	Y3
Y2	W2
V2	U2
T2	R2
P2	N2
M2	L2
K2	J2
H2	G2
F2	E2
D2	C2
C3	C4
C5	C6
C7	C8

BALL No.	BALL No.
C9	C10
C11	C12
C13	C14
C15	C16
C17	C18
C19	D19
E19	F19
G19	H18
J18	K19
L19	M19
N19	P18
R19	T19
U19	V19
W19	W18
W17	W16
W15	W14
W13	W12
W11	W10
W9	W8
W7	W6
W5	W4
W3	V3
U3	T3
R3	P3
N3	M3

BALL No.	BALL No.
L3	K3
J3	H3
G3	F3
E3	D3
D4	D5
D6	D7
D8	D9
D10	D11
D12	D13
D14	D15
D16	D17
D18	E18
F18	G18
H18	J18
K18	L18
M18	N18
P18	R18
T18	U18
V18	W17
V16	V15
V14	V13
V12	V11
V10	V8
V6	V7
V8	V5

BALL No.	BALL No.
Y4	U4
T4	R4
P4	N4
M4	L4
K4	J4
H4	G4
F4	E4
E5	F7
F8	F9
F10	F11
F12	F13
F14	F15
F16	G16
H16	J16
K18	L18
M16	N16
P16	R16
T16	T15
T14	T13
T12	T11
T10	T9
T8	T7
T6	R6
P6	N6
N8	L8

BALL No.	BALL No.
K6	J6
H6	G6
G7	G8
G9	G10
G11	G12
G13	G14
G15	H15
J15	K15
L15	M15
N15	P15
R15	R14
R13	R12
R11	R10
R9	R8
R7	P7
N7	M7
L7	K7
J7	H7
H8	H9
H10	H11
H12	H13
H14	J14
K14	L14
M14	N14
P14	P13

BALL No.	BALL No.
P12	P11
P10	P9
P8	N8
M8	L8
K8	J8

Figure 48. 360ZWJ Daisy Chain Net List

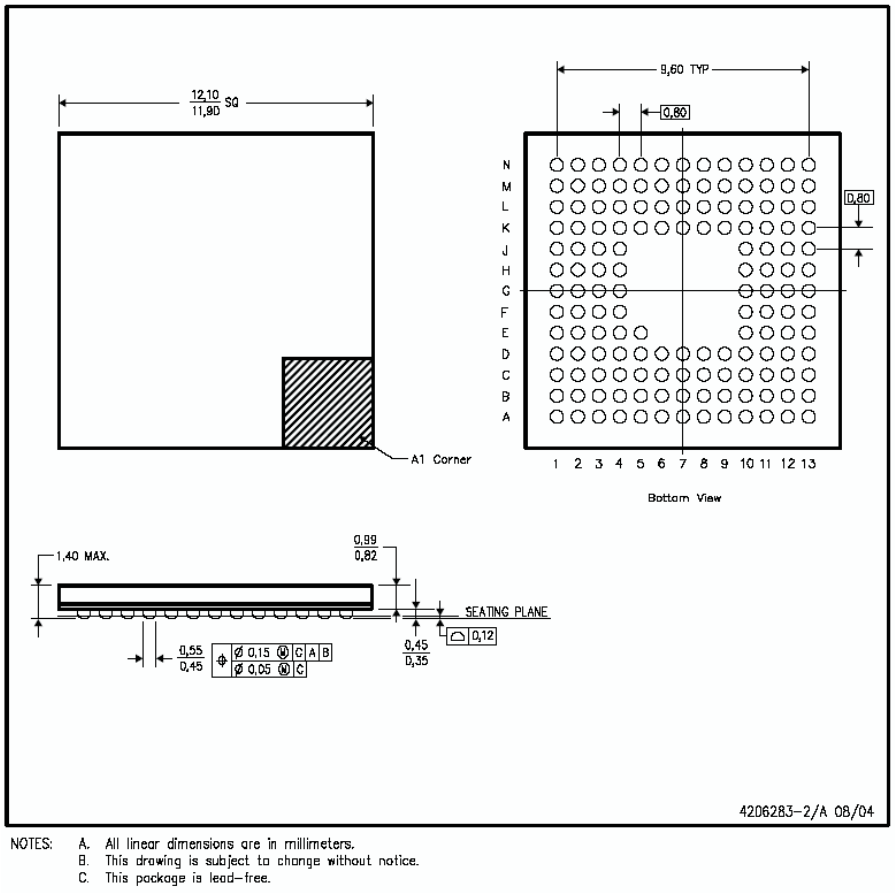


Figure 49. 145ZWS Package Outline (12 x 12mm, 0.8mm pitch)

145ZWS Daisy Chain Net List Not Available

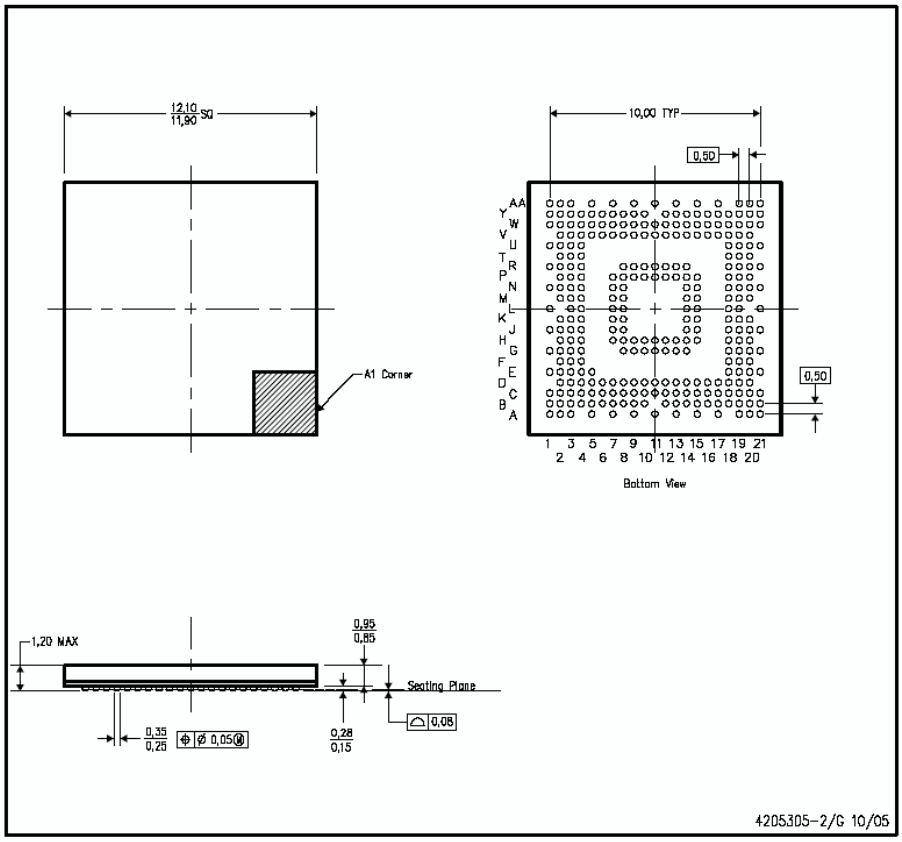


Figure 50. 289ZVL Package Outline (12 x 12mm, 0.5mm pitch)

289ZVL Daisy Chain Net List Not Available

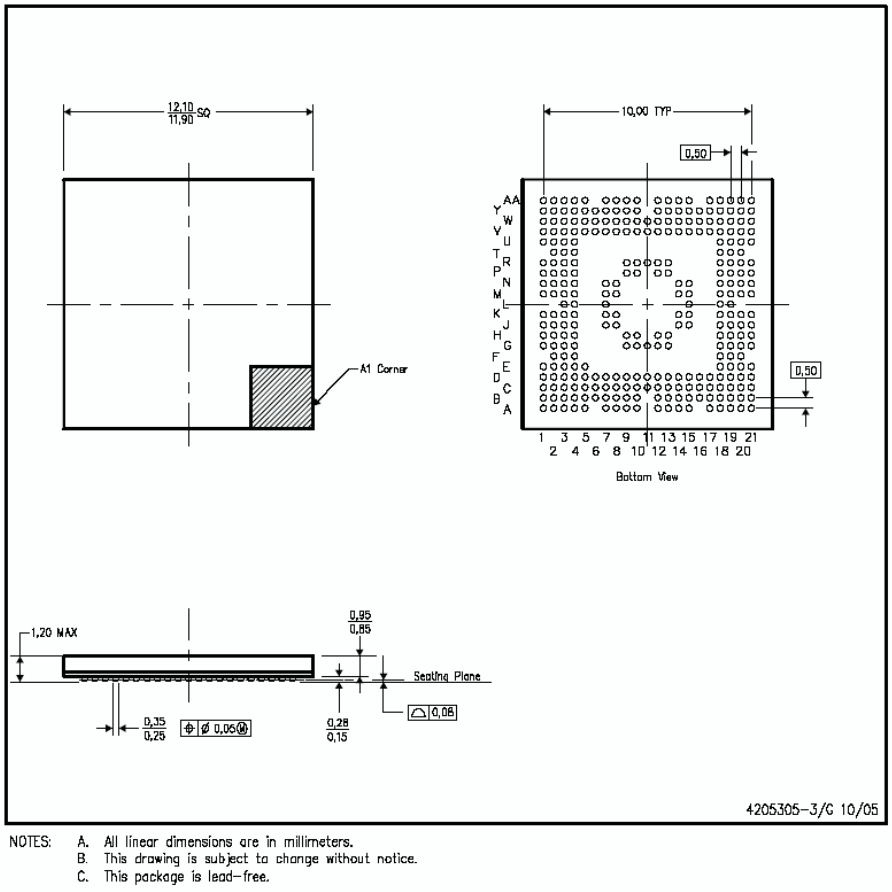


Figure 51. 293ZVL Package Outline (12 x 12mm, 0.5mm pitch)

293ZVL Daisy Chain Net List Not Available

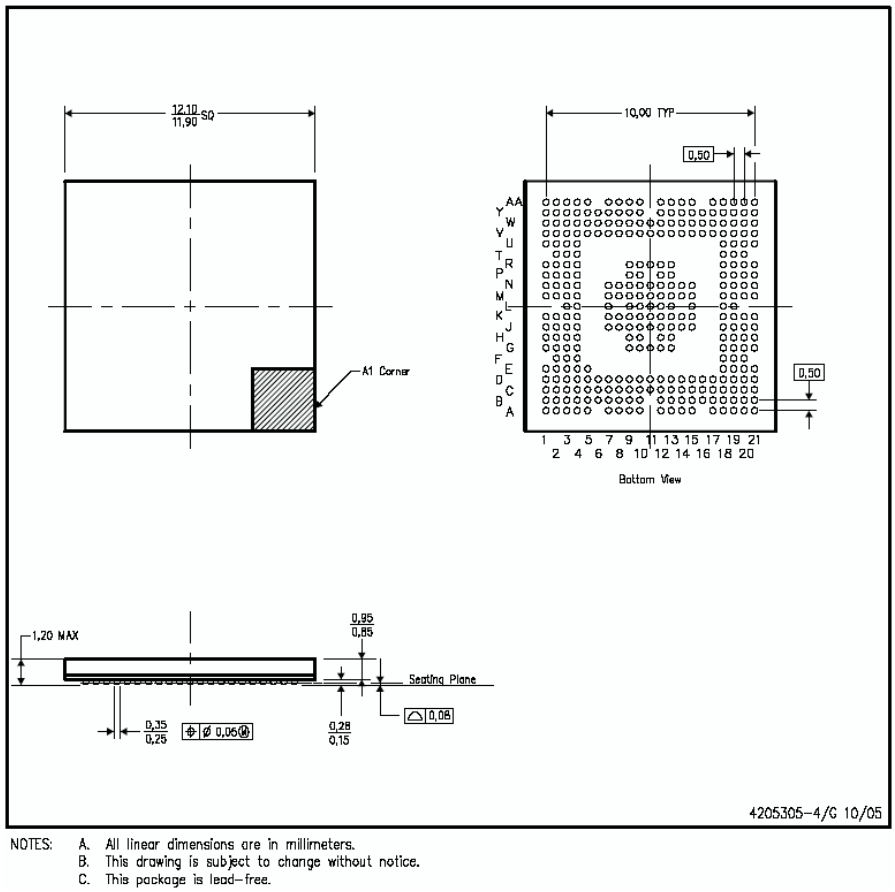
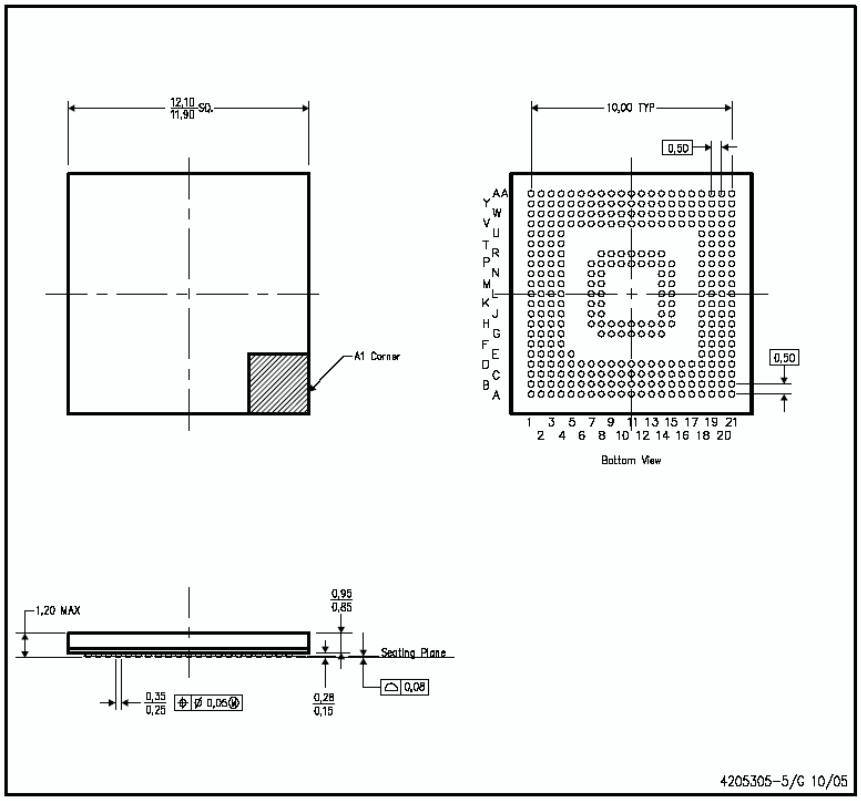


Figure 52. 318ZVL Package Outline (12 x 12mm, 0.5mm pitch)

318ZVL Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure 53. 325ZVL Package Outline (12 x 12mm, 0.5mm pitch)

BALL No.	BALL No.
A1	B2
A10	A11
A12	A13
A14	A15
A16	A17
A18	A19
A2	A3
A20	B20
A21	B21
A4	B4
A5	B5
A6	B6
A7	B7
A8	A9
AA1	Y1
AA10	AA9
AA11	AA12
AA13	AA14
AA15	Y15
AA16	Y16
AA17	Y17
AA18	Y18
AA19	AA20
AA2	Y2
AA21	Y20
AA3	AA4
AA5	AA6
AA7	AA8
B1	C1
B10	C10
B11	C11
B12	C12
B13	C13
B14	C14
B15	C15
B16	C16
B17	C17
B18	C18
B19	C19
B3	C4
B8	C8

BALL No.	BALL No.
B9	C9
C2	C3
C20	C21
C5	D5
C6	D6
C7	D7
D1	D2
D10	G10
D11	G11
D12	G12
D13	G13
D14	G14
D15	D16
D17	D18
D19	E18
D20	D21
D3	D4
D8	G8
D9	G9
E1	E2
E19	E20
E21	F21
E3	E4
E5	
F1	F2
F18	G18
F19	F20
F3	F4
G1	G2
G19	G20
G21	H21
G3	G4
H1	H2
H10	H9
H11	H12
H13	H14
H15	H18
H19	H20
H3	H4
H7	H8
J1	J2

BALL No.	BALL No.
J14	J15
J18	J19
J20	J21
J3	J4
J7	J8
K1	K2
K14	K15
K18	K19
K20	K21
K3	K4
K7	K8
L1	L2
L14	L15
L18	L19
L20	L21
L3	L4
L7	L8
M1	M2
M14	M15
M18	M19
M20	M21
M3	M4
M7	M8
N1	N2
N14	N15
N18	N19
N20	N21
N3	N4
N7	N8
P1	R1
P10	P11
P12	P13
P14	P15
P18	P19
P2	P3
P20	P21
P4	P7
P8	P9
R10	V10
R11	V11
R12	V12

BALL No.	BALL No.
R13	V13
R14	V14
R18	R19
R2	R3
R20	R21
R4	T4
R8	V8
R9	V9
T1	U1
T18	T19
T2	T3
T20	T21
U18	U19
U2	U3
U20	U21
U4	V3
V1	V2
V15	W15
V16	W16
V17	W17
V18	V19
V20	V21
V4	V5
V6	V7
W1	W2
W10	Y10
W11	Y11
W12	Y12
W13	Y13
W14	Y14
W18	Y19
W19	W20
W21	Y21
W3	Y3
W4	Y4
W5	Y5
W6	Y6
W7	Y7
W8	Y8
W9	Y9

Figure 54. 325ZVL Daisy Chain Net List

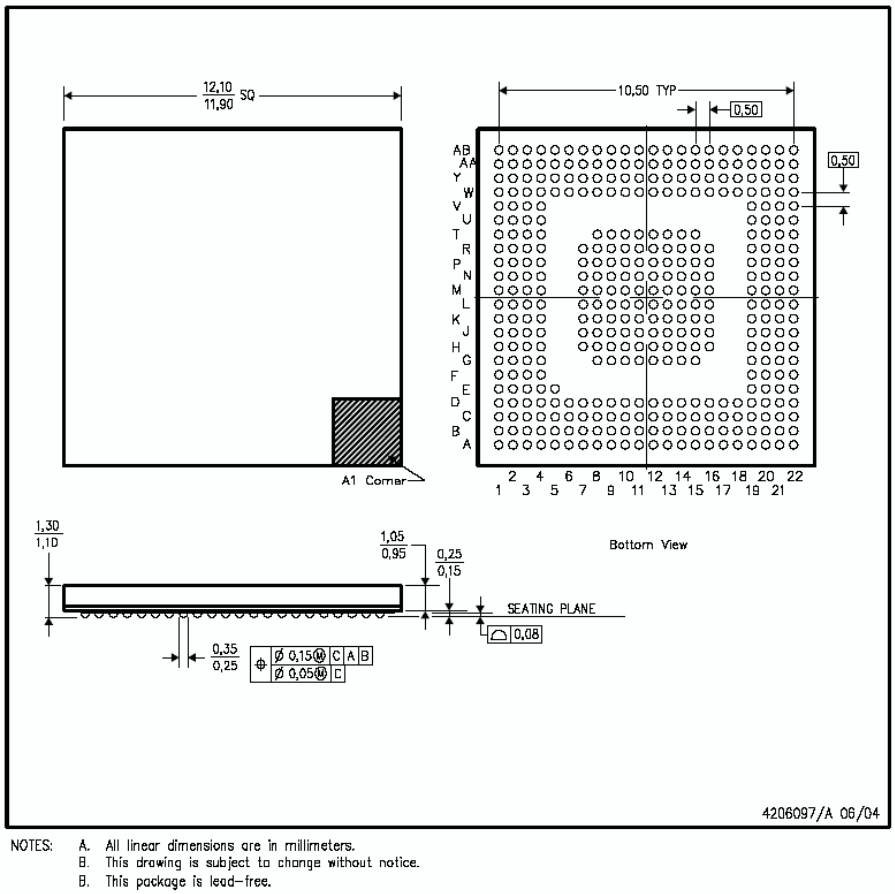
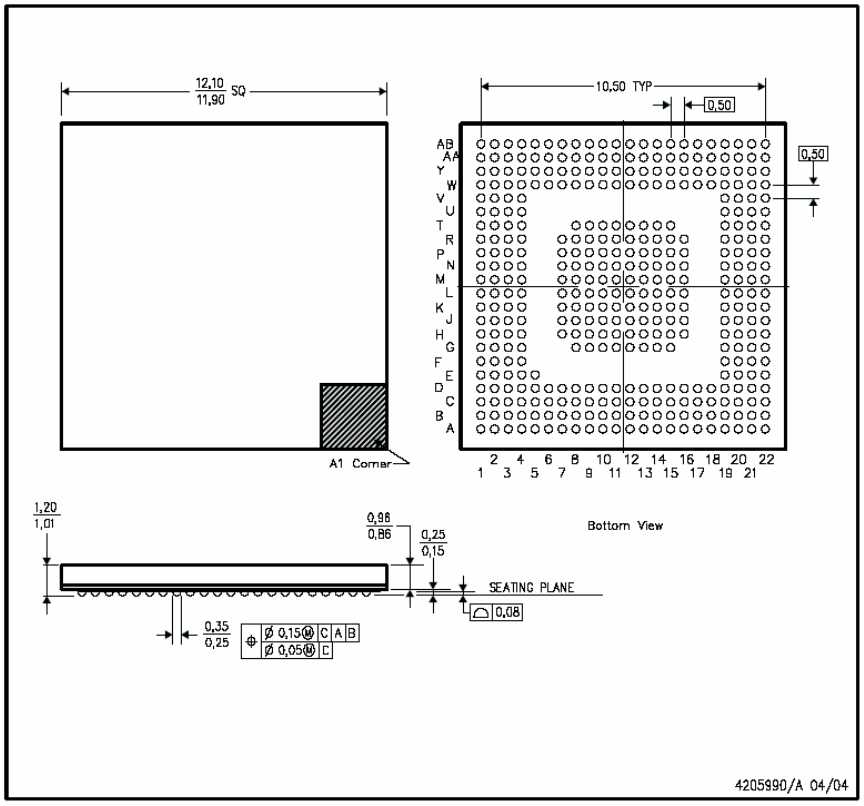


Figure 55. 385ZWM Package Outline (12 x 12mm, 0.5mm pitch)

385ZWM Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
B. This package is lead–free.

Figure 56. 385ZWK Package Outline (12 x 12mm, 0.5mm pitch)

BALL No.	BALL No.	BALL No.
A1	A2	
AA1	B1	
B2	C1	
D1	D2	
E1	E3	
F1	G2	
G1	G3	
H1	H2	
J1	J2	
K1	K2	
L1	L2	
M1	M2	
N1	N3	
P1	P2	
R1	T3	
T1	T2	
U1	U2	
V1	W1	
AA2	Y1	
AB1	AB2	
C2	C3	D4
D3	E2	
F2	F3	
N2	N4	
R2	R3	

BALL No.	BALL No.	BALL No.
V2	V3	
AA3	W2	
W3	Y2	
A20	A3	
B3	C4	
H3	H4	
J3	K3	
L3	L4	
M3	M4	
P3	P4	
U3	U4	
AA4	Y3	
AB20	AB3	
A4	B4	
E4	E5	
F4	G4	
J4	K4	
R4	T4	
V4	W5	
W4	Y4	
AA5	AB4	
A5	C6	
B5	C5	
D5	D6	
W6	Y5	

BALL No.	BALL No.	BALL No.
AB5	AB6	
A6	B6	
AA6	Y6	
A7	C8	
B7	C7	
D7	D8	
H7	J7	
K7	K8	
L7	L8	
M7	N7	
P7	R7	
W7	W8	
Y7	Y8	
AA7	AB7	
A8	B8	
C8	G9	
H8	J8	
M8	N8	
P8	P9	
R8	R9	
T8	T9	
AA8	AB8	
A9	B9	
C10	C9	
D10	D9	

BALL No.	BALL No.	BALL No.
H10	H9	
J10	J9	
K9	L9	
M9	N9	
W9	Y9	
AA9	AB9	
A10	B10	
G10	G11	
K10	K11	
L10	L11	
M10	M11	
N10	N11	
P10	P11	
R10	R11	
T10	T11	
W10	W11	
AA10	Y10	
AB10	AB11	
A11	B11	
C11	D11	
H11	J11	
AA11	Y11	
A12	B12	
C12	D12	
G12	H12	

Figure 57. 385ZWK Daisy Chain Net List

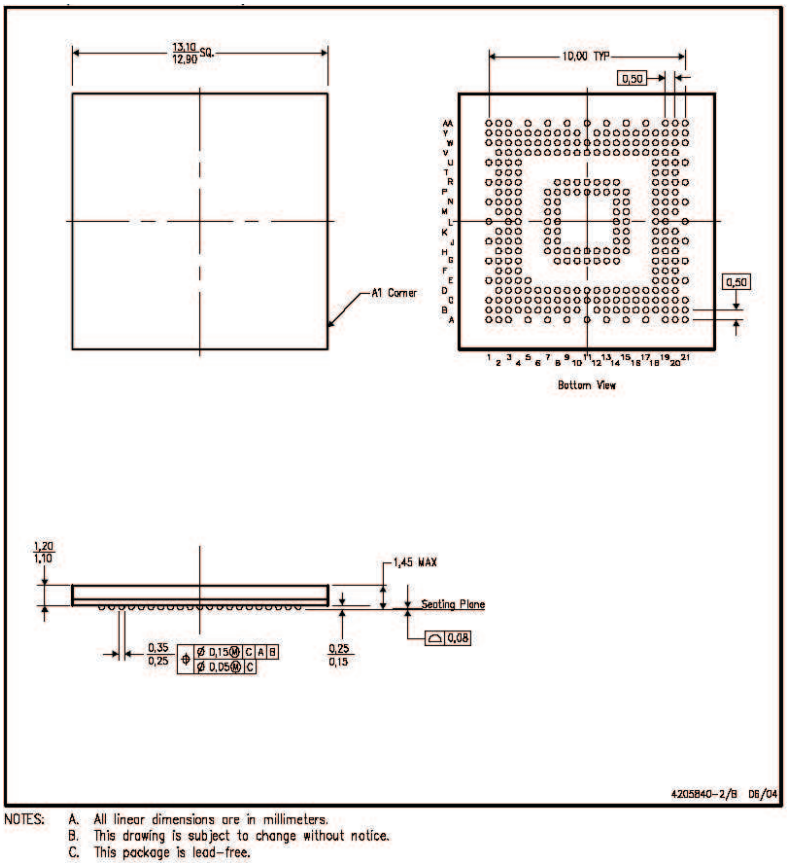
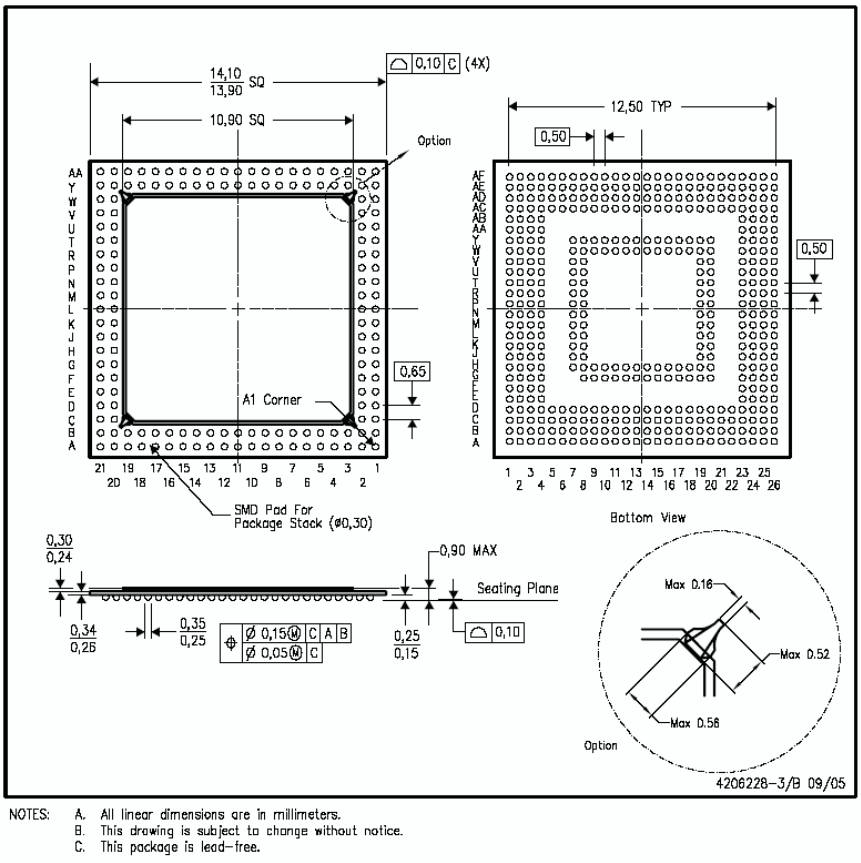


Figure 58. 289ZWE Package Outline (13 x 13mm, 0.5mm pitch)

289ZWE Daisy Chain Net List Not Available



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure 59. 447ZAC Package Outline (14 x 14mm, 0.5mm pitch)

447ZAC Daisy Chain Net List Not Available

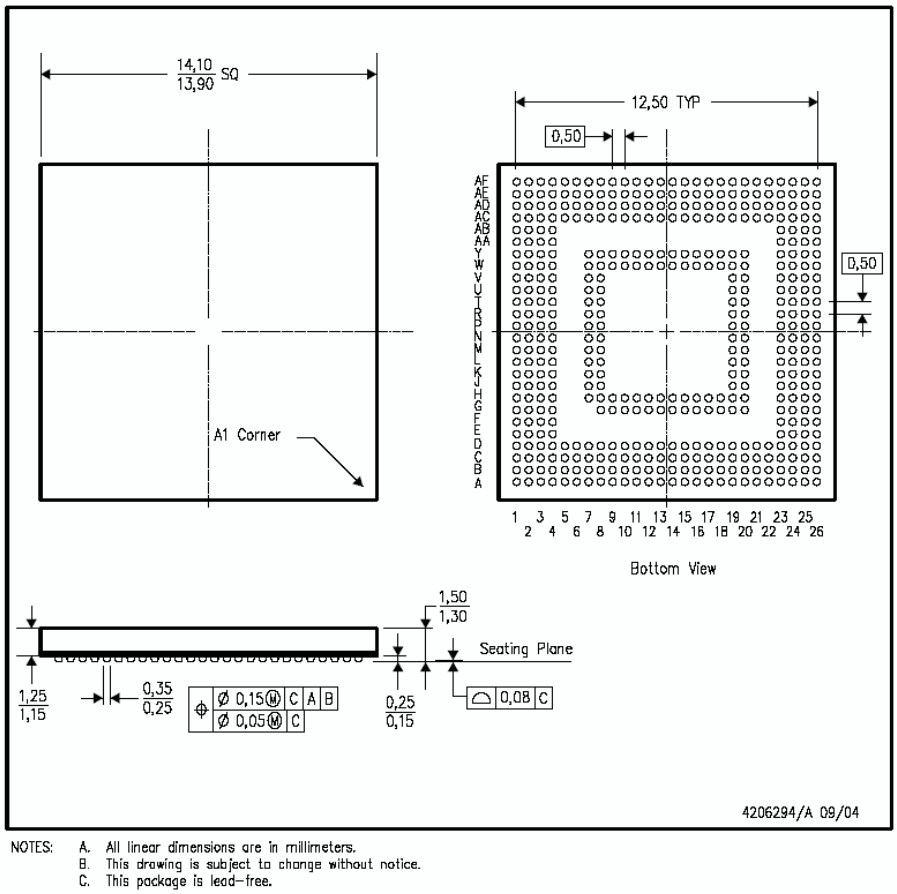


Figure 60. 447ZAF Package Outline (14 x 14mm, 0.5mm pitch)

447ZAF Daisy Chain Net List Not Available

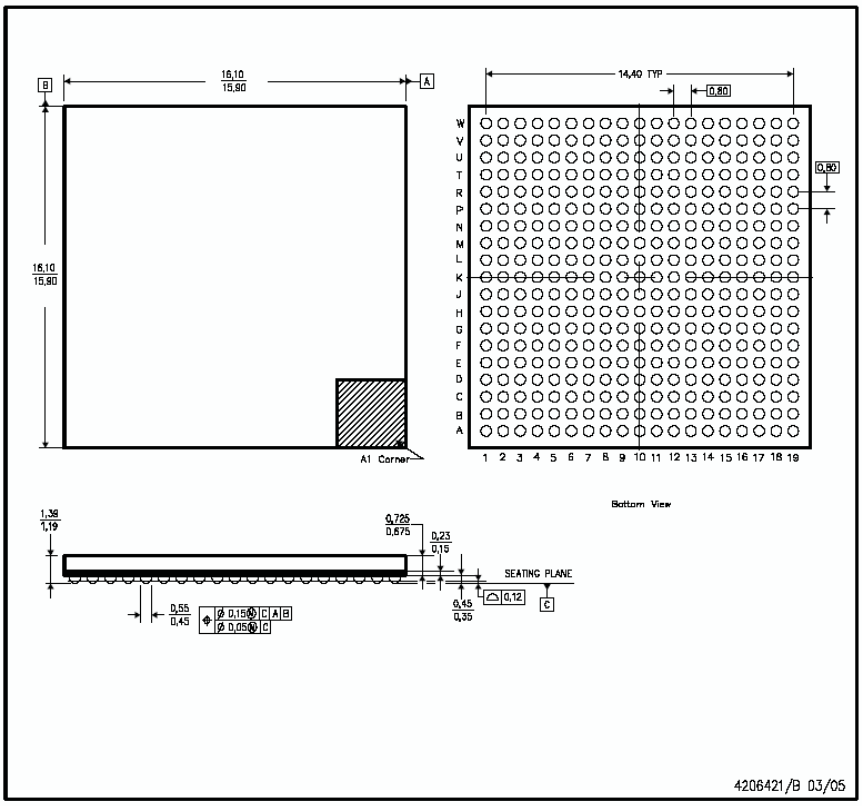


Figure 61. 361ZWT Package Outline (16 x 16mm, 0.8mm pitch)

BALL No	BALL No
A1	B1
C1	C2
D1	D2
E1	F1
G1	G2
H1	H2
J1	K1
L1	L2
M1	M2
N1	P1
R1	R2
T1	T2
U1	V1
A2	A3
B2	C3
E2	E3
F2	F3
J2	J3
K2	K3
N2	N3
P2	P3
T3	U2
U3	V2
W1	W2
B3	C4

BALL No	BALL No
D3	D4
G3	G4
H3	H4
L3	L4
M3	M4
R3	R4
V3	W3
A4	B4
E4	E5
F4	F5
J4	J5
K4	K5
N4	N5
P4	P5
T4	U4
V4	W4
A5	B5
C5	D5
G5	G6
H5	H6
L5	L6
M5	M6
R5	T5
U5	V5
W5	W6

BALL No	BALL No
A6	A7
B6	C6
D6	E6
F6	G7
J6	J7
K6	K7
M7	N6
N7	P6
R6	T6
U6	V6
B7	C7
D7	E7
F7	G8
H7	H8
L7	L8
P7	R7
T7	U7
V7	W7
A8	B8
C8	D8
E8	F8
J8	J9
K8	K9
M8	N8
P8	R8

BALL No	BALL No
T8	U8
V8	W8
A9	B9
C9	D9
E9	F9
G9	H9
L9	M9
N9	P9
R9	T9
U9	V9
W10	W9
A10	A11
B10	C10
D10	E10
F10	G10
H10	J10
K10	
L10	M10
N10	P10
R10	T10
U10	V10
B11	C11
D11	E11
F11	G11
H11	J11

BALL No	BALL No
K11	K12
L11	L12
M11	N11
P11	R11
T11	U11
V11	W11
A12	B12
C12	D12
E12	F12
G12	H12
J12	J13
M12	M13
N12	P13
P12	R12
T12	U12
V12	W12
A13	B13
C13	D13
E13	F13
F14	G13
G14	H13
K13	K14
L13	L14
N13	P14
R13	T13

BALL No	BALL No
U13	V13
W13	W14
A14	A15
B14	C14
D14	E14
H14	H15
J14	J15
M14	M15
N14	N15
R14	T14
U14	V14
B15	C15
D15	E15
F15	F16
G15	G16
K15	K16
L15	L16
P15	P16
R15	R16
T15	U15
V15	W15
A16	B16
C16	D16
E16	E17
H16	H17

BALL No	BALL No
J16	J17
M16	M17
N16	N17
T16	T17
U16	V17
V16	W16
A17	B17
B18	C17
C18	D17
F17	F18
G17	G18
K17	K18
L17	L18
P17	P18
R17	R18
U17	V18
W17	W18
A18	A19
D18	D19
E18	E19
H18	H19
J18	J19
M18	M19
N18	N19
T18	T19

BALL No	BALL No
U18	U19
B19	C19
F19	G19
K19	L19
P19	R19
V19	W19

Figure 62. 361ZWT Daisy Chain Net List

Thermal Modeling Results

Table 11, Table 12, and Table 13 detail thermal modeling results from 8x8mm, 12x12mm, and 16x16mm nFBGA packages, respectively.

Table 11. 8×8 mm nFBGA Thermal Simulation Result

Power = 1w	Die Size (mm)	2.0 × 2.0 mm		4.0 × 4.0 mm		6.0 × 6.0 mm	
	Velocity (m/s)	1S0P	2S2P	1S0P	2S2P	1S0P	2S2P
θJA (°C/W)	0	140.148	101.061	100.476	61.161	89.286	50.352
	1	129.084	97.211	89.269	57.353	78.173	46.554
	2	124.432	96.281	84.656	56.439	73.714	45.622
	3	121.435	95.611	81.895	55.675	70.399	44.774
Pusai JT (°C/W)	0	2.244	2.076	0.625	0.462	0.509	0.342
	1	2.238	2.066	0.582	0.429	0.480	0.308
	2	2.215	2.062	0.559	0.403	0.441	0.290
	3	2.196	2.059	0.545	0.399	0.429	0.278
Pusai JB (°C/W)	0	78.144	80.346	32.656	33.063	20.345	21.658
	1	75.007	77.987	30.032	32.785	18.921	21.539
	2	74.760	77.876	29.997	32.687	18.710	21.437
	3	74.616	77.742	29.733	32.200	18.306	21.380
θJC (°C/W)		29.984	—	12.050	—	7.347	—
θJB (°C/W)		77.056	78.643	31.636	33.043	19.899	21.226

Table 12. 12×12 mm nFBGA Thermal Simulation Result

Power = 1w	Die Size (mm)	3.0 × 3.0 mm		6.5 × 6.5mm		10.0 × 10.0 mm	
	Velocity (m/s)	1S0P	2S2P	1S0P	2S2P	1S0P	2S2P
θJA (°C/W)	0	89.520	62.812	61.940	35.763	53.538	28.380
	1	80.639	59.169	52.553	32.150	44.582	24.786
	2	77.284	58.444	49.596	31.427	41.273	24.032
	3	75.257	57.923	47.675	30.897	39.314	23.518
Pusai JT (°C/W)	0	0.855	0.623	0.373	0.274	0.306	0.216
	1	0.791	0.589	0.356	0.239	0.246	0.183
	2	0.782	0.588	0.321	0.209	0.236	0.176
	3	0.732	0.585	0.300	0.207	0.227	0.156
Pusai JB (°C/W)	0	46352	49.411	15.822	18.310	8.886	10.687
	1	45.699	49.091	15.689	17.954	8.650	10.422
	2	45.553	48.646	15.499	17.922	8.472	10.405
	3	45.483	48.208	15.424	17.903	8.287	10.380
θJC (°C/W)		16.586	—	5.742	—	4.428	—
θJB (°C/W)		46.695	47.787	15.894	16.429	8.180	8.604

Table 13. 16×16 mm nFBGA Thermal Simulation Result

Power = 1w	Die Size (mm)	3.0 × 3.0 mm		8.5 × 8.5mm		14.0 × 14.0 mm	
	Velocity (m/s)	1S0P	2S2P	1S0P	2S2P	1S0P	2S2P
θJA (°C/W)	0	88.870	69.542	48.861	27.847	39.056	21.145
	1	81.509	66.538	69.164	24.125	31.690	17.579
	2	79.283	65.851	36.777	23.404	28.913	16.870
	3	77.860	65.395	35.387	22.974	27.514	16.410
Pusai JT (°C/W)	0	0.888	0.820	0.290	0.355	0.237	0.181
	1	0.828	0.755	0.226	0.280	0.177	0.103
	2	0.808	0.740	0.225	0.155	0.164	0.099
	3	0.801	0.737	0.218	0.153	0.159	0.098
Pusai JB (°C/W)	0	59.993	61.429	11.901	12.620	5.252	5.523
	1	59.895	61.026	11.667	11.925	5.231	5.470
	2	59.349	59.877	11.270	11.591	4.806	5.267
	3	59.284	59.842	11.176	11.584	4.776	5.104
θJC (°C/W)		20.002	—	3.797	—	1.853	—
θJB (°C/W)		57.658	58.886	10.183	10.717	4.898	5.158

Revision History

Changes from A Revision (September 2015) to B Revision	Page
• Updates were made in Section 2.2.	7

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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