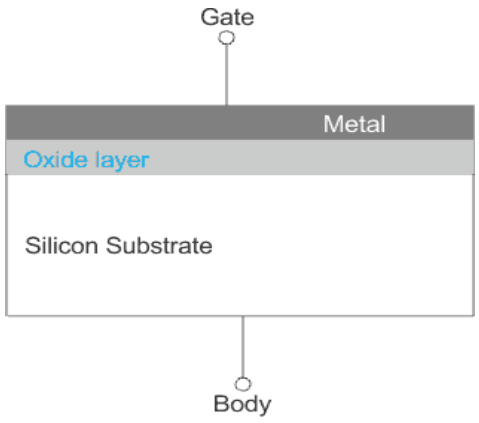
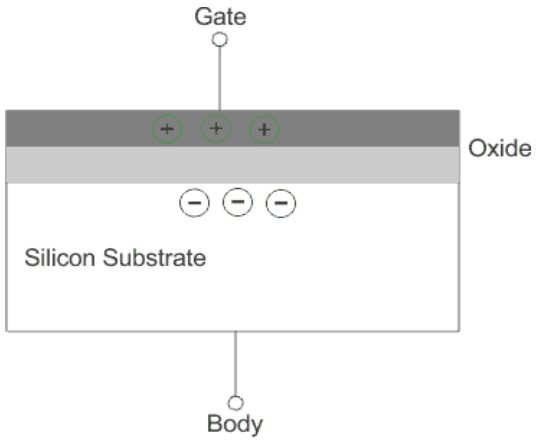
MOS Capacitor | MOS Capacitance C V Curve

The acronym MOS stands for Metal oxide semiconductor. An **MOS capacitor** is made of a semiconductor body or substrate, an insulator and a metal electrode called a gate. Practically the metal is a heavily doped n+ poly-silicon layer which behaves as a metal layer. The dielectric material used between the capacitor plates is silicon dioxide (SiO2). The metal acts as one plate of the capacitor and the semiconductor layer which may be n-type or p-type acts as another plate.



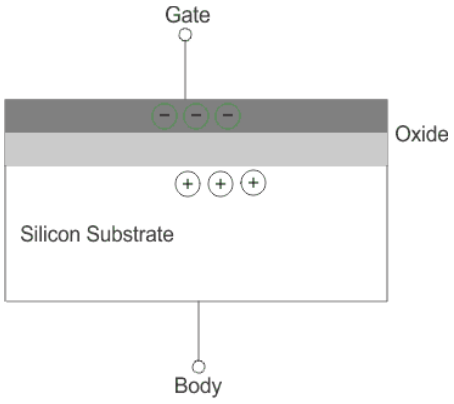
MOS capacitor structure

The capacitance of the MOS capacitor depends upon the voltage applied on the gate terminal. Usually the body is grounded when the gate voltage is applied. The flat band voltage is an important term related to the MOS capacitor. It is defined as the voltage at which there is no charge on the capacitor plates and hence there is no static electric field across the oxide. An applied positive gate voltage larger than the flat band voltage ($V_{gb} > V_{fb}$) then positive charge is induced on the metal (poly silicon) gate and the only negative charged electrons are available as negative charges and they accumulate at the surface. This is known as surface accumulation.



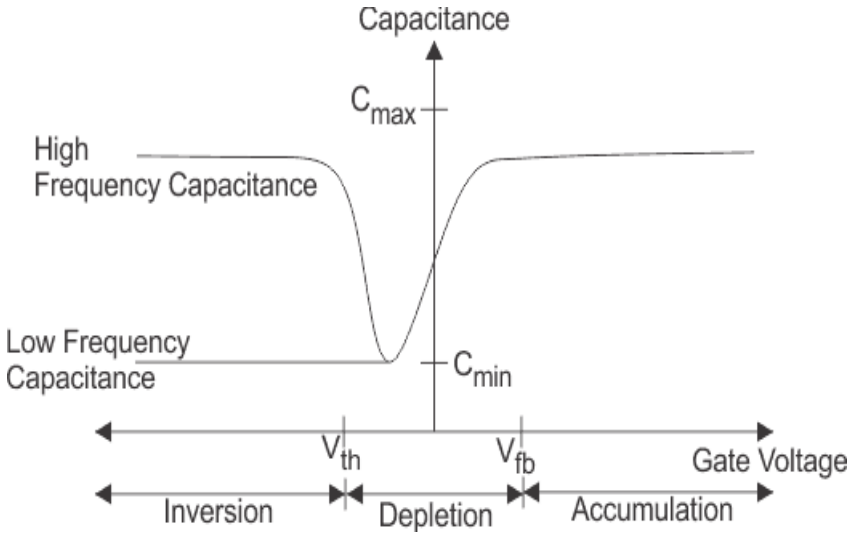
MOS capacitor structure

If the applied gate voltage is lower than the flat band voltage ($V_{gb} < V_{fb}$) then a negative charge is induced at the interface between the poly-silicon gate and the oxide and positive charge in the semiconductor.
This is only possible by pushing the negatively charged electrons away from the surface exposing the fixed positive charges from donors. This is known as surface depletion.



MOS capacitor structure

The **MOS capacitor** is not a widely used device in itself. However, it is part of the MOS transistor which is by far the most widely used semiconductor device. The typical capacitance-voltage characteristics of a MOS capacitor with n-type body is given below,



Capacitance vs. Gate Voltage (CV) diagram of a **MOS Capacitor**. The flatband voltage (V_{fb}) separates the Accumulation region from the Depletion region. The threshold voltage (V_{th}) separates the depletion region from the inversion region.

1) What is MOS capacitor?

A) A MOS capacitor also known as a Metal oxide semiconductor capacitor, it is a device used in integrated circuits. IT consists of material electrode (M) an insulating layer of oxide (O), and a semiconductor substrate(S). The MOS capacitor is used to store charge and control the flow of current in MOSFET devices.

2) What is MOSFET?

A) A MOSFET is a type of transistor commonly used in electronic circuits. It consists of a gate source and a channel. The MOSFET operates by applying a voltage to the gate which controls the flow of current between the source and drain. It is widely used for amplification, switching, and other electronic functions.

3) How does a MOS capacitor work?

A) A MOS capacitor works by applying a voltage to the metal electrode (gate) and creating and electric field within the gate and creating an electric field with in the insulating oxide layer. This electric field attracts or repels charges in the semiconductor substrate, forming a depletion region. By modulating the voltage applied to the gate, the width o the depletion region and the amount of charge stored in the capacitor can be controlled.

4) What are the applications of MOS capacitors?

A) MOS capacitors find various applications in integrated circuits and microelectronics. They are commonly used in memory devices, such as DRAM (dynamic random access memory) and flash memory. MOS capacitors are used in analog circuits for voltage controlled oscillators, filters and voltage references.

5) What are the different types of capacitances in a MOSFET?

A) There will be five capacitances: Cgs, Cgd, Cgb, Csb and Cdb where the subscripts indicate the terminals

Cgs=Capacitor across gate and source

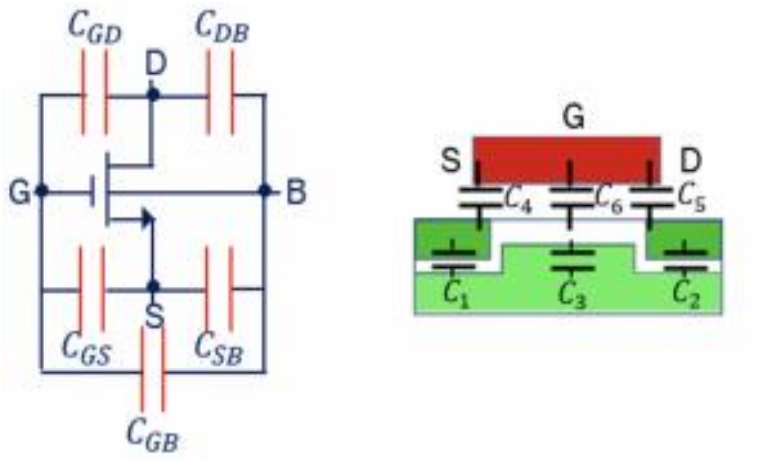
Cgd= Capacitor across gate and drain

Cgb= Capacitor across gate and bias

Csb= Capacitor across source and bias

Cdb= Capacitor across drain and bias

The above figure shows the capacitors of Cross-section view and the top view of typical n-channel MOSFET.



6) What is MOS capacitor threshold voltage?

A) A MOS capacitor can be in three regions accumulation, depletion, and inversion. The boundary between accumulation and depletion is flat-band voltage and the boundary between depletion and inversion is the threshold voltage.

7) What is MOS capacitor threshold voltage?

A) MOSFET threshold voltage is defined as the gate voltage at which significant current starts to flow from the source to the drain.

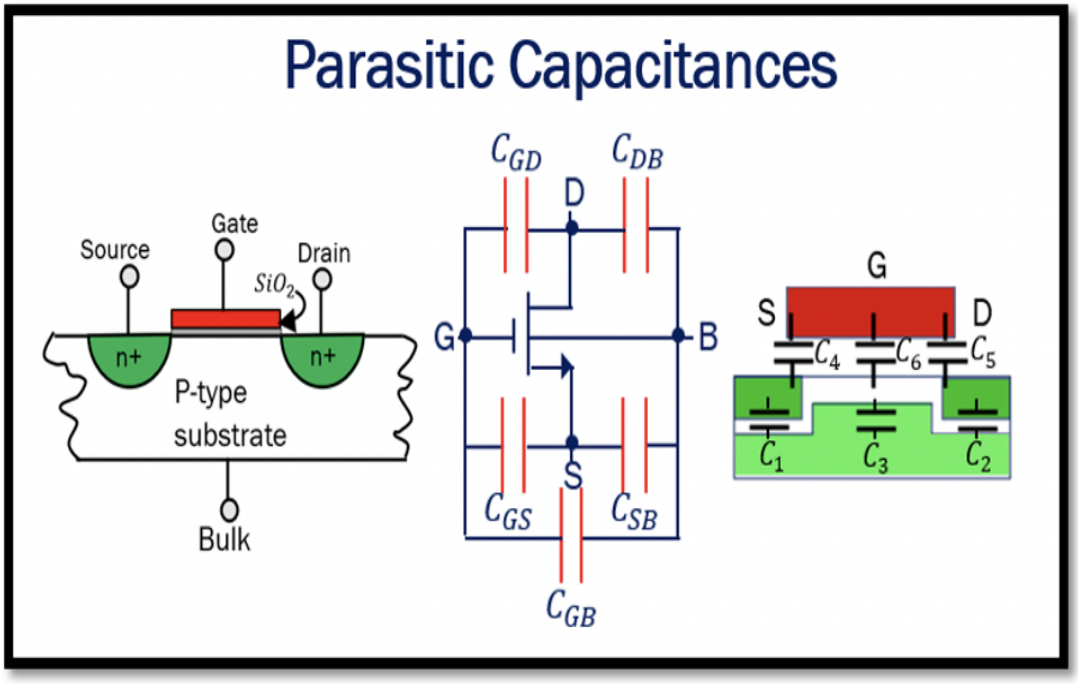
(Or)

The threshold voltage, commonly abbreviated as V_{th} or $V_{GS(th)}$, of a field-effect transistor (FET) is the minimum gate-to-source voltage (V_{GS}) that is needed to create a conducting path between the source and drain terminals.

8) List the three regions of MOS capacitor

A) Accumulation
Depletion
Inversion

Explain different parasitic capacitances of MOSFET (or) Explain different capacitances in MOSFET



MOS Transistor parasitic capacitances are formed due to the separation of mobile charges at various regions within the structure. Parasitic Capacitances are the unwanted component in the circuit which are neglected while working in low-frequency. But cannot be avoided when working in high-frequency RF circuits; therefore, we have to be careful about parasitic capacitance while designing.

The impedance for capacitance is 1/jcw. For low frequency, it is considered infinity; hence it is open and doesn't affect the circuit. However, when the frequency increases, the capacitance in the circuit behaves like an impedance, and it can change the behaviour of our transistor by limiting its speed. Hence, the transistor has limits while working with high frequencies.

These capacitances are formed within the transistor due to its arrangement. As you can see from the transistor's cross-section, the C1 capacitance is formed due to the depletion regions—the depletion region around forms separation between bulk and source. In the same way, there is capacitance C_2 due to separation between bulk and drain. As there is an n-type and p-type semiconductor, they are the depletion capacitances. These depletion capacitances are a drain to bulk C_{DB} and source to bulk C_{SB}.

Looking closely into the MOSFET structure, we could see an overlap at the gate metal oxide and source region edges. When voltage V_{gs} is applied, charges get accumulated at this region, forming a capacitance (C_4/C_{GS}), similar to the parallel plate capacitor where the lower plate is source region n+ type (NMOS) and the upper plate is metal. Similarly, a capacitance (C_5/C_{GD}) is

formed between gate metal oxide and drain region. They are called overlap capacitance. C_3 & C_6 are formed between the gate and substrate. The capacitance that is from channel to bulk depends on the state of the substrate. The capacitance from gate to bulk C6, there is an oxide layer as we know. This capacitance can be between gate and channel and between channel and bulk (C3). C_{GB} represents this capacitance.