DIGANTARA

Assessment: Junior FPGA Design Engineer

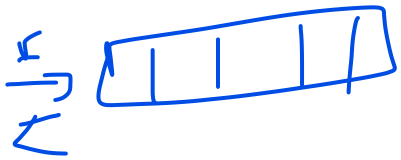
Hello,

Greetings of the day!

UART Packetizer with FSM and FIFO Integration

Question 1: Design a digital system which accepts parallel data packets and transmits them serially over a UART-like interface. The digital logic design of the system shall include the RTL development of the following modules.

1. A Packetizer FSM.
2. An asynchronous FIFO buffer.
3. A UART-like serial output block.
4. A top module interconnecting the above three modules.



System Description:

This module receives 8-bit data words from an external data source and stores them in a FIFO. An FSM reads from this FIFO and generates a serial stream with a custom protocol as described below.

Functional Requirements:

- Data width: 8 bits.
- Baud Rate: Parameterizable (e.g., 9600, 115200).
- Start bit: 1 (logic low).
- Stop bit: 1 (logic high).
- No parity or flow control.

Inputs:

- clk: System clock (50 MHz)
- rst: Active-high synchronous reset
- data_in[7:0]: Incoming data byte
- data_valid: Pulse when new data is valid
- tx_ready: Indicates external receiver is ready i.e., to simulate handshaking.

Outputs:

- serial_out: Serial output line
- fifo_full: High when FIFO is full
- tx_busy: High while transmission is in progress

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Module level requirements:

1. **FIFO Buffer:**
    - Depth: 16.
    - Asynchronous or synchronous FIFO.
    - Provide fifo_full, fifo_empty, and data_out_valid signals.
2. **FSM Logic steps:**
    - Detects when FIFO non-empty.
    - Waits for tx_ready signal.
    - Reads FIFO.
    - Transmits 10-bit packet via serial_out bit by bit.
    - Returns to IDLE when done.

Considering the above description, provide the following.

a) Design VHDL/Verilog RTL code for the modules.

b) Develop a simulation testbench and provide the following results.

1. FIFO write and read.
2. Serial output waveform along with fifo_full and tx_busy signals.
3. At least 2 valid packets with proper framing.
4. FSM state transitions.

c) Generate documentation with following details

1. FSM state diagram along with state transitions.
2. FIFO usage explanation.
3. Rational for synchronous/asynchronous FIFO.

Question 2

a) Carry out synthesis, place and route on AMD-Xillinx Vivado tool with a target FPGA from chosen from Kintex/Virtex family of FPGAs?

b) Provide the synthesis and timing reports generated by AMD-Xillinx Vivado tool.

c) Report the resource utilization and achieved maximum operating clock frequency at Synthesis level and post-place and route level?

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d) Describe the encoding technique is used in the FSM implementation. Provide a tool generated report indicating the type of encoding technique used for FSM implementation.

e) Propose techniques to increase the maximum operating frequency of the RTL modules developed in question 1.

Note:

- Send the response as a zip file with clear instructions on how to open the file.
- Assume necessary parameters for implementing the above RTL modules and list the assumptions at the relevant sections.
- Well-structured and clean RTL code will earn brownie points.
- Open-source RTL modules shall not be utilized and strongly discouraged.
- Avoid generic answers.
- Provide the response within five pages, excluding the source code and support files.

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