Review on Low Power Designing in VLSI Chips and Analysing Power Dissipation Trends over a Decade of Processor generations

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***Abstract*— Reducing power consumption is an indispensable quest in our modern world. With the ever-present need for portable devices like smartphones and laptops, minimizing energy usage dissipation has become a central challenge. This pressing concern has driven the development of innovative techniques to curb power loss in Very-Large-Scale Integration (VLSI) chips, the workhorses of modern electronics.**

While CMOS technology offers scaling advantages and inherently low static power dissipation, challenges persist. Despite significant increases in transistor count and operating frequency, modern processors grapple with leakage currents similar to their decade-old counterparts. Understanding the various power dissipation mechanisms However, the pursuit of ever-smaller, faster, and lower-power chips necessitates a delicate balancing act between power consumption, performance, and chip area. This paper explores the multifaceted problem of power dissipation in CMOS circuits, delving into both dynamic and static power sources .

This review underscores the critical role of low-power design in shaping the future of VLSI technology.

***Keywords*— low power dissipation, VLSI chips, CMOS, low power designing, dynamic power, Static power leakage, processor .**

I. INTRODUCTION

The ever-growing demand for portable and battery-powered electronics has thrust low-power design into the spotlight of VLSI development. While CMOS technology boasts excellent scaling properties and inherently low static power dissipation, challenges remain. This progress comes with a significant challenge: power dissipation[13]. Despite vast increases in transistor count and operating frequency, modern processors like the 14th generation Core i7 exhibit comparable leakage currents to their predecessors from a decade ago [5]. Before we jump to the concepts of how to reduce power dissipation, we must first discuss the various types of power dissipations that exist. Understanding these sources and their influence on factors like frequency is paramount in crafting power-efficient VLSI chips. Understanding these sources and their impact on frequency is essential for designing power-efficient VLSI chips.

II. POWER DISSIPATION

Power dissipation remains a critical challenge in achieving high integration levels in VLSI design [2] While CMOS technology offers excellent scaling properties and low power consumption, understanding the various power dissipation mechanisms is crucial for efficient circuit .This research explores the two main contributors to power dissipation in CMOS circuits: dynamic and static power.[1]

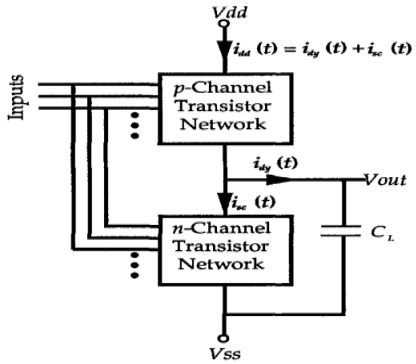

Figure 1: CMOS (Combination of PMOS and NMOS)

A. Dynamic Power

This component arises from charging and discharging the load capacitance *(C_L)* during signal transitions. It is primarily influenced by C_L, supply voltage *(V_{DD})*, activity factor (α, representing the average switching frequency), and clock frequency *(f)* [14]. The formula

$$P_{dyn} = C_L \times (V_{DD})^2 \times \alpha \times f$$

captures this relationship. [2][6][4]

1) Switching Power Dissipation

Switching power dissipation is a critical factor limiting battery life and necessitating low-power design approaches in VLSI circuits. It arises from the charging and discharging of the capacitive load at the output of each logic gate during transitions between logic states [1]. The exact value of this load capacitance depends on several parameters, including the fan-out of the gate, its output capacitance, and the wiring capacitances involved [7]. These parameters are all influenced by the underlying fabrication technology generation.

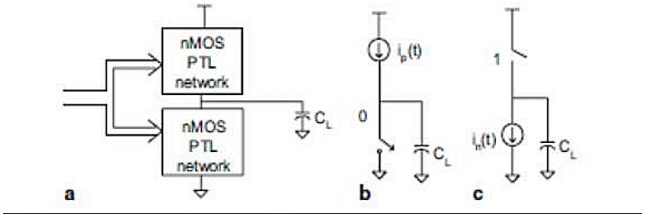

Figure : 2 Switching power dissipation model

A simplified model (Figure 2a) can be used to estimate the switching power dissipation. Consider a standard CMOS inverter driving a load capacitance *(C_L)* . As the input to the inverter changes, the PMOS or NMOS network conducts accordingly, charging or discharging the capacitor (Figures 2b and 2c). During charging (from low to high), power is drawn from the supply to accumulate energy in the capacitor. Conversely, power is dissipated during discharging (from high to low).

$$P_{average} = (1/T).(C_{load}).(V_{dd})^2 \qquad (1)$$

$$P_{average} = (f).(C_{load}).(V_{dd})^2 \qquad (2)$$

While a basic formula (Equation 1 or 2) can be derived based on load capacitance, supply voltage *(V_{DD})*, and operating frequency *(f)*, it assumes only one transition per clock cycle. In reality, logic gates can experience multiple transitions, necessitating a more nuanced approach.

$$P_{average} = (\alpha_T).(f_{clk}).(C_{load}).(V_{DD}) \qquad (3)$$

The concept of the node transition factor *(α)* is introduced to account for the actual number of transitions occurring at each clock cycle. This refined formula (Equation 3) provides a more accurate estimate of switching power dissipation.

$$P_{average} = \sum[(\alpha_{Ti}).(C_i).(V_i)].(f_{clk}).(V_{DD}) \qquad (4)$$

Furthermore, for complex logic gates, internal nodes besides the output can also undergo transitions during operation. To account for this, a more comprehensive formula (Equation 4) considers the capacitance *(Ci)*, voltage *(Vi)*, and transition factor *(αTi)* of each individual node[14]. The summation across all nodes provides a more holistic picture of switching power dissipation in VLSI circuits.

By understanding and optimizing switching power dissipation through techniques like voltage scaling, designers can achieve significant power reduction in VLSI chips, leading to longer battery life and improved performance in portable electronic devices.

2)Glitching Power

Beyond switching activity and short-circuit power, glitching power dissipation presents another hurdle in achieving low-power VLSI design. Glitches refer to unwanted, transient voltage fluctuations at the output of a logic gate. These glitches occur due to imbalances in the propagation delays of various input signals within a combinational circuit [1,4].

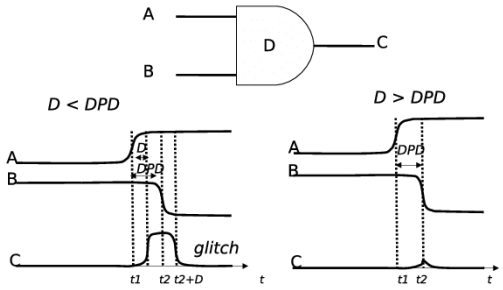

Figure 3: Glitch power dissipations

In The figure a glitch power dissipation curve (1). It depicts the power dissipated by a glitch in a transistor circuit. The x-axis represents time (t), while the y-axis represents power dissipation (D).

The curve shows a voltage glitch, which is a short-duration unintended voltage spike that occurs on a signal line. The glitch causes a surge in power dissipation (DPD) that lasts for a short period (t1 to t2) before settling back to zero [3]. The curve suggests that the higher the glitch amplitude (the difference between A and B), the greater the surge in power dissipation.
Glitch power dissipation is a significant concern in low-power circuit design. Minimizing glitches can substantially reduce the overall power consumption of a circuit.

3)Short-Circuit Power Dissipation

Beyond switching and glitching power, short-circuit power dissipation emerges as another challenge in achieving low-power VLSI design. This phenomenon arises due to the finite rise and fall times of input signals in CMOS logic gates. During these transitions, a brief period exists where both the PMOS and NMOS transistors are partially ON simultaneously [8] . This creates a direct path between the power supply (V_{DD}) and ground (GND), leading to a surge in current flow.

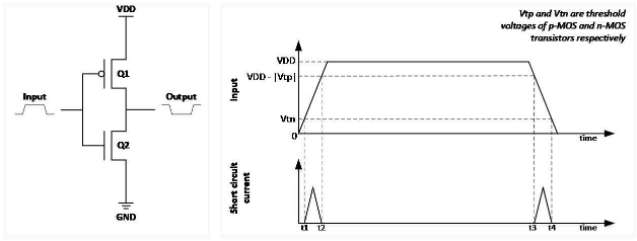

Figure 4: Short circuit leakage current

Figure (4) depicts a CMOS inverter, where short-circuit current occurs when the input voltage lies between the threshold voltages of the PMOS and NMOS transistors [6].Short circuit power is given as

$$P_{ac} = V_{DD}I_{mean} = (\beta/12).(V_{DD} - 2V_t)^3 \, \tau.f \qquad (5)$$

As the clock frequency decides how many times the output changes per second, the short-circuit power is proportional to the frequency. The short- circuit current is also proportional to the rise and fall times. Short-circuit currents for different input slopes are shown in Fig. 5

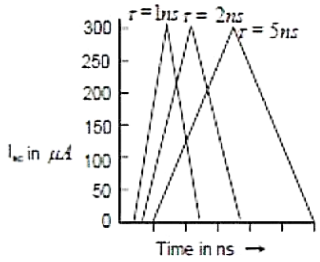

Figure: 5 Short circuit current as a function of input rise/fall time

To estimate this current, a simplified model (Figure 5) can be employed. Here, τ represents the rise and fall times of the input (assumed to be equal), and the inverter is considered symmetrical.

Short-circuit power dissipation is influenced by several factors. Clock frequency plays a crucial role, as it determines the number of output transitions per second, directly impacting the short-circuit current. Additionally, the rise and fall times of the input signal are proportional to the short-circuit current.

Power supply scaling offers a significant advantage in mitigating short-circuit power due to the cubic dependence of the current on V_{DD}. However, there are trade-offs to consider.[1] While increasing the load capacitance (C_{load}) reduces short-circuit current, it also slows down the circuit. A well-balanced approach involves designing for equal input and output slopes.

B. Static Power (Leakage Power)

A Growing Threat in Low-Power VLSI Design. Unlike the previous three components, static power is continuously dissipated even when the circuit is inactive.[1] Leakage currents, influenced by V_{DD}, threshold voltage (V_t), and transistor size, are the primary culprits. As process technology scales, leakage becomes a more significant concern, potentially consuming over 30% of total power [2].

Traditionally, dynamic power dissipation caused by circuit activity has been a primary focus in low-power VLSI design. However, with the miniaturization trend leading to deep-submicron devices, static leakage power is emerging as a significant and growing concern [6].

There is reduction in static power dissipation [5] with each passing year, as depicted in Figure 6

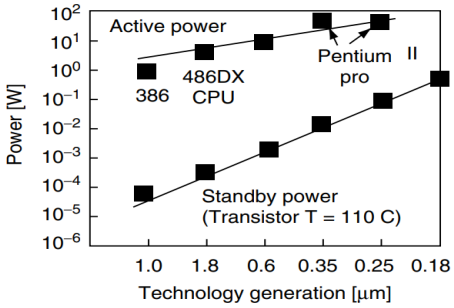

Figure 6: Static Power Evolution with Respect to Technology

Some key leakage components include:

1.Reverse-bias junction leakage: Leakage currents flow through the reverse-biased junctions formed by transistors, even when they are off. [10,12] In deep-submicron devices, tunnelling effects can further exacerbate this leakage.

2.Subthreshold leakage: When the gate voltage *(V_{gs})* is lower than the threshold voltage *(V_t),* a small current persists between the source and drain of the transistor. This leakage becomes more significant as the threshold voltage is scaled down for performance reasons [9].

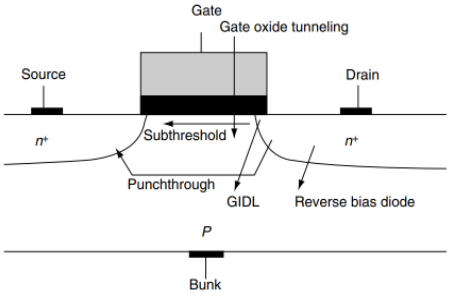

Figure 7: The Different Sources of Leakage Current in MOS Transistors

While these individual leakage currents may seem negligible, the cumulative effect across millions of transistors in a VLSI chip can be substantial[12].This highlights the growing importance of static leakage power in the overall power consumption profile of modern circuits.

Mitigating static leakage power remains a critical aspect of achieving energy-efficient VLSI design, particularly for battery-powered portable devices.

III. COMPARING PROCESSORS OVER A DECADE (i7 4th Gen. VS i7 14th Gen.)

Core i7 processor is a state-of-the-art processor and is the latest and fastest processor present today. The i7 4th Generation the processor had an operational voltage of 1.72V while having 2.6 billion transistors, and base frequency of 3.4 GHz had a leakage current of 150μA. But after a decade of development, the i7 14th gen. having over 48 billion transistors, while maintaining low/same leakage current. This low power dissipation in the processor was achieved using low power designing techniques like pipelining, parallel processing and clock gating, when scaling the no. of transistor by such a high factor. [6] Also, the clock speed has been increased to 4.3 GHz which is expected to also increase in the transition factor hence producing a larger power dissipation. This would not be possible without dynamic voltage frequency scaling.

But these techniques have their own cons. Reduction of drawn length leads to a reduced distance between the source and the drain, leading to loss of control of the transistor. Also, using 20 times the number of transistors while keeping the chip area the same leads to a significant increase in the parasitic capacitance and glitching (which in turn leads to an increase in power dissipation)[13]. While reducing power supply voltage can reduce the electric field, it also reduces the overall performance of the chip. While processors control voltage ramp rates internally to ensure glitch-free transitions, low-power designing and related methods are therefore essential for overcoming these shortcomings [11]

IV. CONCLUSION

Despite the growing concern of static power dissipation in scaled technologies, demanding further exploration of leakage reduction techniques, the evolution of processors like the Core i7 series exemplifies the effectiveness of low-power design. This review has explored the various mechanisms of power dissipation and the low-power design techniques that can mitigate them. Techniques like voltage scaling, logic optimization, and clock gating offer significant reductions in dynamic power even with substantial increases in transistor count and operating frequency.

However, as with all design considerations, there are trade-offs. While low-power design approaches achieve

impressive results, the pursuit of ever-smaller, faster, and lower-power chips presents a complex challenge. We are constantly pushing the boundaries of silicon technology, and alternative materials like Gallium Arsenide [1] are being explored for their potential benefits.

The future of low-power VLSI design lies in striking a delicate balance between power, performance, and area. Techniques like dynamic voltage and frequency scaling (DVFS) [11] offer promising avenues for managing power consumption while maintaining performance. However, long-term solutions may necessitate entirely new technologies that can deliver superior power efficiency without compromising performance or area constraints. By continuously exploring innovative design techniques and fostering a deep understanding of power mechanisms, we can create energy-efficient chips that meet the ever-growing demands of modern computing while ensuring a sustainable future.

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