Low Power designing in VLSI chips

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***Abstract*— Reducing power consumption is an indispensible subject in today's world. In today's scenario, reducing power consumption is the key challenge. The increasing need and usage of portable devices such as cell phones, laptops etc and the need to decrease power usage and power loss has led to an inclination towards development of new techniques to curb this problem. This paper discusses the various causes of power dissipation in VLSI chips, and reviews all the strategies and methodologies that can be applied for low power designing. A comparison between the 4004 processor and the core i7 processor has also been drawn to throw light on the practical need for low power designing and where it has led us to as of now.**

Keywords—low power dissipation; VLSI chips; CMOS; low power designing; processor

I. INTRODUCTION

Power and its consumption are the primary concerns due to the lavish growth and success of person specific computing devices and wireless. Due to this, low power designing continues to increase at an alarming rate. Hence, apart from area and performance issues, power consumption is a new, but crucial addition to the already long list of problems. The development of processors with better and more functionality continues to take place, with core i7 processor being the latest. But the issue of power consumption is still intact. Before we jump to the concepts of how to reduce power dissipation, we must first discuss the various types of power dissipations that exist in a conventional CMOS logic circuit. Several high level performance digital circuit designs that emphasize on low-power and low-voltage operation have been introduced. These circuits act as great examples for low-power design [4].

II. SWITCHING POWER DISSIPATION

The switching power dissipation is defined as the power dissipated/lost during transition. This power dissipation is the most common form of power dissipation that exists in digital circuits [2]. The figure 1 depicts a combination of a PMOS and NMOS. The VDD and ground are also depicted. At the output, we take a capacitor(C load).

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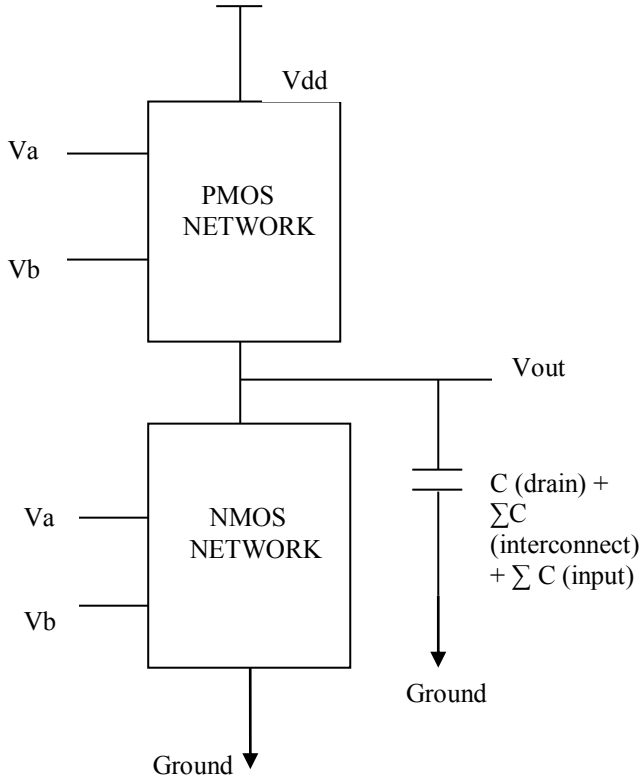

Fig.1 Combination of PMOS and NMOS.

The power dissipated is stated as:

$$P_{average} = (1/T).\ (C_{load}).\ (V_{DD})^2 \quad (1)$$

Also, (1) can be written as:

$$P_{average} = (f).\ (C_{load}).\ (V_{DD})^2 \quad (2)$$

In (2)," f" is the switching frequency (1/T) [1]. But, the above expression for switching power is true only when there exists one and only one transition in each clock cycle .But, this is not always true. Hence, we consider a new factor represented by alpha, called node transition factor, which is the actual number of power consuming transitions on every clock cycle. Hence, the new expression is given by:

$$P_{average} = (\alpha_T).\ (f_{clk}).\ (C_{load}).\ (V_{DD}) \quad (3)$$

But, the 'C load' is not complete in itself. In reality, in case of complex CMOS logic gates, most of the circuit nodes also undergo transitions during switching. Taking this factor into consideration:

$$P_{average} = \sum [(\alpha_{Ti}).(C_i).(V_i)].(f_{clk}).(V_{DD}) \quad (4)$$

Here, in (4) the capacitance, voltage and the transition factor of each node is considered to obtain the final switching power dissipation. The summation is taken from i=1, to i= Number of nodes.

III. Short Circuit Power Dissipation

During the switching process, there exists some current which passes through both the PMOS and the NMOS. This current does not contribute towards charging the load capacitor(C load). Hence, this current is known as short circuit current. In the figure 2 the input/output voltage waveforms and the short circuit current are shown.

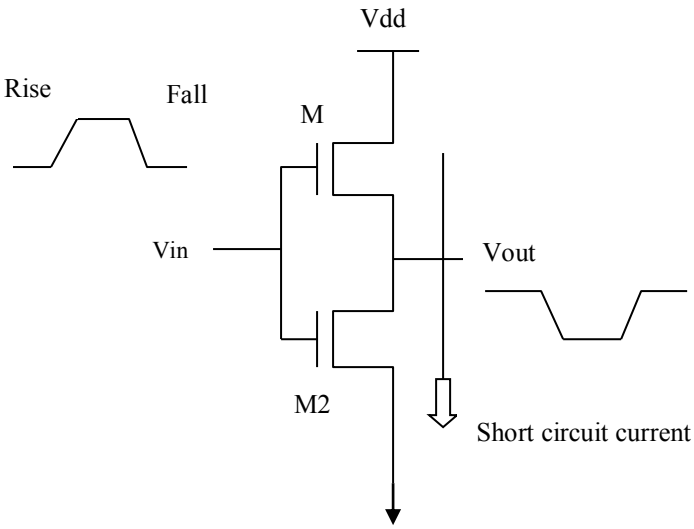

Fig.2 the input/output voltage waveforms and the short circuit current.

The short circuit current occurs if the load capacitor(C load) is small and/or when the gap between the rise time and fall time is very large. The representation of a similar case is show in figure 3. The figure shows the input and output voltages, the supply and the short circuit current. The large amount of short circuit current represents a large amount of short circuit power dissipation.

Let us consider a CMOS inverter with threshold voltages of both PMOS and NMOS to be equal, and with a very small load capacitance. Considering equal rise and fall times, the average short circuit current with respect to time is given by (5):

$$I_{average}\ (short\text{-}circuit) = (1/12).((k.f_{clk}.\mu)/V_{DD}).(V_{DD} - V_T)^3 \quad (5)$$

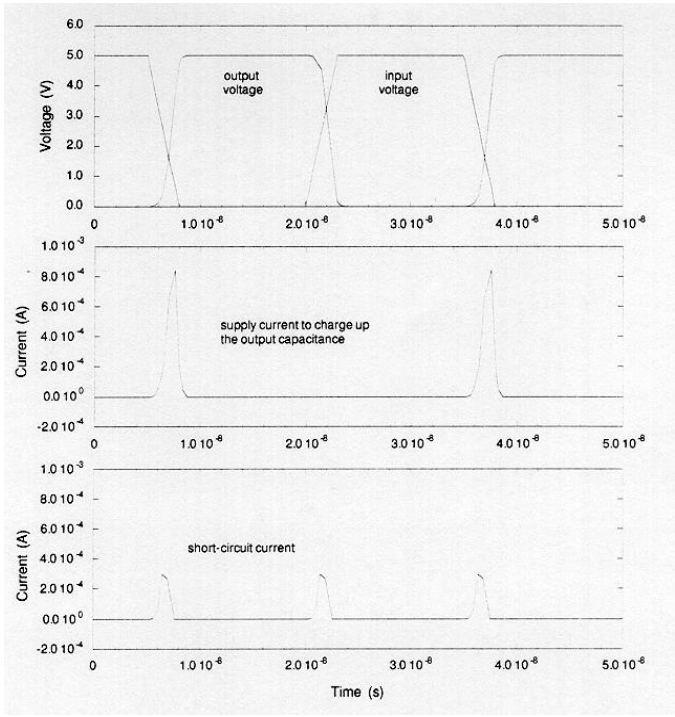

Fig.3 Effects of Short Circuit Power Dissipation [4]

lso, if we increase the load capacitance and decrease the input transition times, the short circuit current decreases and hence, the short circuit power is affected as shown in figure 4.

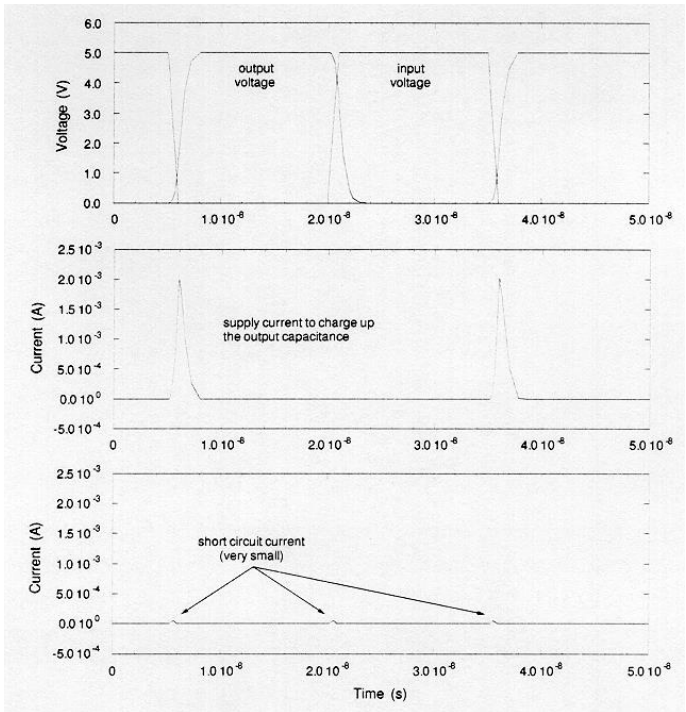

Fig.4 Reduced effects of Short Circuit Power Dissipation. [4]

IV. Leakage Power Dissipation

The CMOS logic gate have two leakage currents, which are: Reverse diode leakage current and sub threshold current.

Individually, these currents are very small to be considered as a source of power dissipation .But, a VLSI chip has many CMOS logic gates. Hence, all the leakage currents together contribute to the power dissipation.

The reverse leakage current occurs due to reverse biased p-n junction. The reverse biased pn junction gives rise to a reverse saturation current, which is drawn from the power supply. This current is called the reverse saturation current. The reverse leakage current (I rev) of a pn junction is:

$$I_{reverse} = A.J_S.(e^{(q.Vbias)/(k.T)} - 1) \quad (6)$$

Here, V bias is the reverse bias voltage, Js is the reverse saturation current density and A is the junction area. Also, reverse leakage current increases as the temperature increases.

The second part of the leakage current is the sub threshold current. This current occurs due to carrier diffusion during the sub threshold region / weak inversion region. This region occurs when the gate voltage (Vgs) is lesser than the threshold voltage (V t), but close to it. [1]

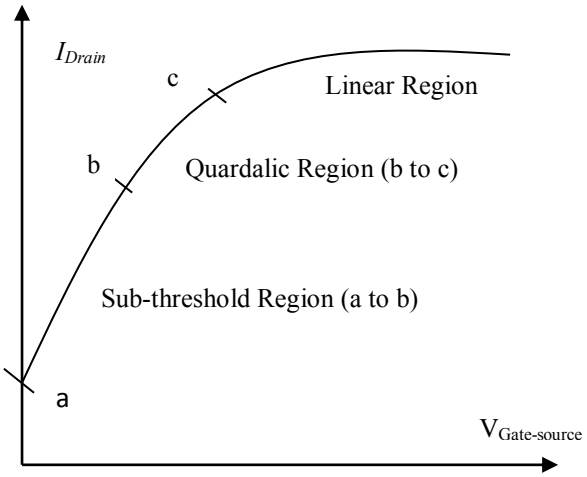

Fig.5 The various regions in a MOSFET

V. Techniques For Low Power Designing

A. Voltage

One technique that can be used for low power designing is to reduce the supply voltage. However, as VDD becomes lower, the performance and the ability to perform multiple functions reduce. For the performance at low VDD to be consistent, there are three techniques: (a) utilizing parallel and/or pipeline architectures to compensate for the reduced speed. In case of pipelining, each task is divided into various segments, all being a part of the same pipeline. Hence, the overall speed of performance is increased. (b) Lowering the threshold voltage, VTH and (c) lower V DD only for non-critical circuits. In the (b) technique the supply and threshold voltages should be optimized according to speed requirement. In case of (c), they should be altered from circuits to circuits [5].

B. Capacitance

External memory access consumes considerable power dissipation due to large parasitic capacitance along external signal lines. Embedding external memory on a chip reduces system power dissipation considerably [5].

C. Switching Activity

The switching activity involves the clock frequency and E (sw), which is the number of transitions obtained in each arrival [5]. The E (sw) along with the capacitance C gives the switch capacitance, C sw =C.E (sw). E (sw) Cn actually be controlled and reduced by selecting algorithms properly and by architecture optimization, which results in less power dissipation Using the adiabatic switching principals is another approach. For more information on adiabatic switching refer to [8]. [6]

VI. Core i7 Processor V/S 4004 Processor

Core i7 processor is a state of the art processor and is the latest and fastest processor present today. The 4004 microprocessor had an operational voltage of 5-15V. But, the i7 has an operational voltage of 1V, which reduces the power dissipation. Also, it reduces the electric field and will prevent the device from breaking down. The drawn length is also reduced from 10micro in 4004 microprocessor to 32/45 nanometer in i7, all thanks to scaling. Also, the clock speed has been increased to 3-3.5 GHz. The i7 has approximately 780 million transistors, while the 4004 microprocessor has only 2300, while keeping the chip area same. But these techniques have their own cons. Reduction of drawn length leads to a reduced distance between the source and the drain, leading to loss of control of the transistor. Also, using multiple transistors while keeping the chip area same leads to a significant increase in the parasitic capacitance (which in turn leads to an increase in power dissipation). While reducing power supply we can reduce electric field, but it will affect the overall performance of the chip, i.e. reduce it. The increase in clock frequency will also lead to an increase in the transition factor, and both will together contribute to an increase in the power dissipation. Hence, low power designing and its techniques are indispensible to overcome these flaws.

VII. CONCLUSION

To reduce power consumption and to increase the speed, a lot of innovations are being made, which include replacing the base material of the chips from silicon to some other materials, such as Gallium Arsenide. But, the need for lower power systems is increasing day by day. The low power designing leads to another big problem to the already existing design problem, which is that the design has to satisfy low power usage, high performance and small area. Techniques such as power management, and varying supply voltage and speed according to the process taking place can be considered. Even though design challenges should further be taken, a new technology is the need of the hour that can provide a long-term solution to the power problems, while not affecting the performance.

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