Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 460N Spring 2014
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Exam 2
April 16, 2014

Name:_____

Problem 1 (30 points):_____

Problem 2 (10 points):_____

Problem 3 (25 points):_____

Problem 4 (25 points):_____

Total (90 points):_____

You have 75 minutes to take this exam.
Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

Please sign the following. I have not given nor received any unauthorized help on this exam.

Signature:_____

GOOD LUCK!

Name:_____

Problem 1 (30 points):

Part a (5 points): What is the wobble between the sub-normal binade and the smallest normal binade? Recall that the wobble between two binades is the ratio of the ULP of the two binades.

Part b (5 points): What is the maximum possible IPC of a machine that has a 100% accurate branch predictor, 100% cache hit ratio, and the ability to fetch up to 4 instructions/cycle, execute up to 8 instructions/cycle, and retire up to 6 instructions/cycle?

Part c (5 points): In _____ I/O, software can communicate with the I/O devices using regular load/store instructions.

Part d (5 points): On an I/O bus where devices have different priorities, the piece of logic that decides who is going to use the I/O bus next is called _____. The inputs to this logic includes the SACK and _____ signals from the devices and the outputs are the _____ signals to the devices.

Name:_____

Problem 1 continued

Part e (5 points): Consider two microarchitectures for the LC-3b. One is an OoO processor which runs at a frequency of 1.5GHz, achieves an IPC of 1.33, and consumes 2W of power. The alternate is an InOrder processor which runs at a frequency of 2.5GHz, achieves and IPC of 0.8, and consumes 1.6W of power. Which one would you recommend for use in a smartphone? Which microarchitecture will you recommend to a friend for a desktop? Explain your choice for each one in less than 15 words.

Smartphone:

Desktop:

Part f (5 points): An aggie has designed a new branch predictor she calls FTBN (Forward-taken, Backward not-taken). As the name implies, it predicts all forward branches to be taken and all backward branches to be not taken. What will be the branch prediction accuracy of FTBN when executing the following code?

```
; The code counts the number of zeros in an array
; Assume: R1 = 4; R2 = Address of first ARRAY element; R3 = 0
LOOP       LDR R4, R2, R1
           BRnp  END
           ADD R3, R3, #1
END        ADD R1, R1, #-1
           BRzp LOOP
           HALT
ARRAY      .fill 0xfeed
           .fill 0xbeef
           .fill 0xcafe
           .fill 0xceed
           .fill 0x0
```

Branch Preditor Accuracy:

Name:_____

Problem 2 (10 points):

Consider an 8-bit, radix-2, IEEE-like floating point specification. We know the highest representable value is $\frac{15}{8} \times 2^9$. Calculate the excess, number of exponent bits, and number of fraction bits. Show your work.

Number of fraction bits: ☐

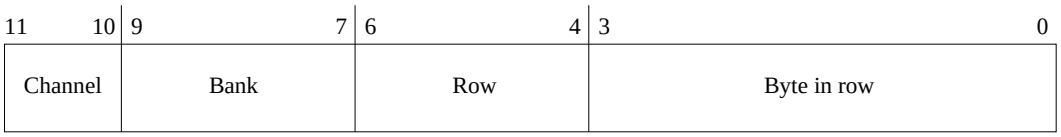
Number of exponent bits: ☐

Excess: ☐

Name:_____

Problem 3 (25 points):

In this problem, you will work with a byte addressable memory with a 16 bit memory bus. The memory address is split as follows:



Part a (1 point): What is the total size of physical memory?

Bytes

Part b (2 points): What is the total number of ranks needed for this memory?

Ranks

Part c (2 points): What is the total number of byte addressable chips needed for this memory?

Chips

Part d (20 points): Assume an optimal memory scheduler, which schedules requests to complete them in minimum possible time, is presented with the physical addresses shown on the next page.

Notes:

1. The memory bus is 16 bits and so are the accesses.
2. An older request must be scheduled first unless there is a performance gain otherwise.
3. On a row buffer hit, an access takes 1 cycle. On a row buffer miss, an access takes 3 cycles.
4. For all banks in memory, assume Row 0 is currently open.
5. Assume all banks are free at cycle 0.
6. A particular address can be sent to memory in a particular cycle if (1) the corresponding bank is free (notice how B is sent in cycle 0), or (2) the data from the previous request to that bank is being transferred concurrently (Notice D is sent in cycle 1).
7. Address0 and Data0 represent the lines to Channel0, and Address1 and Data1 are the lines to Channel1.

Name:_____

Problem 3 continued

Your job: Complete the timing diagram representing the cycles during which addresses are sent and the corresponding data is received. We have filled requests B and D as examples. You may not need to fill in all the cycles shown.

Oldest →

A	0 01 000 1100	E	0 00 001 1110
B	1 00 000 1010	F	0 00 001 0000
C	0 00 000 0100	G	1 11 111 1110
D	1 00 001 0000	H	1 10 110 0000

← Newest

	0	1	2	3	4	5	6	7	8	9
Address0										
Data0										
Address1	B	D								
Data1		[B]			[D]					

Name:_____

Problem 4 (25 points):

Consider an out-of-order processor with seven registers (R0-R6) with the following properties:

1. There is one multiplier and one adder. Both units are pipelined. These units take an unknown number of cycles to execute instructions.
2. There is a common Reservation Station (RS) shared between the multiply and the add unit.
3. The Allocate Reorder Buffer, Allocate RS and Update RAT takes place in the Decode stage. Thus, the pipeline looks like F-D-E1-E2-...-WB.
4. Only one instruction can be fetched, decoded, and retired in one cycle.
5. Instructions enter the reservation stations in program order. I.e. I1 is allocated in slot A, I2 is allocated in slot B and so on.
6. An instruction's reservation station entry is freed as soon as it begins execution.
7. The calculated value is broadcast to the Reservation station, Register Allocation Table and Reorder Buffer at the end of the last stage of execution (data will be available at the beginning of the next cycle).
8. There is in-order retirement, but the Reorder Buffer is not shown.

Part a (18 points): Identify the five instructions, I1-I5, to complete the partially filled table. Figure 1 (on next page) shows the Architectural Register File before I1 is fetched (i.e. at the beginning of cycle 0) and after I5 retires (i.e. at the end of cycle 14). Figure 2 shows a snapshot of the Reservation Station and the functional units at the end of cycle 6.

	Opcode	DR	SR1	SR2
I1				
I2				R0
I3			R6	
I4				
I5				

Part b (7 points): Circle the number of cycles for the respective functional units.

ADD : 2 3 4

MUL : 2 3 4

PROBLEM IS CONTINUED ON THE NEXT PAGE!

Name:_____

Problem 4 continued

	Cycle 0 Value
R0	10
R1	5
R2	3
R3	21
R4	68
R5	26
R6	16

	Cycle 14 Value
R0	8
R1	63
R2	3
R3	21
R4	48
R5	89
R6	16

Figure 1: Architectural Register File

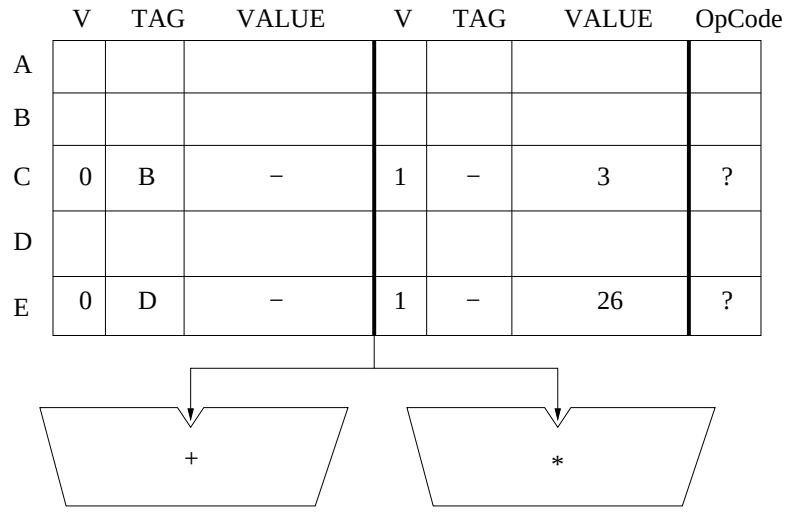


Figure 2: Reservation Station and functional units at the end of cycle 6.
Note: Instruction tagged as B is being executed in the add functional unit and instruction tagged as D is being executed in the multiply functional unit. Instruction A has finished executing.

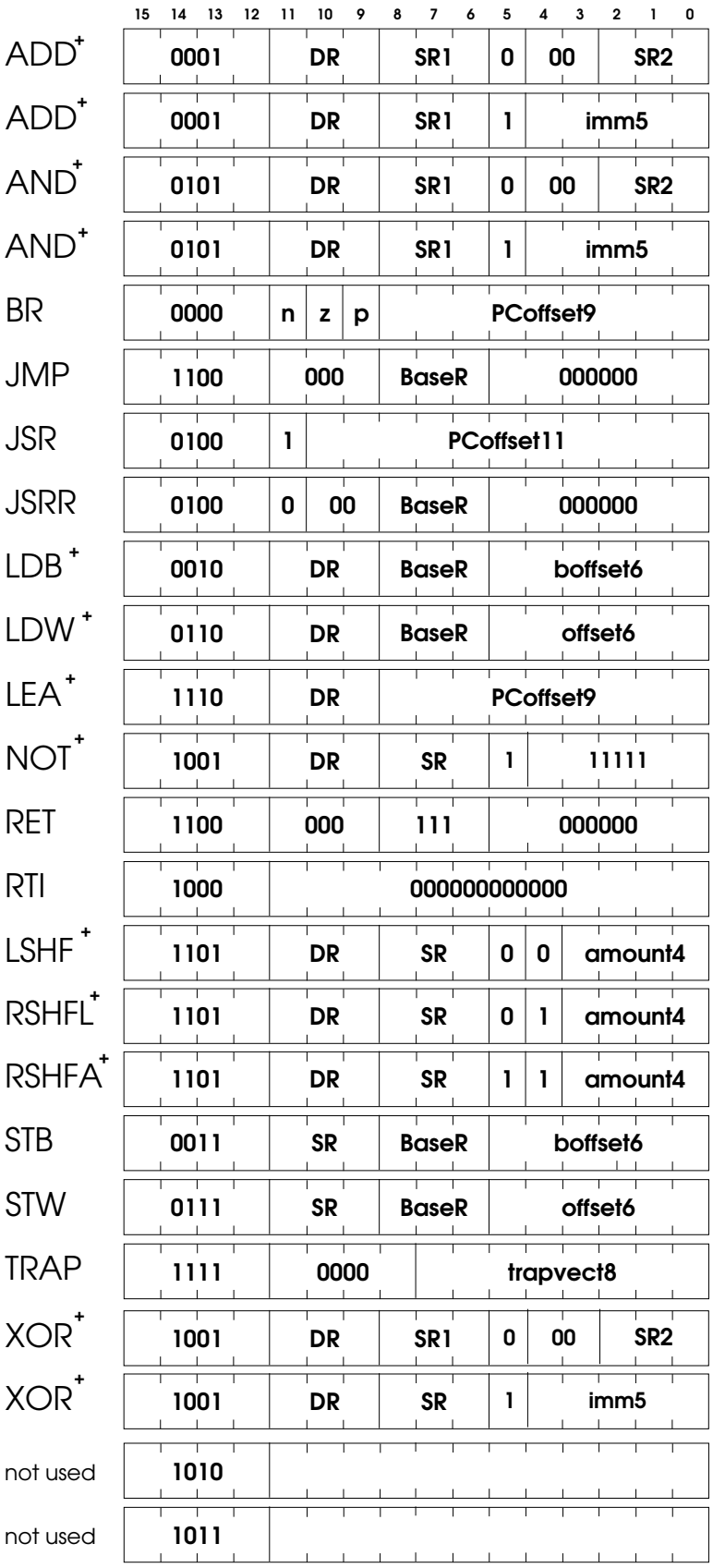


Figure 3: LC-3b Instruction Encodings

Table 1: Data path control signals

Signal Name	Signal Values	
LD.MAR/1:	NO(0), LOAD(1)	
LD.MDR/1:	NO(0), LOAD(1)	
LD.IR/1:	NO(0), LOAD(1)	
LD.BEN/1:	NO(0), LOAD(1)	
LD.REG/1:	NO(0), LOAD(1)	
LD.CC/1:	NO(0), LOAD(1)	
LD.PC/1:	NO(0), LOAD(1)	
GatePC/1:	NO(0), YES(1)	
GateMDR/1:	NO(0), YES(1)	
GateALU/1:	NO(0), YES(1)	
GateMARMUX/1:	NO(0), YES(1)	
GateSHF/1:	NO(0), YES(1)	
PCMUX/2:	PC+2(0)	;select pc+2
	BUS(1)	;select value from bus
	ADDER(2)	;select output of address adder
DRMUX/1:	11.9(0)	;destination IR[11:9]
	R7(1)	;destination R7
SR1MUX/1:	11.9(0)	;source IR[11:9]
	8.6(1)	;source IR[8:6]
ADDR1MUX/1:	PC(0), BaseR(1)	
ADDR2MUX/2:	ZERO(0)	;select the value zero
	offset6(1)	;select SEXT[IR[5:0]]
	PCoffset9(2)	;select SEXT[IR[8:0]]
	PCoffset11(3)	;select SEXT[IR[10:0]]
MARMUX/1:	7.0(0)	;select LSHF(ZEXT[IR[7:0]],1)
	ADDER(1)	;select output of address adder
ALUK/2:	ADD(0), AND(1), XOR(2), PASSA(3)	
MIO.EN/1:	NO(0), YES(1)	
R.W/1:	RD(0), WR(1)	
DATA.SIZE/1:	BYTE(0), WORD(1)	
LSHF1/1:	NO(0), YES(1)	

Table 2: Microsequencer control signals

Signal Name	Signal Values	
J/6:		
COND/2:	$COND_0$	;Unconditional
	$COND_1$	;Memory Ready
	$COND_2$	;Branch
	$COND_3$	;Addressing Mode
IRD/1:	NO, YES	

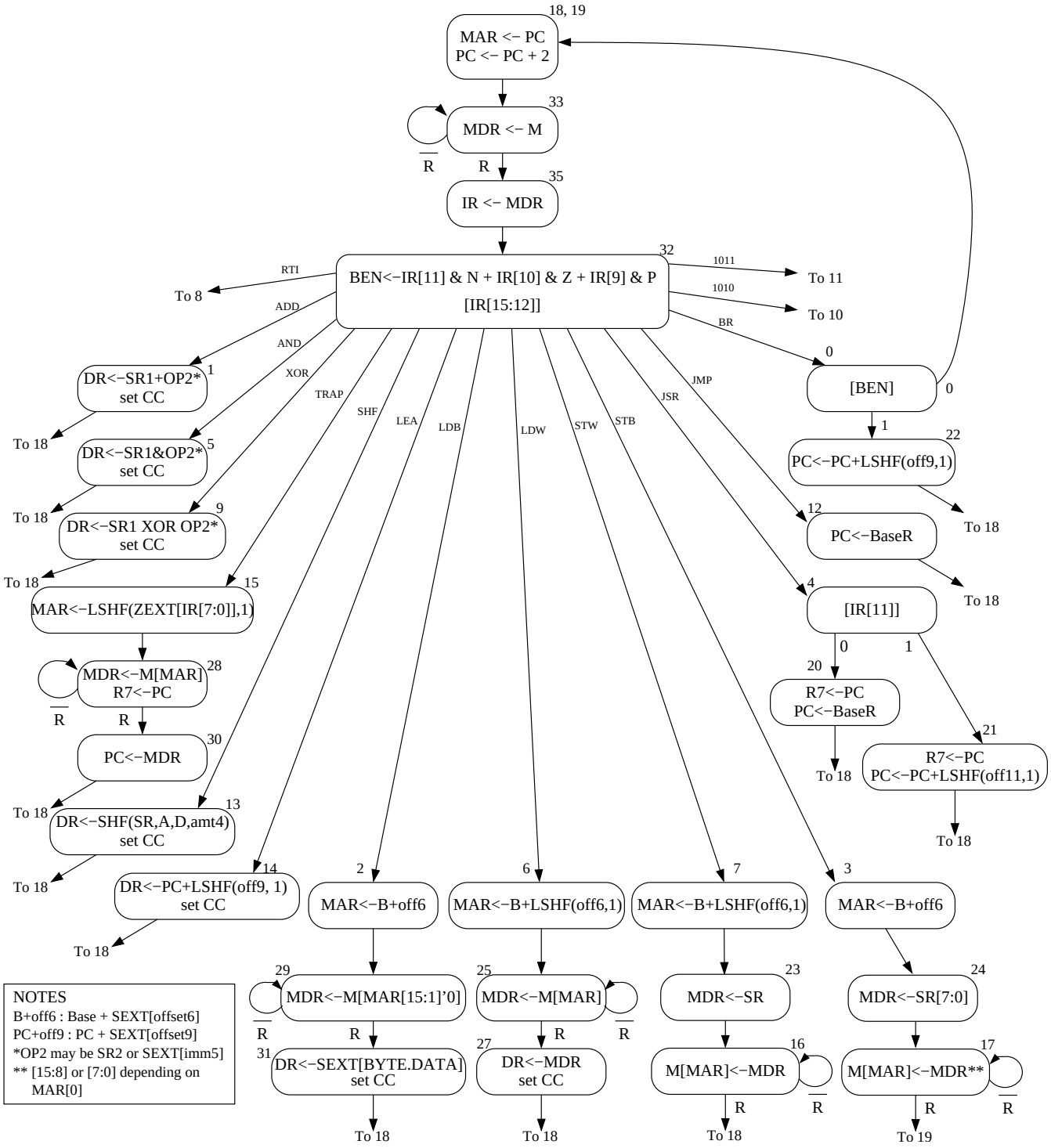


Figure 4: A state machine for the LC-3b

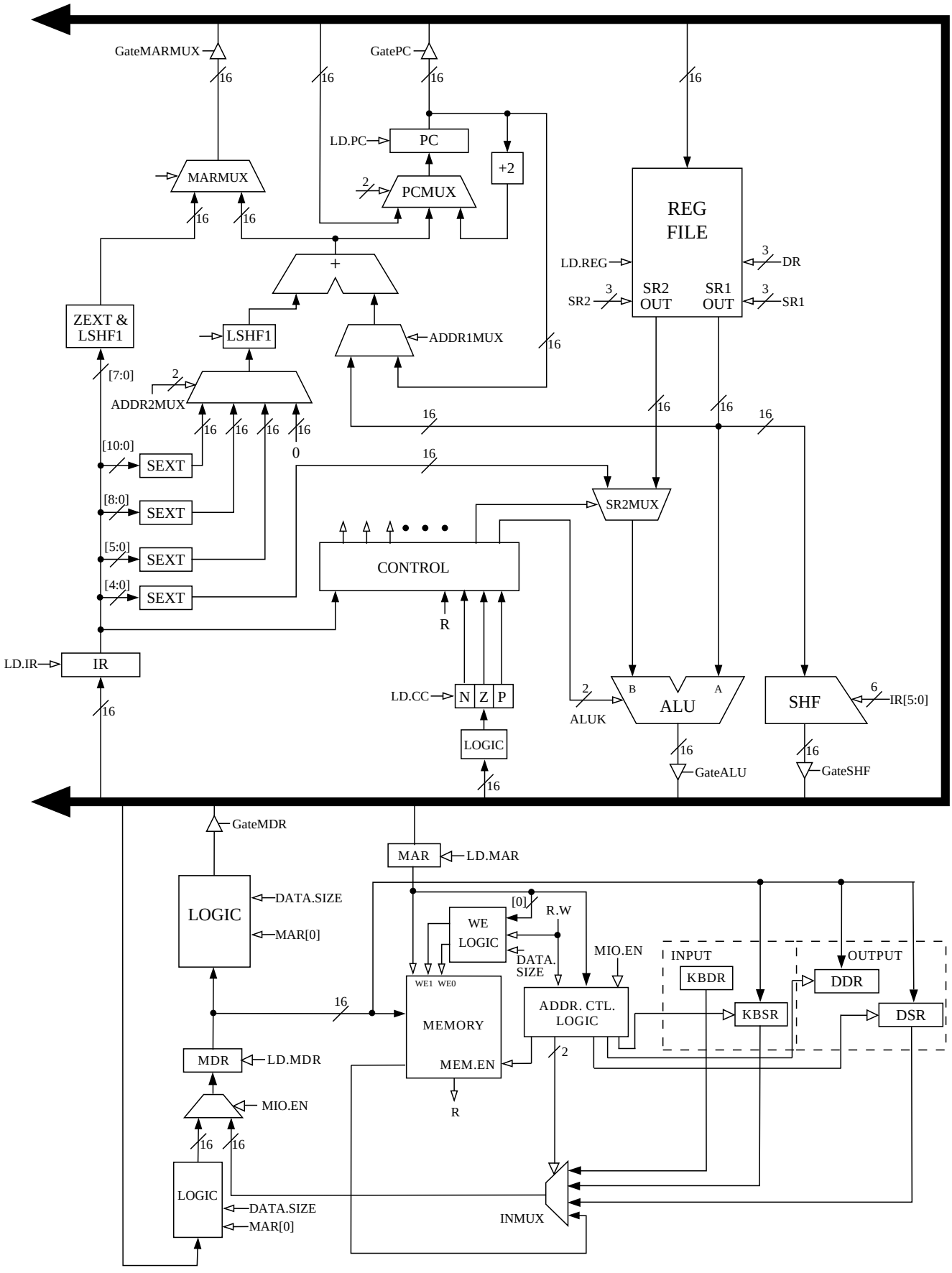


Figure 5: The LC-3b data path

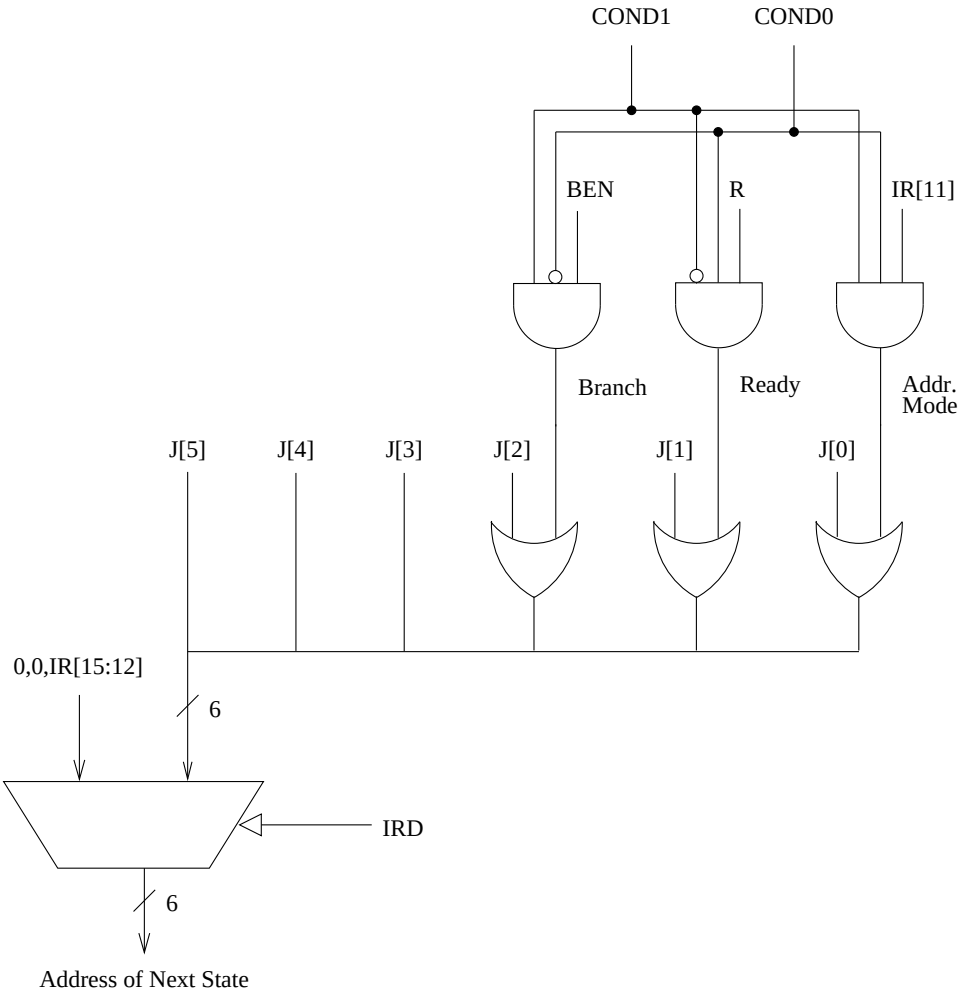


Figure 6: The microsequencer of the LC-3b base machine

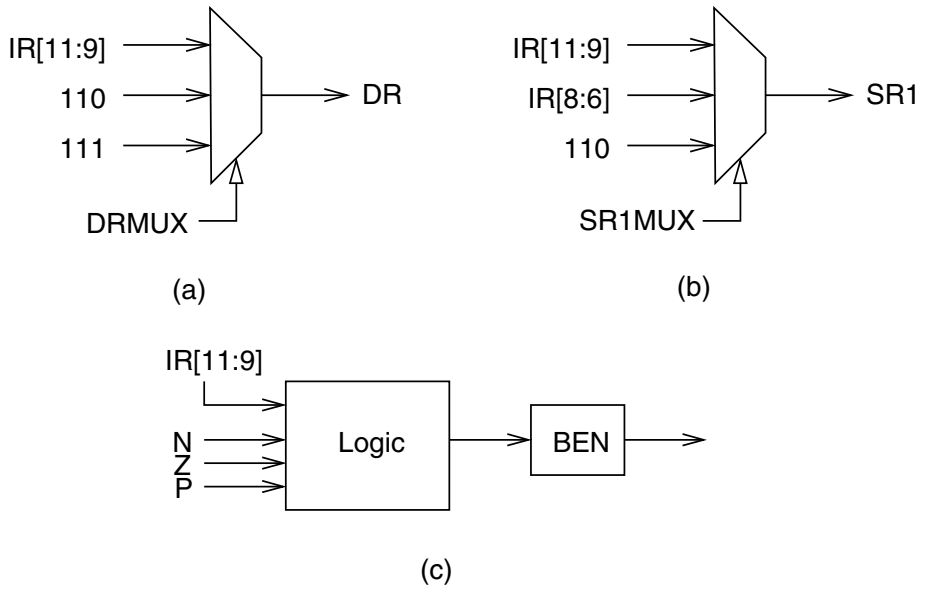


Figure 7: The microsequencer of the LC-3b base machine