Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 460N Fall 2013
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Exam 1
October 16, 2013

Name:____

Problem 1 (20 points):________

Problem 2 (15 points):________

Problem 3 (10 points):________

Problem 4 (25 points):________

Problem 5 (20 points):________

Total (90 points):________________

You have 75 minutes to take this exam.
Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

Please sign the following. I have not given nor received any unauthorized help on this exam.

Signature:____

GOOD LUCK!

Name:____________________________________

Problem 1 (20 points):

Part a (5 points): What is the 8-bit two's complement representation of the number -55?

Answer: | | | | | | | | |

Part b (5 points): A periodic [ ] operation is required to ensure that the [ ] in a DRAM cell does not lose its stored value.

Part c (5 points): Instructions enter the reservation stations **Circle one:** in-order/out-of-order and write the results to the ROB **Circle one:** in-order/out-of-order.

Part d (5 points): In the LC-3b microarchitecture shown in Appendix C, how much of a performance gain is expected from a branch predictor?

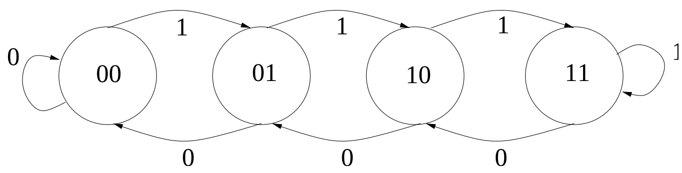
Answer: [ ] **%**

Please explain (in less than 15 words).

Name:___________________________________

Problem 2 (15 points):

In the class we studied a branch predictor where all branches access/update a single 2-bit counter. Let's take it a step further and assume a branch predictor with four 2-bit counters where different branches access/update different counters. Which counter to use is selected based on bits [2:1] of the branch's PC, i.e., counter 1 is used if the PC is 0x3002 (PC[2:1]=01) and counter 3 is used if PC=0x3006. Once a counter has been selected, the access/update of the 2 bit counter works exactly as discussed in class: a branch is predicted taken if the counter is in states 10 and 11, and predicted not-taken if the counter is in states 00 and 01.



Part a. (10 points) Fill in the final state of the branch predictor after executing the LC-3b program below. Please show your work for partial credit.

```
       .ORIG x3000
       AND R1, R1, #0
       AND R2, R2, #0
       LEA R0, VALUE
       LDW R0, R0, #0 ; R0 = xF521
LOOP   BRzp SKIP0
       ADD R1, R1, #1 ; Increment R1 if high bit of R0 is 1
       ADD R0, R0, #0 ; Reset the condition codes
SKIP0  BRn SKIP1
       ADD R2, R2, #1 ; Increment R2 if high bit of R0 is 0
SKIP1  ADD R0, R0, R0 ; Left shift R0
       BRnp LOOP
       HALT
VALUE  .FILL xF521
       .END
```

Part b. (5 points) What is the prediction accuracy of this predictor for this program? ☐ %

Name:____________________________

Problem 3 (10 points):

For the byte-addressable physical memory address specified below, answer parts (a-d).

15 12	11	10 8	7 5	4 2	1 0
Row	Channel	Rank	Bank	Byte−in Row	Chip

Part a. (2 points) What is the total size of the physical memory?

KB

Part b. (3 points) How many ranks are there in **total**?

Part c. (2 points) How many chips are there in **total**?

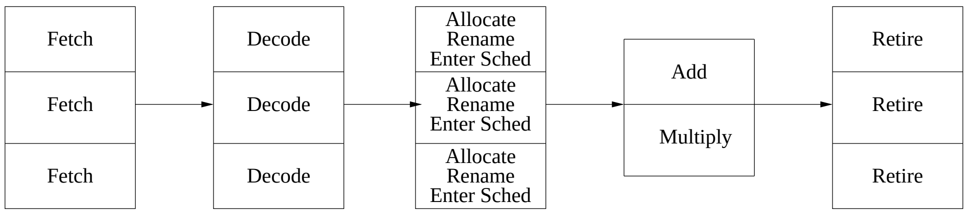
Part d. (3 points) What is the size of each rank?

KB

Name:____________________________________

Problem 4 (20 points):

Consider the core460N microarchitecture discussed in class. For a refresher, we have drawn a diagram of core460N pipeline below.



Notes:
1. There is one 2-cycle non-pipelined adder
2. There is one 3-cycle non-pipelined multiplier
3. There is only one reservation station entry per reservation station
4. Fetch, decode, allocate, and retire take one cycle
5. Instructions enter the Reservation stations in program order in Allocate stage
6. An instruction's reservation station entry is freed *as soon as it begins execution*.
7. The ROB, RAT, and RS are updated at the *end* of the execution stage

Five instructions (I1-I5) are executed.

Your job: Using the information on the next page, identify I1-I5 and fill in the following table.

	Opcode(+ OR *)	DR	SR1	SR2
I1				
I2				
I3				
I4				
I5				

PROBLEM IS CONTINUED ON THE NEXT PAGE!

Name:____________________________________

Problem 4 continued

Contents of the Register Alias Table (RAT) *before* the Fetch of I1 and *after* retirement of I5 :

Before Fetch

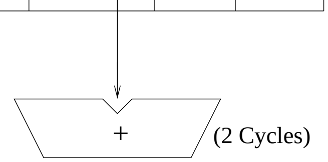
	VALID	VALUE	TAG
R0	1	0	−
R1	1	5	−
R2	1	3	−
R3	1	9	−
R4	1	0	−
R5	1	9	−
R6	1	4	−
R7	1	2	−

After Retire

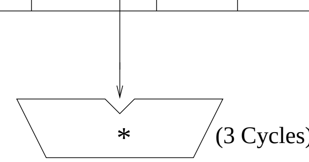
	VALID	VALUE	TAG
R0	1	10	−
R1	1	5	−
R2	1	3	−
R3	1	17	−
R4	1	0	−
R5	1	4	−
R6	1	0	−
R7	1	2	−

Contents of the two reservation stations at the end of cycle 5:

V	TAG	VALUE	V	TAG	VALUE
1	−	2	1	−	10



V	TAG	VALUE	V	TAG	VALUE
0	B	−	1	−	0



Contents of the ROB at the end of cycle 5:

Tag	Ready	DR	Value
A	1	R0	10
B	0	R5	5
C	0	R6	15
D	0	R3	4
E	0	R3	0

Name:____________________________________

Problem 5 (20 points):

Exactly copied below is the description of the LC-1b ISA you previously saw in Problem Set 1.

Opcode	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADD	0	0	0	DR		A	SR	
AND	0	0	1	DR		A	SR	
BR(R)	0	1	0	N	Z	P	TR	
LDImm	0	1	1	SIM				
LEA	1	0	0	SO				
LD	1	0	1	DR		0	TR	
ST	1	1	0	SR		0	TR	
NOT	1	1	1	DR		1	1	1

SIM = Signed immediate
SO = Signed PC offset

- Interpretation of all instructions is similar to that of the LC-3b, unless specifically stated otherwise.
- The LC-1b is a two-address machine. The destination register of the ADD and AND instructions is the same as the first source operand. The destination register of the NOT instruction is the same as the source operand.
- The destination register for the instructions LDImm and LEA is always register R0. (e.g. LDImm #12 loads decimal 12 to register R0.)
- TR stands for Target Register. In the case of the conditional branch instruction BR, it contains the target address of the branch. In the case of LD, it contains the address of the source of the load. In the case of ST, it contains the address of the destination of the store.
- ADD and AND provide immediate addressing by means of a steering bit, IR[2], labeled A. If A is 0, the second source operand is obtained from SR. If A is 1, the second source operand is obtained by sign-extending IR[1:0] of the instruction. A bit is called a steering bit if its value steers the interpretation of other bits (instruction bits 1:0 in this case).
- Bits labeled 0 must be zero in the encoding of the instruction.

Your job: Answer the questions on the following pages.

Additional Notes:
1. The ALUK bits and the PCmux bits hold the same values as they do in the LC-3b (ALUK=ADD,AND,XOR,PASSA etc.).
2. LC-1b's register file works similar to LC3-b except that one of the read ports is labelled DR OUT and it works as DR OUT=REG[DR].

You are welcome to tear this page out of the exam.

Name:________________________________

Problem 5 continued:

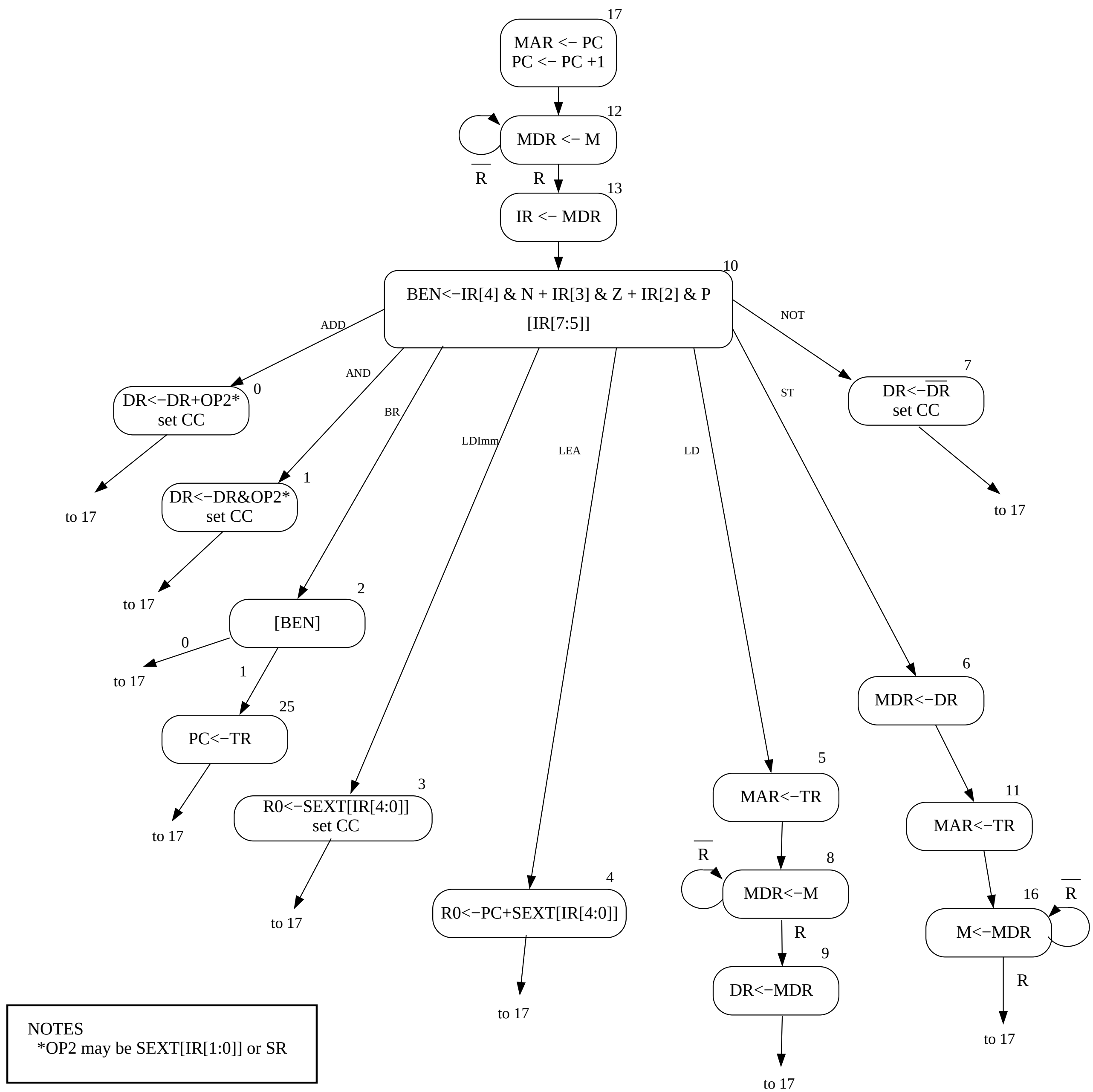


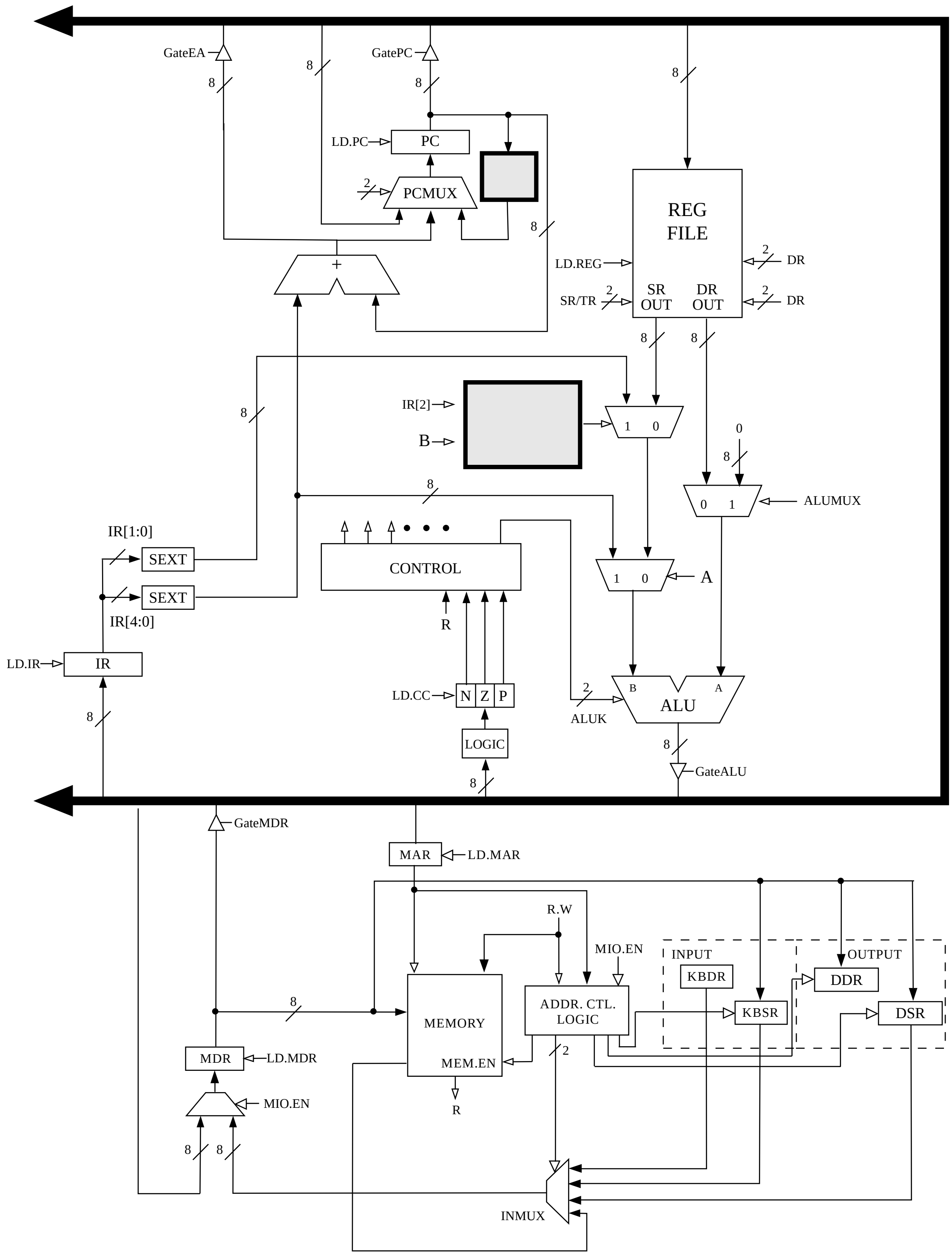
Figure 1: State diagram for the LC-1b

You are welcome to tear this page out of the exam.

Name:___________________________________

Problem 5 continued:

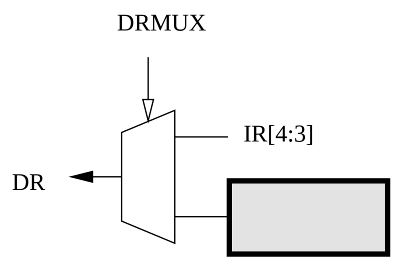
Part a (6 points): Complete the implementation of the LC-1b by filling the two empty, shaded, boxes with the required logic gates or a clear umambiguous description of the logic.



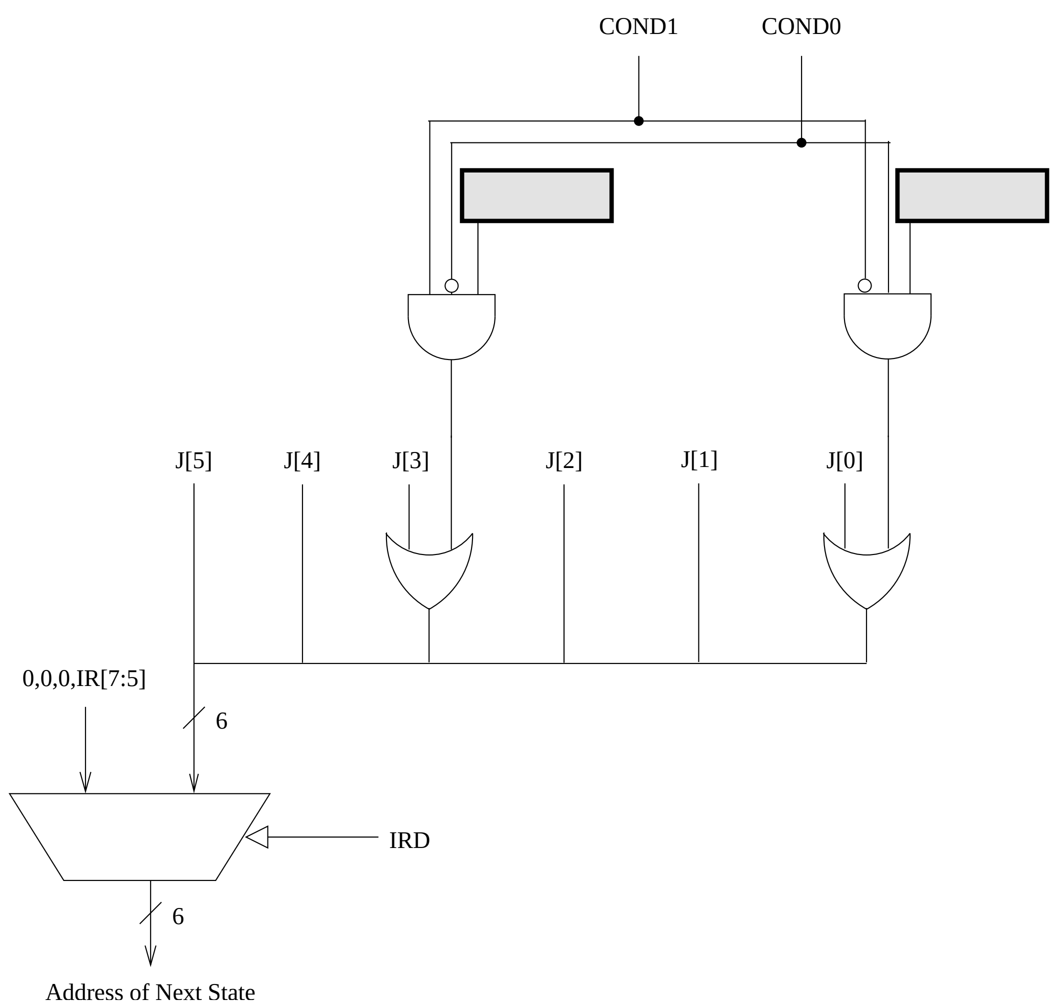
Name:____________________________________

Problem 5 continued:

Part b (3 points): Fill out the empty input to the DRMUX.



Part c (4 points): Fill out the empty boxes in the microsequencer.



Name:____________________________________

Problem 5 continued:

Part d (5 points): Fill out the microcode entries for the specified control signals.

State	ALUMUX	ALUK[1:0]	GateALU
1			
3			
4			
6			
11			

Part e (2 points): In which states do the control signals labelled A and B need to be a 1?

Signal	State Number(s)
A	
B	