Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 460N Fall 2013
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Exam 2
November 20, 2013

Name:_____

Problem 1 (15 points):_____

Problem 2 (15 points):_____

Problem 3 (15 points):_____

Problem 4 (20 points):_____

Problem 5 (25 points):_____

Total (90 points):_____

You have 75 minutes to take this exam.
Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

Please sign the following. I have not given nor received any unauthorized help on this exam.

Signature:_____

GOOD LUCK!

Name:_____

Problem 1 (15 points):
Part a (5 points): Assume a program where 12% code is completely sequential, 40% is completely parallelizable, and the remaining 48% is partially parallelizable such that the speed up, Sp, is defined as:

$Sp = P$ if $P <= 4$,
$Sp = 4 + 0.5 * (P - 4)$ else

How much overall speedup will be obtained with 8 cores ($P = 8$)? [ ]

Part b (5 points): The following table describes the working of each of the 3 replacement bits. For example, if state[2] = 0, the ways Way0 - Way1 will be considered LRU while ways Way2 - Way3 will be considered MRU.

	0	**1**
State[2]	Way0 - Way1	Way2 - Way3
State[1]	Way0	Way1
State[0]	Way2	Way3

Complete the following partial truth table for Tree Replacement Policy applied on a 4-way set associative cache.

Current State	**Accessed Way**	**New State**	**New Victim Way**
110	3	010	1
011	1		

Part c (5 points): A set dirty bit in a tag store entry indicates that the corresponding cache block in the cache is different from memory and [ ] has a stale value. A set dirty bit in the page table indicates that the data stored in the corresponding [ ] is different from the [ ] and the latter has a stale value. Assume the system has only one core.

Name:_____

Problem 2 (15 points)

Assume an 8-bit, radix-2, IEEE-like floating point specification, where the rounding mode is set to **always** round up. The following calculations result in the inexact values shown.

$1/4 + 1/64 \rightarrow 9/32$
$1/4 - 1/64 \rightarrow 1/4$

Calculate the excess, number of exponent bits, and number of fraction bits. Show your work.

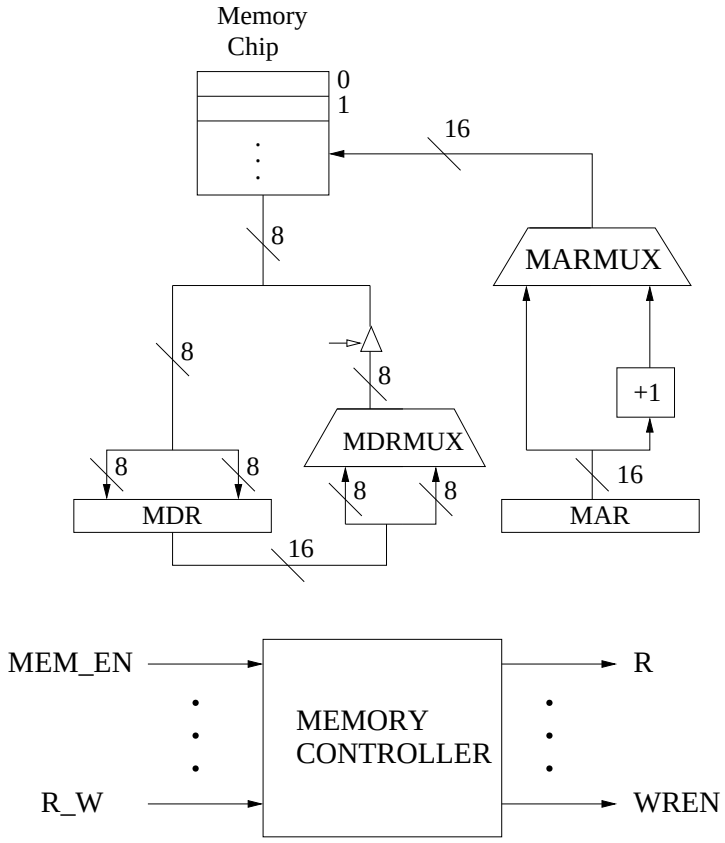
Number of fraction bits: | |

Number of exponent bits: | |

Excess: | |

Name:_____

Problem 3 (15 points)
We show a partial data path for a new memory system that stores data as little endian.



The interface between the controller and the processor is similar to the LC-3b. To start an access, the processor loads the MAR with the address (and MDR with the data to be stored, if doing a store) and sets the MEM_EN signal, together with other required signals. When the access is complete, the memory controller sets the R signal. The table below defines the inputs and outputs of the memory controller.

Inputs			**Outputs**		
signal	**0**	**1**	**signal**	**0**	**1**
MEM_EN	disabled	enabled	R	not ready	ready
DATA_SIZE	8	16	MDRMUX	MDR[7:0]	MDR[15:8]
R_W	read	write	MARMUX	MAR	MAR+1
			LD_MDRHI	don't load	load MDR[15:8]
			LD_MDRLO	don't load	load MDR[7:0]
			CHIPEN	disabled	enabled
			GATE_MDRMUX	off	on
			WREN	off	on

Name:_____

Problem 3 continued

Part a (5 points): If the processor issues a 16-bit load from address A (LD16 R0, A), for what values of A will this memory system need to access the chip **twice**? (Answer in 5 words or less)

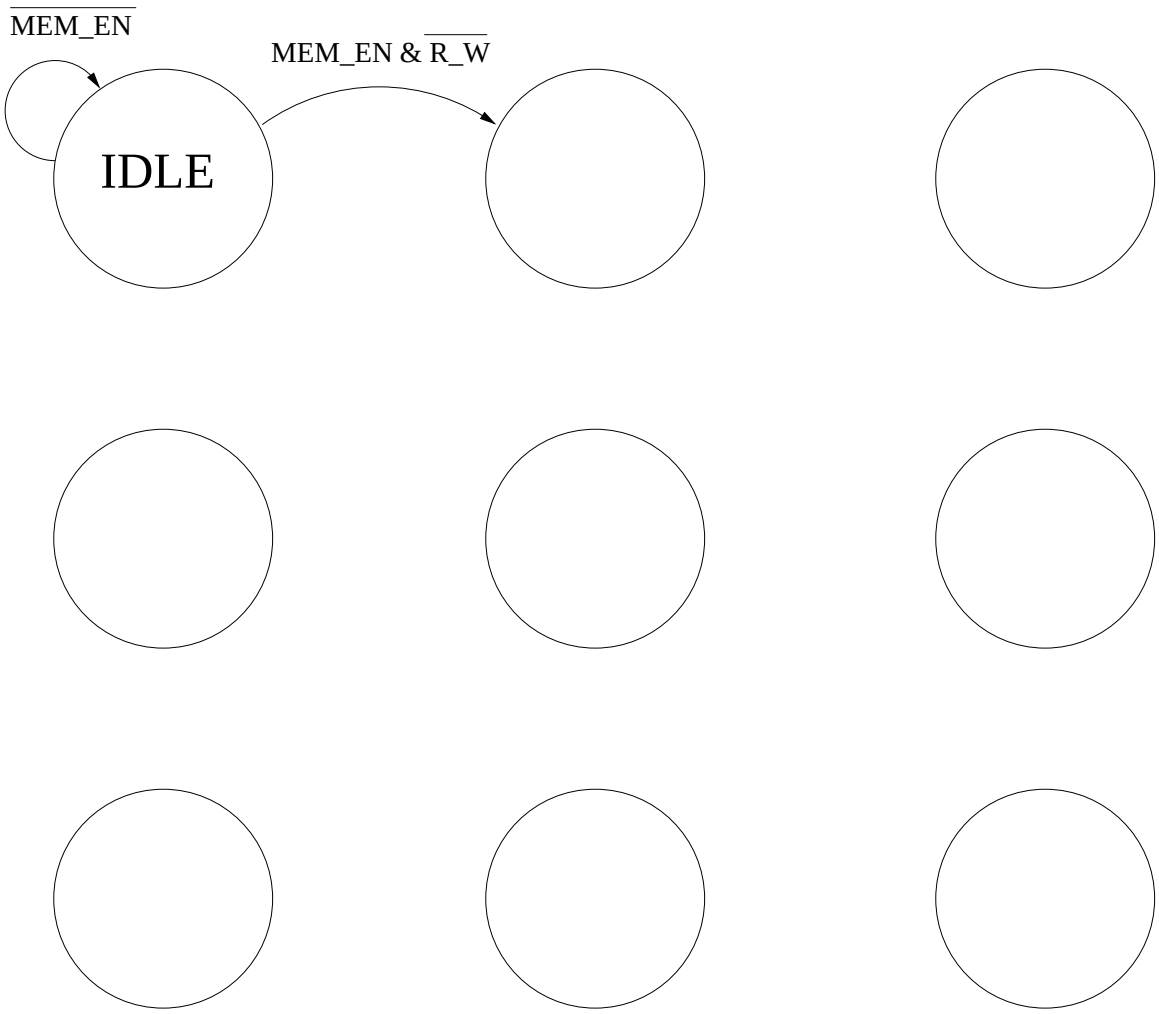
Part b (10 points): Using the states **given on the next page**, design the state machine for the memory controller.

Notes:
1. For simplicity, your controller needs to handle **only** load instructions.
2. Your controller must handle both 8 and 16 bit loads.
3. All inputs from the processor will remain steady throughout the access **except** MEM_EN.
4. The MEM_EN signal from the processor will be high for only one cycle.
5. It takes two cyckes to get the data from the memory chip.

Please follow the convention that signal names listed inside the state bubble are assumed high and all remaining signals are assumed low. You may not need all the states provided.

Name:_____

Problem 3 continued



Name:_____

Problem 4 (20 points)

Little Computers Inc. has added a one-level direct mapped cache to the LC-3b. Their engineer (an Aggie) did not document all the attributes of the cache. **Your job is to figure out the following three missing attributes about the cache:** the number of replacement bits in each set, the cache line size, and the number of sets.

We already know that:

- The LC-3b always accesses the cache before it accesses memory.
- On a cache hit, the access takes only 1 cycle. On a cache miss, the access takes an **additional** 7 cycles.
- Each tag store entry is 1 byte.
- The cache is physically indexed and physically tagged, i.e., PIPT.
- When we run this simple program on the modified LC-3b computer with an empty cache, and measure the number of cycles taken to execute each instruction, we get the following result:

```
        .ORIG x3000
        LEA R0, ADDR    ; 12 cycles
        LDW R0, R0, #0  ; 14 cycles
        LDB R1, R0, #0  ; 21 cycles
        ADD R1, R1, #1  ; 5 cycles
        STB R1, R0, #0  ; 14 cycles
ADDR    HALT
        .END
```

Number of bits for replacement per set: [ ]

Cache line size (in bytes): [ ]

Number of sets: [ ]

Name:_____

Problem 5 (25 points)

You are given a machine with an x86-like 2-level byte-addressable virtual memory. Virtual addresses are 9-bits, where VA[8:6] are used to index in to the system page table, VA[5:3] are used to index into the process page tables, and VA[2:0] are Byte-in-Page (BIP) bits.

Both the system and user page tables always start at the page boundary. The Physical addresses are 8 bits. Each PTE is 1 byte. The machine has a Direct-mapped, Virtually-Indexed-Virtually-Tagged (VIVT) cache, and a 2-entry fully associative TLB that uses the LRU replacement policy.

For simplicity, we will assume that:
1. The cache only stores the data and not the results of page table accesses.
2. The TLB stores PTEs from only the User Page Table and not the System Page Table.
3. All entries of the Cache and TLB were invalid before the accesses.

The state of the entire cache and the TLB after 3 accesses from the processor are shown below.

	Valid	Tag	Data
Set 0	0	01010	omitted
Set 1	1	10011	omitted
Set 2	1	omitted	omitted
Set 3	0	00010	omitted

VIVT Cache

Valid	Dirty	PFN

PTE Layout

Valid	VPN	PTE
1	001001	1001100

Valid	VPN	PTE
1	omitted	1000100

TLB

Also shown below are some of the Physical memory locations that were accessed in their order of access. Determine the missing Physical and Virtual address entries.

	Physical Addresses
Access 1	1110 0010
Access 2	1001 1101
Access 3	0110 1000
Access 4	_____
Access 5	0011 0001
Access 6	_____ 011
Access 7	_____
Access 8	0010 1110
Access 9	_____ 101

	Virtual Addresses
Access 1	_____
Access 2	_____
Access 3	_____