Department of Electrical and Computer Engineering
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EE 460N Spring 2011
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Exam 2
April 20, 2011

Name:_____

Problem 1 (30 points):_____

Problem 2 (20 points):_____

Problem 3 (25 points):_____

Problem 4 (25 points):_____

Total (100 points):_____

Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

Please sign the following. I have not given nor received any unauthorized help on this exam.

Signature:_____

GOOD LUCK!

Name:_____

Problem 1 (30 points)

Part a (6 points): A problem takes 2 hours to solve on a sequential machine. It consists of two parts, which must be done in sequence. Each part takes one hour on the sequential machine. The first part is 90% parallelizable, the second part is 60% parallelizable. Show your work below.

With infinite computing resources this problem would take how long?

This represents a maximum speed-up of what?

With 4 processors, the speed-up for this problem would be what?

Part b (6 points): We have discussed in class various kinds of memory, one of which is a content-addressable memory. Two structures we have discussed in class actually use content addressable memory. For each case, identify the structure, and show all parts of an entry. Circle the element in each entry that is used for content addressing.

Name of structure: _____

An entry in this structure:

Name of structure: _____

An entry in this structure:

Part c (6 points): Classical VLIW machines do not make effective use of their instruction caches. Why? Explain.

Name:_____

Problem 1 continued

Part d (6 points): We detect an interrupt or an exception; when does it get handled? We noted in class that interrupts are normally handled

whereas exceptions are normally handled

However, as is often the case in computer architecture, “normally” is not the same as “always”.

An example of an interrupt which is not handled at the time you stated above is

An example of an exception which is not handled at the time you stated above is

Part e (6 points): Two device controllers A and B are on BR level #3. Device controller A is closer to the PAU. Suppose device controller A does not want the bus, but device controller B does. This is the highest priority bus request so the PAU grants the bus with BG #3. Before device controller A sees the BG signal, its device wants the bus. What does device controller A do when the BG signal arrives?

Is this a race condition (yes/no) Explain.

Name:_____

Problem 2 (20 points)

Suppose IEEE decided to extend the Floating Point standard to include a 12 bit representation, keeping all the characteristics of the IEEE Standard intact. They assign bits to exponent and fraction such that the smallest representable positive number (i.e., smallest subnormal) is 1/1024 and the smallest normalized positive number is 1/16.

Part a: How many bits for exponent: [ ]

How many bits for fraction: [ ]

What is the value of n in "excess-n" code for exponents: [ ]

Part b: How do you represent "minus infinity": [ ]

Part c: How do you represent the largest normalized number: [ ]

What is its value: [ ]

Part d: Consider the value 139/128 times 2^8. If we change how many bits we allocate to exponent and fraction, and we insist that the exponent 0 is represented by 011..1, can we represent this value exactly.
If **yes**, identify the number of fraction bits, the number of exponent bits, and show the representation of this value:

[ ]

If **no**, explain why not, and represent the number according to the scheme of parts a,b,c above. If rounding is required, round to unbiased nearest.

[ ]

Name:_____

Problem 3 (25 points)

A byte-addressable cache of fixed total size and fixed line size is implemented both as a k-way set associative cache and also as a fully associative cache. Assume perfect LRU replacement and line allocate on a write miss policies. For this problem, please show your work below.

If the two implementations are presented with the same sequence of addresses for byte accesses, they generate hits/misses as shown below:

Address	R/W	**k**-way associative (Miss/Hit)	Fully associative (Miss/Hit)
011011100	W	Miss	Miss
011001100	R	Miss	Miss
111000111	R	Miss	Miss
011011000	R	Hit	Hit
010101100	R	Miss	Miss
001111111	R	Miss	Miss
011001111	R	Miss	Hit
111110010	R	Miss	Miss
110100111	R	Miss	Miss
111000011	R	Hit	Miss

Part a: How many cache lines are there in the two cache implementations? ☐

Part b: The set associative cache is k-way, where k =

☐ 1-Way (Direct Mapped)
☐ 2-Way
☐ 3-Way
☐ 4-Way
☐ 5-Way
☐ 6-Way
☐ 7-Way
☐ 8-Way
☐ 9-Way

(check the appropriate box).

Part c: For the k-way cache, how many tag bits: ☐ and index bits: ☐

Part d: Recall in the preamble, that this cache does an allocate on write miss. Complete the hit/miss behavior table if the cache did not allocate on a write miss.

Address	R/W	**k**-way associative (M/H)	Fully associative (M/H)
011011100	W		
011001100	R		
111000111	R		
011011000	R		
010101100	R		
001111111	R		
011001111	R		
111110010	R		
110100111	R		
111000011	R		

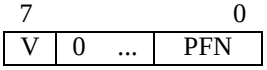
Name:_____

Problem 4 (25 points)

Consider the following **two level** virtual memory system, similar to the VAX:

Virtual Address Space:	512 Bytes	Physical Memory Size:	128 Bytes
User Space Range:	x000 to x0FF	Page Size:	8 Bytes
System Space Range:	x100 to x1FF	PTE Size:	1 Byte

The machine is byte addressable. Assume the system does not include a TLB. The PTE format is as follows:



Part a: How many bits are allocated for the PFN in the PTE?

Answer: _____

We wish to execute the instruction:

ADDM R2, R0, R1

where ADDM takes the contents of the memory location specified by R0, adds to it the value in R1, and stores the result in the memory location specified by R2. That is,

M[R2] <— M[R0] + R1

Before this instruction is executed, the following values are stored as shown:

R0: x0B9
R1: x12
UBR (User Space Page Table Base Register): x140

Memory:

x00	x70	x20	x85	x40	x78	x60	x8D
x01	x71	x21	x74	x41	x83	x61	x8A
x02	x8C	x22	x75	x42	x84	x62	x86
x03	x88	x23	x81	x43	x79	x63	x7C
x04	x72	x24	x8C	x44	x89	x64	x7D
x05	x82	x25	x76	x45	x7A	x65	x88
x06	x8F	x26	x77	x46	x7B	x66	x7E
x07	x73	x27	x80	x47	x87	x67	x7F

Name:_____

Problem 4 continued

Part b: After the instruction was fetched and decoded, six subsequent memory accesses were required to process this instruction. There were no page faults, interrupts or other uhappy events.

Your job: Complete the table below:

Access #	VA	PA	Data	Description
1		x42		
2				
3				
4				
5				
6		x64		

Note: "N/A" is a potential answer for entries in the VA column. Data is the data that is Read from or Written to memory. Use the Description column to describe what is being read/written (e.g. "PTE for page xx," "Operand data for ADDM").

Part c: What is the value of the SBR (System Space Page Table Base Register)?

Answer:

Part d: What is the maximum number of Page Faults ANY execution (excluding instruction fetch) of the ADDM instruction could generate?

Answer: