Even-Odd Numbers using Digital Counter

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***Abstract*—This paper presents the design of a digital counter that can count even as well as odd numbers simultaneously. The Counter behaves as an even counter if the control input favors the even counter and similarly, the counter will behave as an odd counter if the control input favors the odd counter. This Multi-use counter can be developed for as many bits possible, but in this paper, the demonstration is done using 3-bit Counter. These counters are synchronous counter that gets trigger with posedge (positive edge) clock.**

***Keywords*—Synchronous, posedge.**

I. Description

Counters are made up of number of flip-flops. Flip-Flops are the storage element that is used to store the binary information, technically Flip-Flops are the digital circuits that are switched between two stable states and are used to store binary data. Generally, we can use any flip-flop to build a counter, but mostly we use T Flip-Flop to build a digital counter, because T Flip-Flop also known as Toggle Flip Flop changes its output on every clock pulse. Based on clock pulses, counters are of two types, Synchronous and Asynchronous. Here, synchronous counters are used, as the clock pulse across all the flip-flops used are same and are derived from common source at same time. Clocks can be used as (posedge)positive edge triggered or (negedge)negative edge triggered.

II. State Diagram

The state diagram of the desired system is given in the Figure 1. Clock has been applied in all the flip-flops used in the circuit. There is a control switch M, which is used to control the counting of counter. When M = 0, counter will behave as Even-Counter and when M = 1, counter will behave is Odd-Counter. Hence when M = 0, counter starts counting from 000→010→100→110→000, while when the control input is changed to M = 1, no matter what the last counting was, the counter will reset to 000 and then Odd-Counter starts from 001→011→101→111→001.

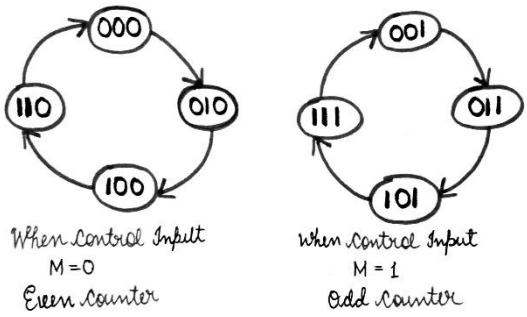

Fig. 1. State diagram for Odd-Even Counter

III. Waveform

The Figure 2 shows the functioning the system defined in Figure 1. Here Clk stands for Applied Clock Pulse. Time has been defined on x-axis and digital signals logic 1 and logic 0 has been defined on y-axis. Q0 is Least Significant Bit while Q2 is the Most Significant Bit.

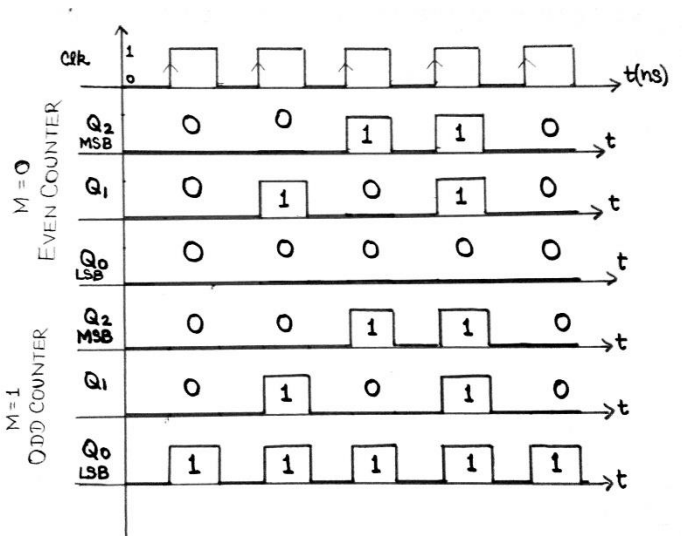

Fig. 2. Waveforms of Odd-Even Counter

References

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