Sensitivity Analysis

Summary

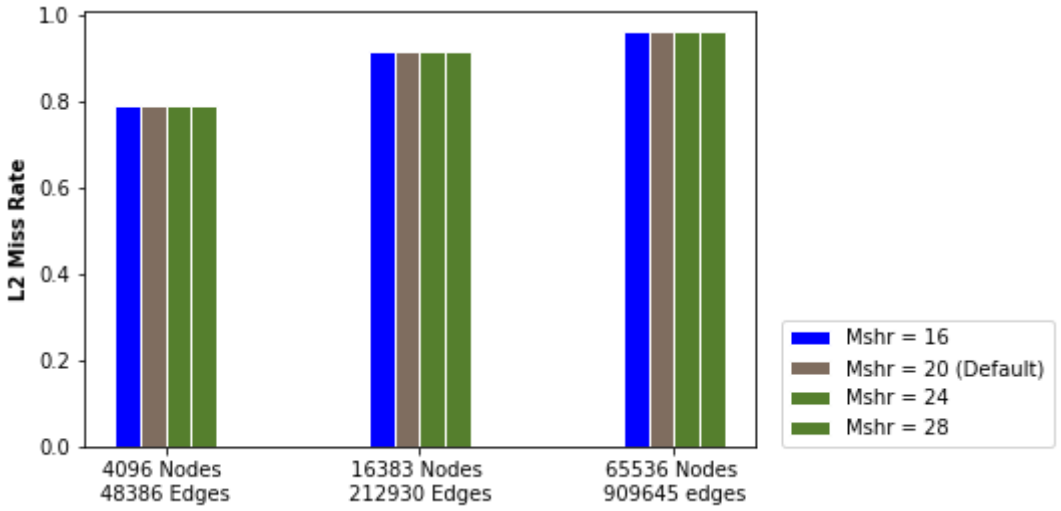
A sensitivity analysis has been performed to have an Increased understanding of the relationships between input and output variables in a system. Input variables are the following:

Graph Size
Association
Prefetcher
Replacement policy
Number of write buffers
Number of miss status handling registers (MSHR).

Output variable is the miss rate of L2 cache.

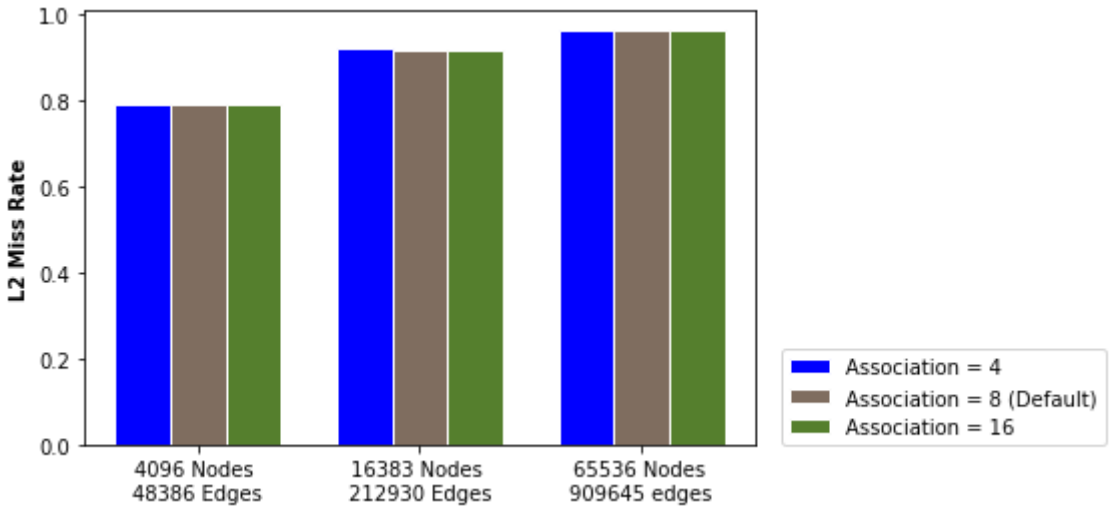
Results

Only number of L2 miss status handling register (MSHR) changed:



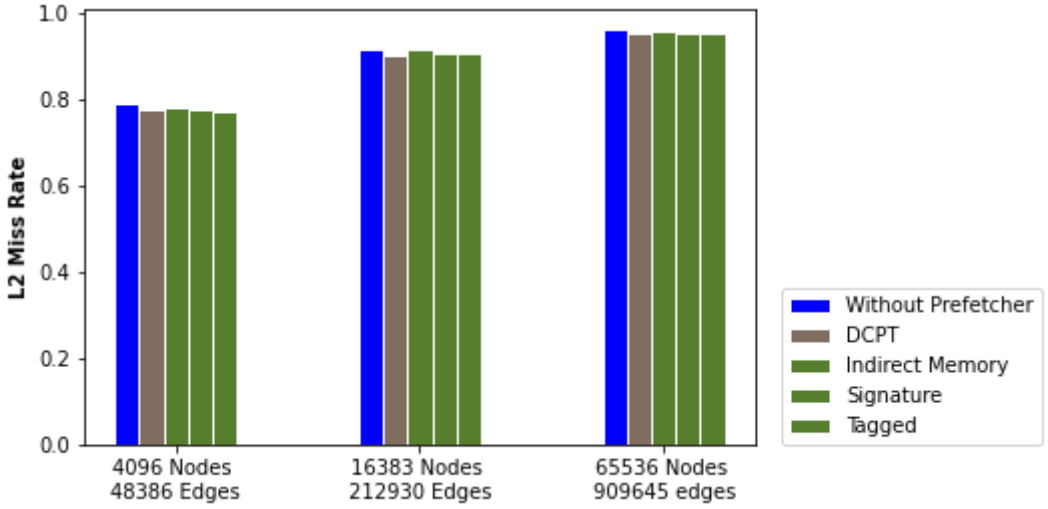
Graph Size	**mshr16**	**mshr20 (default)**	**mshr24**	**mshr28**
4096 Node	0.79231	0.792062	0.792062	0.792062
16383 Node	0.918557	0.918588	0.918588	0.918588
65536 Node	0.96272	0.962732	0.962732	0.962732

Only L2 association changed:



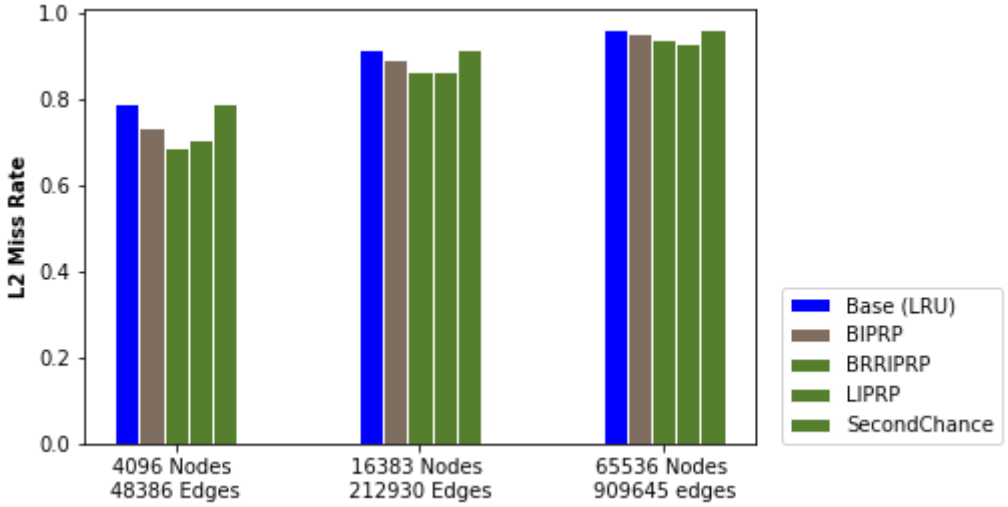
Graph Size	**Assoc4**	**Assoc8 (Default)**	**Assoc16**
4096 Node	0.790253	0.792062	0.790679
16383 Node	0.920258	0.918588	0.917401
65536 Node	0.963627	0.962732	0.962037

Only L2 prefetcher changed:



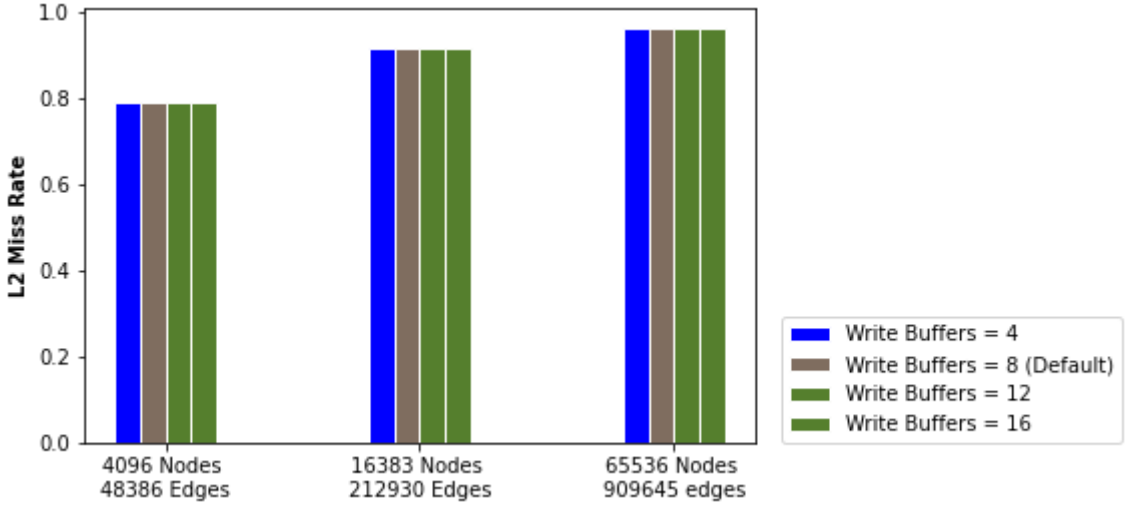
Graph Size	**Base**	**DCPT**	**Indirect Memory**	**Signature**	**Tagged**
4096 Node	0.792062	0.775529	0.78171	0.775014	0.771912
16383 Node	0.918588	0.903899	0.915643	0.907275	0.909079
65536 Node	0.962732	0.951888	0.960298	0.952865	0.955021

Only L2 replacement policy changed:



Graph Size	**Base**	**BIPRP**	**BRRIPRP**	**LIPRP**	**SecondChance**
4096 Node	0.792062	0.733296	0.688941	0.707409	0.790894
16383 Node	0.918588	0.892981	0.86763	0.864498	0.918048
65536 Node	0.962732	0.95444	0.941707	0.931166	0.962397

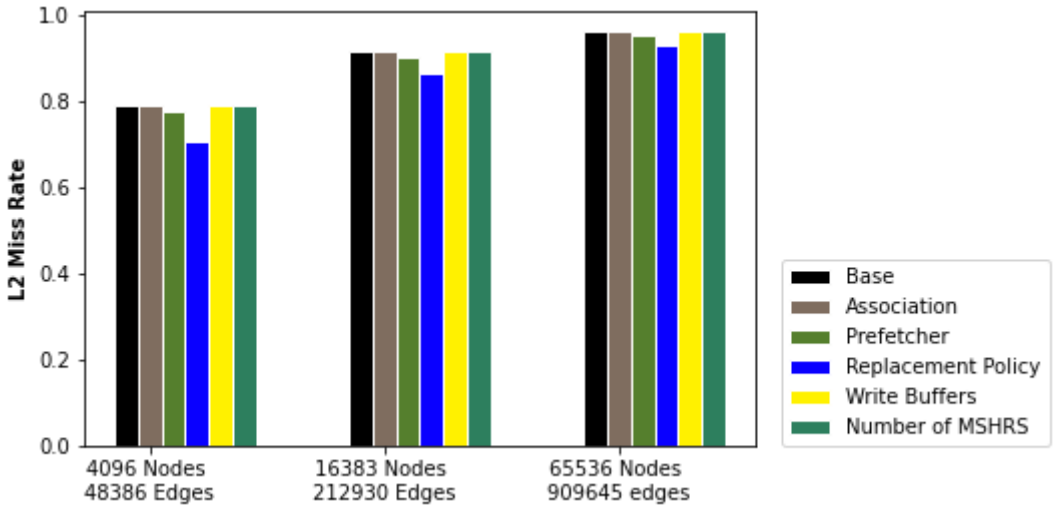
Only number of L2 write buffers changed:



write4	write8	write12	write16
0.792235	0.792062	0.792082	0.792082

0.918456	0.918588	0.918598	0.918598
0.962592	0.962732	0.962704	0.962704

All variables combined:



Graph Size	**Base**	**Association**	**No of MSHRS**	**Prefetcher**	**Replacement Policy**	**Write Buffer**
4096 Node	0.792062	0.790253	0.792062	0.775529	0.707409	0.792082
16383 Node	0.918588	0.917401	0.918557	0.903899	0.864498	0.918598
65536 Node	0.962732	0.962037	0.96272	0.951888	0.931166	0.962704

Conclusions

- Changing number of MSHR, number of write buffer and association have almost no effect on the L2 cache miss rate.
- Adding a prefetcher improves the L2 cache miss rate. Delta Correlating Prediction Tables[1] (DCTP) prefetcher performs better than other prefetchers as the graph size increases.
- LRU Insertion Policy (LIP) is a specific case of Bimodal Interval Prediction (BIP) replacement policy where bimodal throttle parameter is 0. Since it is a trash resistant policy, it improves the miss rate for memory intensive workloads[2].

References

1. https://www.jilp.org/vol13/v13paper2.pdf
2. https://people.csail.mit.edu/emer/papers/2007.06.isca.dip.pdf