88E6141 Datasheet

6-port Gigabit Ethernet Switch with 4 Integrated GE PHYs and 2.5 Gbps Serdes

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Document Conventions

	**Note:** Provides related information or information of special importance.
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Document Status

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Preface

About this Document

The 88E6141 datasheet is part of a multi-part set that includes the following documents:

- **Link Street® 88E6341/88E6141 Switch Functional Specification**
  Provides a a functional description of the device core.

- **Link Street® 88E6341/88E6141 PHY and SERDES Functional Specification**
  Provides a functional description of the PHY and SERDES.

- **Link Street® Integrated Management Processor (IMP) Functional Specification**
  Provides a description of the Integrated Management Processor.

88E6141 Datasheet

6-port Gigabit Ethernet Switch with 4 Integrated GE PHYs and 2.5 Gbps Serdes

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OVERVIEW

The Marvell® 88E6141 device is a single-chip integration of a 6-port Ethernet switch with four integrated Gigabit Ethernet transceivers and one SerDes interface. This device supports “Best in Class” Quality of Service (QoS) and the highest “real world” performance. This device is uniquely suited for Small Office Home Office (SOHO) and Small-to-Medium Business (SMB) applications.

The device contains four 10/100/1000 triple speed Ethernet transceivers (PHYs), one SerDes interface and one digital interface that supports a combination of RGMII, MII, and RMII interfaces in an 88-lead QFN package.

The sixth port is a SerDes interface supporting 2500BASE-X (2.5Gbps), 1000BASE-X, and SGMII.

The device has a high-speed, non-blocking four traffic class QoS switch fabric that uses the unique Marvell Dynamic Queue Limit architecture. The QoS architecture switches packets into one of four traffic class queues based upon Port, IEEE 802.1p, IPv4 Type of Service (TOS) or Differentiated Services (Diff-Serv), IPv6 Traffic Class, 802.1Q VLAN ID, DA MAC address or SA MAC address. The device also contains a high-performance address lookup engine with support for up to 2K active nodes, and a 1Mbit frame buffer memory. Back-pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The MAC units in the devices comply fully with the applicable sections of IEEE 802.3 and support frame sizes up to 10KBytes.

The device’s RGMII (or MII/RMII) interface supports a direct connection to Management or Router CPUs with integrated MACs. This interface, along with BPDU handling for IEEE 802.1D Spanning Tree Protocol, 802.1w Rapid Spanning Tree, 802.1s Multiple VLAN Spanning Tree, programmable per-port VLAN configurations, 802.1Q and Port States, supports fully managed switches and truly isolated WAN vs. LAN firewall applications. The device supports 4,096 802.1Q VLAN IDs which can be enabled on a per port basis. Three levels of 802.1Q security is supported with error frame trapping and logging.

The device supports multiple address databases (up to 4096), which allows packet routing without modification of the MAC address. This allows the same MAC address to exist multiple times in the MAC Address database with multiple port mappings, to completely isolate the WAN from the LAN database.

The PHY units in the device support the latest 802.3az Energy Efficient Ethernet (EEE) standard. They are designed with Marvell® cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. The device also integrates MDI interface termination resistors into the PHYs. This resistor integration facilitates board layout and reduces board cost by reducing the number of external components. Both the PHY and MAC units in the devices comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

The PHYs also include an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

The 88E6141 also supports Wake-on-LAN and Wake on Frame event detection allowing an attached CPU to enter sleep mode and enabling even greater system power savings.

The device supports up to 16 LEDs (3 per port). The combining of multiple ports Link/Activity LED into a single LED is also supported.

The 88E6141 device also includes an integrated 200 MHz microprocessor with 60Kbytes of integrated RAM. The microprocessor’s has direct access to all switch registers and its integrated Ethernet controller enables support for Ethernet protocols as well as lightly managed or smart switches.

The device also integrates an I^2C master interface for connection and control of external peripherals.

The device’s many operating modes can be configured using SMI (serial management interface - MDC/MDIO) or through the Remote Management Interface. The device also supports a standalone QoS mode or configuration via a low cost serial EEPROM.

Highlighted Features

- Integrated 200MHz Z80 compatible microprocessor
  - Integrated60Kbyte zero wait state RAM
  - Boots via EEPROM, SMI interface, or Remote Management Unit
  - Integrated Ethernet NIC connects directly to switch fabric
- Supports 802.3az Energy Efficient Ethernet
- Wire speed performance with Maximum Frame size up to 10K Bytes
- Quality of Service support with 4 traffic classes
- QoS determined by Port, IEEE 802.1p tagged frames, IPv4's Type of Service (TOS) & Differentiated Services (DS), IPv6's Traffic Class 802.1Q VID, Destination MAC address, or Source MAC address
- Frame and Queue priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- 'Best-in-Class' per port TCP/IP Ingress Rate Limiting along with independent Storm Prevention
  - Integrated power monitor and power reset controller
  - 5 Ingress Rate Limiting buckets per port, supporting Rate-based and Priority-based rate limiting
  - Non-Rate Limited frames based on SA or DA
- Per port, programmable MAC hardware address learn limiting
- Wake-on-LAN and Wake of Frame Event Detection
- Layer 2 Policy Control List (PCL) enables drop, trap, or mirroring based on SA, DA, VID, Ethertype, VBAS, PPPoE, UDP, and DHCP Option 82
- Remote Management capabilities allow device configuration and readback via Ethernet frames
- Per port, programmable MAC hardware address learn limiting
- DSCP (layer 3) to frame priority (layer 2) marking
- Frame and Queue priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Strict, Weighted, or mixed mode QoS selectable per port
- Globally Programmable QoS weighting via a 128-entry table
- 802.1Q VLAN support for the full 4,096 VLAN IDs
- Supports multiple provider ports within a single chip via a programmable Ethertype per port
- Enhanced 802.1s Per VLAN Spanning Tree supporting up to 64 spanning tree instances
- I^2C Master interface

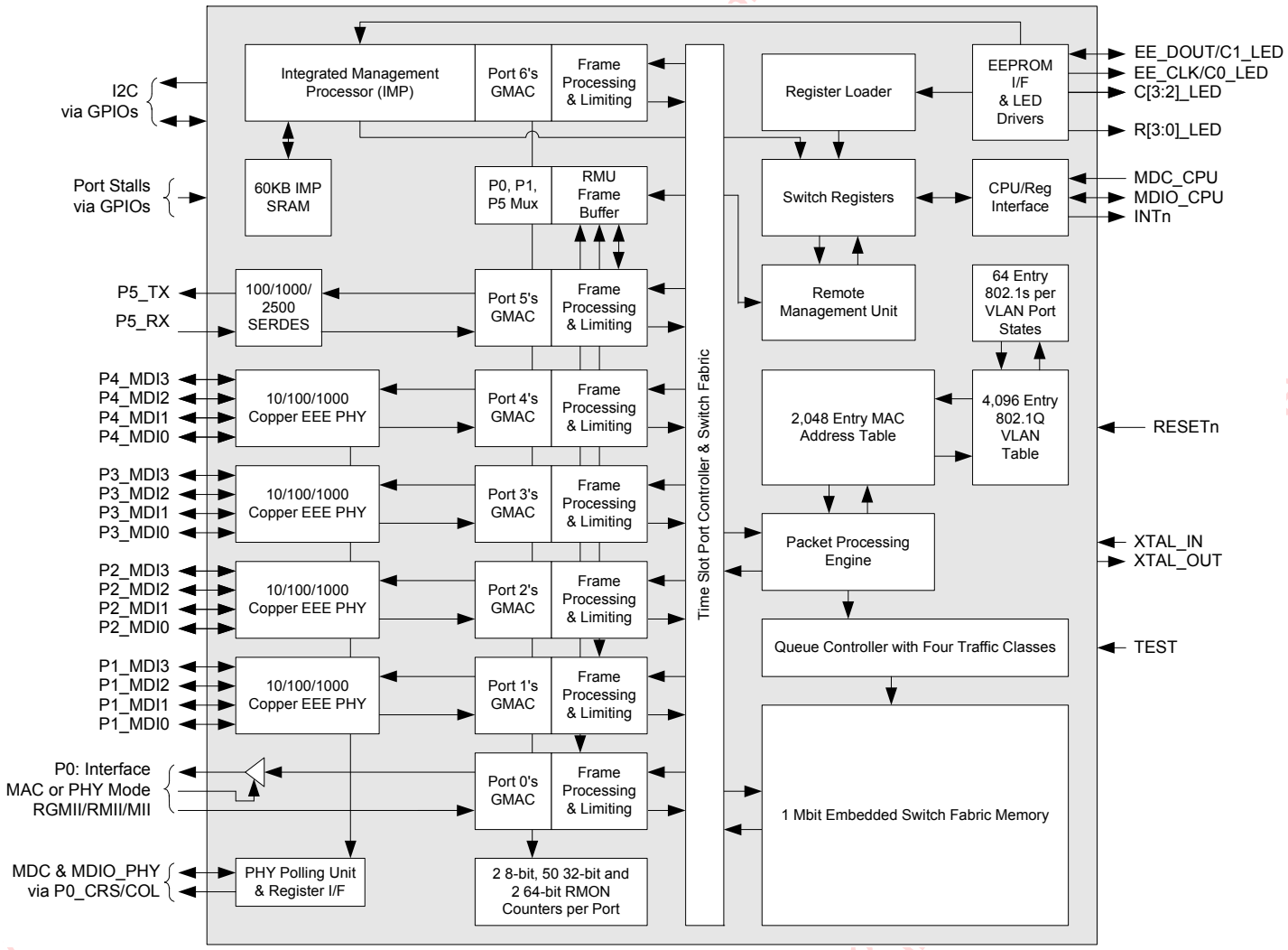
Features

- Marvell® Header for increased Routing performance
- Shared 1Mbit on-chip memory-based switch fabric with true non-blocking switching performance
- High performance lookup engine with support for up to 2K MAC address entries with automatic learning and aging
- MAC SA based 802.1X authentication
- Port Trunking and Port Monitoring/Mirroring
- Egress tagging/untagging selectable per port or by 802.1Q VLAN ID
- Port based VLANs supported in any combination across multiple chips
- Port States & BPDU handling for Spanning Tree
- 28 32-bit and 2 64-bit RMON Counters per port
- Egress Rate shaping on all ports
- Strict, Weighted, or mixed mode QoS selectable per port
- Integrated SerDes interface
  - Supports 2500BASE-X, 1000BASE-X, and SGMII
- 4 integrated Gigabit Ethernet PHYs fully compliant with the applicable sections of IEEE802.3 and IEEE802.3u
  - Integrated MDI interface termination resistors
  - Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- RGMII/MII/RMII interface supporting 1.8V, 2.5V, or 3.3V I/O
- Supports 2-Wire EEPROMs for configuration
  - 32Kbit to 512Kbit densities supported
  - Able to program attached EEPROMs to save configurations
- 10 x 10mm 88-lead QFN package

Applications

- Broadband Gateway
- Industrial Switch

Figure 1: 88E6141 Block Diagram



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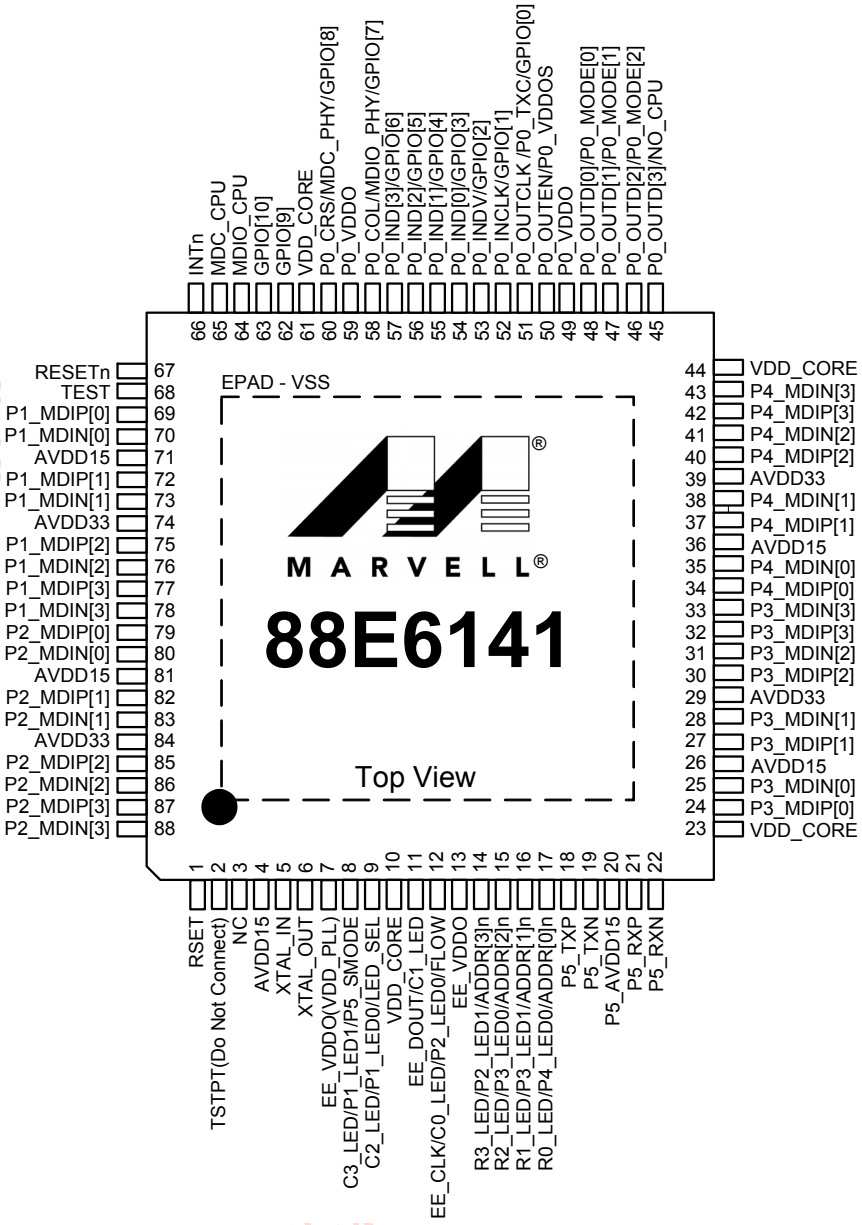
1 Signal Description

1.1 Pin Map

Figure 2: 88E6141 Device Pin Map



1.2 Pin Description

Table 1: Network 1G/2.5G SERDES Interface (Port 5)

Pin #	Pin Name	Type	Description
21	P5_RXP	Input	Port 5 receiver input – Positive. P5_RXP connects directly to the fiber-optic receiver's positive output or to another device's TXP (Transmitter output – Positive) pins.
22	P5_RXN	Input	Port 5 receiver input – Negative. P5_RXN connects directly to the fiber-optic receiver's negative output or to another device's TXN (Transmitter output – Negative) pins.
18	P5_TXP	Output	Port 5 transmitter output – Positive. P5_TXP connects directly to the fiber-optic transmitter's positive input or to another device's RXP (Receiver input – Positive) pins.
19	P5_TXN	Output	Port 5 transmitter output – Negative. P5_TXN connects directly to the fiber-optic transmitter's negative input or to another device's RXN (Receiver input – Negative) pins.

Note

This device supports internal terminated media pins. They must be left floating if they are unused.

Table 2: Network 10/100/1000 PHY Interface (Ports 1 to 4)

Pin #	Pin Name	Type	Description
34 24 79 69 35 25 80 70	P4_MDIP[0] P3_MDIP[0] P2_MDIP[0] P1_MDIP[0] P4_MDIN[0] P3_MDIN[0] P2_MDIN[0] P1_MDIN[0]	Input/Output	Media Dependent Interface [0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] corresponds to BI_DA±. In MDIX configuration, MDIP/N[0] corresponds to BI_DB±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] must be left floating if not used.
37 27 82 72 38 28 83 73	P4_MDIP[1] P3_MDIP[1] P2_MDIP[1] P1_MDIP[1] P4_MDIN[1] P3_MDIN[1] P2_MDIN[1] P1_MDIN[1]	Input/Output	Media Dependent Interface [1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] corresponds to BI_DB±. In MDIX configuration, MDIP/N[1] corresponds to BI_DA±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. MDIP/N[1] must be left floating if not used.
40 30 85 75 41 31 86 76	P4_MDIP[2] P3_MDIP[2] P2_MDIP[2] P1_MDIP[2] P4_MDIN[2] P3_MDIN[2] P2_MDIN[2] P1_MDIN[2]	Input/Output	Media Dependent Interface [2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] corresponds to BI_DC±. In MDIX configuration, MDIP/N[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. MDIP/N[2] must be left floating if not used.
42 32 87 77 43 33 88 78	P4_MDIP[3] P3_MDIP[3] P2_MDIP[3] P1_MDIP[3] P4_MDIN[3] P3_MDIN[3] P2_MDIN[3] P1_MDIN[3]	Input/Output	Media Dependent Interface [3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] corresponds to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. MDIP/N[3] must be left floating if not used.

Table 3: Reference, Clock and Reset

Pin #	Pin Name	Type	Description
1	RSET	Analog	Resistor Current reference. A 4.99k ohm 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.
5	XTAL_IN	Input	25 MHz system reference clock input provided from the board. The clock source can come from an external crystal or an external oscillator. This is the only clock required (for small package). Refer to Section TBD for “Clock Timing” timing requirements.
6	XTAL_OUT	Output	System reference clock output provided to the board. This output can only be used to drive an external crystal. It cannot be used to drive external logic. If an external oscillator is used this pin should be left unconnected.
67	RESETn	Input, PU	Hardware reset. Active low. The device is configured during reset. When RESETn is low some configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or sometime after. Other configuration pins are active during RESETn low and become inputs after RESETn rises. These pins latch their configuration data sometime after RESETn rises and then these pins become their defined function. Refer to section TBD of the AC Electrical Specifications for Reset and Configuration Timing details.

Table 4: Port Status LEDs

Pin #	Pin Name	Type	Description
14 15 16 17	R3_LED /P2_LED1 /ADDR[3]n R2_LED /P3_LED0 /ADDR[2]n R1_LED /P3_LED1 /ADDR[1]n R0_LED /P4_LED0 /ADDR[0]n	Typically Output, PU	Parallel multiplexed LED outputs. These active low LED pins directly drive the port's LEDs supporting a range from 1 to 4 LEDs in a multiplexed fashion. In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to one of the Cx_LED pins below. These same pins can be used to directly drive from 1 to 4 LEDs in a non-multiplexed fashion (4 from this set of pins – P[4:3]_LED0, P[3:2]_LED1). In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to a power source. The LEDs can be configured to display many options (see section TBD). The LEDs are turned on whenever RESETn is low so their functionally can be visually verified during PCB manufacturing testing. Rx_LED are multifunction pins which are used to configure the device after a hardware reset. After reset is asserted, the Rx_LED pins become inputs and the configuration information below is latched 1 mSec after the rising edge of RESETn as follows: ADDR[3:0]n sets the device's SMI address. Note: The inverted values 'seen' on these CONFIG pins are used as the SMI address. If ADDR[3:0] are all 0's the device is configured in single device addressing mode (the default value due to the internal pull up resistors Rx_LED pins are internally pulled high via a resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to VSS for a configuration low.
11	EE_DOUT /C1_LED	Input/Output, PU	Serial EEPROM data I/O to/from a 2-wire EEPROM device and Column 0 for the LEDs. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive and send the EEPROM address/data to/from the external serial EEPROM (if present). 2-wire EEPROMs require that this pin is connected to EE_VDDO through a 4.7k ohm pull-up resistor. EE_DOUT is internally pulled high via a resistor so the pin can be left floating when unused.

Table 4: Port Status LEDs (Continued)

Pin #	Pin Name	Type	Description
12	EE_CLK /C0_LED /P2_LED0 /FLOW	Typically Output, PD	Serial EEPROM clock and column 1 for the LEDs. EE_CLK is the serial EEPROM clock reference output by the devices. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin which is also used to connect to the anode of LED column 1 for each row, if used in the multiplexed LED mode (see R[3:0]_LED above). If EEPROM is not connected, then this pin can be used to directly drive a LED in a non-multiplexed fashion (P1_LED0). If EEPROM is connected, this pin cannot be used when the LEDs are in a non-multiplexed mode It is also used to configure the device after a hardware reset. After reset is asserted, EE_CLK becomes an input and the FLOW configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0x0 = Disable flow control on all ports 0x1 = Enable advertisement of full-duplex flow control on all PHYs and enable “forced collision” flow control on all half duplex ports Full-duplex flow control requires support from the end station. It is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (i.e., FLOW = 1 at reset), and sees that the end station also supports Pause (from data returned during Auto-Negotiation). Half-duplex flow control is active on all half-duplex ports when enabled. Note: The inverted values ‘seen’ on these CONFIG pins are use by internal logic. EE_CLK is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to EE_VDDO for a configuration high.
9	C2_LED /P1_LED0 /LED_SEL	Typically Output, PD	C2_LED is a multi-function pin which is used to connect to the anode of LED column 2 for each row, if used in the multiplexed LED mode (see R[3:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P1_LED0). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. It is also used to configure the device after a hardware reset. After reset is asserted, C2_LED becomes an input and the LED_SEL configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0 = Link/Activity w/ Separate Speed LED 1 = Link/Activity w/ Speed by 3 Color C2_LED is internally pulled low via a resistor so the pin can be left floating when unused.

Table 4: Port Status LEDs (Continued)

Pin #	Pin Name	Type	Description
8	C3_LED /P1_LED1 /P5_SMODE	Typically Output, PD	C3_LED is a multi-function pin which is used to connect to the anode of LED column 3 for each row, if used in the multiplexed LED mode (see R[4:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P1_LED1). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. It is also used to configure the device after a hardware reset. After reset is asserted, C3_LED becomes an input and the p5_SMODEconfiguration information below is latched 1 mSec after the rising edge of RESETn as follows: 0 = 2.5Gbps Operation. 1 = SGMII/1000X Operation base on the whether PHY is detected connecting to P5 (see PHYDetect bit 0x0 bit[12]). C3_LED is internally pulled low via a resistor so the pin can be left floating when unused.

Table 5: Port 0 xMII Receive Interface

Pin #	Pin Name	Type	Description
52	P0_INCLK /GPIO[1]	Input/Output, PU	Input Clock. INCLK is a reference for INDV and IND. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. INCLK is an output when the xMII is configured in a PHY mode (when the port's Px_MODE = 0x0, or 0x1) or when it is a GPIO pin which is configured to be an output. When the port is in RMII mode or disabled (by its Px_MODE = 0x4, 0x5 or 0x6) this pin becomes GPIO[1]. INCLK is tri-stated during RESETns and it is internally pulled high so the pin can be left floating when unused.
53	P0_INDV /GPIO[2]	Input, PD	Input Data Valid. Input Data Valid is used to indicate when IND[3:0] (or IND[1:0] where appropriate) contains frame information. INDV must be synchronous to INCLK for all modes except for RMII modes where INDV must be synchronous to OUTCLK. In RGMII mode INDV is used as RX_CTL. When this port is disabled (by its Px_MODE = 0x6) this pin becomes GPIO[2]. INDV is internally pulled low via resistor so the pin can be left floating when unused.
57 56 55 54	P0_IND[3] /GPIO[6] P0_IND[2] /GPIO[5] P0_IND[1] /GPIO[4] P0_IND[0] /GPIO[3]	Input, PU	Input Data. IND[3:0] (or IND[1:0] where appropriate) receives the data to be sent into the switch. IND must be synchronous to INCLK for all modes except for RMII modes. In MII, 200BASE, 100BASE and 10BASE modes IND[3:0] is used. In RMII modes only IND[1:0] are used and they must be synchronous to OUTCLK. In RGMII mode IND[3:0] are used as RXD[3:0]. When this port is disabled (by its Px_MODE = 0x6) these pins becomes GPIO[6:3]. When the port is in RMII mode (by its Px_MODE = 0x4 or 0x5) IND[3:2] become GPIO[6:5]. The IND pins are internally pulled high via resistor so the pins can be left floating when unused.

Table 5: Port 0 xMII Receive Interface (Continued)

Pin #	Pin Name	Type	Description
60	P0_CRS /MDC_PHY /GPIO[8]	Input/Output, PU	Carrier Sense, Management Data Clock, Master, or GPIO[8]. Carrier sense is used to indicate carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is CRS when the port's Px_MODE = 0x1 or 0x2. CRS is an output for Px_MODE = 0x1 and it's an input for Px_MODE = 0x2. As a Management Data Clock, in Master mode, this pin is the reference clock output for the serial management interface (SMI) that connects to an external SMI slave device, typically external PHYs. This pin is MDC_PHY when the port's Px_MODE <> 0x1 or 0x2 and the NO_CPU configuration pin was high at the rising edge of RESETn[1]. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. Alternatively, this pin becomes GPIO[8] which supports an option to be an enable input for Ports 0. In this mode, when this pin is high, the selected port[2] will be enabled. When low the pins being used for the Port's interface will be tri-stated and the port's link will be down[3]. CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the port's Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P0_ ENABLE[4].

Table 5: Port 0 xMII Receive Interface (Continued)

Pin #	Pin Name	Type	Description
58	P0_COL /MDIO_PHY /GPIO[7]	Input/Output, PU	Collision, or Management Data I/O, Master, or GPIO[7]. Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. COL is not synchronous to INCLK. COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's Px_MODE = 0x1 or 0x2. COL is an output for Px_MODE = 0x1 and it's an input for Px_MODE = 0x2. As a Management Data I/O, in Master mode, this pin is used to transfer management data in and out of the device synchronously to MDC_PHY. This pin requires an external pull-up resistor in the range of 4.7K to 10K ohm. This pin is MDIO_PHY when the port's Px_MODE is not 0x1 or 0x2 and the NO_CPU configuration pin was high at the rising edge of RESETn[5]. This device uses External SMI Addresses 0x10 or 0x15 to access the external PHYs for ports 0 and 5 respectively. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. Alternatively, this pin becomes GPIO[7] which supports an option to be an enable input for Ports 0. In this mode, when this pin is high, the selected port[6] will be enabled. When low the pins being used for the Port's interface will be tri-stated and the port's link will be down[7]. COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the port's Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P0_ ENABLE[8].

1. The NO_CPU configuration pin is used to determine the initial function of this pin after reset. The pin's function can be modified by changing a register (see section TBD).
2. The port selection is configured via register (see section TBD).
3. The port's link can be forced up or down via registers (see Port offset 0x01).
4. Certain GPIO pins can be configured to be P0_ENABLE. See Section 2.4.
5. The NO_CPU configuration pin is used to determine the initial function of this pin after reset. The pin's function can be modified by changing a register (see section TBD).
6. The port selection is configured via register (see section TBD).
7. The port's link can be forced up or down via registers (see Port offset 0x01).
8. Certain GPIO pins can be configured to be P0_ENABLE. See Section 2.4.

Table 6: Port 0 xMII Transmit Interface

Pin #	Pin Name	Type	Description
50	P0_OUTEN /P0_VDDOS	Typically Output, PD	Output Enable. Output enable is used to indicate when OUTD[3:0] or OUTD[1:0] contains frame information. OUTEN is synchronous to OUTCLK in all modes. In RGMII mode OUTEN is used as TX_CTL. P0_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: P0_VDDOS 0 = The P0_VDDO pins are powered by 3.3 volts 1 = The P0_VDDO pins are powered by 2.5 volts P0_OUTEN is tri-stated during RESETn or when P0_ ENABL[1]E is low. P0_OUTEN is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to P0_VDDO for a configuration high.
51	P0_OUTCLK /P0_TXC /GPIO[0]	Input/Output, PU	Output Clock. OUTCLK is a clock reference for OUTEN and OUTD[3:0]. The speed of OUTCLK is 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depends on the speed of the Port. The direction of OUTCLK is a function of the port's Px_MODE (Port offset 0x00). See the C_Mode register bits in Port offset 0x00. In RGMII mode OUTCLK is used as TXC. In RMII mode OUTCLK is used as REFCLK. When this port is disabled (by its Px_MODE = 0x6) this pin becomes GPIO[0]. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 6: Port 0 xMII Transmit Interface (Continued)

Pin #	Pin Name	Type	Description
45 46 47 48	P0_OUTD[3] /NO_CPU P0_OUTD[2] /P0_MODE[2] P0_OUTD[1] /P0_MODE[1] P0_OUTD[0] /P0_MODE[0]	Typically Output, PU	Output Data. OUTD[3:0] (or OUTD[1:0] where appropriate) outputs the data to be transmitted from the switch. OUTD is synchronous to OUTCLK in all modes. In RGMII mode OUTD[3:0] are used as TXD[3:0]. In RMII mode OUTD[1:0] are used and OUTD[3:2] are tri-stated. P0_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: OUTD[3] = No CPU OUTD[2:0] = P0_MODE[2:0] No CPU selects the flow control setting as follows: 0 = CPU is attached 1 = No CPU is attached When the 'CPU is attached' mode is selected, all the ports will be initialized in the Disabled Port State and the PHYs will be powered down. This allows software time to boot and fully configure the switch before it allows packets to flow through it. Whenever the switch is used with a CPU, the 'CPU is attached' mode must be used. P0_MODE[2:0] sets Port 0's Mode of operation as follows: 0x0 = Full Duplex Only MII PHY Mode[2] 0x1 = MII PHY mode w/output MII CLKs[3] at 2.5, 25 or 50 MHz[4] 0x2 = MII MAC mode w/input MII CLKs 0x3 = Reserved for future use 0x4 = RMII PHY mode w/output P0_OUTCLK at 50 MHz 0x5 = RMII MAC mode w/input P0_OUTCLKs at 50 MHz 0x6 = Port disabled (with its pins tri-stated)[5] 0x7 = RGMII mode P0_OUTD pins are tri-stated during RESETn or when P0_ ENABLE[6] is low. OUTD pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to VSS for a configuration low.

1. Certain GPIO pins can be configured to be P0_ENABLE. See Section 2.4.
2. This mode is identical to P0_MODE 0x1 except the P0_CRS and P0_COL pins are used for other functions.
3. P0's MII CLKs refer to both P0_OUTCLK and P0_INCLK.
4. P0_OUTCLK's frequency is determined by the port's ForceSpd and AltSpeed bits (Port offset 0x01).
5. In this mode many of P0's pins become GPIO pins.
6. Certain GPIO pins can be configured to be P0_ENABLE. See Section 2.4.

Table 7: GPIO

Pin #	Pin Name	Type	Description
62 63	GPIO[9] GPIO[10]	Input/Output, PU	General Purpose I/O pins. GPIO[10:9] are general purpose input/output pins whose direction and data is controllable via switch registers See P0_VDDO for the list of pins that are powered by this rail. GPIO[10:9] pins are internally pulled high via resistor so the pins can be left floating when unused.

Table 8: System & Register Access

Pin #	Pin Name	Type	Description
65	MDC_CPU	Input, PU	Management Data Clock, Slave. MDC_CPU is the reference clock input for the serial management interface (SMI) that connects to an external SMI master, typically a CPU. A continuous clock stream is not expected. The maximum frequency supported is 20.0 MHz The CPU's SMI interface is used to access the device's registers but it cannot be used until the device's INTn pin becomes active low (indicating the Register Loader is done processing the EEPROM or that no EEPROM was present). MDC_CPU is internally pulled high via a resistor so it can be left floating when unused. **NOTE:** MDC_CPU is powered by the P0_VDDO pins and this pin is 3.3V tolerant if P0_VDDO is powered at 2.5V.
64	MDIO_CPU	Input/Output, PU	Management Data I/O, Slave. MDIO_CPU is used to transfer management data in and out of the device synchronously to MDC_CPU. This pin requires an external pull-up resistor in the range of 4.7K to 10K Ω. The device uses one or all of the 32 possible SMI port addresses (two modes are supported). The address(es) that are used are selectable using the Rx_LED/ADDRn configuration pins. MDIO_CPU is internally pulled high via a resistor so it can be left floating when unused. **NOTE:** MDIO_CPU is powered by the P0_VDDO pins and this pin is 3.3V tolerant if P0_VDDO is powered at 2.5V.
66	INTn	Input/Open Drain Output	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required somewhere on this interrupt net for it to go high when it is inactive. The INTn pin will go active low which indicates the SMI interface (MDC_CPU/MDIO_CPU pins) is available for use.
68	TEST	Input, PD	Test Input. Test is used to place the chip into its manufacturing test modes. Do not connect this pin to anything other than VSS or improper device operation may result. TEST is internally pulled low via resistor so the pin can be left floating when unused.
2	TSTPT	O	DC Test Point. The TSTPT pin should be left floating if not used.

Table 9: Power & Ground

Pin #	Pin Name	Type	Description
49 59	P0_VDDO	Power	Power to Port 0's interface as well as the CPU interface. P0_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P0_VDDOS must be configured accordingly – see P0_OUTEN). 1.8V configuration will be automatically detected by internal voltage sensing logic.
13	EE_VDDO	Power	Power to LED, EEPROM interface (C3_LED, C2_LED, EE_DOUT, EE_CLK, R3_LED, R2_LED, R1_LED, R0_LED) and the RESETn pin. EE_VDDO must be connected to 3.3V for 3.3V I/O.
7	EE_VDDO (VDD_PLL)	Power	Power to PLL EE_VDDO must be connected to 3.3V for 3.3V I/O.
4 26 36 71 81	AVDD15	Power	1.5V power to analog core used to power each Gig PHY interface.
29 39 74 84	AVDD33	Power	3.3V power to analog core used to power each Gig PHY interface.
20	P5_AVDD15	Power	1.5V power to analog core used to power the SERDES interface.
10 23 44 61	VDD_CORE	Power	1.15V power to digital core.
EPAD	VSS	Ground	Ground to the device. The device is packaged in an 88-pin package with an E-PAD (exposed die pad) on the bottom of the package. This E-PAD must be soldered to VSS as it is the main VSS connection on the device. See Table 45, 88-pin QFN (10x10mm) Package Dimensions, on page 83 for details.
3	NC		No Connect. Do not connect this pin to anything. This pin must be left unconnected.

1.3 Pin Assignment List

Table 10: Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
4	AVDD15
26	AVDD15
36	AVDD15
71	AVDD15
81	AVDD15
29	AVDD33
39	AVDD33
74	AVDD33
84	AVDD33
9	C2_LED/P1_LED0/LED_SEL
8	C3_LED/P1_LED1/P5_SMODE
12	EE_CLK/C0_LED/P2_LED0/FLOW
11	EE_DOUT/C1_LED
13	EE_VDDO
7	EE_VDDO(VDD_PLL)
63	GPIO[10]
62	GPIO[9]
66	INTn
65	MDC_CPU
64	MDIO_CPU
3	NC
58	P0_COL/MDIO_PHY/GPIO[7]
60	P0_CRS/MDC_PHY/GPIO[8]
52	P0_INCLK/GPIO[1]
54	P0_IND[0]/GPIO[3]
55	P0_IND[1]/GPIO[4]
56	P0_IND[2]/GPIO[5]
57	P0_IND[3]/GPIO[6]
53	P0_INDV/GPIO[2]
51	P0_OUTCLK /P0_TXC/GPIO[0]
48	P0_OUTD[0]/P0_MODE[0]
47	P0_OUTD[1]/P0_MODE[1]
46	P0_OUTD[2]/P0_MODE[2]
45	P0_OUTD[3]/NO_CPU
50	P0_OUTEN/P0_VDDOS
49	P0_VDDO
59	P0_VDDO
70	P1_MDIN[0]
73	P1_MDIN[1]
76	P1_MDIN[2]
78	P1_MDIN[3]
69	P1_MDIP[0]
72	P1_MDIP[1]
75	P1_MDIP[2]
77	P1_MDIP[3]
80	P2_MDIN[0]
83	P2_MDIN[1]
86	P2_MDIN[2]
88	P2_MDIN[3]
79	P2_MDIP[0]
82	P2_MDIP[1]
85	P2_MDIP[2]
87	P2_MDIP[3]
25	P3_MDIN[0]
28	P3_MDIN[1]

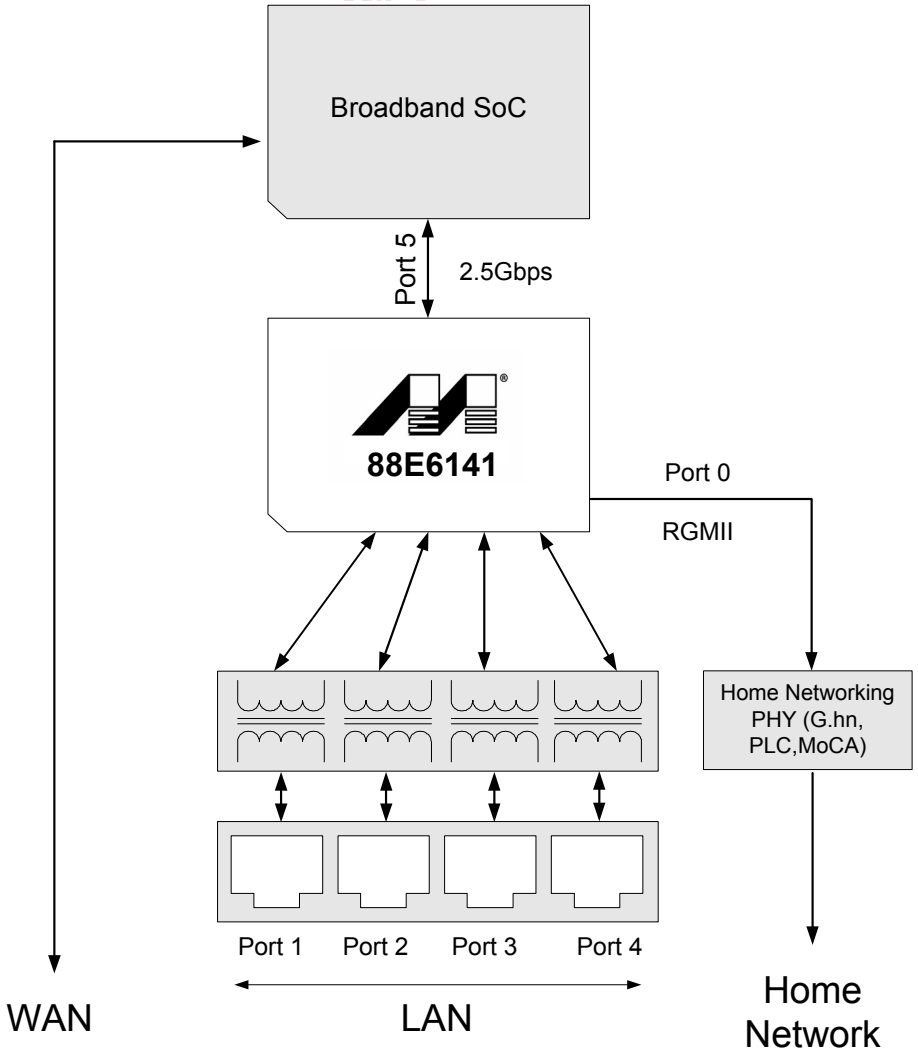
Pin Number	Pin Name
31	P3_MDIN[2]
33	P3_MDIN[3]
24	P3_MDIP[0]
27	P3_MDIP[1]
30	P3_MDIP[2]
32	P3_MDIP[3]
35	P4_MDIN[0]
38	P4_MDIN[1]
41	P4_MDIN[2]
43	P4_MDIN[3]
34	P4_MDIP[0]
37	P4_MDIP[1]
40	P4_MDIP[2]
42	P4_MDIP[3]
20	P5_AVDD15
22	P5_RXN
21	P5_RXP
19	P5_TXN
18	P5_TXP
17	R0_LED/P4_LED0/ADDR[0]n
16	R1_LED/P3_LED1/ADDR[1]n
15	R2_LED/P3_LED0/ADDR[2]n
14	R3_LED/P2_LED1/ADDR[3]n
67	RESETn
1	RSET
68	TEST
2	TSTPT
10	VDD_CORE
23	VDD_CORE

Pin Number	Pin Name
44	VDD_CORE
61	VDD_CORE
EPAD	VSS
5	XTAL_IN
6	XTAL_OUT

2 Application Examples

2.1 Examples using the 88E6141 Device

Figure 3: Broadband Router with 4 LAN ports and 2.5Gbps Uplink



2.2 Device Physical Interfaces

The device contains a number of interfaces that support copper media. Table 11 lists the interfaces supported on each port of the 88E6141 device. Refer to the diagrams further in this section for connection details.

Table 11: 88E6141 Device Interfaces

Port	10BASE-T 100BASE-T	1000BASE-T	RGMII	MII / 200Mbps MII	RMII	1000BASE-X SGMII	2500BASE-X
0			x	x	x		
1-4	x	x					
5						x	x

2.2.1 10/100/1000 PHY Interface

Ports 1 to 4 on the device support a 10/100/1000 PHY interface. In the device, this interface supports 10BASE-T, 100BASE-TX, and 1000BASE-T copper IEEE standards. The MAC inside the switch works the same way regardless of the external interface being used. Each PHY's Link, Speed, Duplex and Flow Control information is directly communicated to the MAC it is attached to so the MAC tracks, or follows, the mode the PHY links up in.

2.2.2 MII 200 Mbps Mode

Port 0's MII interface can be configured to run at a data rate of 200 Mbps, full-duplex. Do not select this mode unless the MAC on the other end of the MII interface can also run at double speed rate. Both PHY (reverse MII) and MAC (forward MII) 200 Mbps modes are supported. When the 200 Mbps PHY mode is selected, the output MII clocks run at 50 MHz rate. (50 MHz is enabled by writing to Port offset 0x00, bit 6.) These is no change in the format of the data, it just runs faster. When the 200 Mbps MAC mode is selected, an external 50 MHz ±50 ppm clock source must be supplied. Again, the format of the data is not changed.

2.2.3 SERDES Interface

Port 5 is a SERDES interface that can be used for these options

- Connection to Marvell® triple speed 10/100/1000 copper PHYs
- Connection to Marvell quad speed 10/100/1000/2500 copper PHYs
- Connection to 1000BASE-X fiber modules
- SGMII interface running up to 2.5Gbps
- Cross-chip connection to other Marvell switch devices - i.e., cross-chip connection

The P5_SMODE pin is used to select the SERDES configuration.

- P5_SMODE = 0 - SERDES configured to 2500BASE-X
- P5_SMODE = 1 - SERDES configured to 1000BASE-X or SGMII

2.2.3.1 Triple Speed PHY SERDES Interface Option

Port 5's SERDES can be configured to use a triple speed PHY interface to an external PHY. In this mode, the SERDES use the SGMII protocol. The in-band Link, Speed and Duplex signals in the SGMII protocol are ignored. The external PHY's Link, Speed, Duplex and Flow Control information must be transferred to the port's MAC so the MAC is in the correct mode. This can be done in software (if the port's PHYDetect bit is zero - Port offset 0x00) or it is done automatically by the PHY Polling Unit (PPU - Section 2.2.5)

The triple speed PHY interface can support Marvell PHYs with Auto-Media Detect™ for auto switching between copper and fiber. This can be supported in software or automatically in hardware by the PHY Polling Unit (PPU) and by setting the port's MGMII bit to a one (in the port's Port Status Register - offset 0x00). If the port's MGMII bit is not set to a one, the PPU will support copper only and will not support Auto-Media Detect.

2.2.3.2 IEEE 1000BASE-X SERDES Interface Option

Port 5's SERDES can be configured for 1000BASE-X/SGMII modes.

The port enters 1000BASE-X mode, if configured, even if an external PHY is detected at the port's SMI address.

1000BASE-X mode uses a PCS to auto-negotiate with a link partner to determine if Flow Control should be supported or not (auto-negotiation can be disabled). Speed is always 1000 Mbps and Duplex is always full-duplex on 1000BASE-X ports. An interrupt can be generated on the ports when link changes state (see Global 2, offset 0x00 and 0x01).

2.2.3.3 Port Status Registers

Each switch port of the devices has a status register that reports information about that port's MAC, SERDES or xMII interface. These registers can be used to check the current port configuration. See the Functional Specification for details.

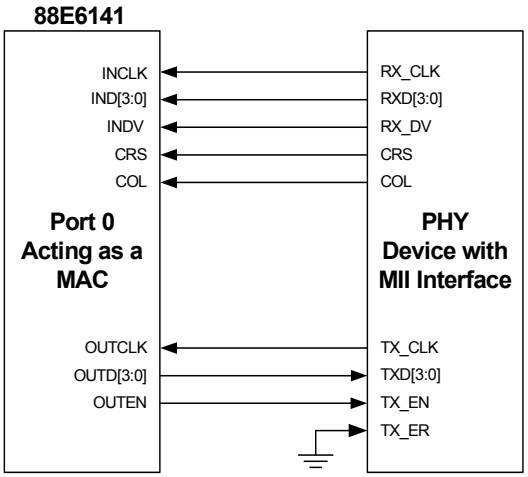
2.2.4 Digital Interface Options

The xMII digital interface supports many different modes defined in the following sections. The mode to use is configured once at reset by external pull-up resistors connected to the P0_MODE[2:0] pins. See Table 6 for more information. If Port 0 is not connected to any device, the port should be disabled.

2.2.4.1 MII MAC Mode

The MII MAC Mode, sometimes called 'Forward MII', configures Port 0's GMAC inside the devices to act as a MAC so it can be directly connected to an external MII-based PHY. In this mode, the devices receive the interface clocks (Px_OUTCLK and Px_INCLK) from the PHY and will work at any frequency from DC to 50 MHz. The two clocks can be asynchronous with each other. Both full- and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII MAC mode is compliant with IEEE 802.3 clause 22. (**Note:** The MII requires only four data bits in each direction so only the lower four data bits are used). P0_MODE should be set correctly at reset (see Table 6) to select this configuration. The PHY's SMI address must be set to 0x00 for auto-negotiation to operate correctly.

Figure 4: MII MAC Interface Pins

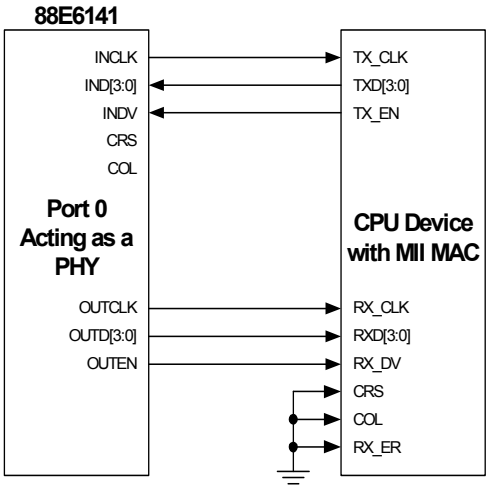


2.2.4.2 MII PHY Mode

The MII PHY Mode, sometimes called 'Reverse MII', configures Port 0's GMAC inside the device to act as a PHY so that it can be directly connected to an external MAC. In this mode, the device drives the interface clocks (INCLK and OUTCLK for both MACs). Only full-duplex modes are supported (since CRS and COL are not driven by the devices outputs) and must match the mode of the link partner's MAC.

The MII PHY mode is compliant with IEEE 802.3 clause 22 in full-duplex mode. At reset, P0_MODE should be set for the appropriate speed — see Table 6. In this mode, there is no external PHY for Port 0 so it is skipped by the PPU. In Reverse MII mode, initially the link status is down requiring the system software to force the port's link up to enable the port.

Figure 5: MII PHY Interface Pins

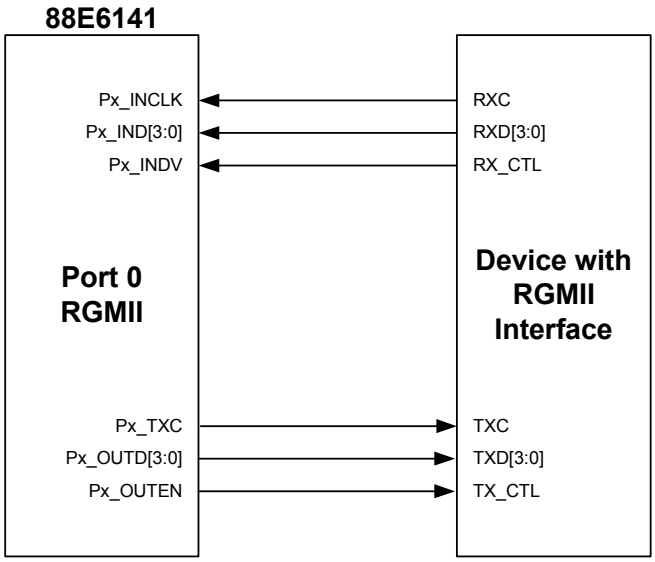


2.2.4.3 RGMII Mode

The RGMII Mode configures Port 0's GMAC to act as a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit PHY or CPU. When the RGMII mode is selected, transmit control (P0_OUTEN) is presented on both clock edges of P0_TXC. Receive control (P0_INDV) is presented on both clock edges of P0_INCLK.

A triple speed interface is supported in RGMII mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's settings. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The interface pins will track the speed that the MAC is set to.

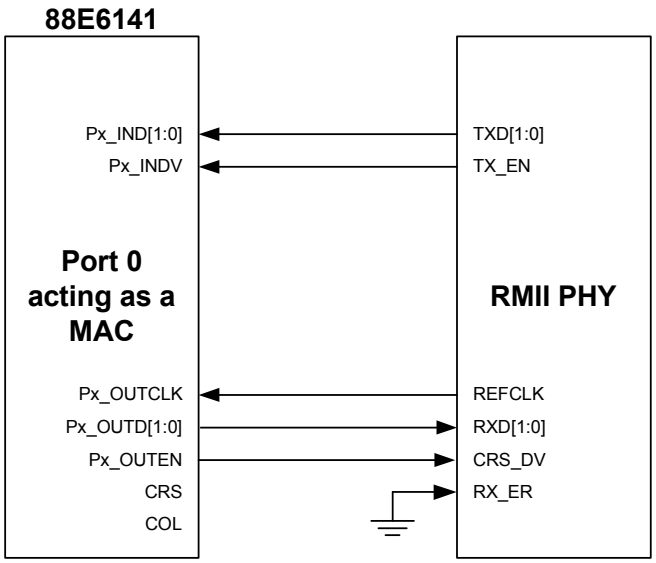
Figure 6: RGMII Interface Pins



2.2.4.4 RMII MAC Mode

RMII MAC Mode (Reduced MII) configures the desired MAC inside the device to act as a 10 or 100 Mbps MAC, enabling it to be directly connected to an external PHY supporting an RMII interface.

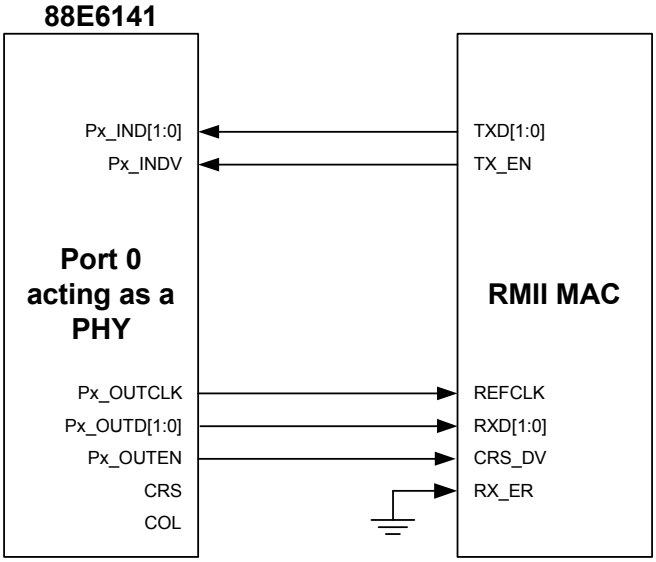
Figure 7: RMII MAC Interface Pins



2.2.4.5 RMII PHY Mode

RMII PHY Mode (Reduced MII) configures the desired MAC inside the device to act as a 10 or 100 Mbps PHY, enabling it to be directly connected to an external CPU supporting an RMII interface.

Figure 8: RMII PHY Interface Pins



2.2.5 PHY Polling Unit (PPU)

The devices contain a PHY Polling Unit (PPU) to transfer Link, Speed, Duplex and Pause information from an external PHY to its associated MAC (the internal PHYs use a direct approach such that this information is transferred even if PHY polling is disabled on the port by its PHYDetect bit being zero - Port offset 0x00). The PPU can perform this job only if the SMI address of the external PHY matches the physical port number it is connected to in the switch (i.e., the PHY connected to Port 5 uses SMI address 0x05, the PHY connected to Port 6 uses SMI address 0x06, etc.).

If PHY polling is disabled on a port (i.e., the port's PHYDetect bit is zero), software must perform the job of setting the switch MAC's mode to the mode of the PHY (for the external PHYs) by forcing the MAC's link, speed, duplex and pause settings (in the port's PCS Control Register - offset 0x01) based upon what it sees in the PHY's registers. Link up must be the last mode register set and link down must be the first mode register cleared (i.e., the port's speed, duplex and pause modes must only be changed while the port's link is down).

Even though the PPU has full access to the external and internal PHY's registers, software can access all of the PHY registers at any time by using the SMI Command and Data registers (Global 2, offsets 0x18 and 0x19).

2.3 LED Interface

The device uses a matrixed LED interface allowing each PHY port to have up to 4 LEDs. The cathode of each LED is connected to a single row signal (Rx_LED). The anode of each LED is connected to a single column signal (Cx_LED). The physical LEDs on the device pins are organized as 4 rows with 4 columns. Table 12 shows the port to physical mapping.

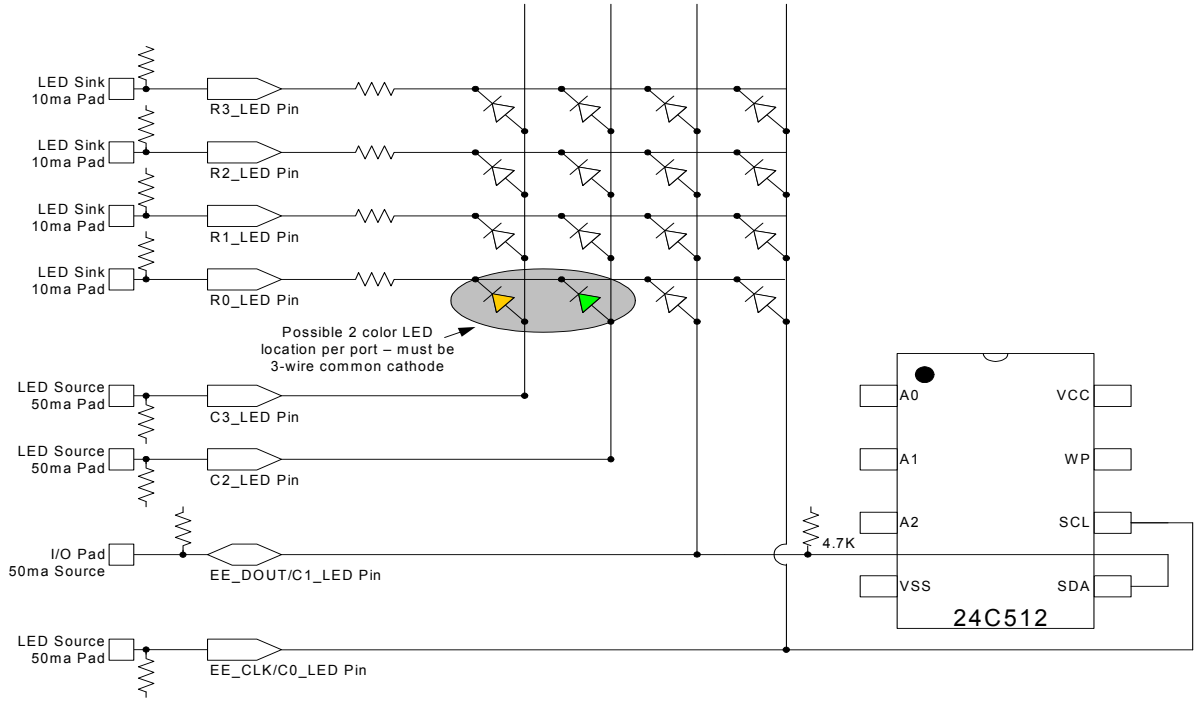
Table 12: LED Mapping

	C0_LE	C1_LED	C2_LED	C3_LED
R0_LED	Port 1, LED 0	Port 1, LED 1	Port 1, LED 2	Port 1, LED 3
R1_LED	Port 2, LED 0	Port 2, LED 1	Port 2, LED 2	Port 2, LED 3
R2_LED	Port 3, LED 0	Port 3, LED 1	Port 3, LED 2	Port 3, LED 3
R3_LED	Port 4, LED 0	Port 4, LED 1	Port 4, LED 2	Port 4, LED 3

The column signals (Cx_LED) are also shared with the EEPROM interface, and the architecture allows for the LEDs and EEPROM to operate at the same by time multiplexing the bus into 5 time cycles (C0_LED, C1_LED, C2_LED, C3_LED, and EEPROM). This prevents EEPROM access from interfering with LED operation and vice versa.

Although an EEPROM is not required for most applications, the device supports 2 wire EEPROMs. Figure 9 illustrates typical LED connections with 2 wire EEPROM connections.

Figure 9: Two LEDs plus 2 wire EEPROM



2.3.1 LED Options

Each port supports up to 4 LEDs that can be configured individually to show many different options.

These options include:

- Link (off = no link, on = link)
- Activity (off = no activity, on = blink)
- Link/Activity (off = no link, on = link, blink = activity)
- 10 Mbps Link (off = no link, on = 10 Mbps link)
- 10 Mbps Link/Activity (off = no activity, on = 10 Mbps link, blink = activity)
- 100 Mbps Link (off = no link, on = 100 Mbps link)
- 100 Mbps Link/Activity (off = no activity, on = 10 Mbps link, blink = activity)
- 10/100 Mbps Link (off = no link, on = 10/100 Mbps link)
- 10/100 Mbps Link/Activity (off = no activity, on = 10/100 Mbps link, blink = activity)
- Gig Link (off = no link, on = Gig link)
- Gig Link/Activity (off = no activity, on = Gig link, blink = activity)
- 10 Mbps/Gig Link (off = no link, on = 10 Mbps or Gig link)
- 10 Mbps/Gig Link/Activity (off = no activity, on = 10 Mbps or Gig link, blink = activity)
- 100 Mbps/Gig Link (off = no link, on = 100 Mbps or Gig link)
- 100 Mbps/Gig Link/Activity (off = no activity, on = 100 Mbps or Gig link, blink = activity)
- Link/Activity/Speed by blink rate (off = no link, on = link, blink = activity, blink speed = link speed)
- Duplex/Collision (off = half-duplex, on = full-duplex, blink = collision)
- Force Blink
- Force On
- Force Off
- Special (see Section 2.3.2)

Each port's LED options can be configured in the switch port registers (port offset 0x16). Please refer to 88E6141 Switch Functional Specification for more information.

2.3.2 Special LEDs

In some applications, two sets of LEDs are desired. One set on the rear panel which would indicate Link/Speed/Activity per port and a second set on the front panel where a common LED can indicate the LAN and/or WAN Activity on a combination of ports. The special LEDs available on the devices can be used for these types of applications.

Special LEDs are available on Ports 1 through 4 and can be configured for the modes available on that port. The special functions are as follows:

Port 1 Special LED - LAN Link/Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Ports 1-4.

Port 2 Special LED - WAN Link Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Port 5.

Port 3 Special LED - CPU Port Link/Activity. This LED can be used to show activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Port 0.

Port 4 Special LED - PTP Activity (88E6341 Only). This LED can be used to show PTP activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows PTP activity on the IMP Port (Port 6).

2.3.3 Power up LED Configurations

The power up LED configuration can be set by the LED_SEL pin. This pin is internally pulled low, setting a default configuration of 0, but can be configured to a 1 at Reset using 4.7Kohm pull-up resistor.

The functions of each LED for the standard configuration options are given in the following tables:

Table 13: LED_SEL = 0 (Default)

	C0_LED	C1_LED	C2_LED	C3_LED
PORT 1 (R0_LED)	Link/Activity	Gig Link	10/100 Link	LAN Link/Activity (default Ports 1-4)
PORT 2 (R1_LED)	Link/Activity	Gig Link	10/100 Link	WAN Link/Activity (default Ports 5)
PORT 3 (R2_LED)	Link/Activity	Gig Link	10/100 Link	Alt Link/Activity (default Ports 0)
PORT 4 (R3_LED)	Link/Activity	Gig Link	10/100 Link	PTP Link/Activity (default Ports 6)

This configuration is designed for systems with three LEDs where one LED is used to show Link/Activity and the other two LEDs are used as a bicolor LED to differentiate between Gig Link and 10/100 Link. The special LAN and WAN LEDs can be used on the front panel of the switch to show LAN/WAN activity (see Figure 10).

Figure 10: LED_SEL = 0 Example Implementation

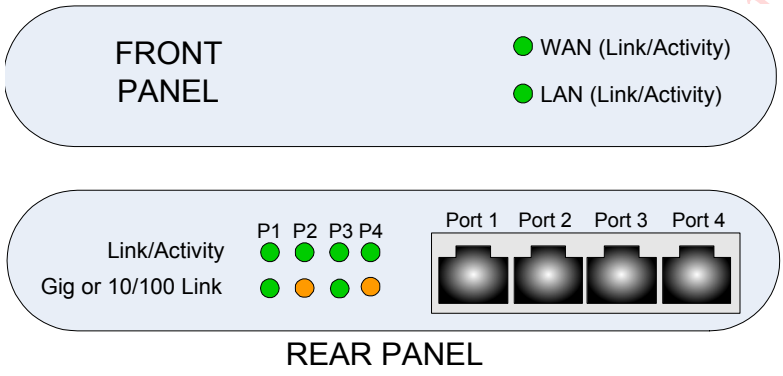


Table 14: LED_SEL = 0x1

	C0_LED	C1_LED	C2_LED	C3_LED
PORT 1 (R0_LED)	Gig Link/Activity	10/100 Link	Activity	LAN Link/Activity (default Ports 1-4)
PORT 2 (R1_LED)	Gig Link/Activity	10/100 Link	Activity	WAN Link/Activity (default Ports 5)
PORT 3 (R2_LED)	Gig Link/Activity	10/100 Link	Activity	Alt Link/Activity (default Ports 0)
PORT 4 (R3_LED)	Gig Link/Activity	10/100 Link	Activity	PTP Link/Activity (default Ports 6)

2.3.4 Optional Direct Drive LED Configuration

The LED interface can optionally be configured to directly drive from 7 LEDs in a non-multiplexed fashion. The 7 LEDs are configured as Ports 1-4 LED0 and Ports 1-3 LED1.

In Direct Drive mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to a power source.

To configure the LED interface to directly drive LEDs, Port 0's Global LED Control register, bit 4 must be configured to 0x1.

Please refer to 88E6341/88E6141 Functional Specification for more information.

2.4 General Purpose I/O Configuration

The device features eleven pins that can be configured to be General Purpose I/O (GPIO). Two pins, GPIO [9:10], are available at all times. The other nine GPIO pins are shared with the xMII interface on the device. The configuration of the xMII interface determines which GPIO signals, if any, are available for use.

The xMII interface is configured based on the setting of the P0_MODE pins at reset (as described in the SSection 1.2, Pin Description, on page 14.

Table 15 summarizes the GPIO pins that are available in each mode.

Table 15: GPIO Summary

P0_MODE	xMII Setting	GPIO Available	Note
000	Full-duplex MII PHY	GPIO[7:8], GPIO[9:10]	In this mode GPIO [7:8] are available in CPU attached mode (NO_CPU = 0 at reset). If NO_CPU = 1 at reset, then GPIO [7:8] become MDC_PHY and MDIO_PHY.
001	MII PHY	GPIO[9:10]	
010	MII MAC	GPIO[9:10]	
100	RMII PHY	GPIO[1], GPIO[5:6], GPIO[7:8], GPIO[9:10]	In these modes GPIO [7:8] are available in CPU attached mode (NO_CPU = 0 at reset). If NO_CPU = 1 at reset, then GPIO [7:8] become MDC_PHY and MDIO_PHY.
101	RMII MAC	GPIO[1], GPIO[5:6], GPIO[7:8], GPIO[9:10]	
110	Disabled	GPIO[0:6], GPIO[7:8], GPIO[9:10]	
111	RGMII	GPIO[7:8], GPIO[9:10]	

Once configured as a GPIO, a pin can be programmed to the following functions:

- General Purpose Input
  - Can be used as Enable pin for P0 xMII interface
- General Purpose Output
- GPIO Port Stall – can be used to stall the transmission of a specific port (or ports) as needed
- I^2C Master interface (using either GPIO [7:8] or GPIO [9:10])

These functions can be programmed through the Scratch and Misc Register at Switch Global 2, Offset 0x1A (see 88E6341/88E6141 Functional Specification).

2.4.1 Configuring GPIO as a Port Enable Pin

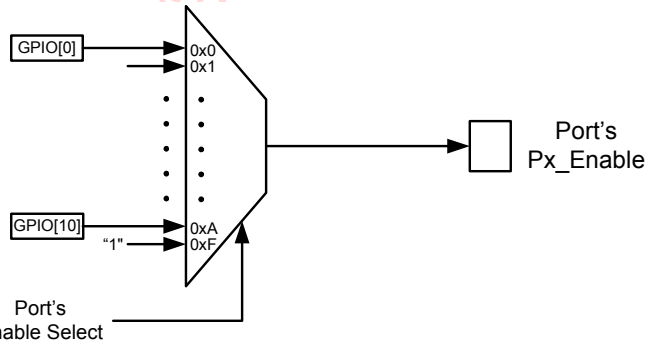
Each of the GPIO pins has the capability to be used as the Port Enable pin for Port 0's xMII interface.

To use a GPIO as a Port Enable pin, the GPIO must first be configured as an input.

To select the specific GPIO to be used as an enable pin, program the xMII port's Enable Select register (Port Offset 0x1E, bits 15:12) to the number of the GPIO pin that will be used as the enable pin.

For example, setting the Enable Select to 0x0 selects GPIO 0, 0x1 selects GPIO 1, etc. Setting the bits to 0xF connects the enable function to a logic high, enabling the interface.

Figure 11: Port's GPIO Enable Select Function



3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 16: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on any 3.3V signal with respect to VSS	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on any 2.5V signal with respect to VSS	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.8)}$	Power Supply Voltage on any 1.8V supply with respect to VSS	-0.5	1.8	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
$V_{DD(1.5)}$	Power Supply Voltage on any 1.5V supply with respect to VSS	-0.5	1.5	+3.6 or $V_{DD(1.8)}$ +0.5[3] whichever is less	V
$V_{DD(1.15)}$	Power Supply Voltage on any 1.15V supply with respect to VSS	-0.5	1.15	+3.6 or $V_{DD(1.5)}$ +0.5[4] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to VSS	-0.5		+3.6 or V_{DDO_PIN}[5] +0.5[6] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[7]	°C

1. VDD(2.5) must never be more than 0.5V greater than VDD(3.3) or damage will result. Power must be applied to VDD(3.3) before or at the same time as VDD(2.5).
2. VDD(1.8) must never be more than 0.5V greater than VDD(2.5) or damage will result. Power must be applied to VDD(2.5) before or at the same time as VDD(1.8).
3. VDD(1.5) must never be more than 0.5V greater than VDD(1.8) or damage will result. Power must be applied to VDD(1.8) before or at the same time as VDD(1.5).
4. VDD(1.15) must never be more than 0.5V greater than VDD(1.5) or damage will result. Power must be applied to VDD(1.5) before or at the same time as VDD(1.15).
5. The VDDO pad ring has separate I/O power supply options. Therefore, the voltage applied to a group of I/O pins must follow what is defined in Section 1.
6. VPIN must never be more than 0.5V greater than VDDO or damage will result.
7. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

3.2 Recommended Operating Conditions

Table 17: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For any 3.3V supply pin[1]	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For any 2.5V supply pin[2]	2.375	2.5	2.625	V
$V_{DD(1.8)}$	1.8V power supply	For any 1.8V supply pin	1.710	1.8	1.890	V
$V_{DD(1.5)}$	1.5V power supply	For any 1.5V supply pin	1.425	1.5	1.575	V
$V_{DD(1.15)}$	1.15V power supply	For any 1.15V supply pin	1.093	1.15	1.2	V
T_A	Ambient operating temperature[3]	Commercial parts	0		70	°C
T_J	Maximum junction temperature				125[3]	°C
RSET	Internal bias reference	External resistor value required to be placed between RSET and VSS pins	4950	5000	5050	Ω

1. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
2. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
3. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on "TJ Thermal Calculations" for more information.

3.3 Thermal Conditions

3.3.1 Thermal Conditions for the 88E6141 device 88-pin QFN Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 88E6141 device 88-Pin QFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		24.7		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		24.2		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		22.9		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		22.3		°C/W
Ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E6141 device 88-Pin QFN package $\Psi_{JT} = (T_J - T_{TOP})/P$. T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.36		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.67		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.98		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.1		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E6141 device 88-Pin QFN package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		11.2		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E6141 device 88-Pin QFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		14.0		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

Table 18: 88E6141 Device Current Consumption

Pins	Parameter	Condition	Min	Typ	Max	Units
AVDD33	3.3V power to analog core for Gig PHY interfaces	All ports active at max speed (Port 1 - Port 4 at 1000 Mbps)		230		mA
		All ports active (Port 1 - Port 4 at 100 Mbps)		90		mA
		All ports active (Port 1 - Port 4 at 10 Mbps)		130		mA
		EEE disabled, all ports idle (Port 1 - Port 4 linked at 1000 Mbps but idle)		230		mA
		EEE disabled, all ports idle (Port 1 - Port 4 linked at 100 Mbps but idle)		90		mA
		EEE disabled, all ports idle (Port 1 - Port 4 linked at 10 Mbps but idle)		74		mA
		Reset		15		mA
		No link on any port		45		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		29		mA
AVDD15	1.5V power to analog core for Gig PHY interfaces	All ports active (Port 1 - Port 4 at 1000 Mbps)		210		mA
		All ports active (Port 1 - Port 4 at 100 Mbps)		85		mA
		All ports active (Port 1 - Port 4 at 10 Mbps)		53		mA
		EEE disabled, all ports idle (Port 1 - Port 4 linked at 1000 Mbps but idle)		210		mA
		EEE disabled, all ports idle (Port 1 - Port 4 linked at 100 Mbps but idle)		85		mA
		EEE disabled, all ports idle (Port 1 - Port 4 linked at 10 Mbps but idle)		53		mA
		Reset		4		mA
		No link on any port		50		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		62		mA

Table 18: 88E6141 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
EE_VDDO	3.3V to EEPROM and LED pins. 3.3V to PLL	All ports active at max speed		48		mA
		All ports active at 100 Mbps		48		mA
		All ports active at 10 Mbps		48		mA
		EEE disabled, all ports idle and linked at max speed		48		mA
		EEE disabled, all ports idle and linked at 100 Mbps		48		mA
		EEE disabled, all ports idle and linked at 10 Mbps		48		mA
		Reset		48		mA
		No link on any port		14		mA
		EEE enabled		48		mA

Table 18: 88E6141 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
P0_VDDO	3.3V for Port 0's RGMII/MII/RMII I/O pins.	All ports active at 1000 Mbps		43		mA
		All ports active at 100 Mbps		24		mA
		All ports active at 10 Mbps		21		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		15		mA
		EEE disabled, all ports idle and linked at 100 Mbps		8		mA
		EEE disabled, all ports idle and linked at 10 Mbps		6		mA
		Reset		0		mA
		No link on any port		15		mA
		EEE enabled		15		mA
	2.5V for Port 0's RGMII/MII/RMII I/O pins.	All ports active at 1000 Mbps				mA
		All ports active at 100 Mbps				mA
		All ports active at 10 Mbps				mA
		EEE disabled, all ports idle and linked at 1000 Mbps				mA
		EEE disabled, all ports idle and linked at 100 Mbps				mA
		EEE disabled, all ports idle and linked at 10 Mbps				mA
		Reset				mA
		No link on any port				mA
		EEE enabled				mA
	1.8V for Port 0's RGMII/MII/RMII I/O pins.	All ports active at 1000 Mbps				mA
		All ports active at 100 Mbps				mA
		All ports active at 10 Mbps				mA
		EEE disabled, all ports idle and linked at 1000 Mbps				mA
		EEE disabled, all ports idle and linked at 100 Mbps				mA
		EEE disabled, all ports idle and linked at 10 Mbps				mA
		Reset				mA
		No link on any port				mA
		EEE enabled				mA

Table 18: 88E6141 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
P5_AVDD15	1.5V power to SERDES	Port 5 2.5Gbps		88		mA
		Port 5 1Gbps		50		mA
		Reset		14		
		EEE Enabled (all ports idle)		39		
VDD_ CORE	1.15V power to digital core	All ports active at max speed (Ports 0-4 at 1000Mbps, Port 5 at 2500Mbps)		400		mA
		All ports active at 1000 Mbps		370		mA
		All ports active at 100 Mbps		170		
		All ports active at 10 Mbps		140		mA
		EEE disabled, all ports idle and linked at max speed		258		mA
		EEE disabled, all ports idle and linked at 1000 Mbps		248		
		EEE disabled, all ports idle and linked at 100 Mbps		65		mA
		EEE disabled, all ports idle and linked at 10 Mbps		41		mA
		Reset		10		mA
		No link on any port		60		mA
		EEE enabled (all ports idle at max speed)		160		mA

3.5 DC Electrical Characteristics

3.5.1 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 19: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VDDO	3.3V/2.5V/1.8V power.	See EE_VDDO, and P0_VDDO pin definitions in Table 9 for details.		3.135	3.3	3.465	V
				2.375	2.5	2.625	V
				1.71	1.8	1.89	V
V_{IH}	High level input voltage	XTAL_IN, SE_SCLK	AVDD15	1.4		1.99	V
		All VDDO	VDDO = 3.135V	VDDO*70%		VDDO+0.4	V
		P0_VDDO GPIO_VDDO	VDDO = 2.375V				V
			VDDO = 1.710V				V
V_{IL}	Low level input voltage	XTAL_IN, SE_SCLK	AVDD15	-0.3		0.54	V
		All VDDO	VDDO = 3.135V	-0.4		VDDO*30%	V
		P0_VDDO GPIO_VDDO	VDDO = 2.375V				V
			VDDO = 1.710V				V
V_{OH}	High level output voltage	LED pins	I_{OH} = -7 mA	VDDO - 0.4			V
		All others (except INTn [1])	I_{OH} = -4 mA	VDDO - 0.4			V
		Others @ 1.8V	I_{OH} = -2 mA	VDDO - 0.2			V
V_{OL}	Low level output voltage	INTn and LED pins	I_{OL}= 7 mA			0.4	V
		All others	I_{OL}= 4 mA			0.4	V
		Others 1.8V	I_{OL}= 2 mA			0.2	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DDO}$			+ 10 - 60	µA
		With pull-down resistor	$0<V_{IN}<V_{DDO}$			+ 60 - 10	µA
		Others	$0<V_{IN}<V_{DDO}$			+ 10 - 10	µA
C_{IN}	Input capacitance	XTAL_IN, SE_SCLK			5		pF
		All others				5	pF

1. The INTn is an active low, open drain pin. See INTn description in the Signal Description.

3.5.2 RESETn

Table 20: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	RESETn		VDDO * 70%			V
V_{IL}	Low level input voltage	RESETn				VDDO * 30%	V

3.5.3 SGMII Interface

SGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website ftp://ftp-eng.cisco/smii/sgmii.pdf. It uses a modified LVDS specification based on the IEEE standard 1596.3. Refer to that standard for the exact definition of the terminology used in the following table. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

3.5.3.1 Transmitter DC Characteristics

	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1400	mV
V_{OL}	Output Voltage Low	700			mV
V_{RING}	Output Ringing			10	%
$\|V_{OD}\|^2$	Output Voltage Swing (differential, peak)	Programmable - see Table 21.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 3.5.3.2 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40		60	Ωs
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when TXP and TXN are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

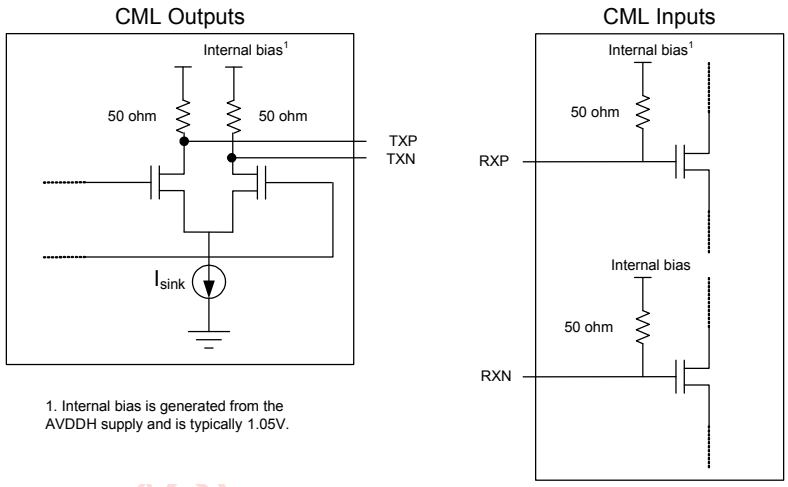
1. Parameters are measured with outputs AC connected with 100 ohm differential load.
2. Output amplitude is programmable by writing to Register 26_1.2:0.

Table 21: Programming SGMII Output Amplitude

Register 26_1 Bits	Field	Description
2:0	SGMII/Fiber Output Amplitude[1]	Differential voltage peak measured. Note that internal bias minus the differential peak voltage must be greater than 700 mV. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

1. Cisco SGMII specification limits are |VOD| = 150 mV - 400 mV peak differential.

Figure 12: CML I/Os



1. Internal bias is generated from the AVDDH supply and is typically 1.05V.

3.5.3.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- AC connection to an LVDS receiver
- AC connection to an CML receiver

If AC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Figure 12 for details. (If AVDD18 is used to generate the internal bias, the internal bias value will typically be 1.1V.)
- The output voltage swing is programmed by Register 26_1.2:0 (see Table 21).
- Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing. See Figure 13 for details.

Figure 13: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

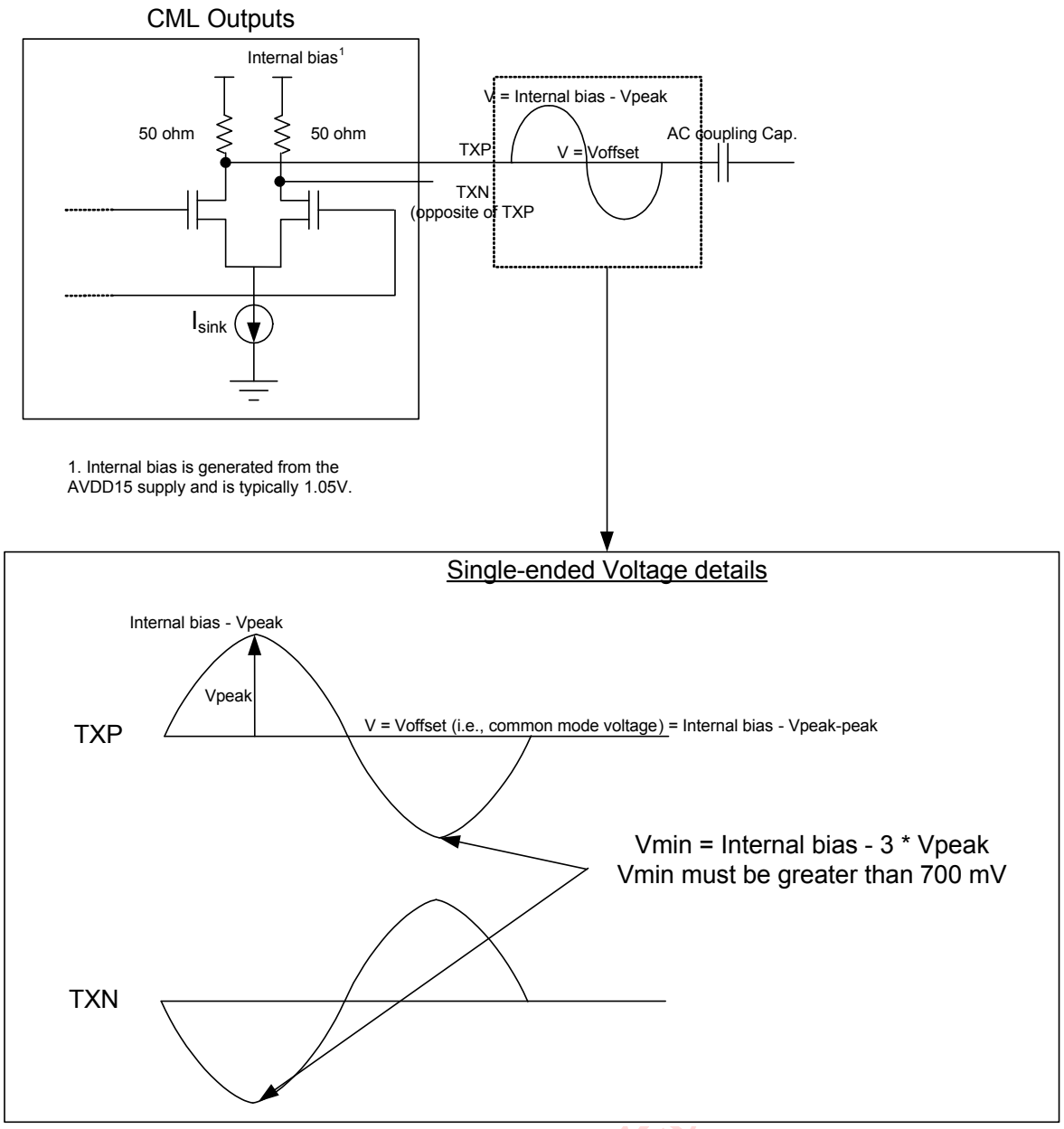
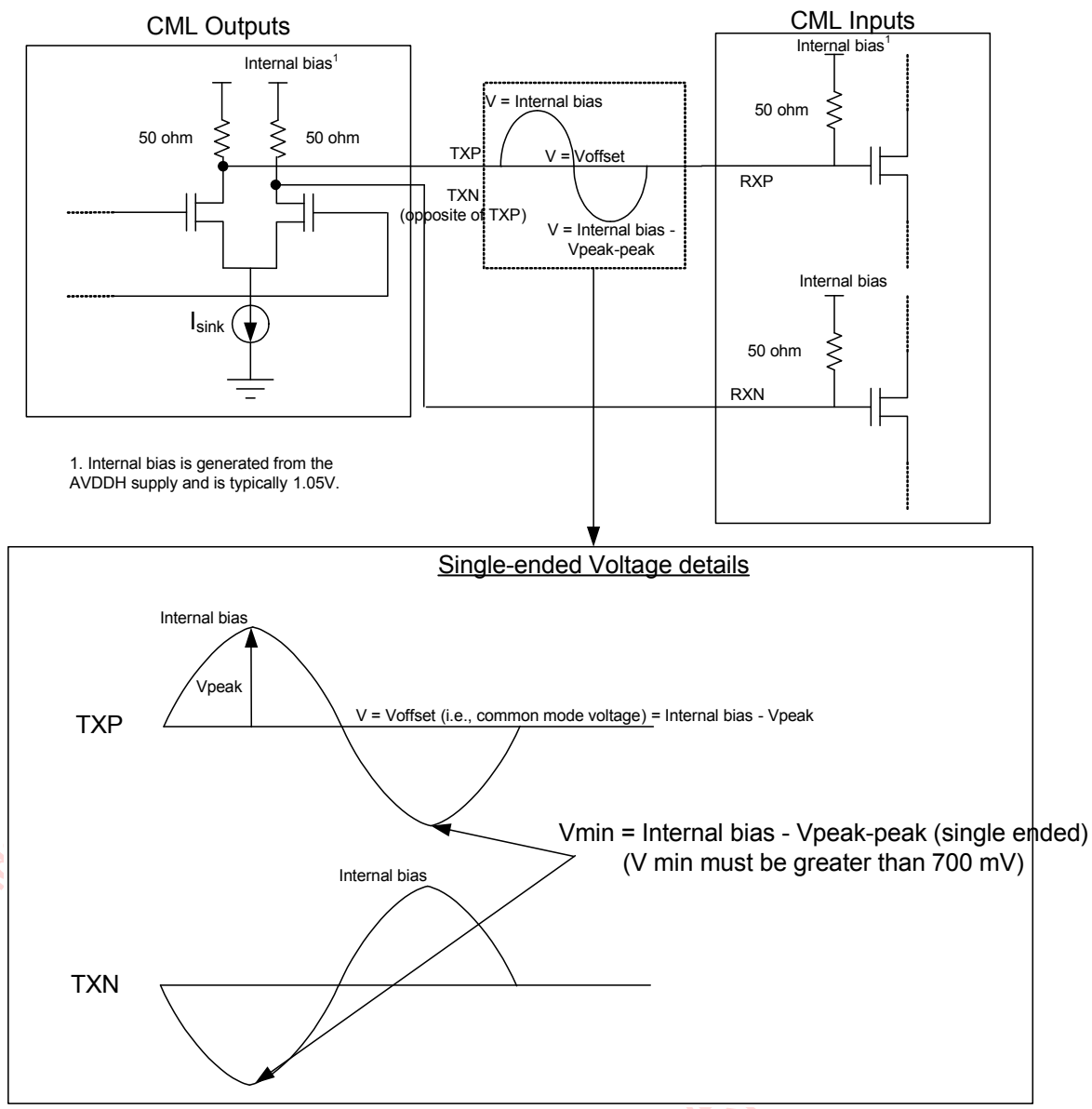


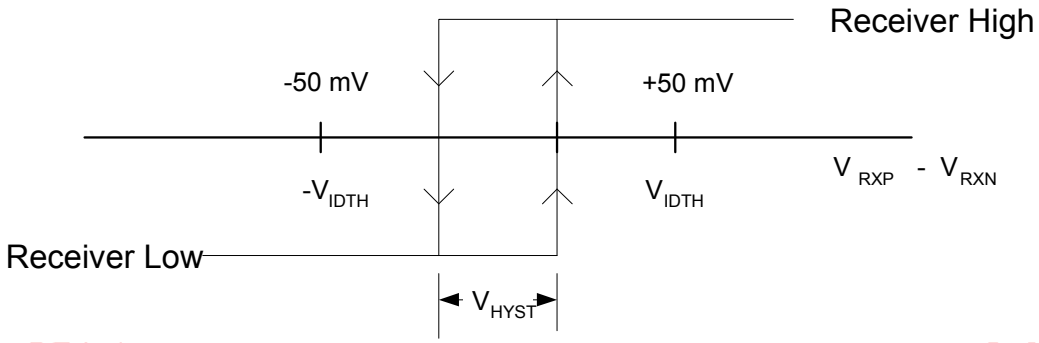
Figure 14: DC connection to a CML receiver



3.5.3.3 Receiver DC Characteristics

	Parameter	Min	Typ	Max	Units
V_I	Input Voltage range a or b	675		1725	mV
V_{IDTH}	Input Differential Threshold	-50		+50	mV
V_{HYST}	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 Ω Differential Input Impedance	80		120	Ω

Figure 15: Input Differential Hysteresis



3.6 AC Electrical Specifications

3.6.1 Reset and Configuration Timing

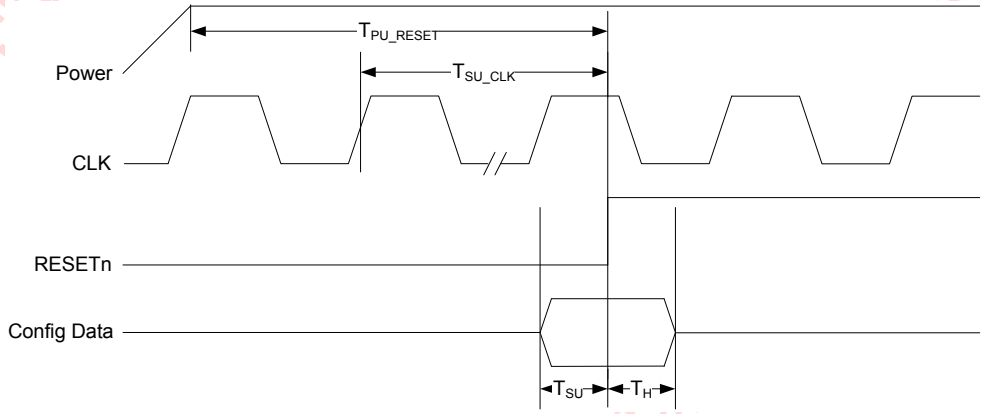
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 22: Reset and Configuration

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or sub-sequent resets after power up	10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			Clks
T_{SU}	Configuration data valid prior to RESETn de-asserted[1]		200			ns
T_{HD}	Config data valid after RESETn de-asserted		0			ns

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn. All configuration pins that become outputs during normal operation will remain tri-stated for 40 ns after the rising edge of RESETn.

Figure 16: Reset and Configuration Timing



3.6.2 Clock Timing

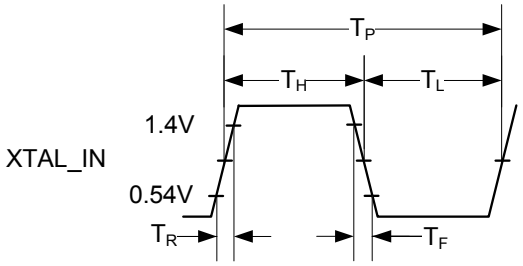
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 23: IEEE DC Transceiver Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns
T_H	XTAL_IN high time		13	20	27	ns
T_L	XTAL_IN low time		13	20	27	ns
T_R	XTAL_IN rise				3	ns
T_F	XTAL_IN fall				3	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[2]				200	ps[3]

1. If the crystal option is used, ensure that the frequency is 25.000 MHz ± 50 ppm.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 17: Oscillator Clock Timing



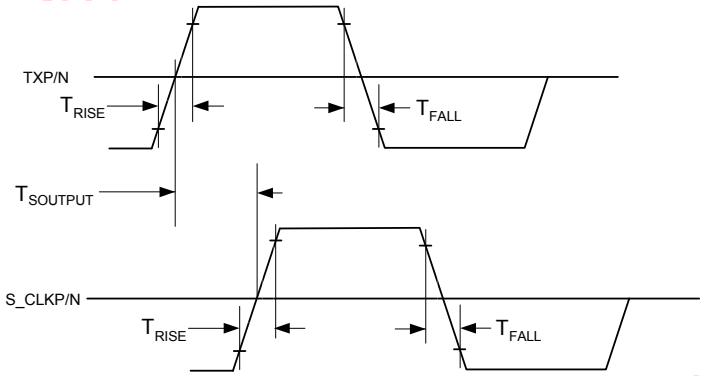
3.7 SGMII Timing

3.7.1 SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{SOUTPUT}$[2]	SERDES output to RxClk_P/N	360	400	440	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.
2. Measured at 50% of the transition.

Figure 18: Serial Interface Rise and Fall Times



3.7.2 SGMII Input AC Characteristics

	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

3.8 MII Timing

3.8.1 MII PHY Mode Receive Timing - 100 Mbps

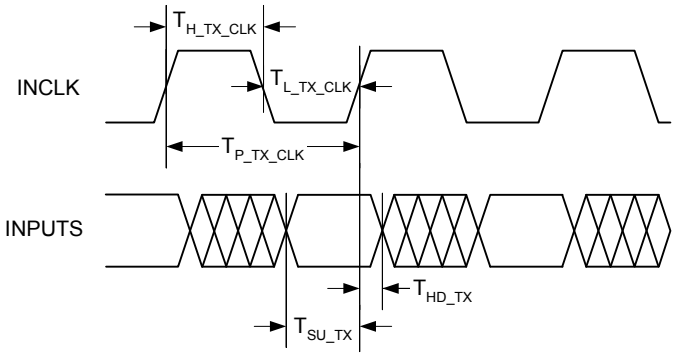
In PHY mode, the P[x]_INCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 24: MII PHY Mode Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$[1]	P[x]_INCLK period	10BASE mode		400		ns
		100BASE mode		40		ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		15			ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		0			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 19: MII PHY Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

3.8.2 MII PHY Mode Transmit Timing - 100 Mbps

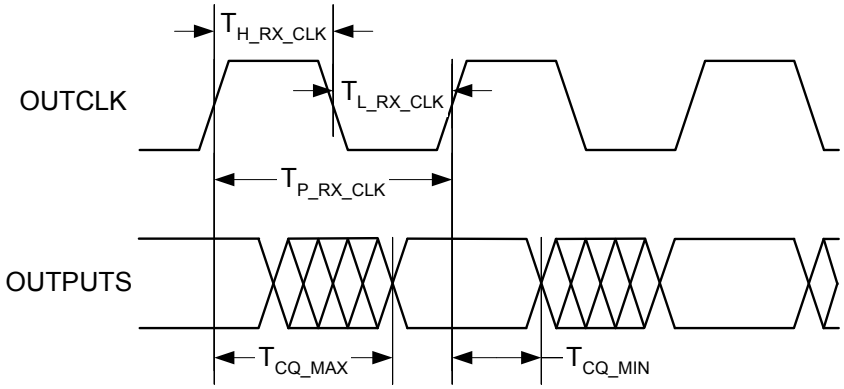
In PHY mode, the P[x]_OUTCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 25: MII PHY Mode Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	10BASE mode		400		ns
		100BASE mode		40		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid				25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		10			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 20: MII PHY Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an output in this mode.

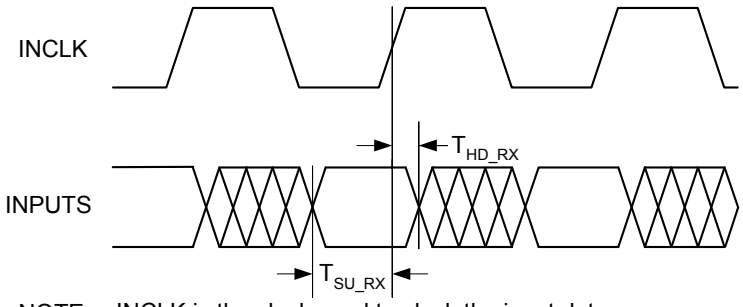
3.8.3 MII MAC Mode Receive Timing

In MAC mode, the P[x]_INCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 26: MII Receive Timing - MAC Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	10			ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	10			ns

Figure 21: MII MAC Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

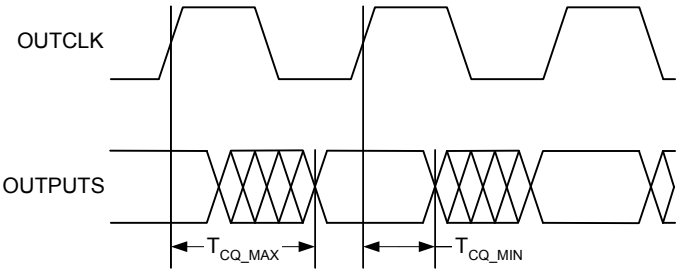
3.8.4 MII MAC Mode Transmit Timing

In MAC mode, the P[x]_OUTCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 27: MII MAC Mode Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid	With 10 pF load			25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) invalid	With 10 pF load	0			ns

Figure 22: MII MAC Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an input in this mode.

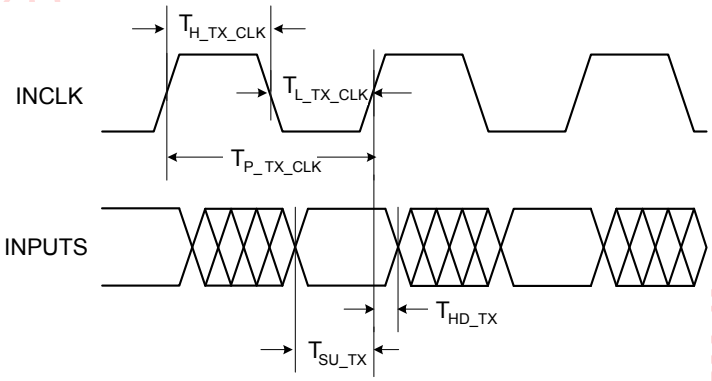
3.8.5 TMII PHY Mode Receive Timing - 200 Mbps

In PHY mode, the P[x]_INCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 28: TMII PHY Mode Receive Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_INCLK period	200BASE mode		20		ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	200BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	200BASE mode	8	10	12	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		5			ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		3			ns

Figure 23: TMII PHY Mode Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

3.8.6 TMII PHY Mode Transmit Timing - 200 Mbps

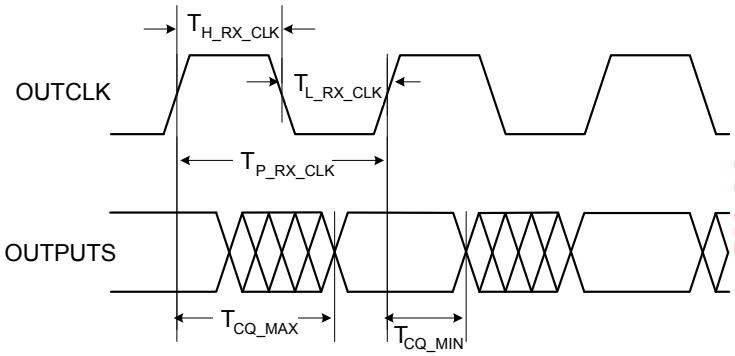
In PHY mode, the P[x]_OUTCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 29: TMII PHY Mode Transmit Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	200BASE mode		20		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	200BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	200BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid				15	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		2			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 24: TMII PHY Mode Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.8.7 TMII MAC Mode Clock Timing - 200 Mbps

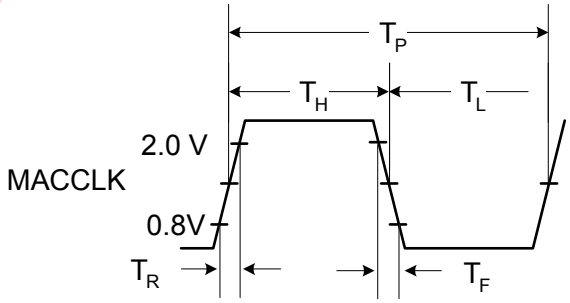
In MAC mode, INCLK and OUTCLK are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 30: TMII MAC Mode Clock Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	MACCLK_IN period		0	20	20 +50 ppm	ns
T_H	MACCLK_IN high time		8			ns
T_L	MACCLK_IN low time		8			ns
T_R	MACCLK_IN rise				3	ns
T_F	MACCLK_IN fall				3	ns

1. DC to 25 MHz

Figure 25: TMII MAC Clock Timing - 200 Mbps



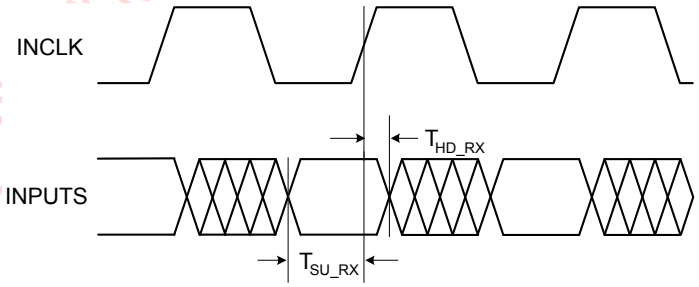
3.8.8 TMII MAC Mode Receive Timing - 200 Mbps

In MAC mode, the P[x]_INCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 31: TMII MAC Mode Receive Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	5			ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	2			ns

Figure 26: TMII MAC Mode Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data. It is an input in this mode.

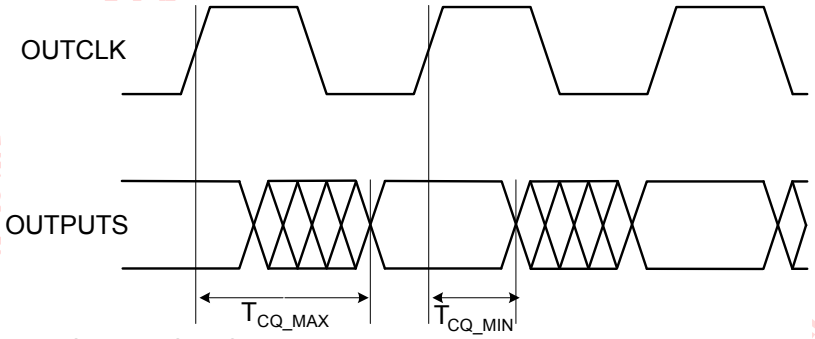
3.8.9 TMII MAC Mode Transmit Timing - 200 Mbps

In MAC mode, the P[x]_OUTCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 32: TMII MAC Transmit Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV valid	With 10 pF load			15	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV invalid	With 10pF load	0			ns

Figure 27: TMII MAC Mode Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an input in this mode.

3.9 RGMII Timing

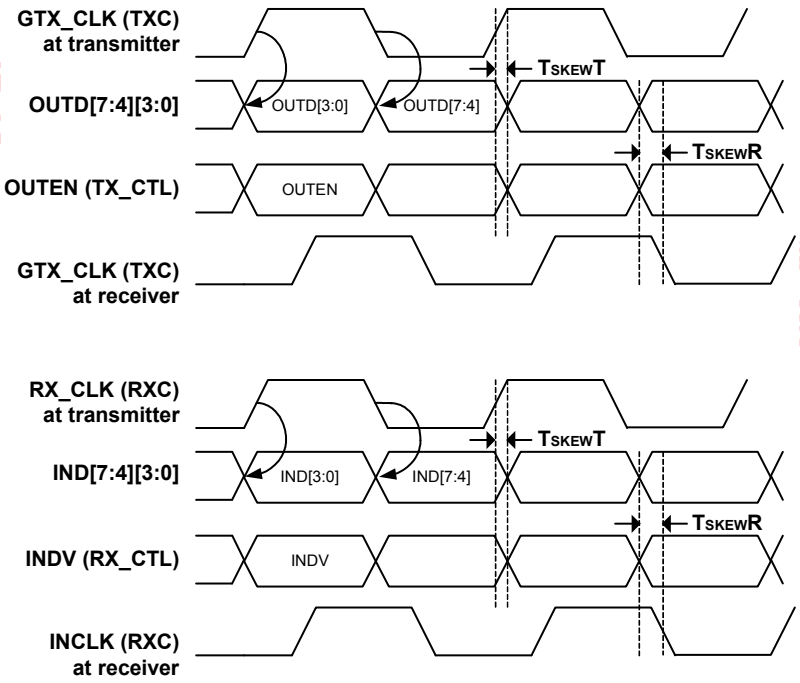
Table 33: RGMII Interface Timing

For other timing modes see Section 3.9.1, RGMII Timing for Different RGMII Modes, on page 72.

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 28: RGMII Multiplexing and Timing



3.9.1 RGMII Timing for Different RGMII Modes

3.9.1.1 RGMII Transmit Timing

Table 34: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{sskew}	RGMII Transmit Delay Control (bit 3) = 0	-0.5		0.5	ns

Figure 29: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 0

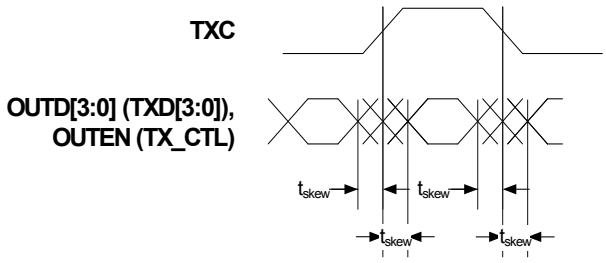
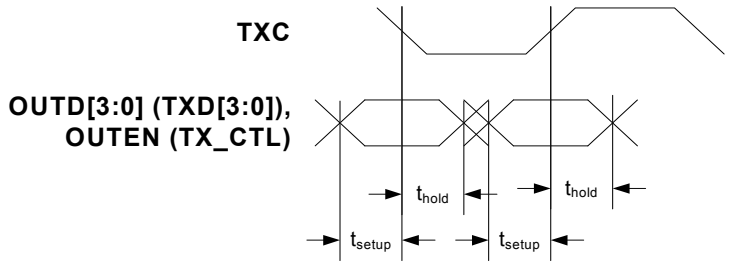


Table 35: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Transmit Delay Control (bit 3) = 1	1.2			ns
t_{hold}		1.2			ns

Figure 30: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 1



3.9.1.2 RGMII Receive Timing

Table 36: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 0	1.0			ns
t_{hold}		0.8			ns

Figure 31: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0

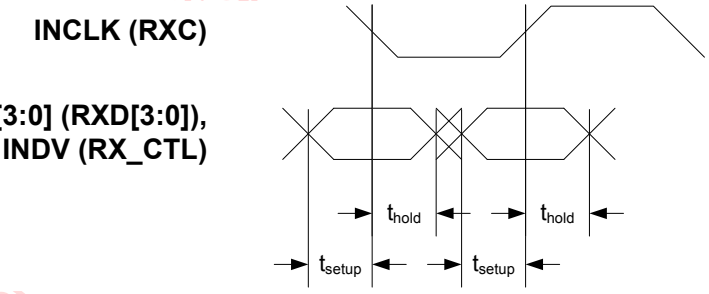
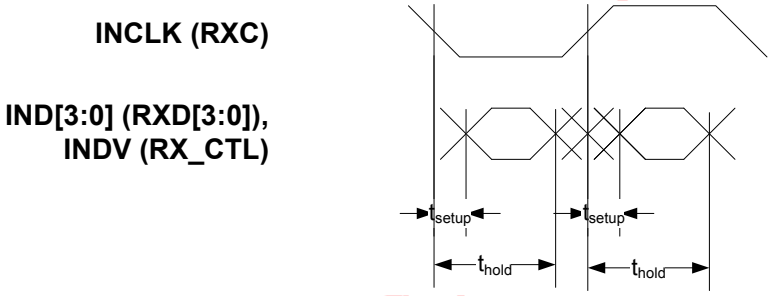


Table 37: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 1	-0.9			ns
t_{hold}		2.7			ns

Figure 32: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1



3.10 RMII Timing

3.10.1 RMII Receive Timing

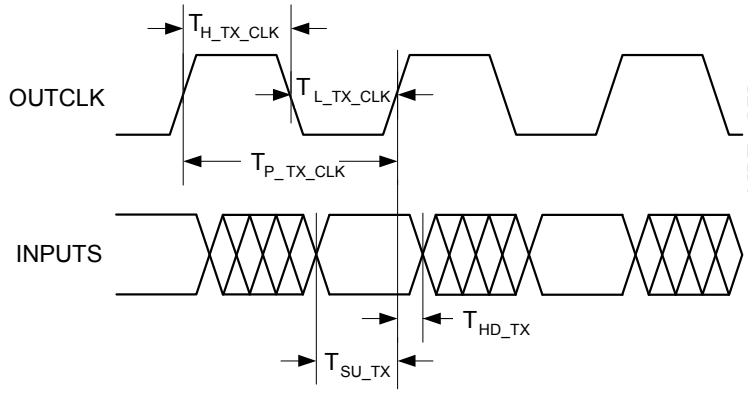
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 38: RMII Receive Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_OUTCLK period[1]	100BASE mode		20		ns
$T_{H\_TX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{SU_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid prior to P[x]_OUTCLK going high.		4			ns
T_{HD_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid after P[x]_OUTCLK going high.		2			ns

1. 50 MHz for 100 Mbps.

Figure 33: RMII Receive Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the input data. It is an output in this mode.

3.10.2 RMII Transmit Timing

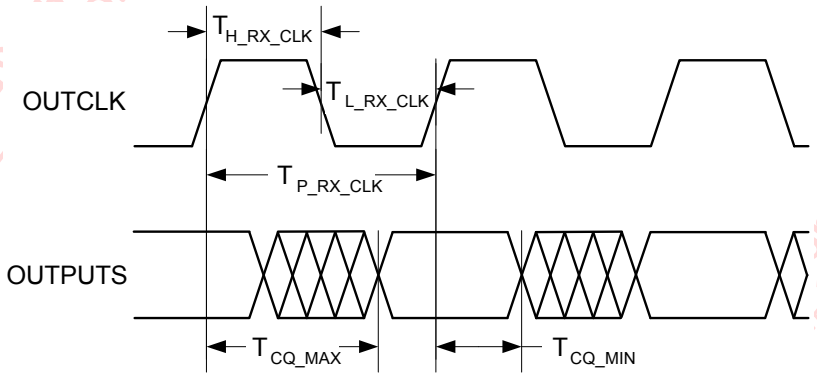
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 39: RMII Transmit Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	100BASE mode		20		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[1:0], P[x]_OUTEN) valid				16	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[1:0], P[x]_OUTEN) invalid		2			ns

1. 50 MHz for 100 Mbps.

Figure 34: RMII Transmit Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.11 Serial Management Interface (SMI) Timing

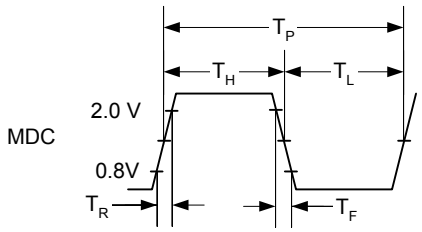
3.11.1 SMI Clock Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 40: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		48			ns	20 MHz
T_H	MDC high time		19			ns	
T_L	MDC low time		19			ns	
T_R	MDC rise				3	ns	
T_F	MDC fall				3	ns	

Figure 35: SMI Clock Timing (CPU Set)



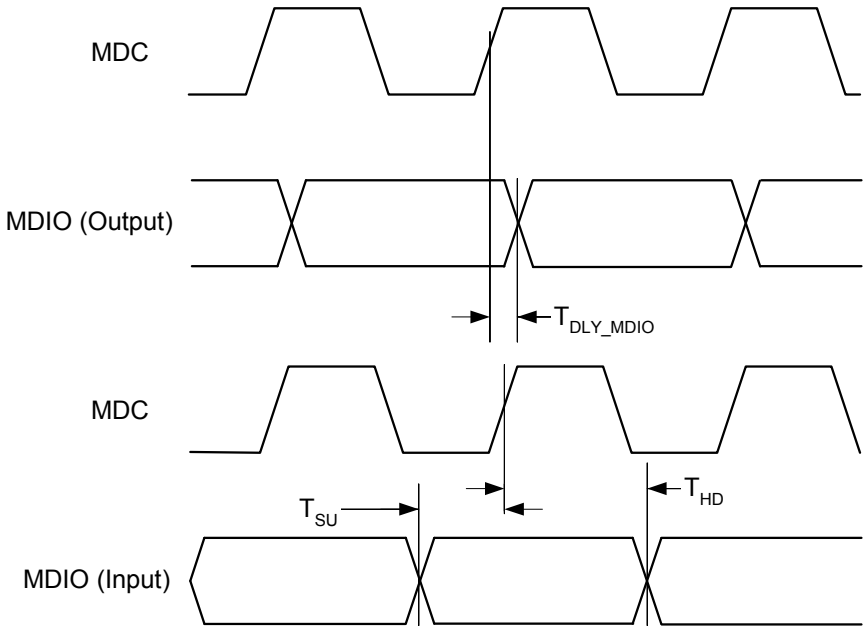
3.11.2 SMI Data Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 41: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		30	ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 36: SMI Data Timing



3.11.3 SMI Timing (PHY Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 42: SMI Clock Timing (PHY Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		48			ns	20.83 MHz
T_H	MDC high time		19			ns	
T_L	MDC low time		19			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	
T_{TX_SU}	MDIO output setup time		10			ns	1
T_{TX_HD}	MDIO output hold time		10			ns	2
T_{RX_SU}	MDIO input setup time						
T_{RX_HD}	MDIO input hold time						
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		5	ns	2

1. MDIO input setup and hold time is intentionally sampled with respect to the MDC falling edge.
2. MDIO data is intentionally clocked out on the falling edge of MDC.

Figure 37: SMI Timing Output (PHY Mode)

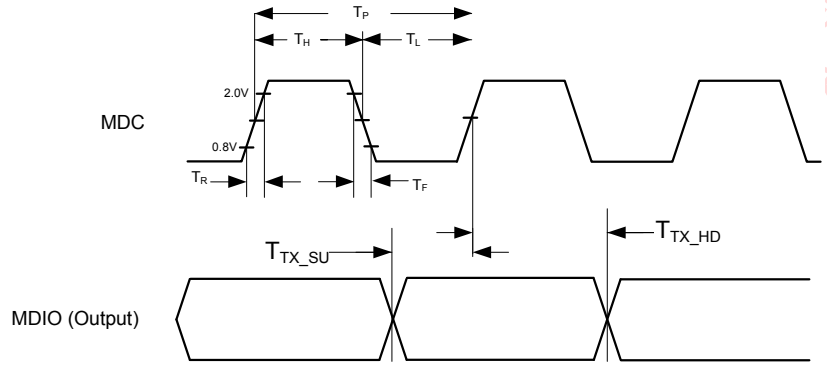
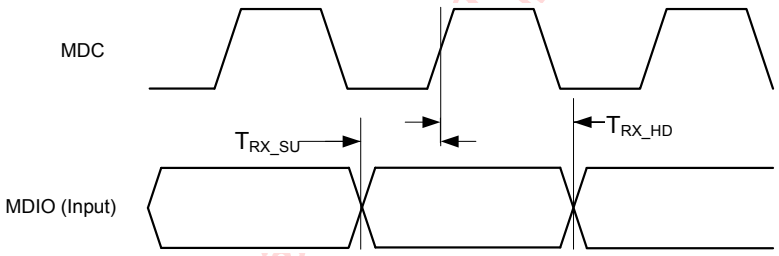


Figure 38: SMI Timing Input (PHY Mode)



3.12 EEPROM Timing

3.12.1 2-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 43: 2-Wire EEPROM Input Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	EE_CLK frequency	3.3V			1000	kHz
T_H	EE_CLK high time	3.3V	500			ns
T_L	EE_CLK low time	3.3V	500			ns
T_{IN}	Data input time	3.3V	50		250	ns

Figure 39: 2-Wire Input Timing

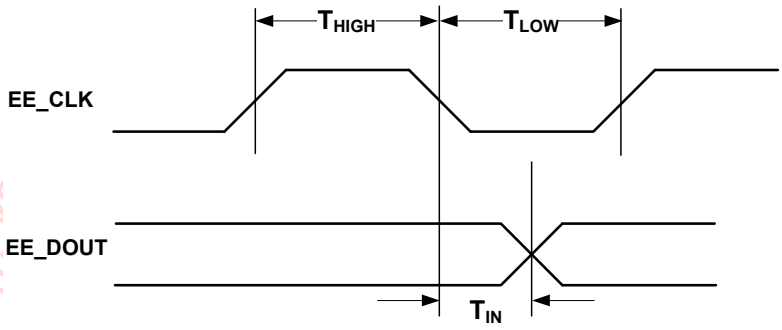
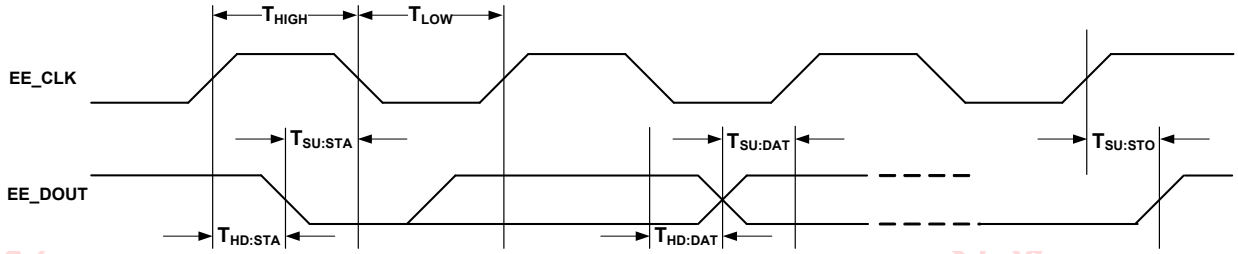


Table 44: 2-Wire EEPROM Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	EE_CLK frequency	3.3V			1000	kHz
T_H	EE_CLK high time	3.3V	500			ns
T_L	EE_CLK low time	3.3V	500			ns
$T_{HD:STA}$	Start condition hold time	3.3V	250			ns
$T_{SU:STA}$	Start condition setup time	3.3V	250			ns
$T_{HD:DAT}$	EE_DOUT data output hold time	3.3V	250			ns
$T_{SU:DAT}$	EE_DOUT data output setup time	3.3V	250			ns
$T_{SU:STO}$	Start condition setup time	3.3V	250			ns

Figure 40: 2-Wire EEPROM Output Timing



3.12.2 IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[4:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[4:0]	100BASE-TX	3.0	4.0	5.0	ns
$T_{RISE/TFALL}$ Symmetry		MDIP/N[4:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[4:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[4:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

4 Mechanical Drawing

Figure 41: 88-pin QFN (10x10 mm) Package Mechanical Drawing

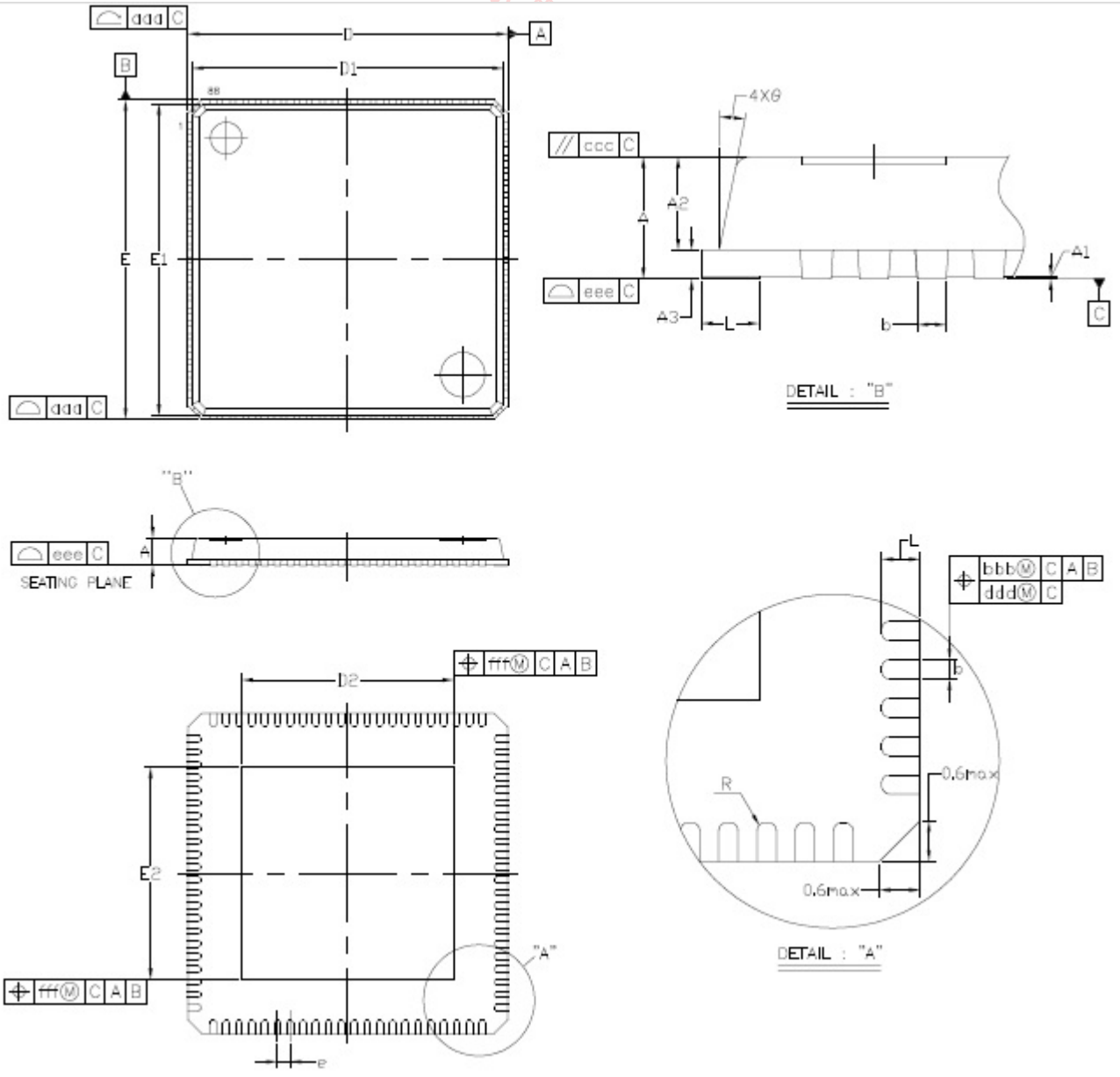


Table 45: 88-pin QFN (10x10mm) Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	9.90	10.00	10.10
D1/E1		9.75 BSC	
e		0.40 BSC	
D2		5.00 ± 0.15	
E2		5.00 ± 0.15	
L	0.30	0.40	0.50
θ	0°		14°
R	0.075	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

5 Part Order Numbering/Package Marking

5.1 Part Order Numbering

Figure 42 shows the part order numbering scheme for the 88E6141. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 42: Sample Part Number

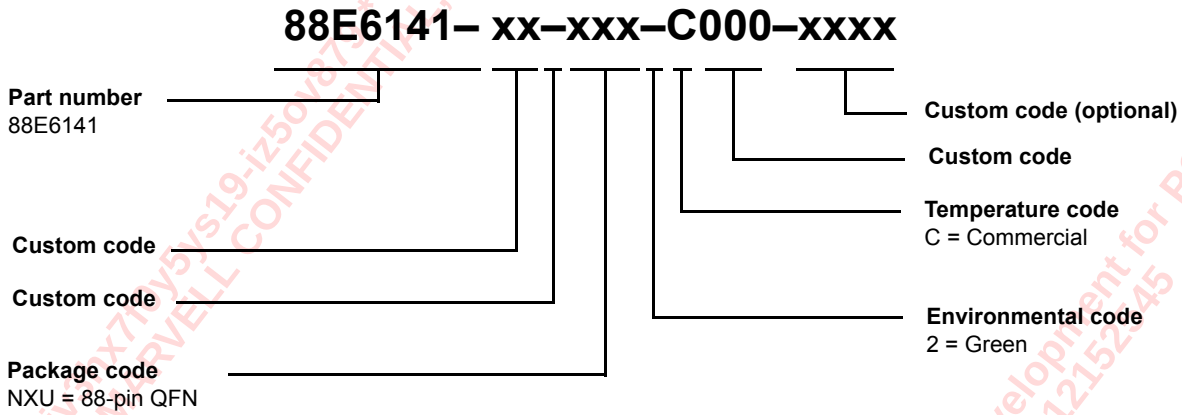


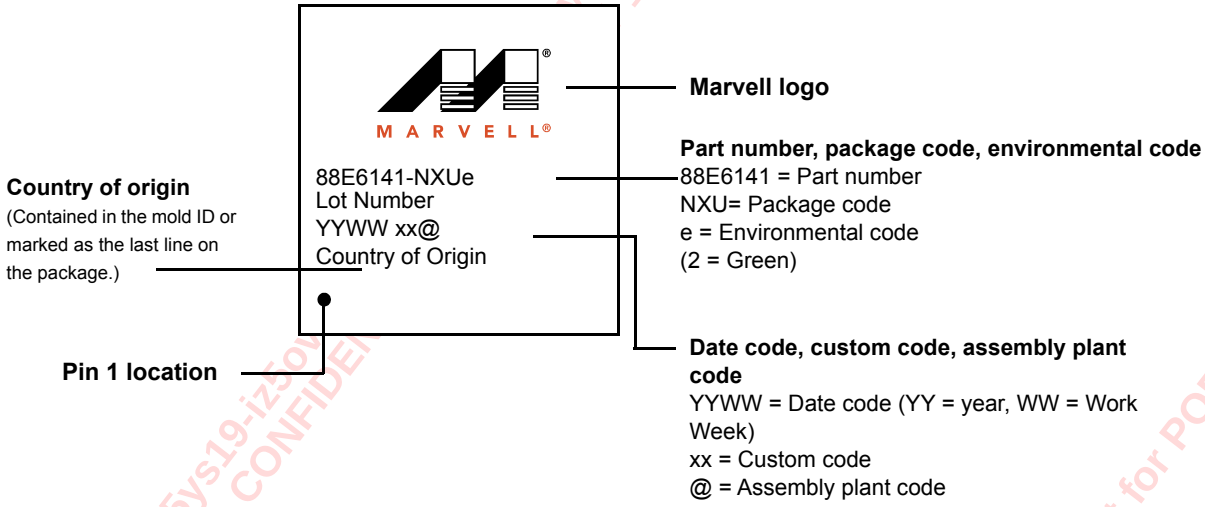
Table 46: 88E6141 Part Order Options

Package Type	Part Order Number
88-pin QFN (10x10mm)	88E6141-xx-NXU2C000 (Green compliant package)

5.2 Package Marking

Figure 43 shows a sample Commercial package marking and pin 1 location for the 88E6141.

Figure 43: Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

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