Phase 2.3 Direct Mapped Cache FSM

Wednesday, April 17, 2019 12:09 PM

Defaults

Done = 0
err = 0
enable = 1
comp = 0
write = 0
wr = 0
rd = 0
cache_offset = q_addr[2:0]
mem_offset = q_addr[2:0]
memtocache = 0
cachetomem = 0
next_state = IDLE
fsm_stall = 1
cachehit = 0