Project 2: Digital Systems Review, Sequential Circuits

Due: 2/2/2022
Points: 10

1 The Objective

The principle objective of this part is to have you review your skills with sequential circuit design and to challenge you with the effective documentation of that circuit. This part also requires you to continue using some CAD tool of your choosing to design a gate level circuit. You can use any CAD tool for this project, even one that is completely different from the tool you used in Project 1. You cannot use libraries of components to build these components. Each circuit must be designed by you using only the following gate level primitives: `and`, `or`, `not`. While you cannot use existing libraries, I encourage you to develop components for your own library and incorporate them into your design and writeup.

2 The Task

For this part you are required to design a sequential circuit that emulates parts of an instruction interpretation cycle. The machine has a collection of that achieves the following behavior (all data inputs/outputs of this circuit are single bits):

Inputs: `indirect`, `program-check`, `C1`, `clock`

Outputs: `fetch`, `decode`, `indirect`, `execute`, `trap`, `S1`, `S2`

States: `fetch`, `decode`, `indirect`, `execute`, `trap`

State Transitions: All state transitions occur with the clock signal and each main state (`fetch`, `decode`, `indirect`, `execute`, `trap`) cycles through two steps coincident with the clock (so the machine transitions to the fetch state at S1 (written `fetch/S1`) and them moves to the `fetch` state at `S2` where it transitions as per the informal specification given below:

fetch
S1. —
S2. goto **decode/S1**
decode
S1. —
S2. if indirect then goto **indirect/S1**
else goto **execute/S1**
indirect
S1. —
S2. goto **execute/S1**
execute
S1. —
S2. if program-check then goto **trap/S1**
else goto **fetch/S1**
trap
S1. —
S2. goto **fetch/S1**

Note however, the following exceptions:

- If condition `C1` is true at the end of `fetch` then the machine transitions back to state `fetch/S1`.

3 The Report

You are limited to a written report of no more than 6 pages. The report should not just be a printed copy of your solution. Your must focus on providing a clear and concise description of your solution. The report must describe a derivation of your solution that includes your finite state machine and your next state equations.

As well as the circuit itself. Of course, the circuit can be broken down into multiple figures to illustrate the solution.

Again as with Project 1: **The real challenge with this part is the communication of a reasonably complex circuit in a single page — find a modular presentation style**.